IHEP ATLAS ITk-Strip Phase2 Upgrade

Xin SHI

On behalf of the IHEP ATLAS ITk Group

IHEP, CAS

3 November 2017

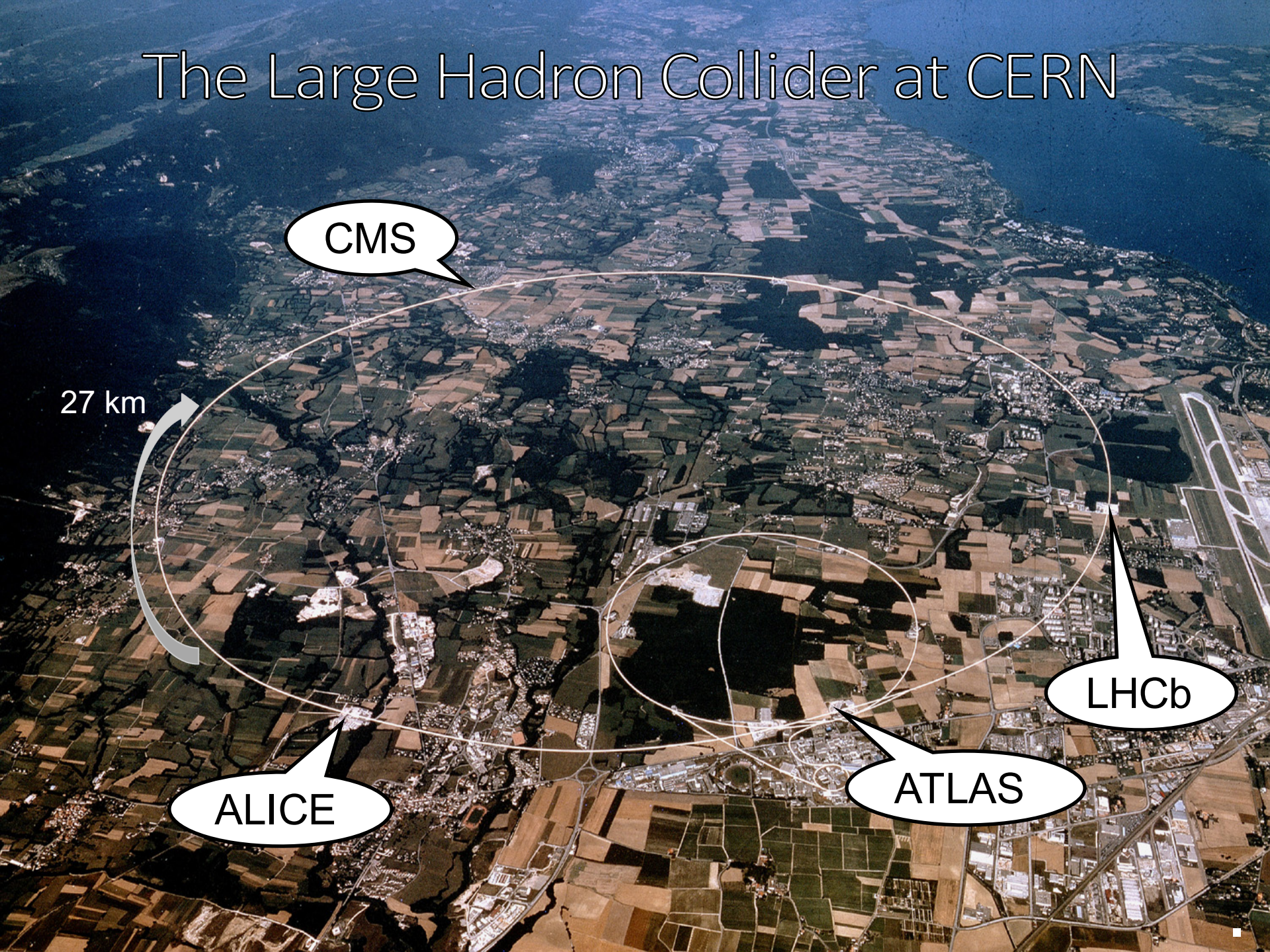
Outline

- ATLAS ITk Upgrade in China

  Joint effort between IHEP and Tsinghua U; received funding support from MOST (+bid to NSFC) to produce ~1000 barrel strip modules: core contribution of 1.8 MCHF

- Main Research Topics
  - Design of the front-end readout ASIC (ABCStar)
  - Assembly and tests of barrel modules
  - Evaluation of CMOS strip sensors
- And more …

The Large Hadron Collider at CERN



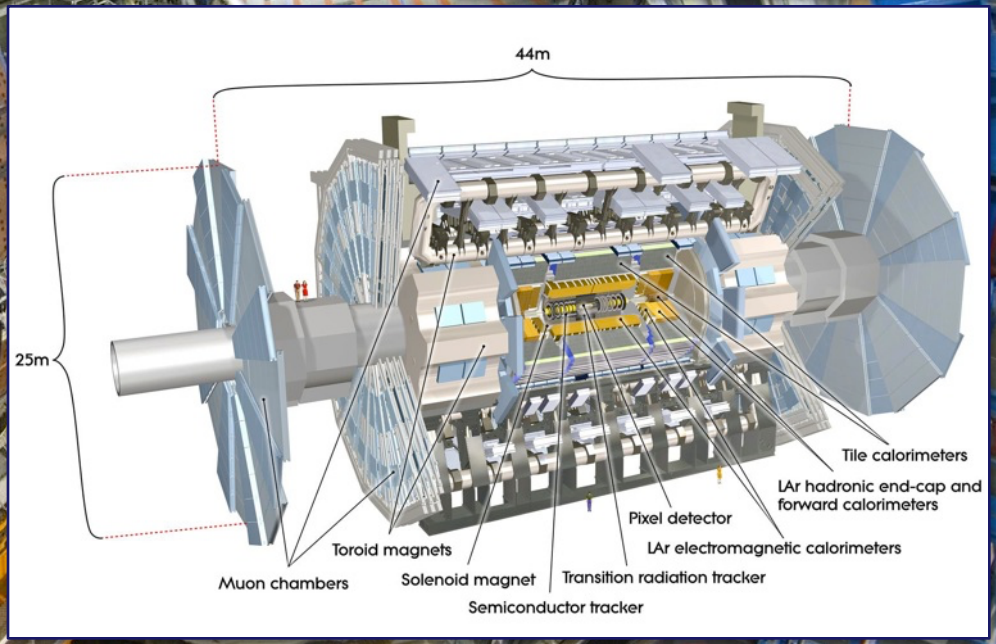
LHC Point 1: The ATLAS Experiment

The ATLAS Collaboration

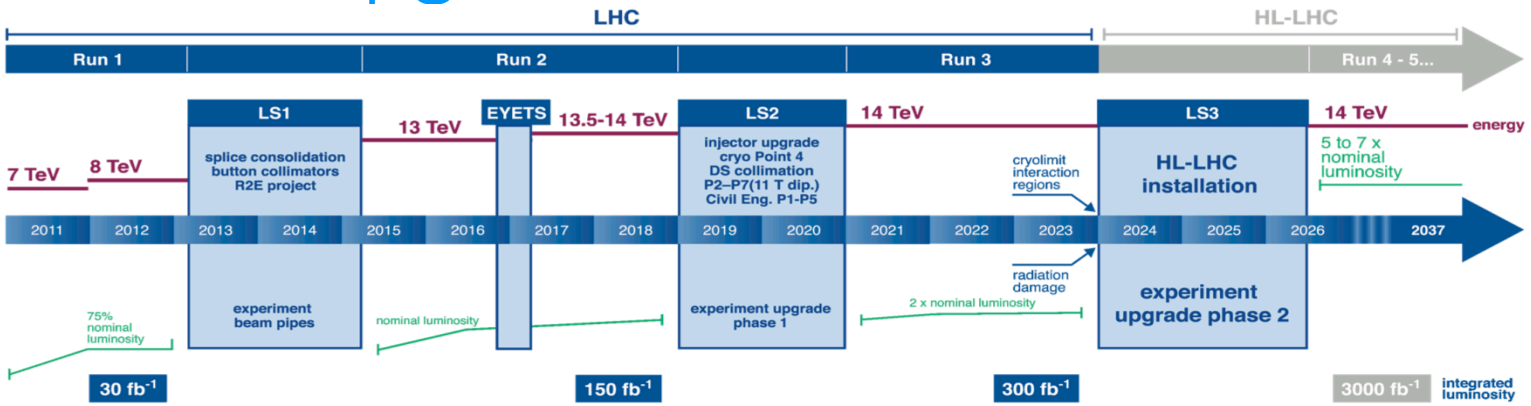
3000 Members

177 Institutes

38 Countries



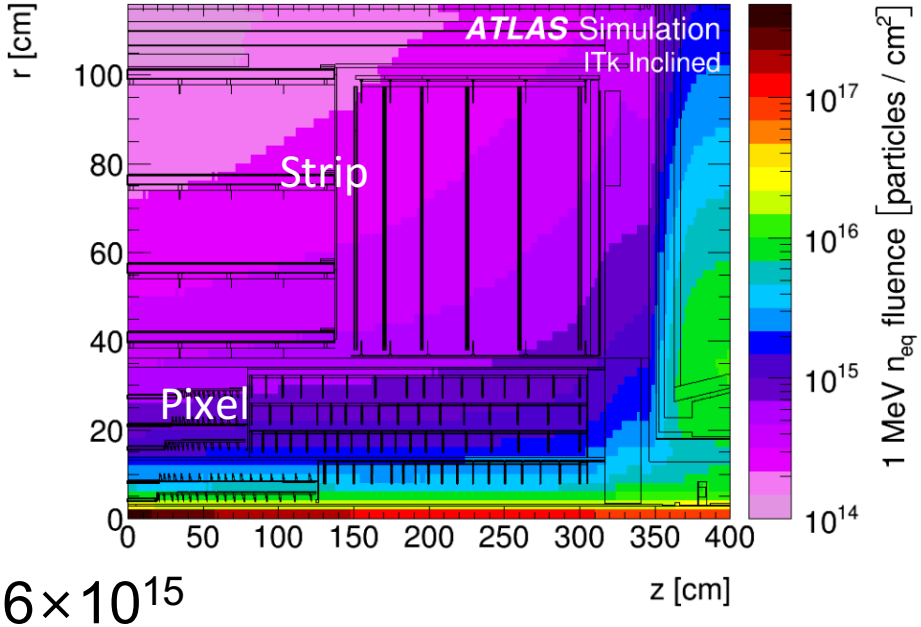
ATLAS ITk Upgrade



- ATLAS Detector upgrade for the LHC high luminosity upgrade, all silicon tracking device

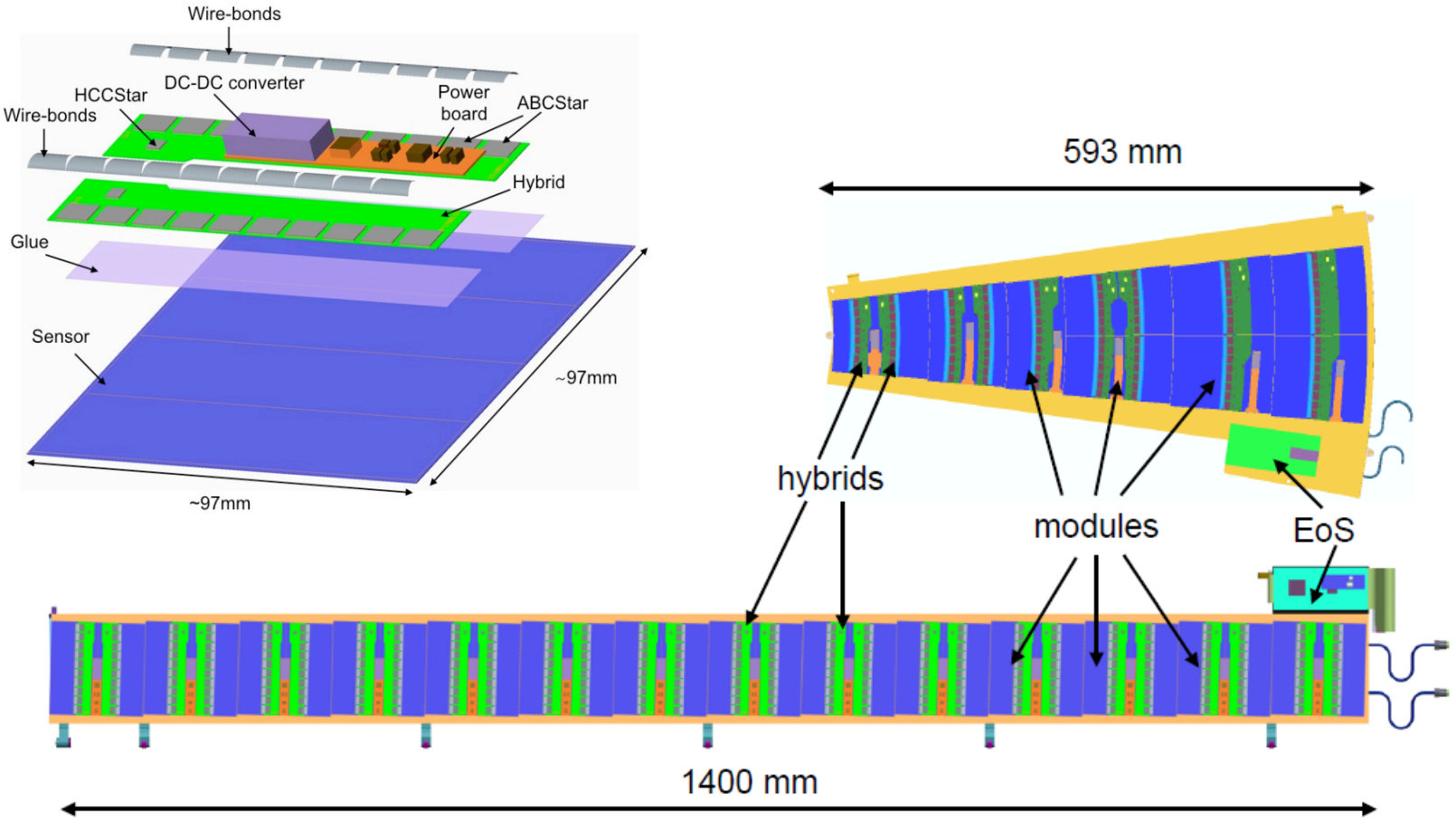
- ITk-Strip
  Barrel Layer 3-4:
  4.8 cm
  Layer 1-2: 2.4cm

- Radiation hardness
  (1MeV n_{eq}/cm^2)
  Barrel short strip: 1.1×10^{15}
  Barrel long strip: 0.6×10^{15}
  Endcap inner layer strip: 1.6×10^{15}

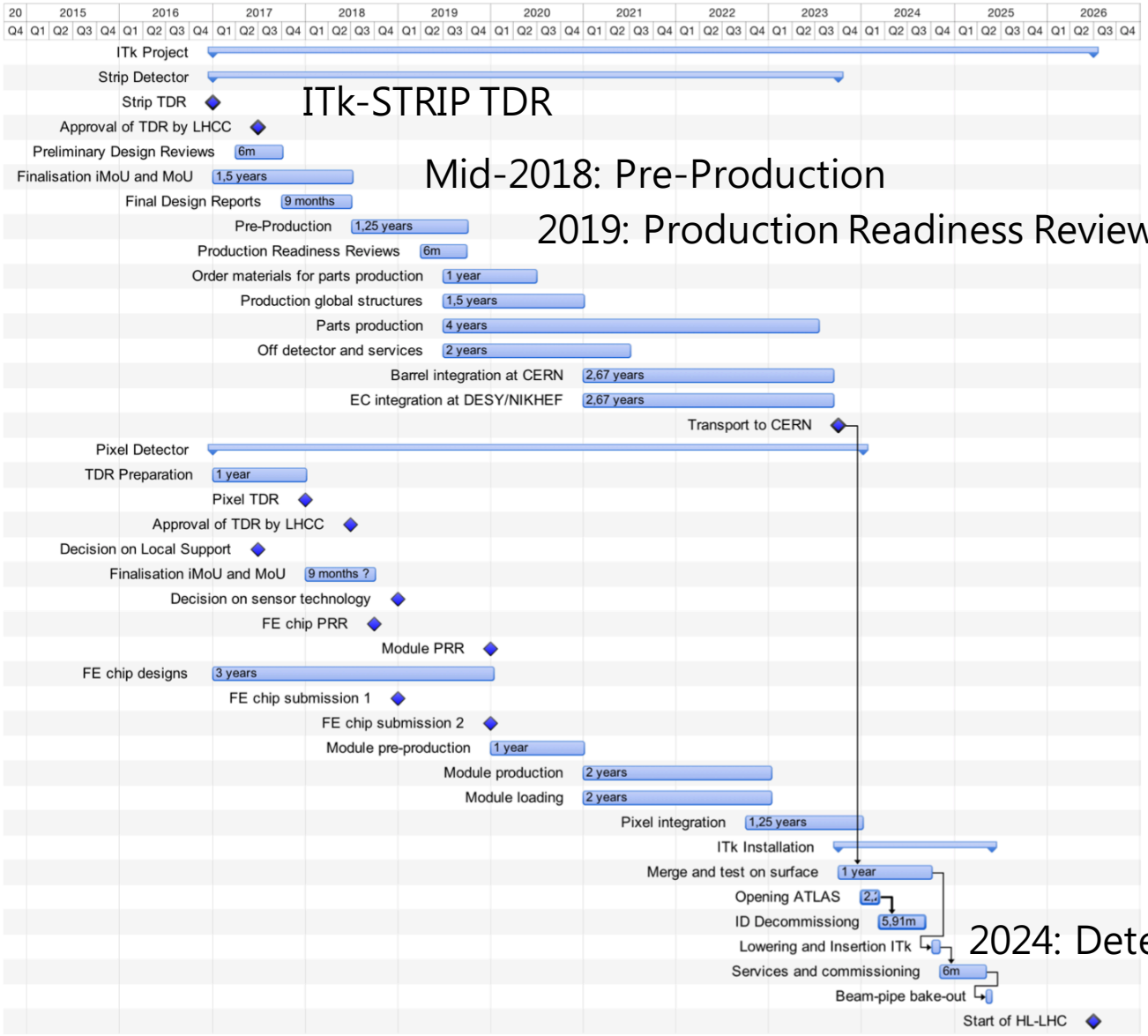


ITk Silicon Strip Detector Concept

- Stave/Petal + Mechanics Supported Silicon Modules



ITk Upgrade Project Timeline



ITk-STRIP TDR

Mid-2018: Pre-Production

2019: Production Readiness Reviews

2024: Detector Install

The Team

8 Staff Members (7 IHEP + 1 THU)

Xinchou Lou

Joao da Costa

Hongbo Zhu

Weiguo Lu

Xin Shi

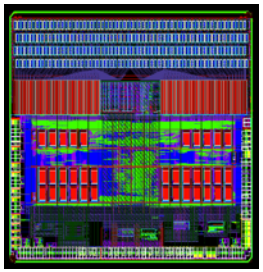
Zhijun Liang

Yiming Li

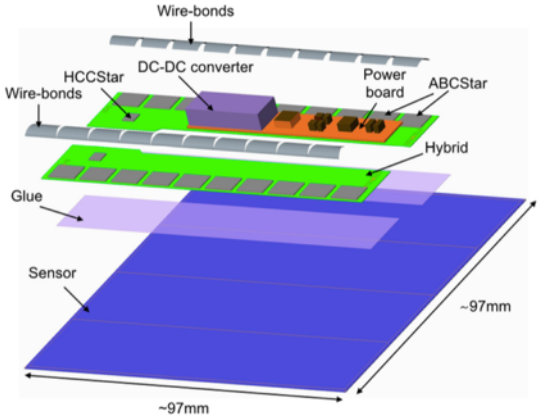
Xin Chen

Main Research Topics

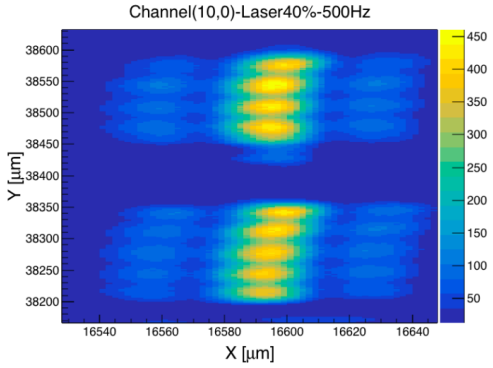
- Design of the front-end readout ASIC (ABCStar)



- Assembly and tests of barrel modules

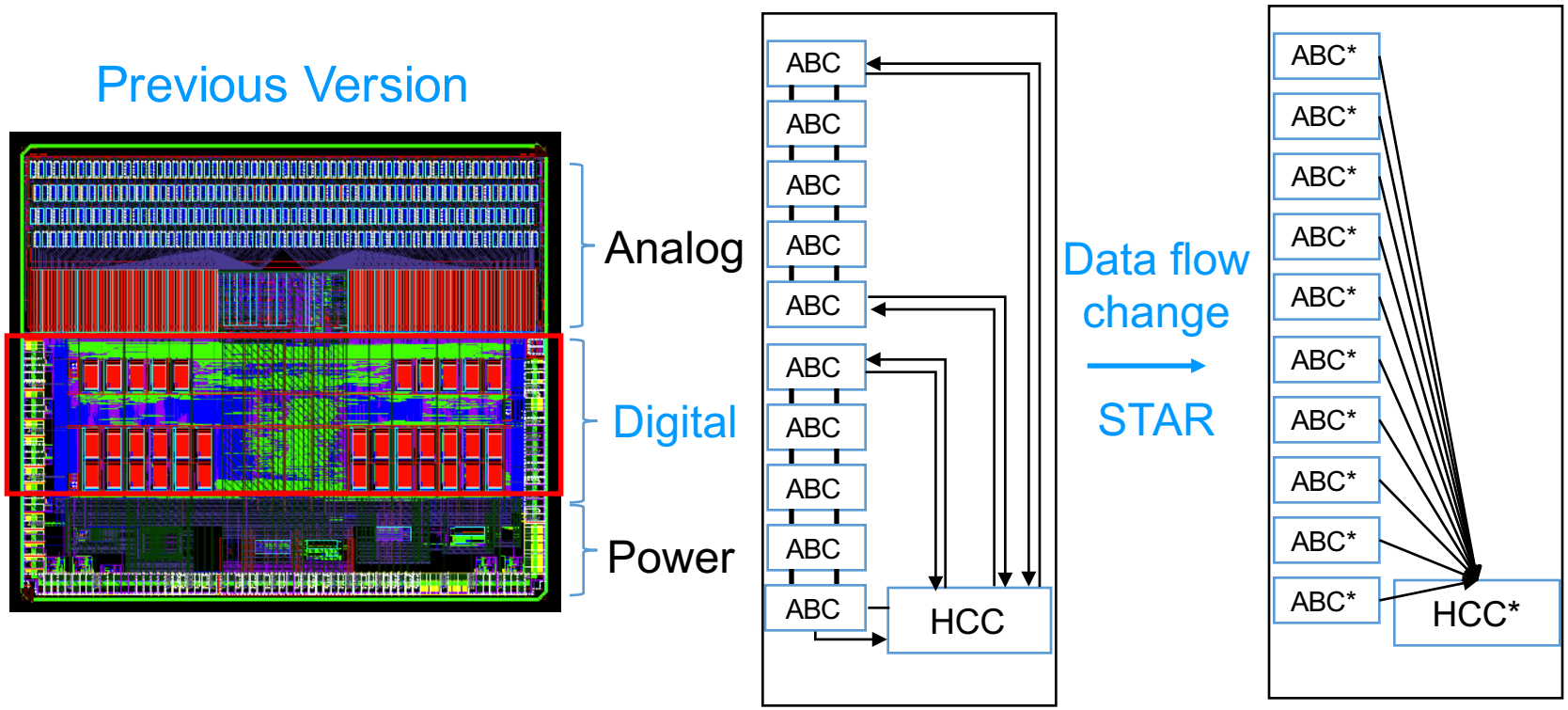


- Evaluation of CMOS strip sensors

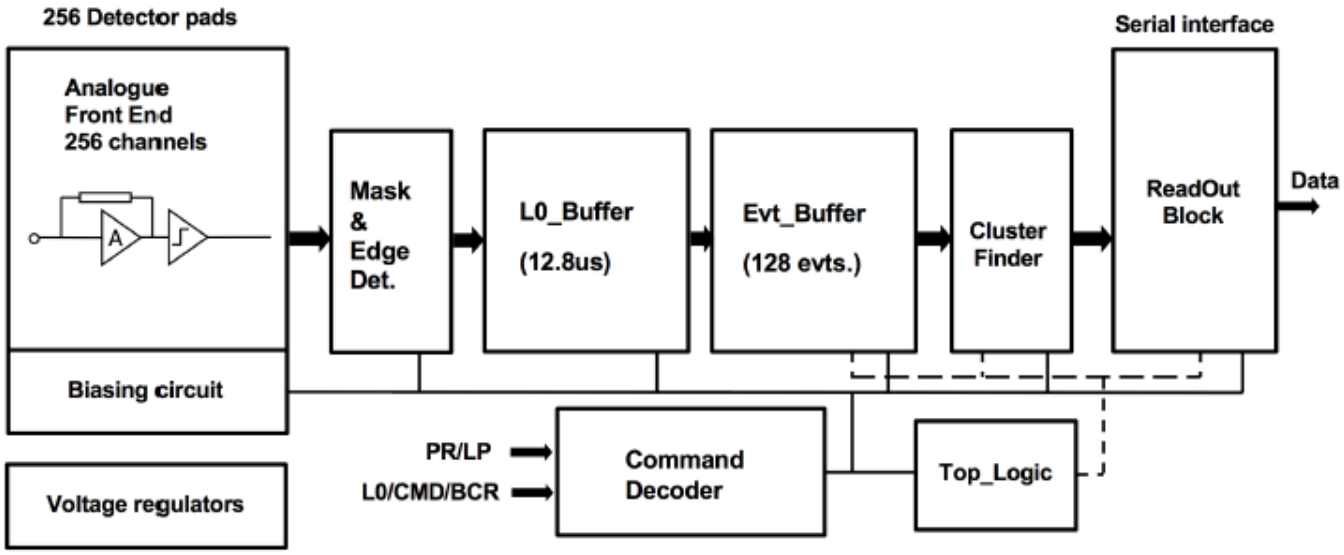


Part 1: Front-end ASIC design

- L0 trigger rate increase, redesign the digital readout GF/IBM 130nm CMOS



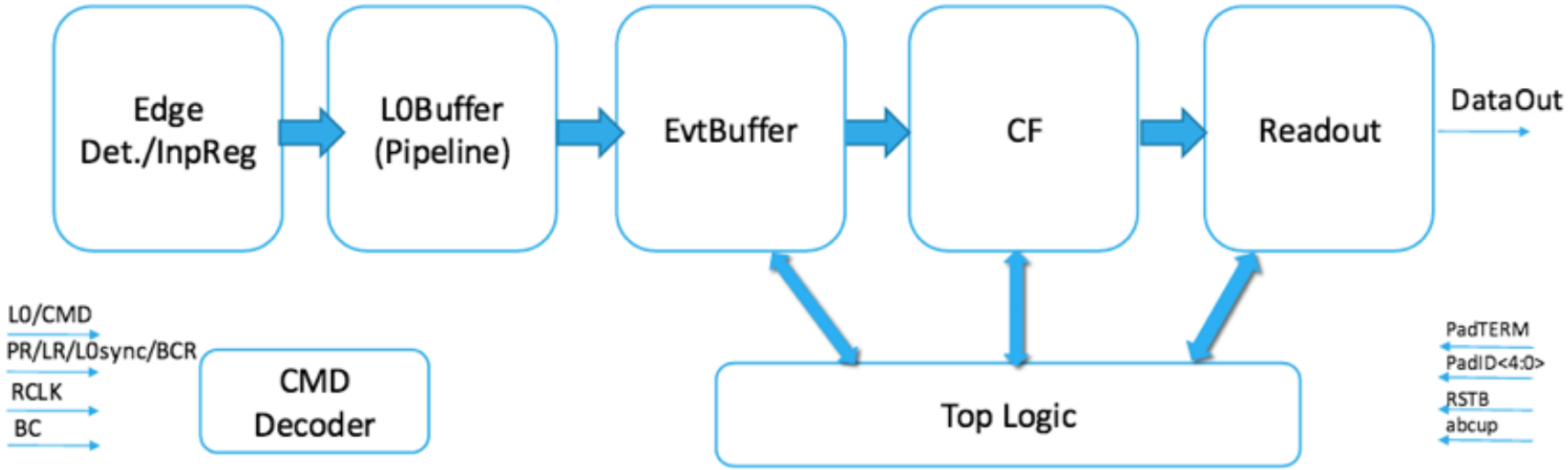
ABC Star ASIC Design



- It uses the standard binary readout architecture
- Data path: amplifier, discriminator, input register block, pipeline, event buffer and a cluster algorithm to compress data for output
- It is being designed to support various trigger modes
- It will be built in GF130nm technology

Digital Readout Design and Verification

- Redesign all digital logic, Verification framework based on SystemVerilog: UVM verification concept used for chip readout for the first time.



- Submit final design by the end of 2017

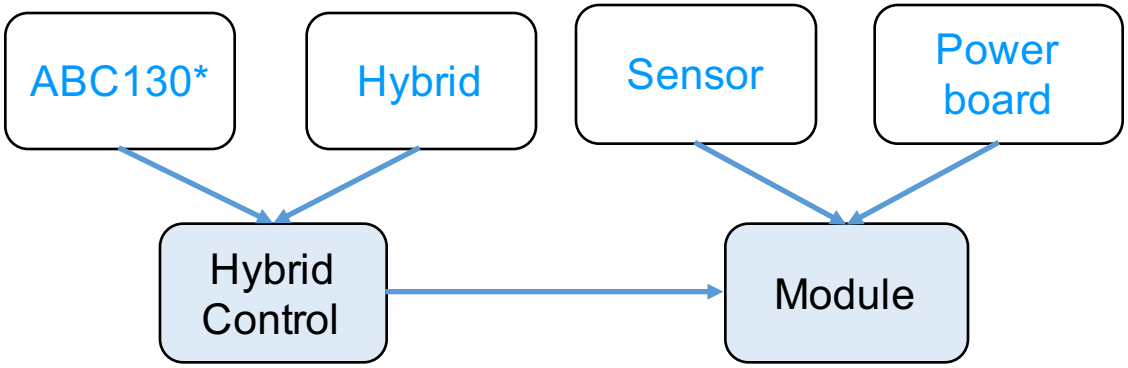
IEEE RT2016 Poster (L. Cheng)
TWEPP2016 Conf. Report (W. Lu)

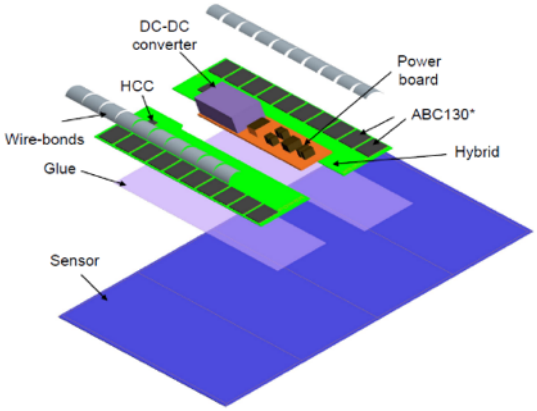
Recent Progress on ASIC Design

Blocks/tasks Analog	status	Our contribution	Blocks/tasks Digital	status	Our contribution
FE	ongoing		InputRegisters	fixed	√
Voltage regulator	ongoing	interested	Two stage buffers	fixed	√
efuse	pending		Cluster Finder	fixed	
Analog monitor	pending	interested	Readout	fixed	
ESD	pending		TopLogic	fixed	√
			LCB and CommandDecoder	ongoing	
			hitsAccumulator	fixed	√
			Functional verification	ongoing	√
			SEU protection	pending	interested
			Digital backend	ongoing	interested

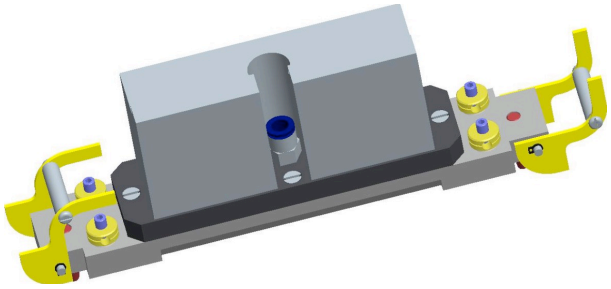
Part 2: Assembly and tests of barrel modules

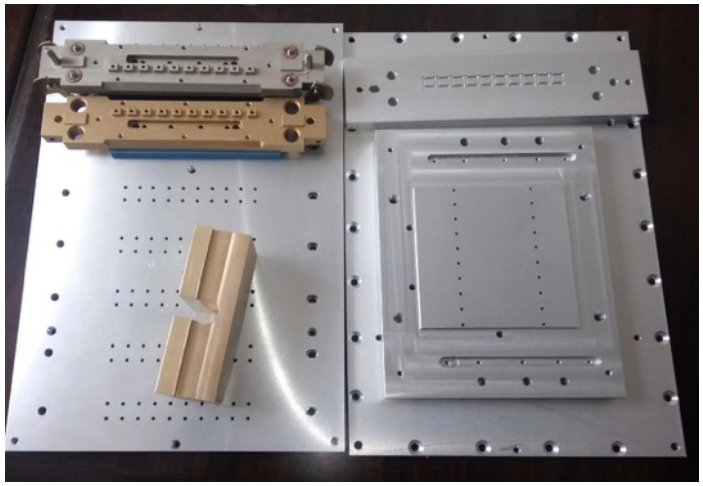
- Produce 50 working modules during pre-production





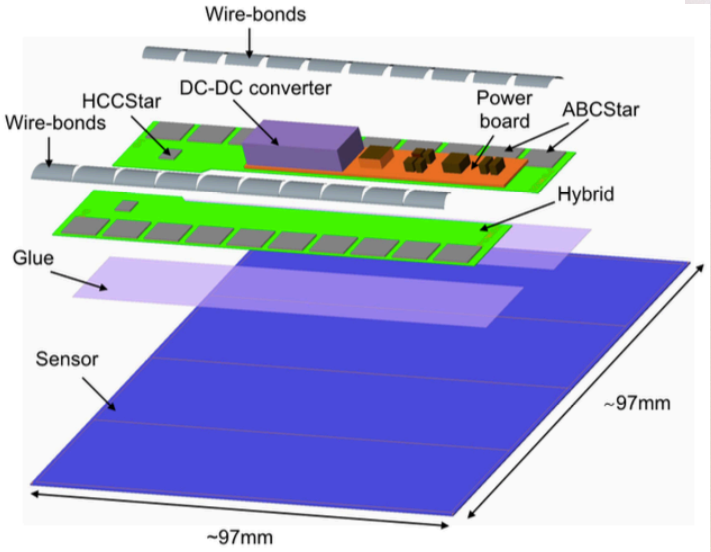
- Tooling for module handling

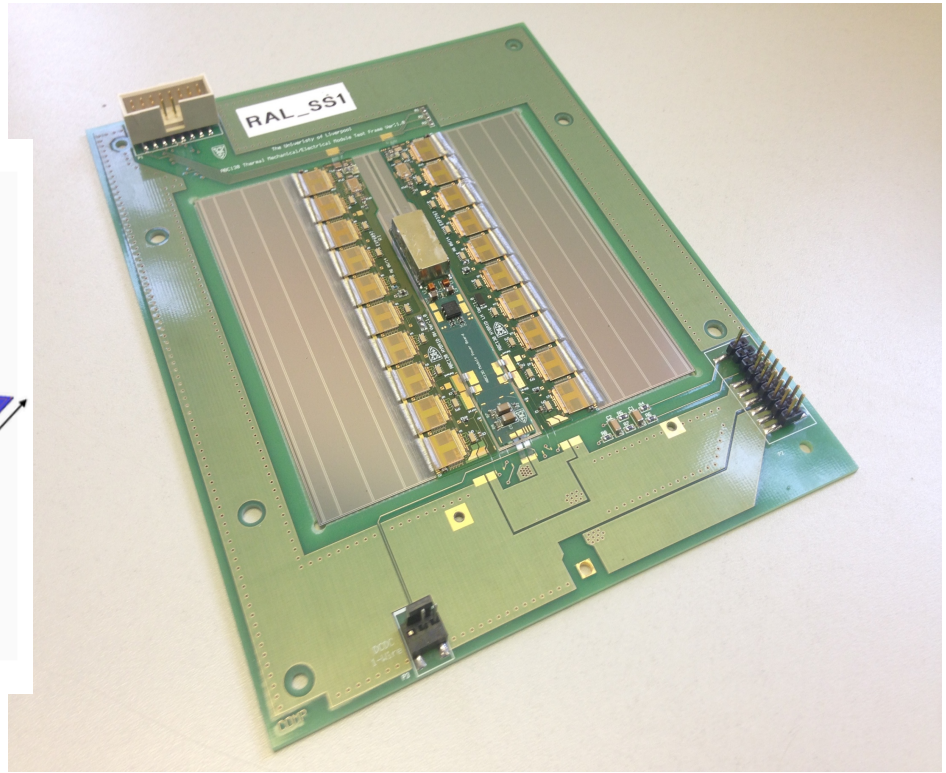




Silicon Strip Detector Module

- Silicon Sensor + Hybrid PCB (with Readout ASICs and control chips) + Power board + Glue and Wire-bonds

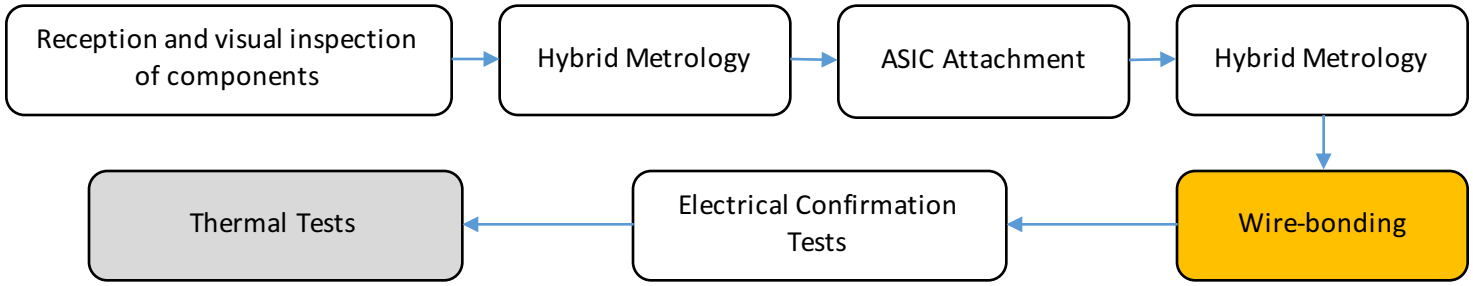




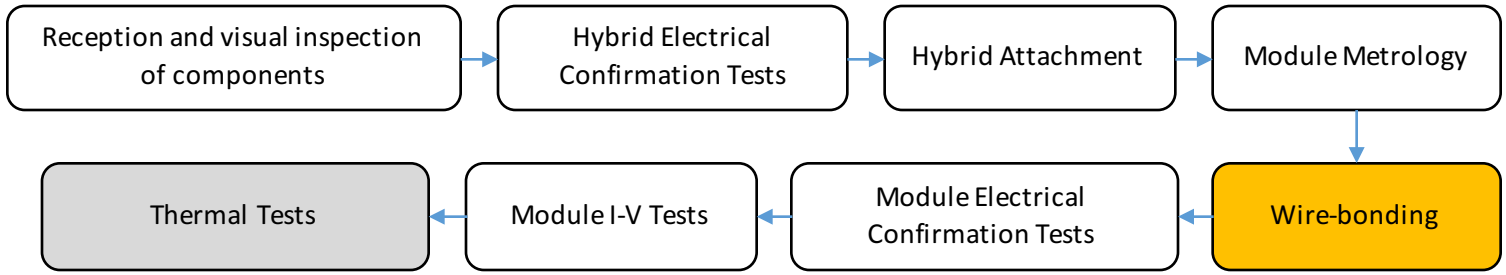
Quality Control

- Based on the prototype study, along with the current ATLAS SCT detector experience, improve the quality control (QC) of module production process

Control board QC

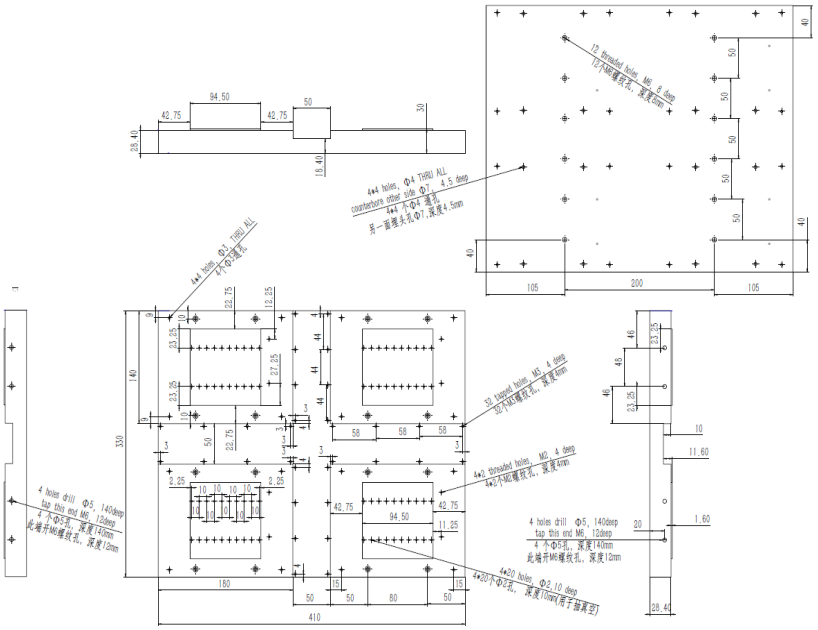


Detector Module QC



Module QC Task: Evaluate max no. of modules in a bonder – by IHEP

- Design workholder for 2x2 module on BondJet820
- Released the first layout (thanks for Craig's help!)
- Processed at IHEP, will be evaluated at RAL



Drawing: Yuzhen Yang

Production: Fang Chen

IHEP Lab for ITk Upgrade

- An existing class 1000 Cleanroom with 150m^2

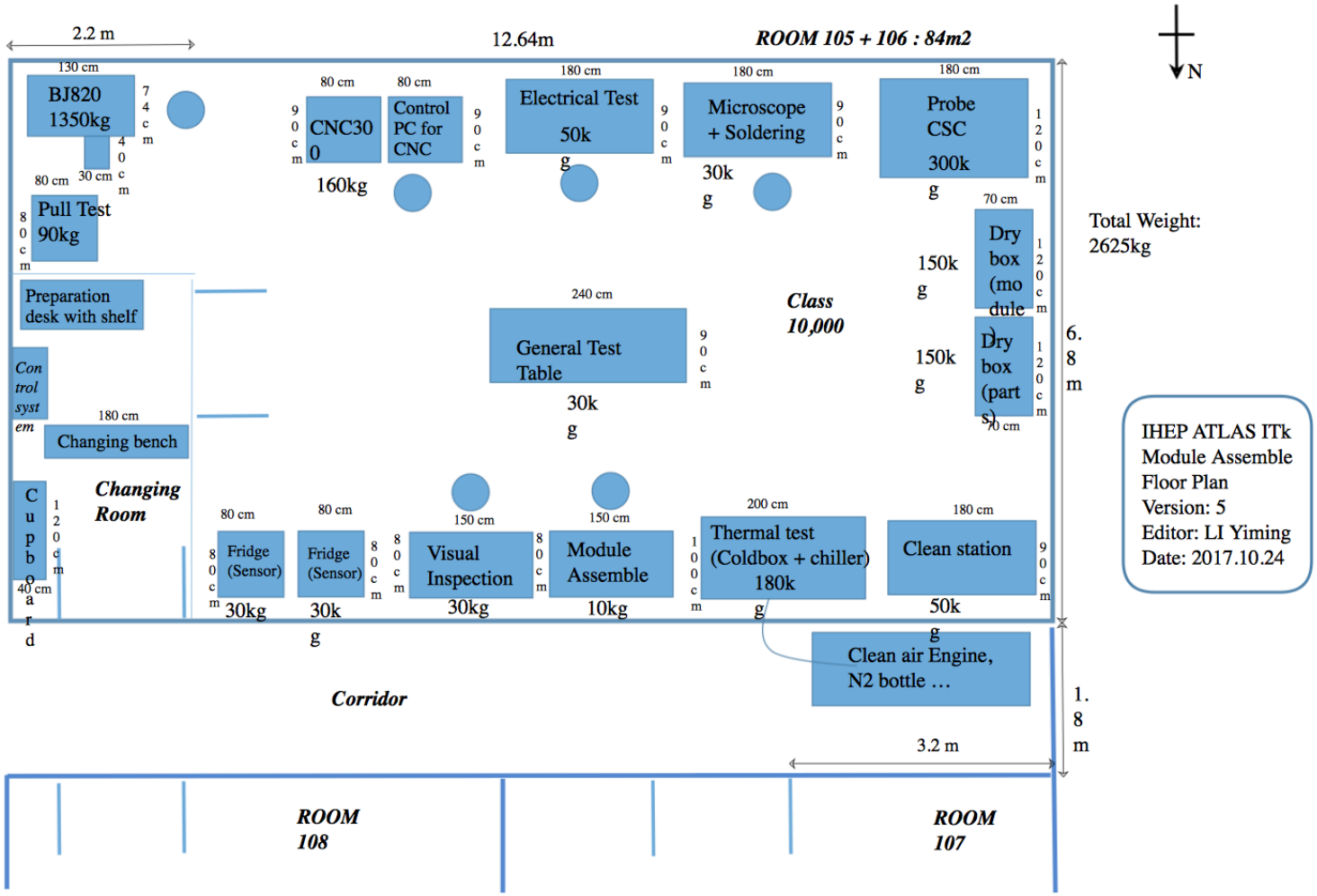
- OGP Flash CNC 300 already purchased
- Hesse BondJet820 is being purchased

Flash CNC 300


HESSE BJ820

IHEP Dedicated Cleanroom for ITk-Strip

- A new cleanroom is proposed for the strip production.



Radiation-hard ASICs Import Issue

- Currently all of the radiation-hard ASICs in module (ABC, HCC, power control AMAC, DC-DC and FESAT are NOT allowed to be imported into China!

- **Milestone**: got export license for GF/IBM ASICs from US Department of Commerce and Export permission from Switzerland government.

- Actively in collaboration with RAL in UK to train our team in parallel

Collaboration with RAL

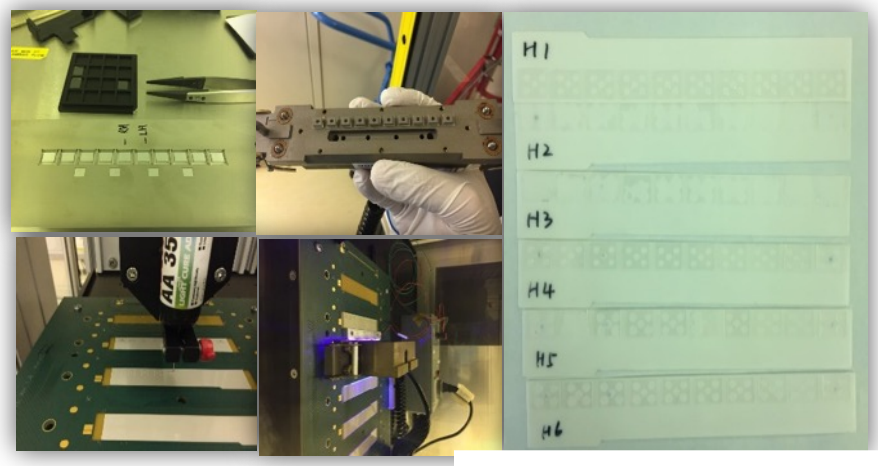
- RAL in UK is the leading institution on ATLAS ITk upgrade.

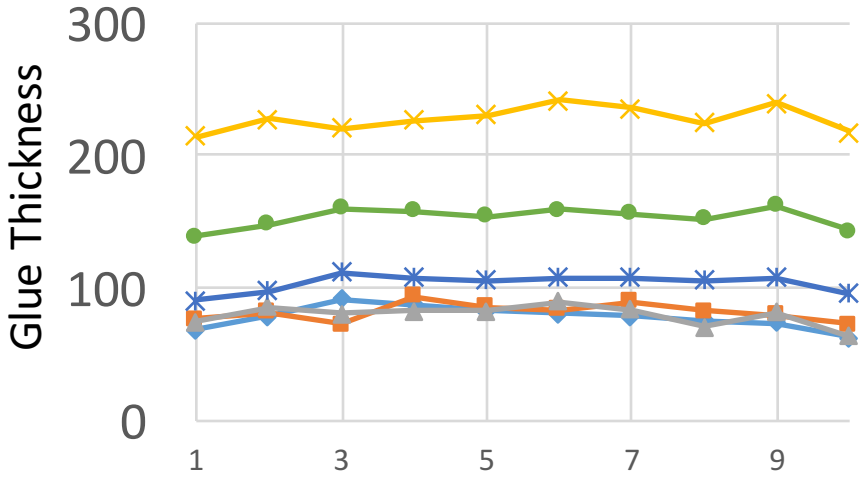
IHEP Team visited RAL on September 19, 2016

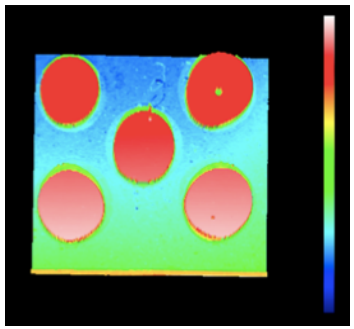
- MoU to be signed with RAL
- Staff rotation plan to maintain 2 FTE's at RAL for the coming years.
- Invited RAL collaborators to China. Craig Sawyer will visit IHEP in August

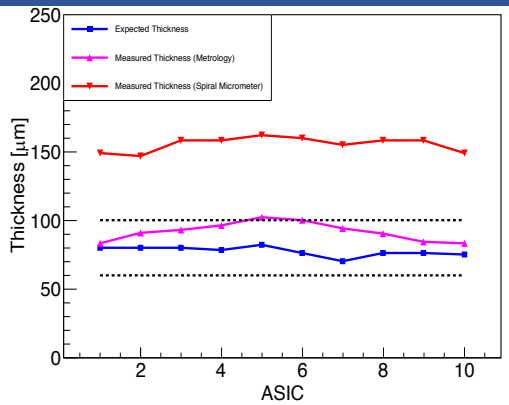
Dummy Module Production at RAL

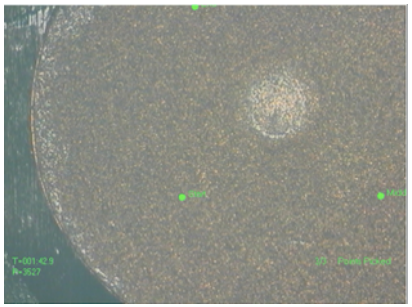
- Use glass-ASICs and plastic hybrid for dummy module production
- Use SmartScope to measure the height of glue

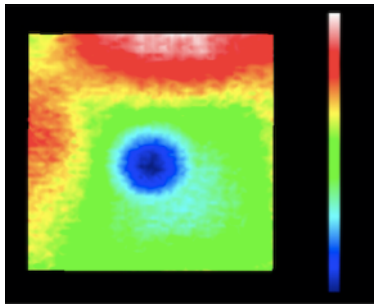






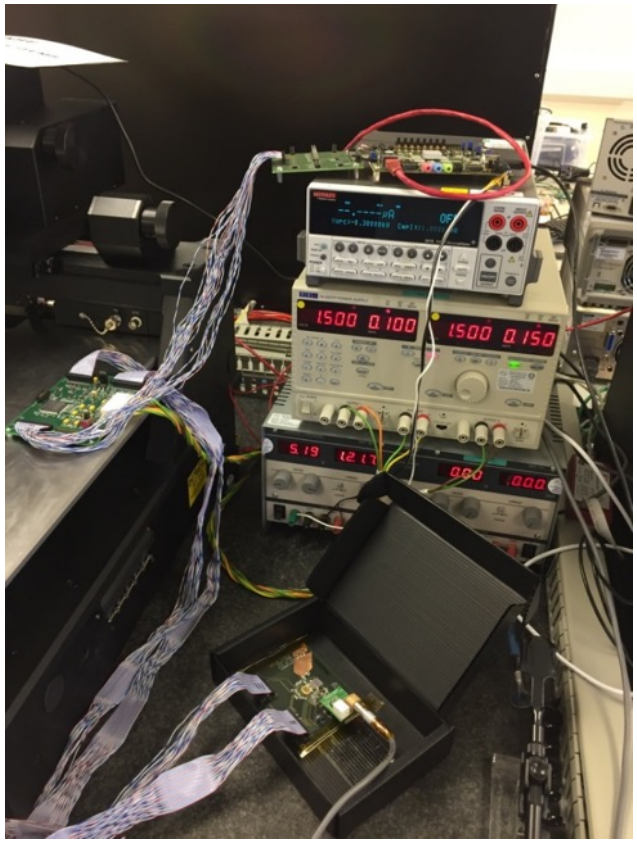


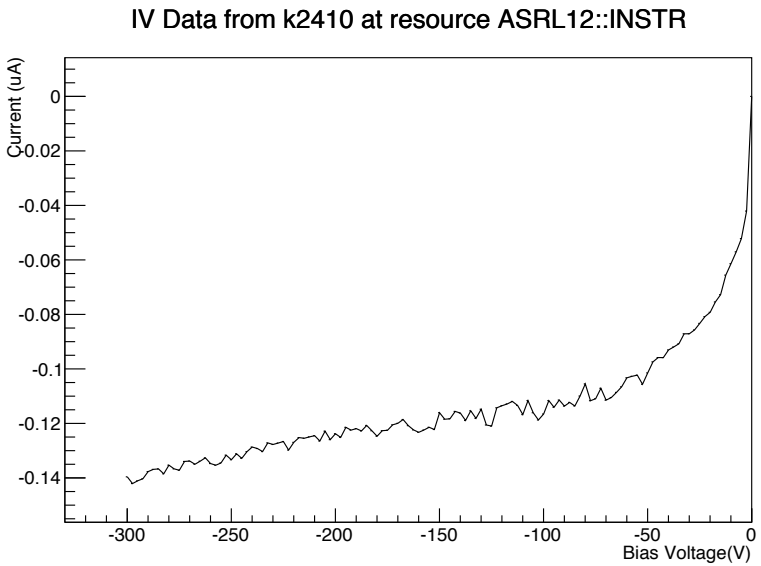




Sensor Electrical test at RAL

- ATLAS 07 Mini Sensor + ABC130 , Learn basic silicon strip sensor test, measure I-V and Equivalent Input Noise

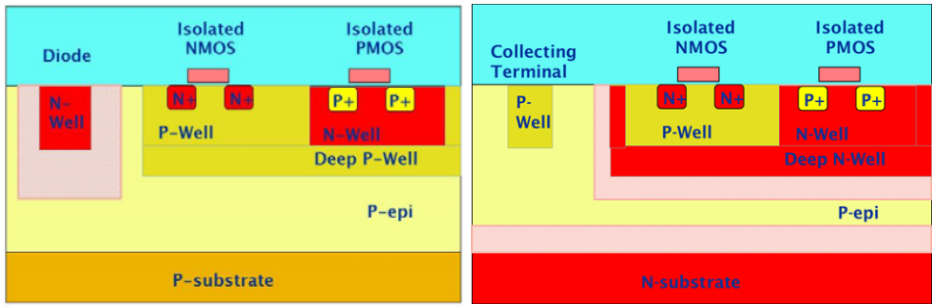




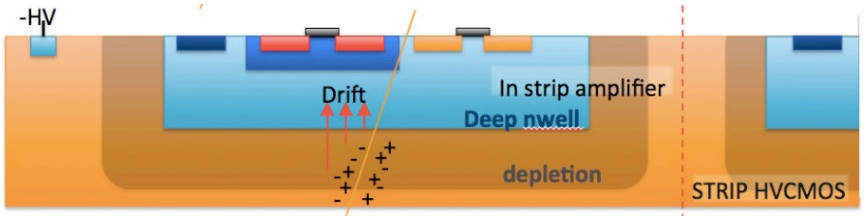
偏置电压	-10 V	-100 V	-300 V
Sensor + ASIC	597.9e	565.9e	563.5e
ASIC	450.5e	449.5e	448.4e

Part 3: CMOS Strip Sensor Study

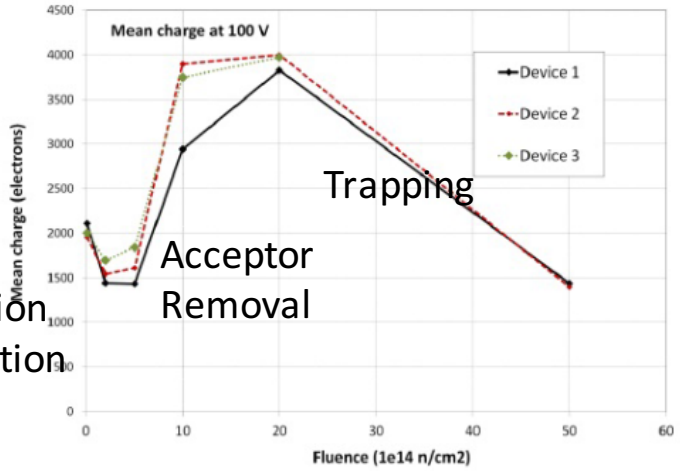
- Based on CMOS technology, with low price, low material budget, good candidate for future silicon detector



HR-CMOS (RAL)



HV-CMOS (UCSC/SLAC)



Diffusion Reduction

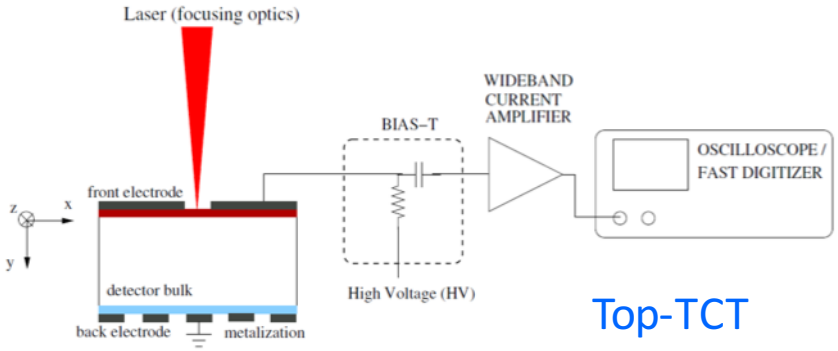
Acceptor Removal

Trapping

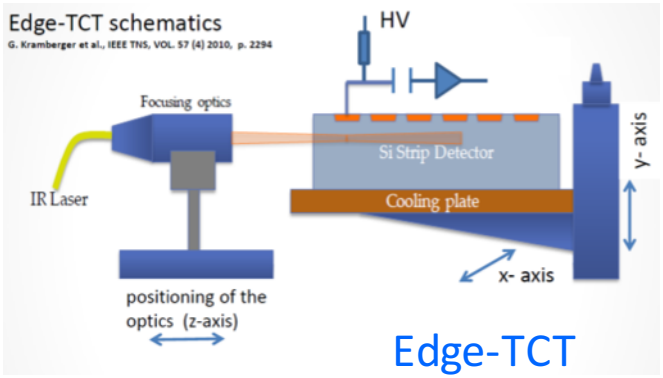
Transient Current Technique（TCT）

G. Kramberger, *Advanced Transient Current Technique Systems*, PoS(Vertex2014)032

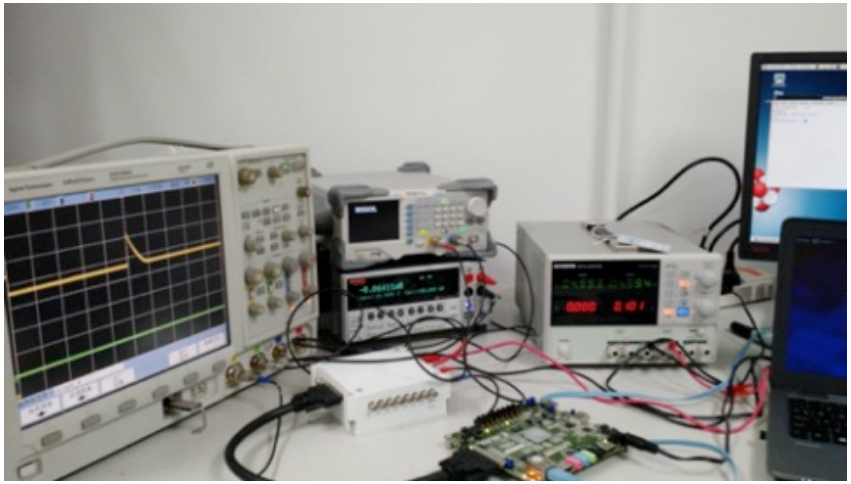
- Check Sensor Response with TCT



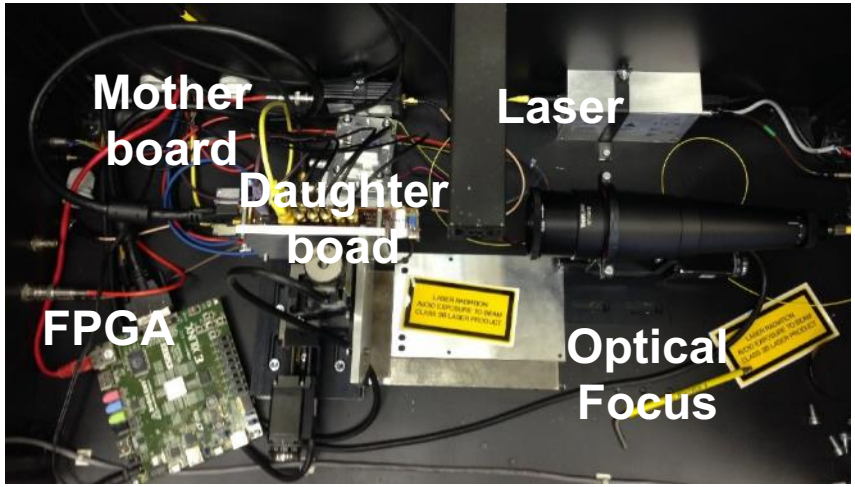
Top-TCT



Edge-TCT



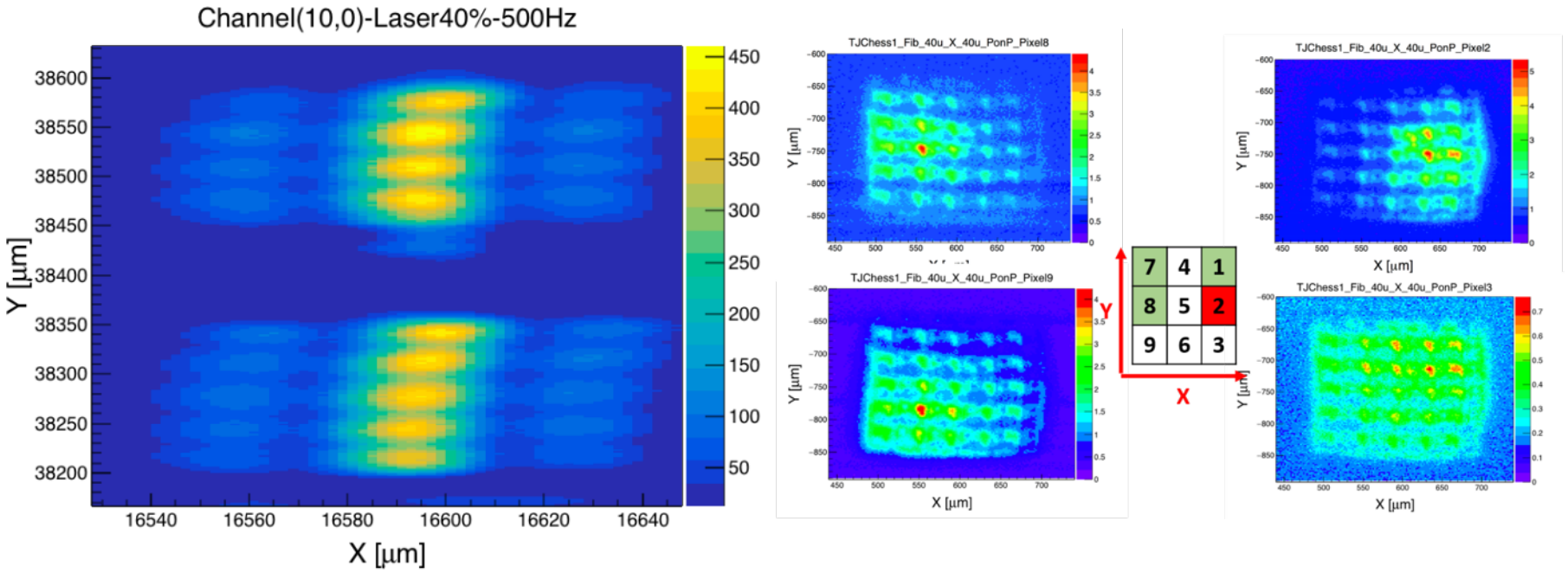
Electrical Test Stand at IHEP



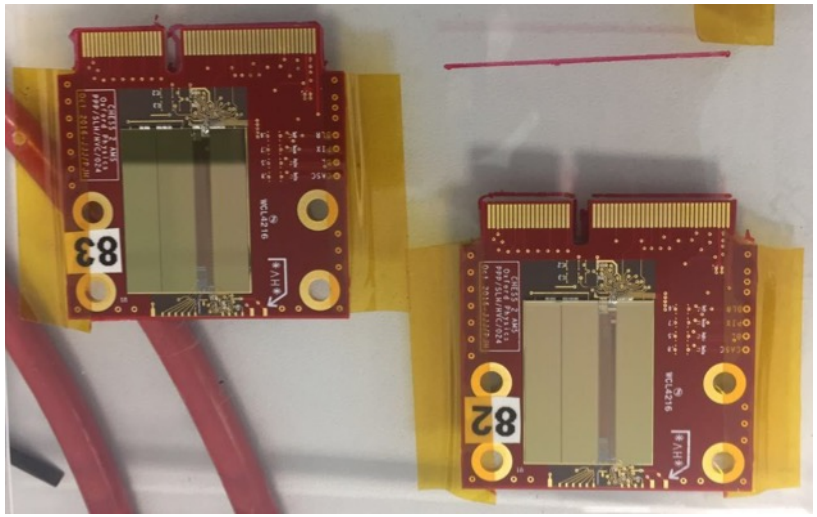
TCT at IHEP

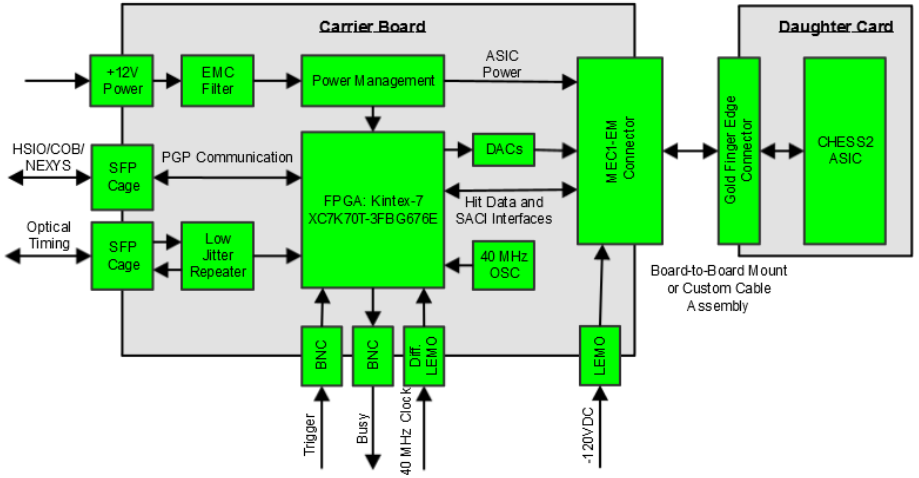
CHESS1-HR CMOS Test

- Use TCT Scan to test CHESS1-HR Sensor Structure



CHESS2-HV Test

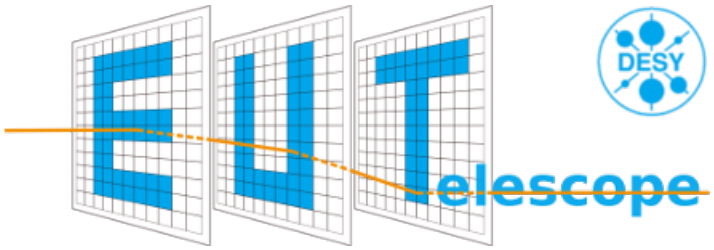


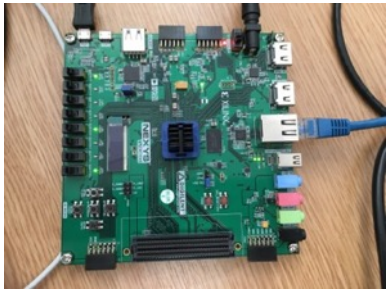


- Based on analog carrier board, revised CHESS1 testboard, will do TCT scan. Finished wire-bonding at RAL, waiting for temporary export permit.
- Setup DAQ to test the digital readout. Participate in the digital ASIC sensor (ABCN') design.

Other Activities

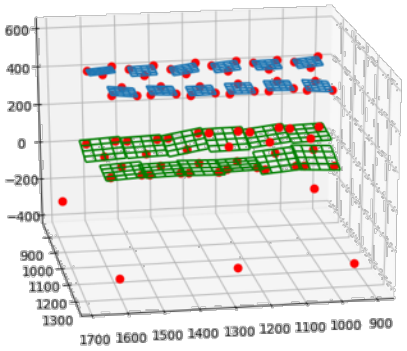
- EUDAQ2.0 and EUTelescope development in collaboration with DESY





- Involved in the ITSDAQ Development

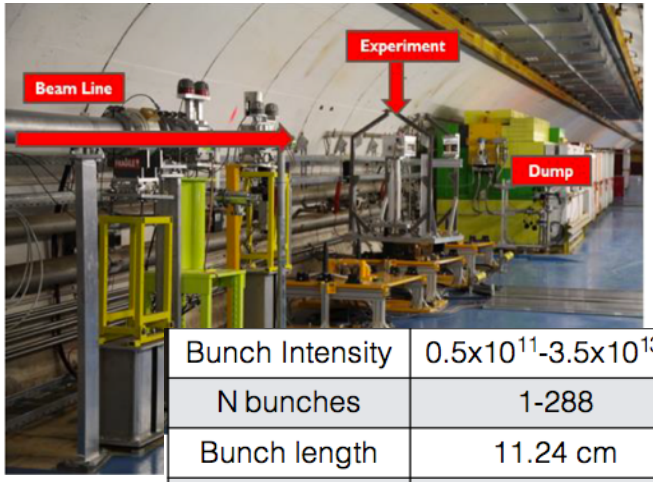
- Glue height measurement with wirebonder
- Study on ATLAS 12A mini-Sensor



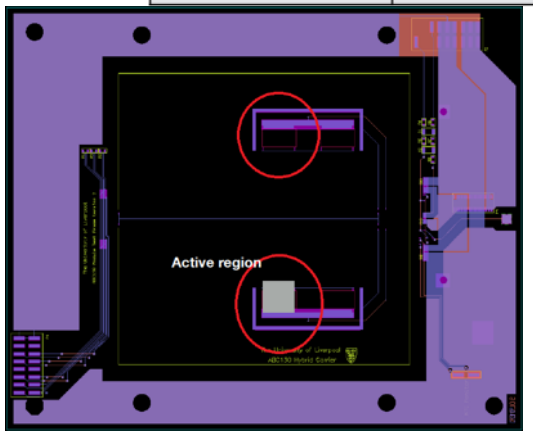
- To build half-ring pixel using dummy modules

Extremely High Radiation Effects on Silicon Detectors

- Study the effects of a beam-loss scenario at the ATLAS
- Assess the tolerance of Strip (Pixel) modules under very high particle fluencies
- Measure the damage threshold using the beam provided by the High-Radiation to Material facility at SPS
- Two tests scheduled in 2017: June and October



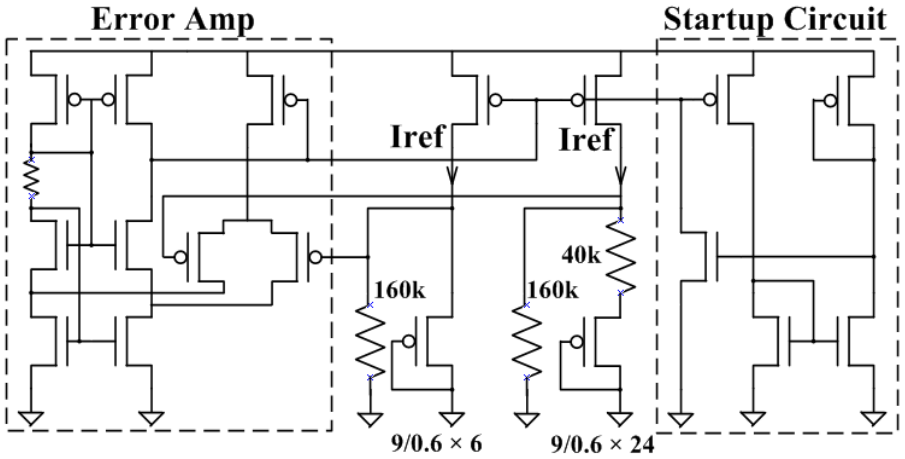
Bunch Intensity	0.5×10^{11}-3.5×10^{13} p
N bunches	1-288
Bunch length	11.24 cm
Bunch spacing	25 ns
Beam size	4.0-0.1 mm
Pulse length	7.2 μs



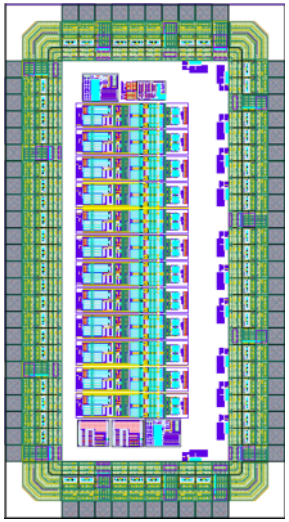
C. Bertella

Contributions to IBL

- We did not sign on the IBL project, but have made direct contributions in several areas:
  - Function blocks design and more for FE-I4 (W. Wei with CPPM)
  - FE-I4 test stand setup and characterization (Y. Lu with LBL)
  - Design of the DRX-12 II chip (Y. Zhang)
  - FPGA firmware development (Histogramer) for Pixel DAQ (J. Hu)
  - Tracking and Vertexing performance studies (Y. Fang with LBL)



Blocks design, simulation and tape-out



DRX-12 II layout

Summary

- China ATLAS ITk team are gaining momentum.
- Actively involved in the following main research topics:
  - Design of the front-end readout ASIC (ABCStar)
  - Assembly and tests of barrel modules
  - Evaluation of CMOS strip sensors
- And more exciting activities to come soon…