Full Silicon Tracking Studies for CEPC

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*http://cepc.ihep.ac.cn/ cepc/cepc_twiki/index.php/Pure_Silicon_Detector

Outline

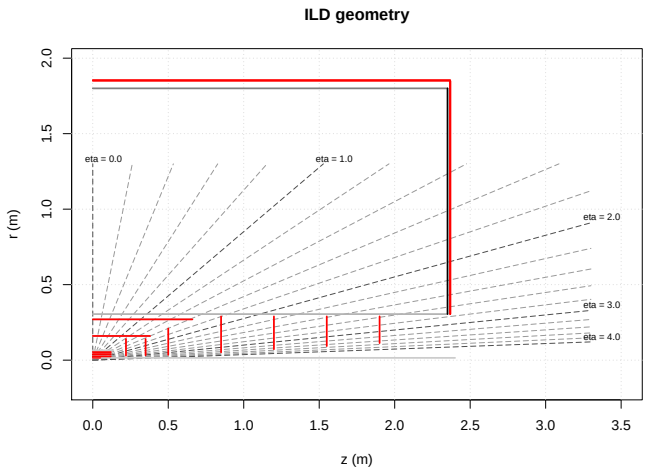
- Introduction.
- Silicon tracker designs and their performances.
- Detector simulation and reconstruction.
- Comparing with CEPC V1 performance.
- Conclusion

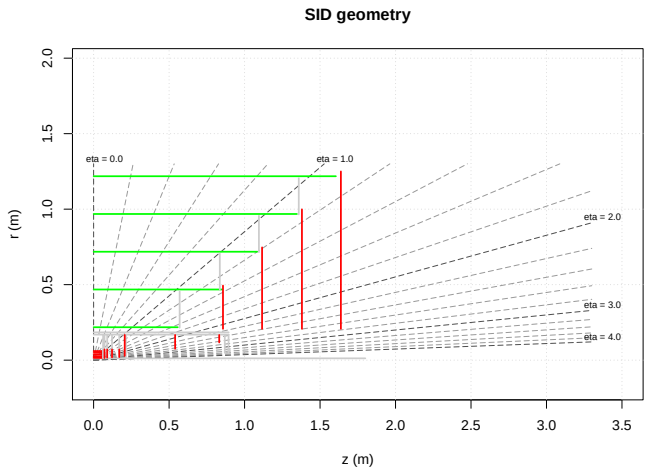
Introduction

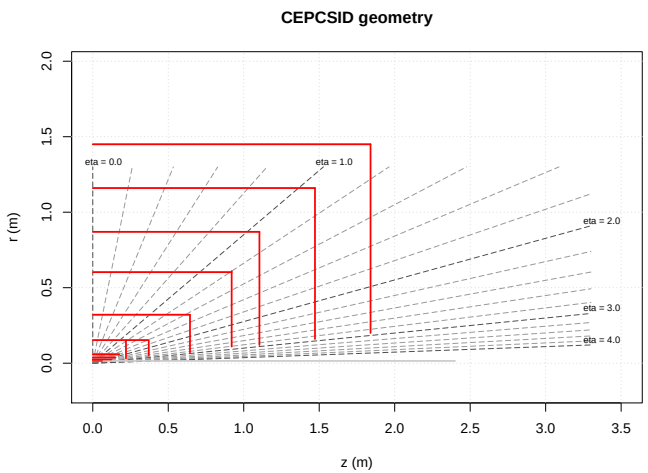
- CEPC full silicon tracker has been implemented in Mokka (Chengdong).
- Based on CEPC V1 silicon elements, we replace TPC with additional SIT layers and FTD endcaps.
- The advantage is to recycle the ILD silicon tracking, which seems work out of box.
- The current design means to prove a principle, but, it's useful for re-optimizing and improve tracking.
- ILC SID vs CEPC: B=5T $\rightarrow$ 3.5(3.0)T, $r_{max} = 1.2 \rightarrow 1.45m$, Barrel strip single $\rightarrow$ double sided.

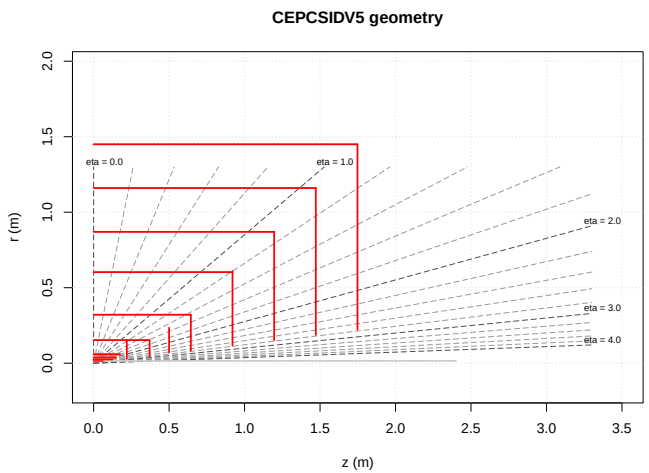
Full Silicon Tracker Concept

- We compared the tracking performance of several design options using a toy MC.









Expected Number of Hits and Radiation Length

- The number of hits and radiation length are comparable to ILC SID.

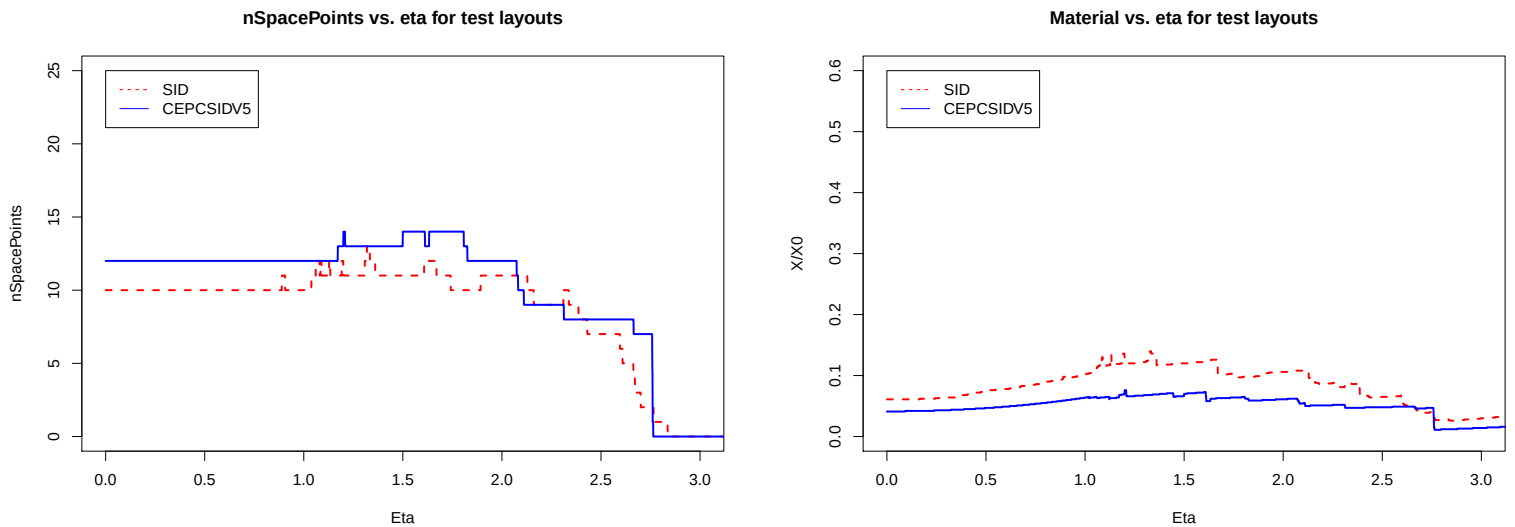


Figure: Expected nhits and radiation length.

Excellent Resolutions

- The expected resolutions from toy simulation is better than ILC SID.

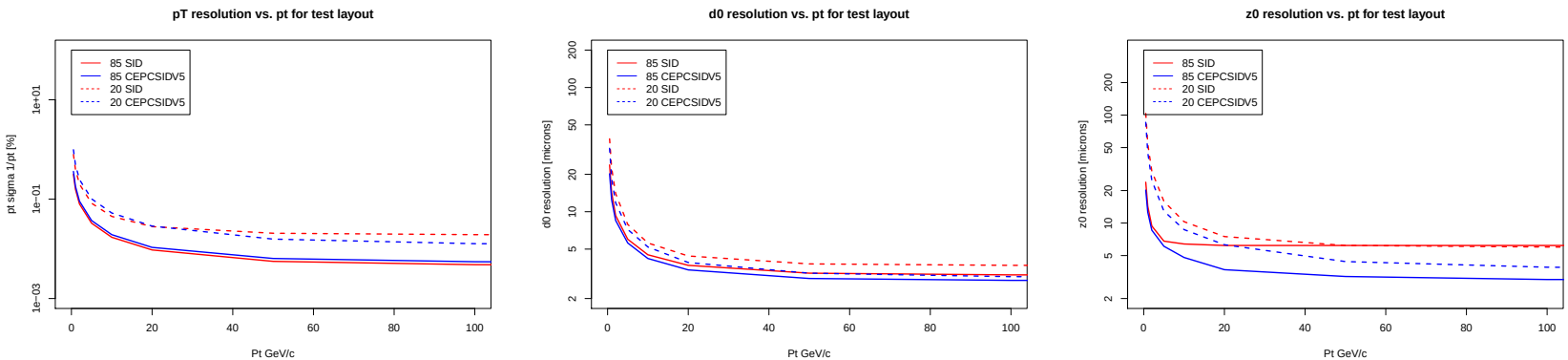
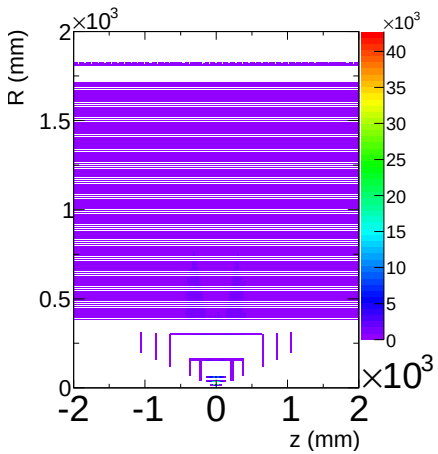


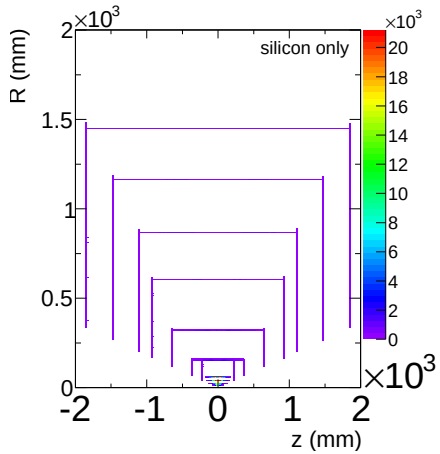
Figure: Resolutions for 1/pt, d0, and z0.

Full Detector Simulation and Reconstruction

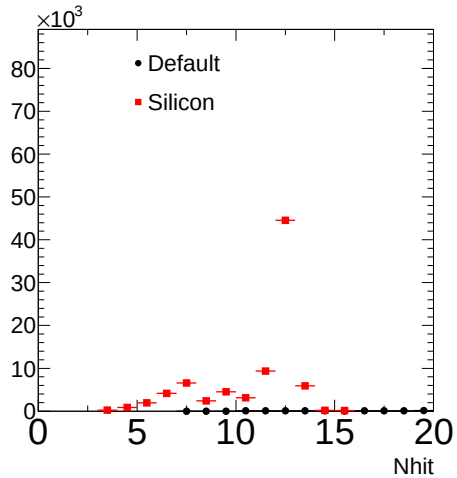
- Generated single muon in CEPC full silicon.
- Reconstructed using Marlin Silicon only.
- Modifying pattern recognition to use more silicon layers.



(a) CEPC V1(Default)



(b) CEPC full silicon



(c) Number of hits

Tracking Efficiencies

- Requiring $P_T > 1.0$ GeV and $0.18 < \theta < 2.96$.
- Efficiency seems bit low compared to CEPCV1, which could be caused by couple issues.

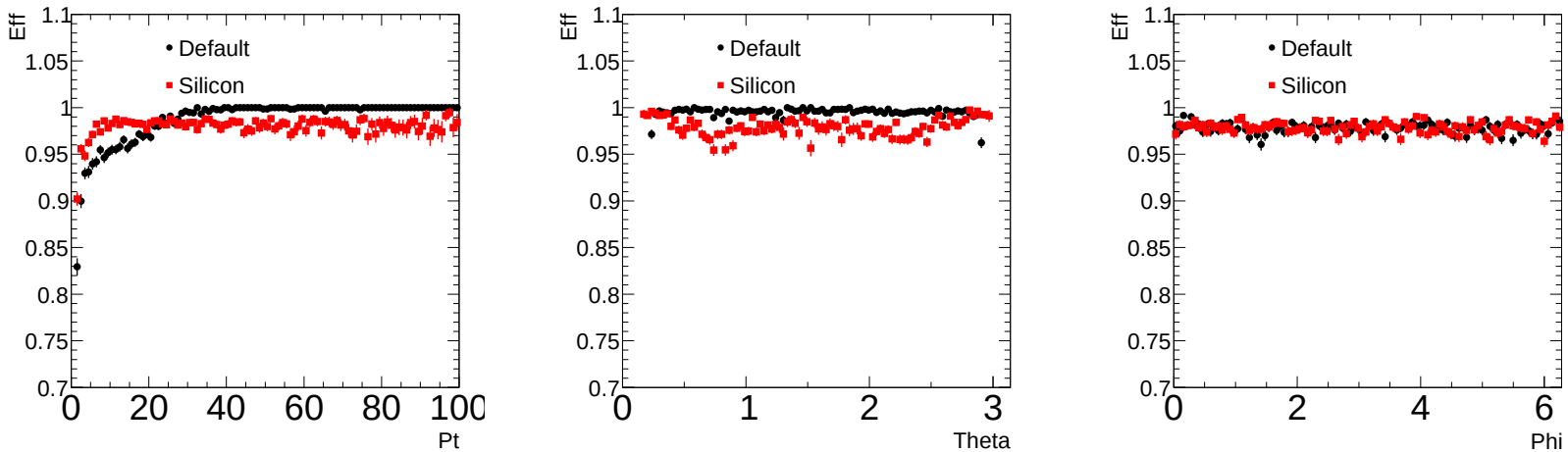
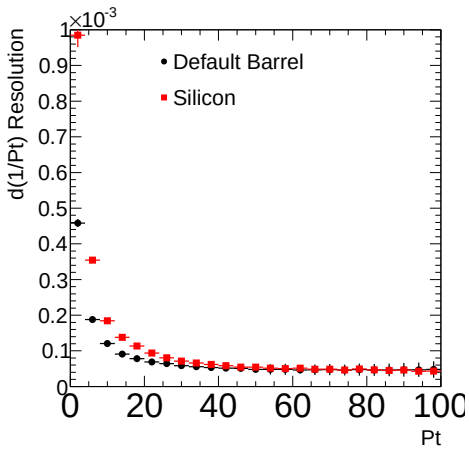
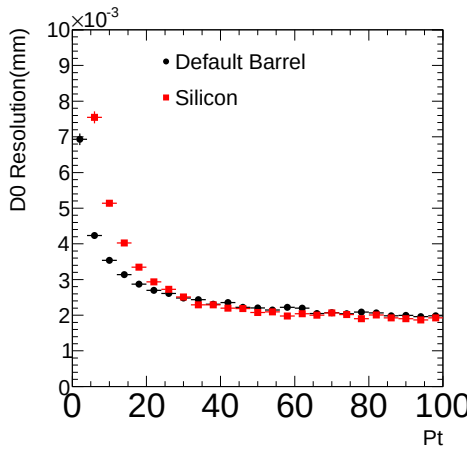
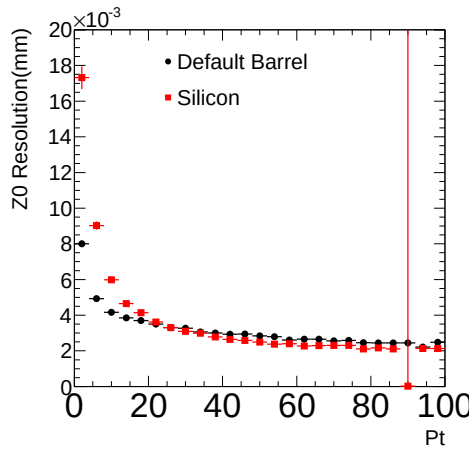


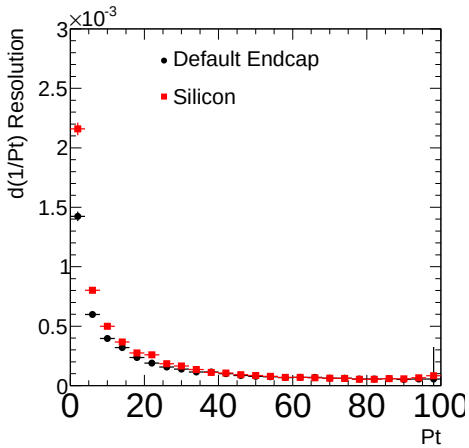
Figure: Efficiencies vs pt, theta and phi

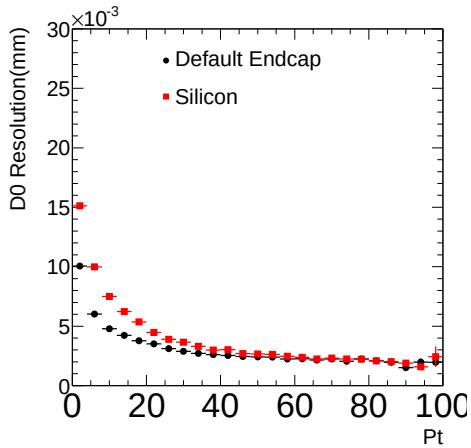
Resolutions











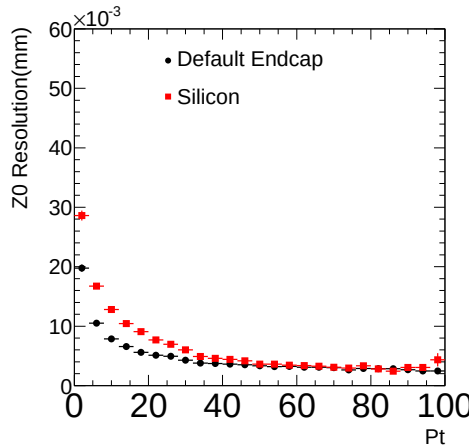


Figure: Pt, d0, z0 resolutions in: Barrel(top), Endcap(bottom).

Issues of Inefficiencies

- Truth tracking runs prefectly, in principle, the hits are available.
- Digitization and clustering are based true hit smearing.(Chengdong).
- Silicon tracking is seeded by set of layers optimized by efficiency and CPU.
- IsOnSurface is buggy for checking strip hits insider the module or not.
  - Petal has different sizes in top and bottom (trapezoid).
  - The modules are tilted for ± 5 degree in endcap and ± 7 degree in barrel
  - A quick fix: $x < 0.5 * max(W_t, W_b) + 0.5 * L * cos(\theta)$
  - Will check once authorized to run jobs at IHEP.

To-DO List

- The concept of full silicon tracker seems work.
- Need to understand these inefficiencies and tracking performances.
- We need to update the studies for CDR.
  - Preparing a set of standard samples for
  - Single track efficiency and resolution
  - Efficiency and fake rates in zh events.
- Silicon usage is 116.6 m^2, about 12% more than CEPC.

Option(m^2)	Pixel(B)	Pixel(E)	Strip(B)	Strip(E)	Total
CEPC	0.138	0.133	82.332	21.244	103.848
CEPCSIV5	0.138	0.291	87.558	28.589	116.577
SIV5/CEPC	1.00	2.19	1.06	1.35	1.12