

Recent progress on cryogenic front-end electronic for CDEX

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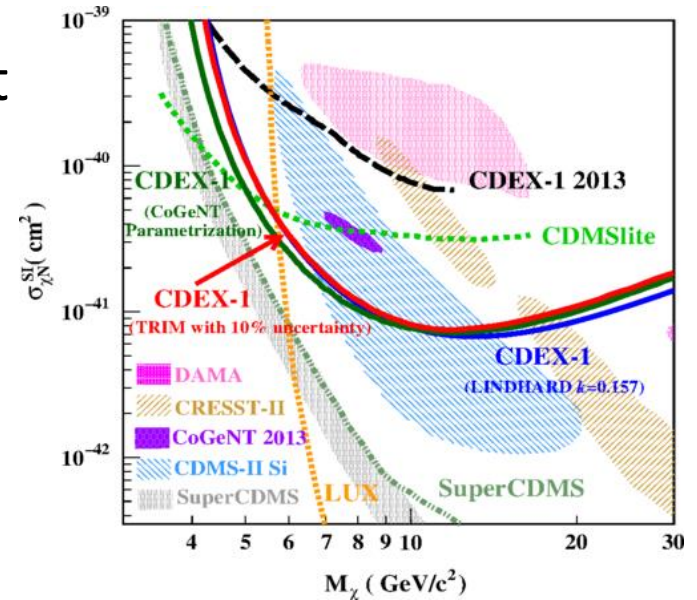
中国锦屏地下实验室
China Jinping Underground Laboratory

Outline

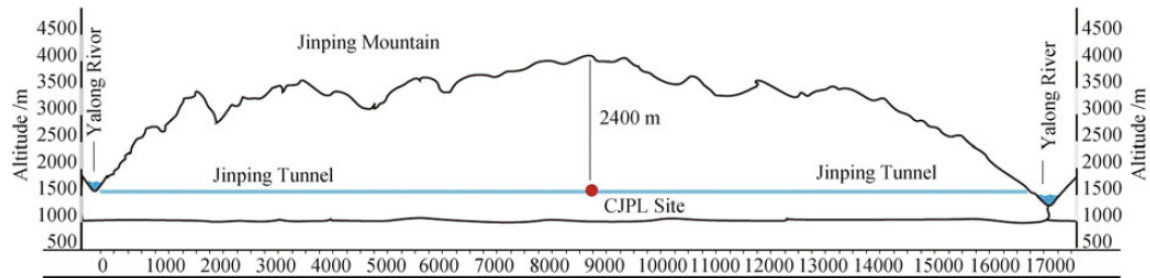
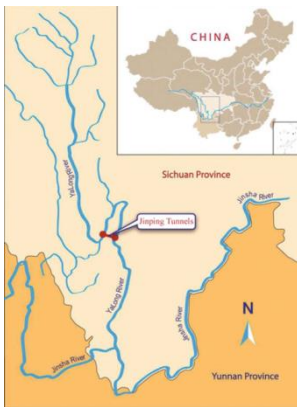
- Introduction
- Progress on cryogenic readout electronics
 - Monolithic CMOS CSA
 - Waveform sampling ADC
- Summary

Introduction

- CDEX: China Dark Matter Experiment
 - Direct detection of light dark matter particles with point-contact high purity germanium detectors with ultralow energy threshold
 - Conducted at CJPL, the world deepest underground laboratory
 - CDEX-1 → CDEX-10 → CDEX-100/200

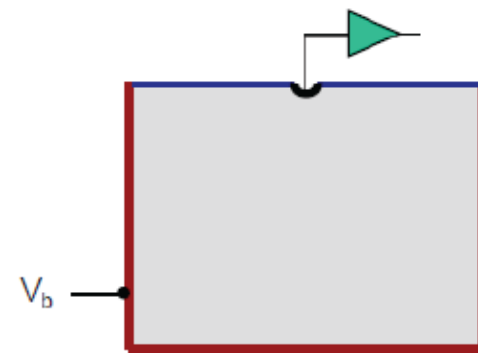
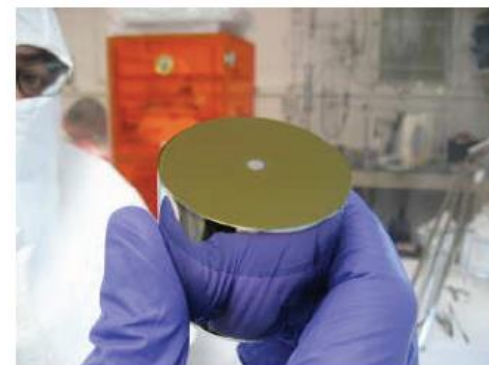
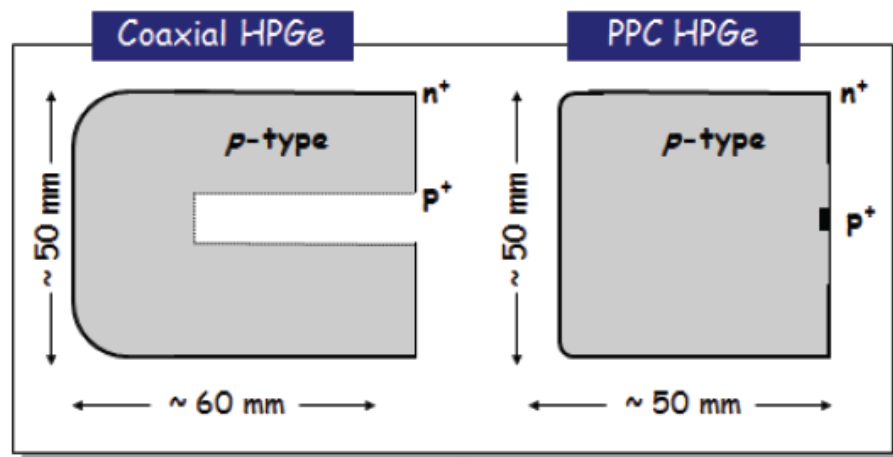


CDEX-1 in 2014



Point-Contact HPGe Detector

- Large crystal with small-contact readout electrode and hence low capacitance, first developed by P.N. Luke @ LBL in 1980s

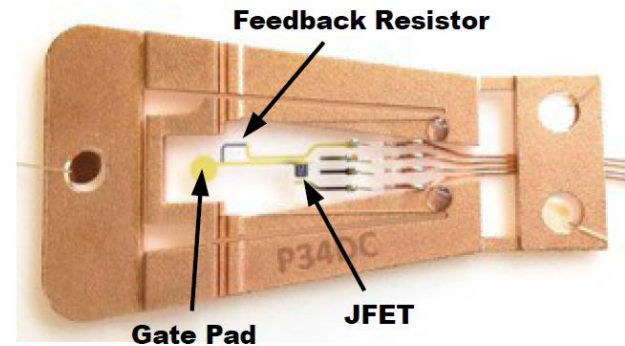
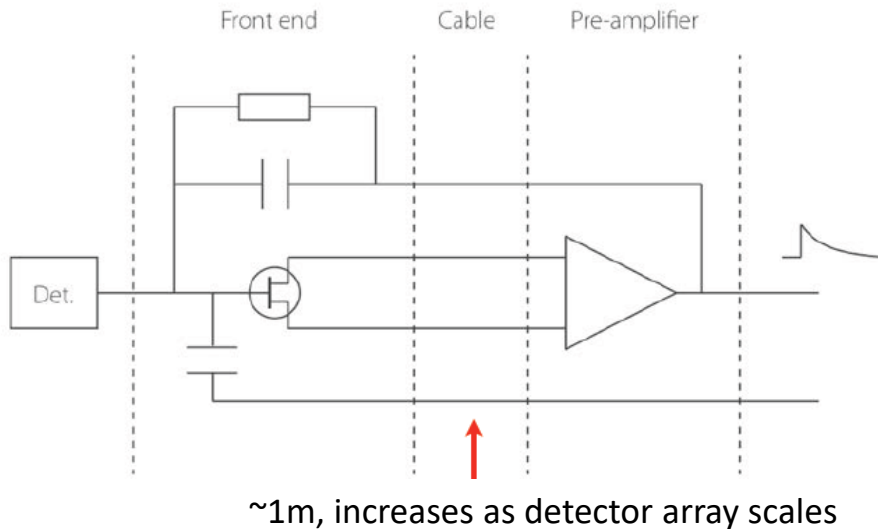


~1pF for 1kg crystal

- Recently regain its interests for DM and neutrino experiments:

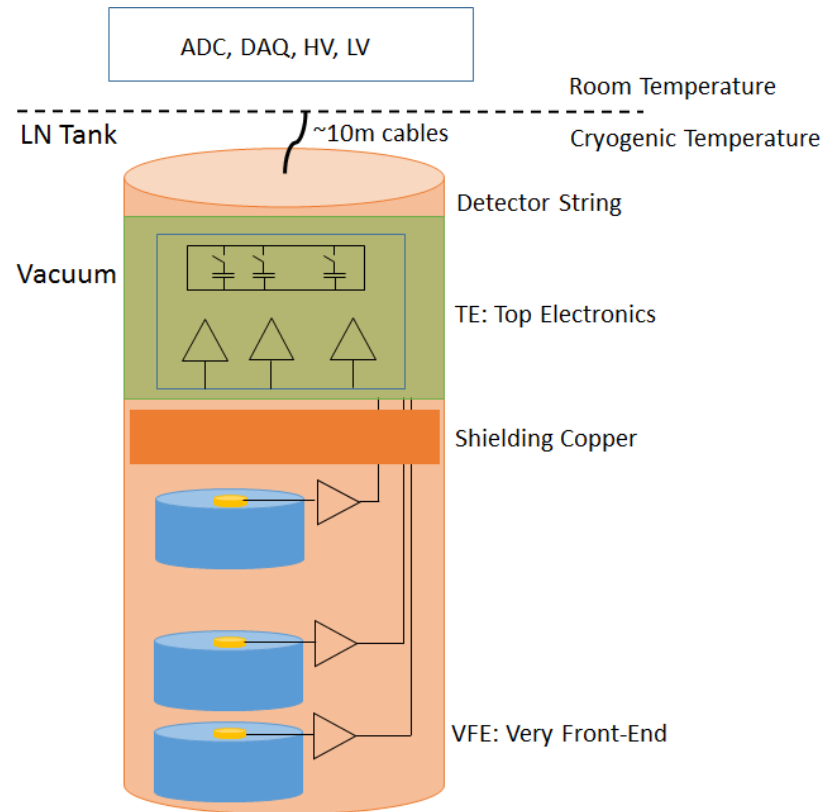
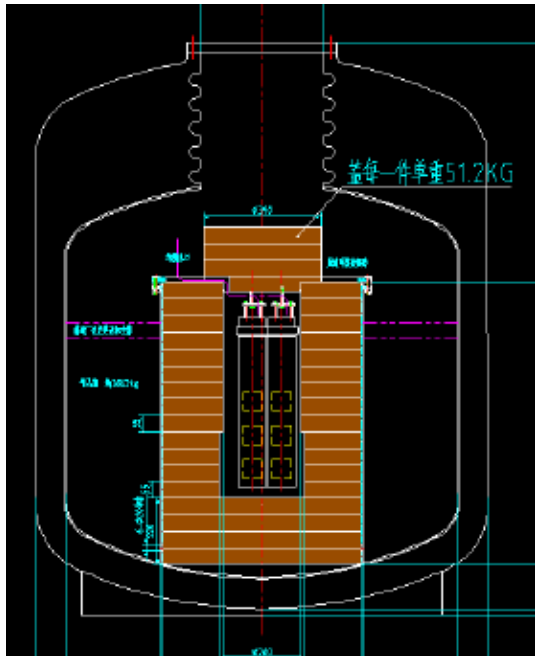
CoGeNT, CDEX, GERDA, MAJORANA

- Requirements for the readout electronics
 - Low energy threshold \rightarrow Low noise
 - Low background \rightarrow low mass and clean material
 - S/B Separation \rightarrow 100MSPS waveform sampling
- Usually JFETs are used due to its low $1/f$ noise



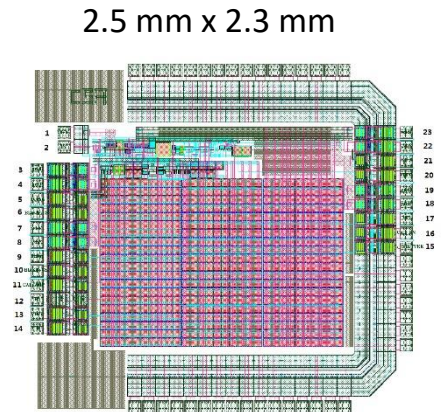
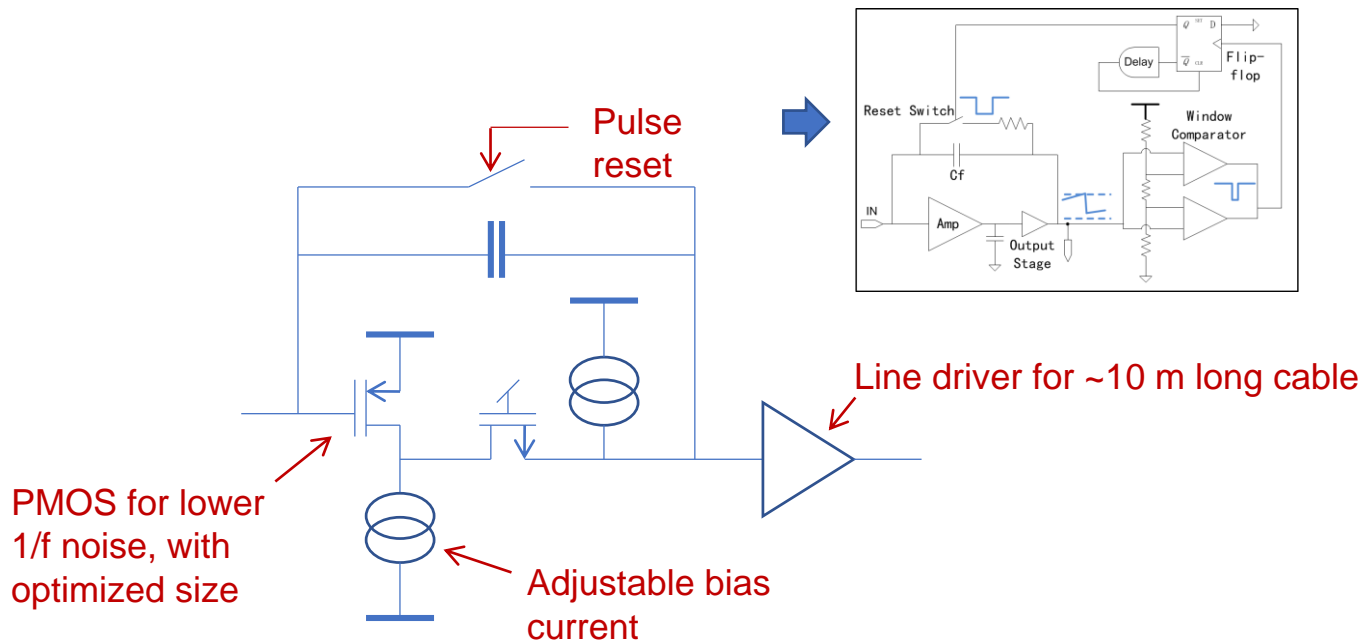
MAJORANA Demonstrator

- Readout scheme for CDEX-large-scale

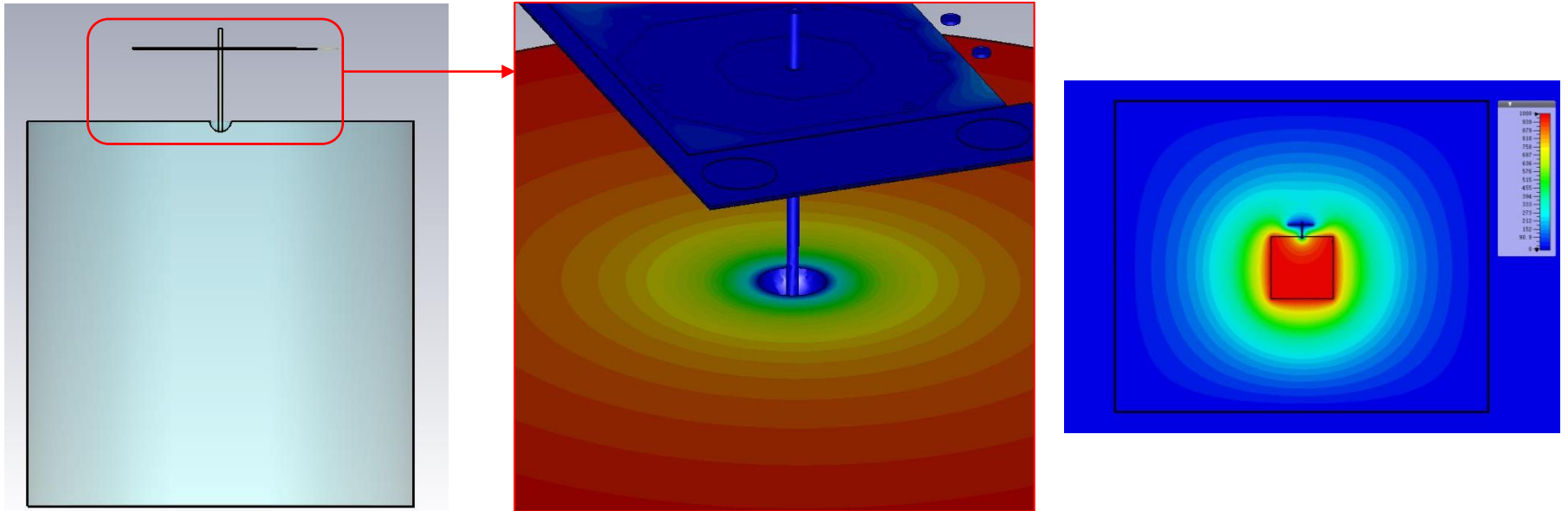


CMOS CSA ASIC for ppc-HPGe

- Scheme and Layout

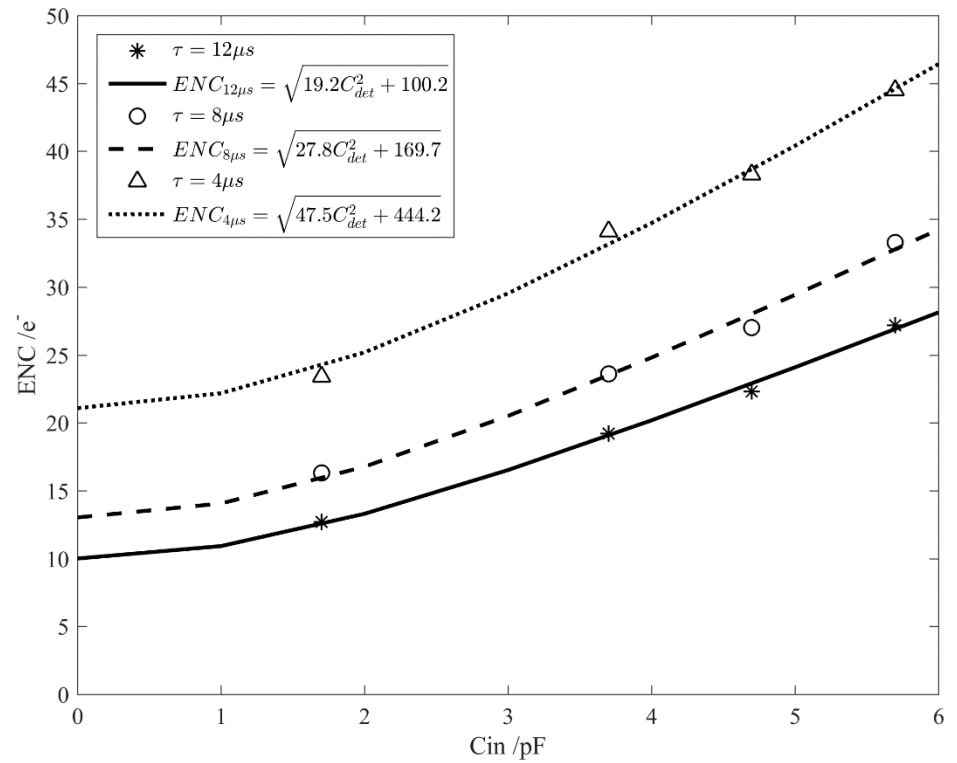
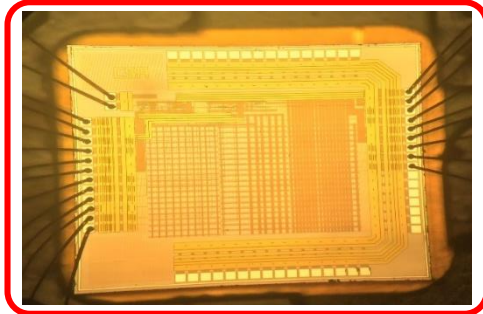
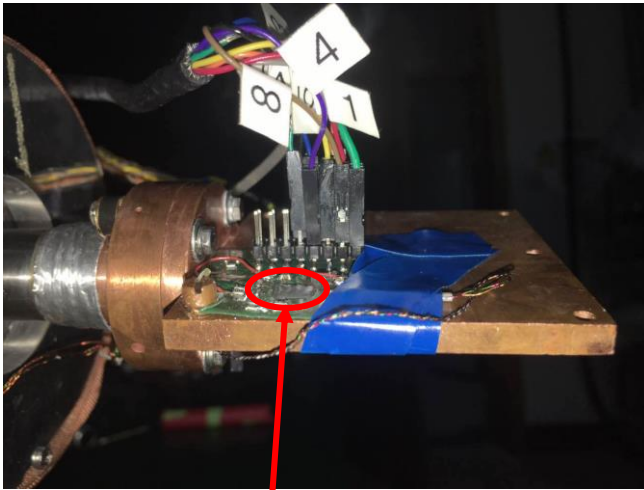


- Noise optimization: capacitance simulation

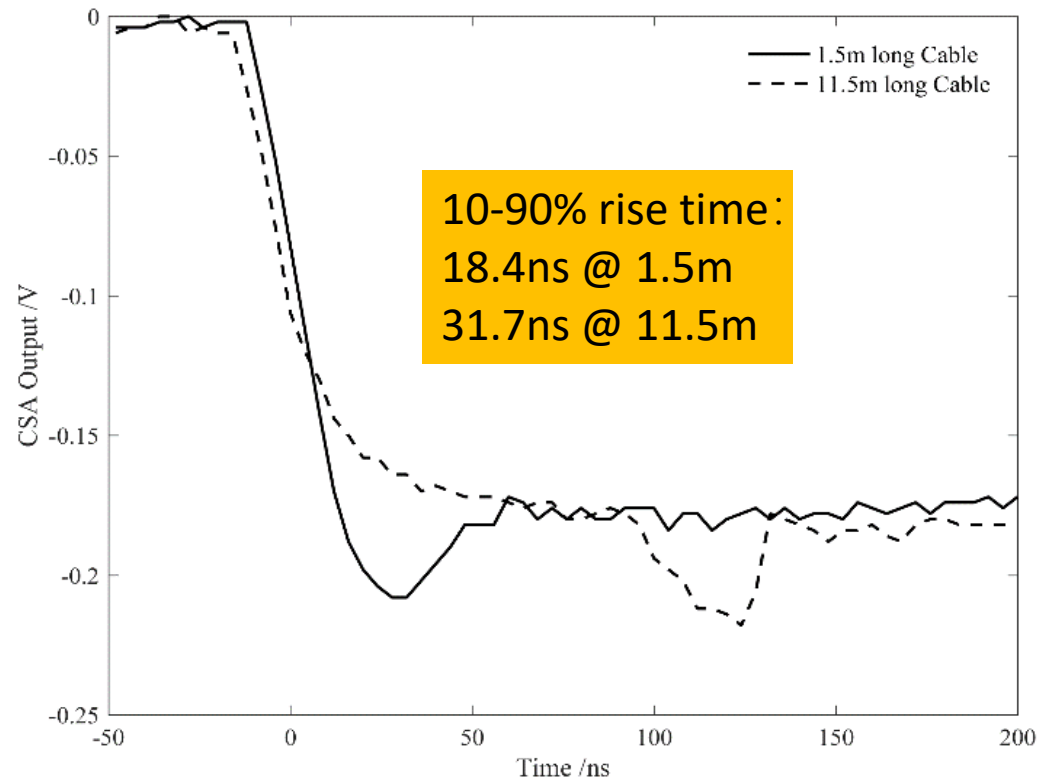


Cap probe: $1.379\text{pF} + 0.363\text{ pF} + 0.294\text{ pF} = 2.04\text{ pF}$

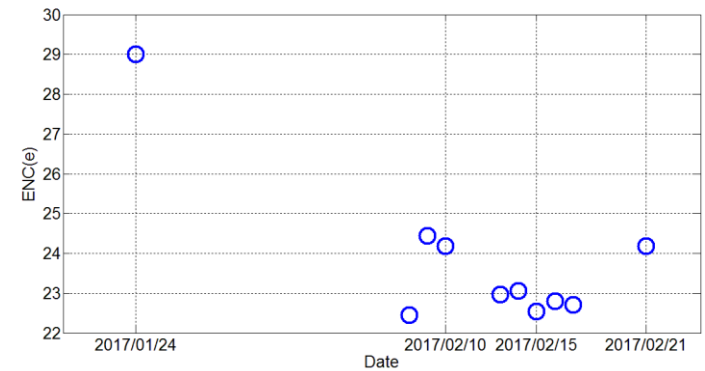
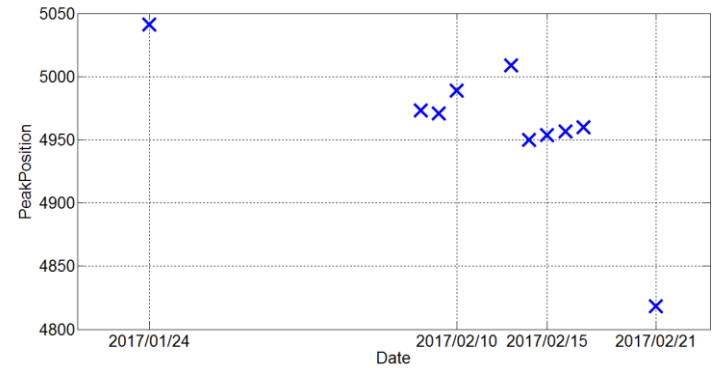
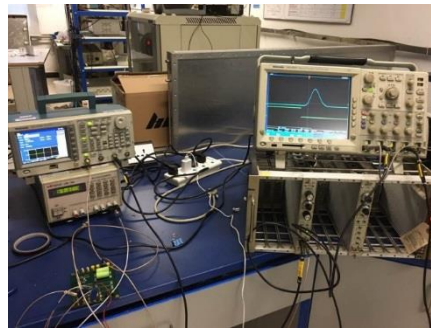
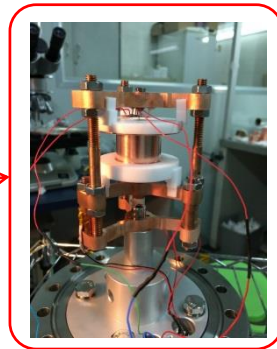
- Noise characterization @ 77K



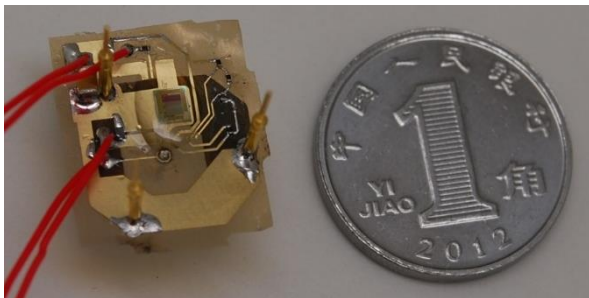
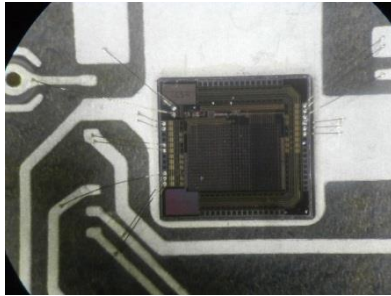
- Cable Drive Capability



- Long-term stability (Preliminary)



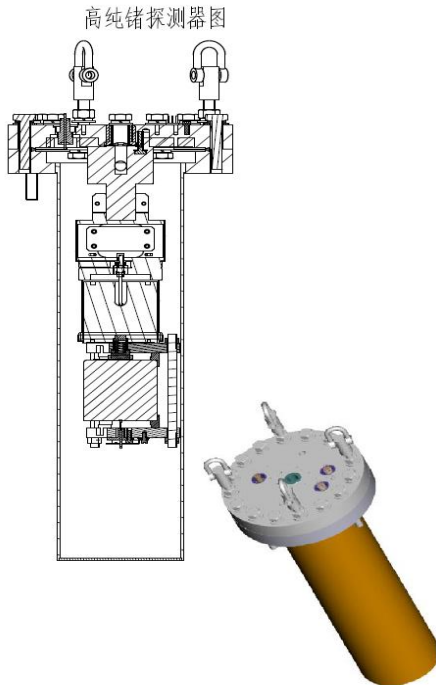
Low Mass ASIC based VFE



- PCB Design:
 - Size: 16 mm x 14 mm
 - Substrate:
 - PTFE Thickness: 51 μm
 - Cu: 18 μm
 - Ni/Pd/Au: $\sim 5\mu\text{m}$
- CSA parameters:
 - Dynamic range: 100 fC/400 fC
 - Pulse Reset
- Other components:
 - 4 resistors (can be omit)
 - 2 capacitors (can be reduced to 1)
- Interfaces:
 - 4 wires: LV(2), CAL, OUT
 - 3 spring needles for ground
 - 1 needle for detector point contact

Test Setup with HPGe detector

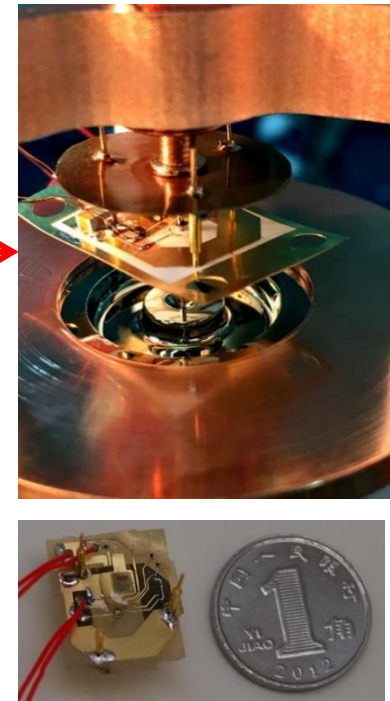
Mechanical Structure



Assembly



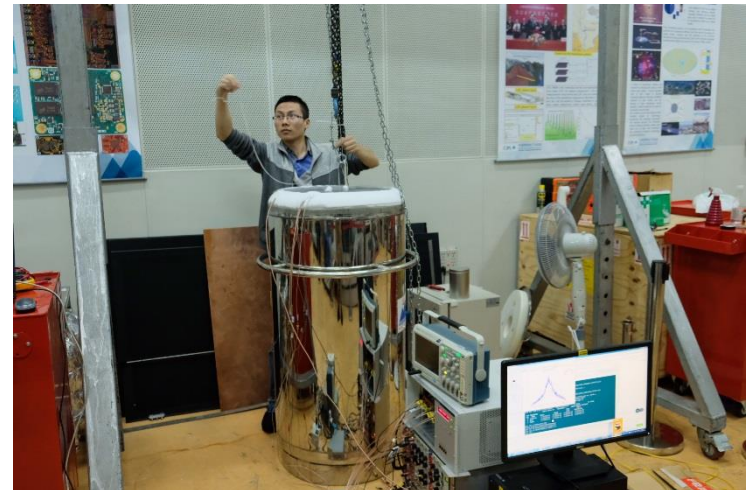
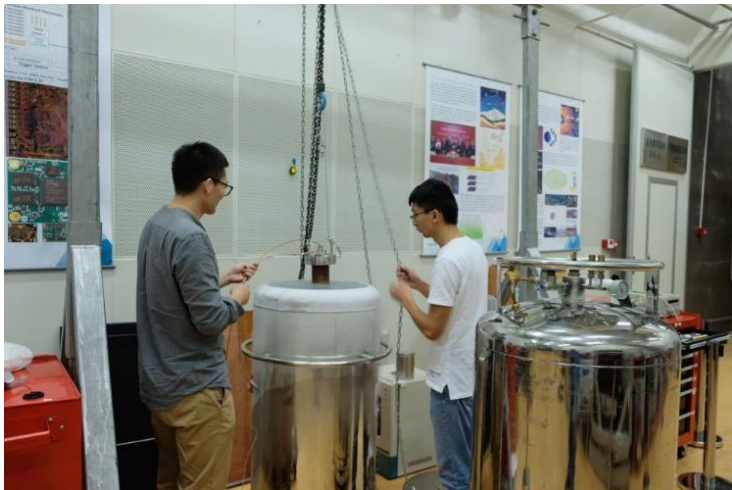
VFE-ASIC



Installation in CJPL

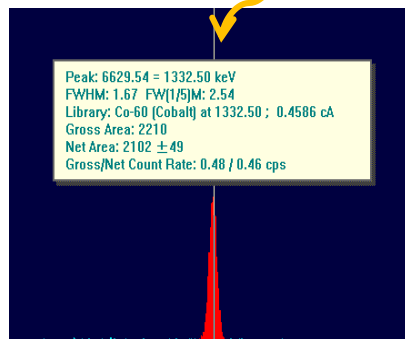
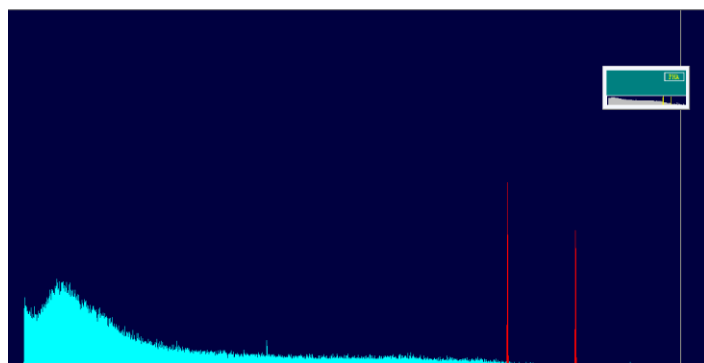


Oct 18, 2017

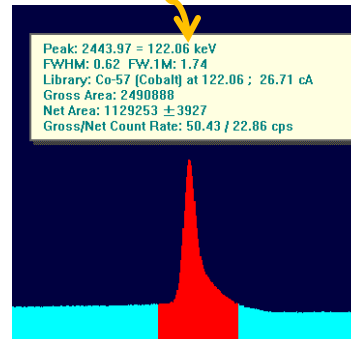
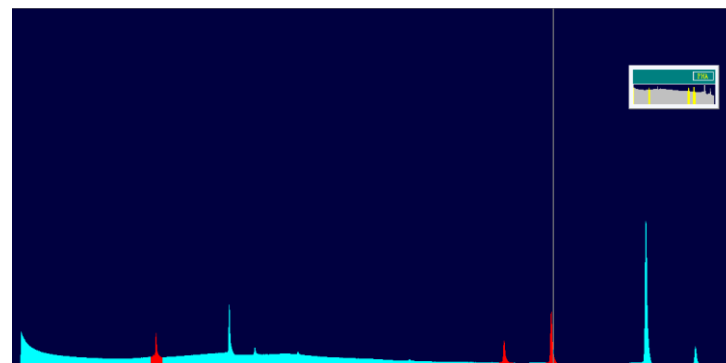


Energy Spectrum

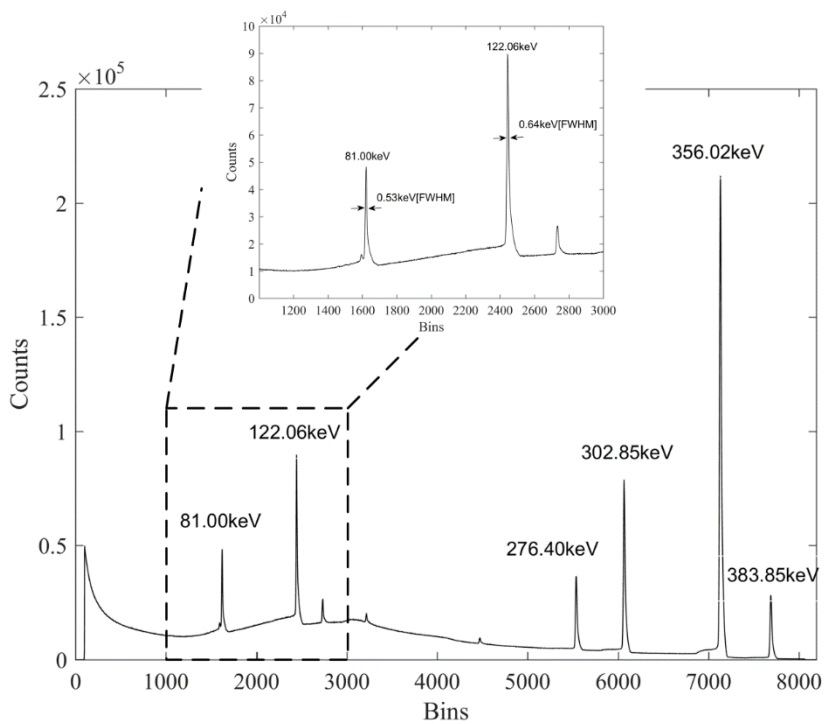
- HPGe Detector:
 - P type, PPC, 50mm x 50mm, 500g



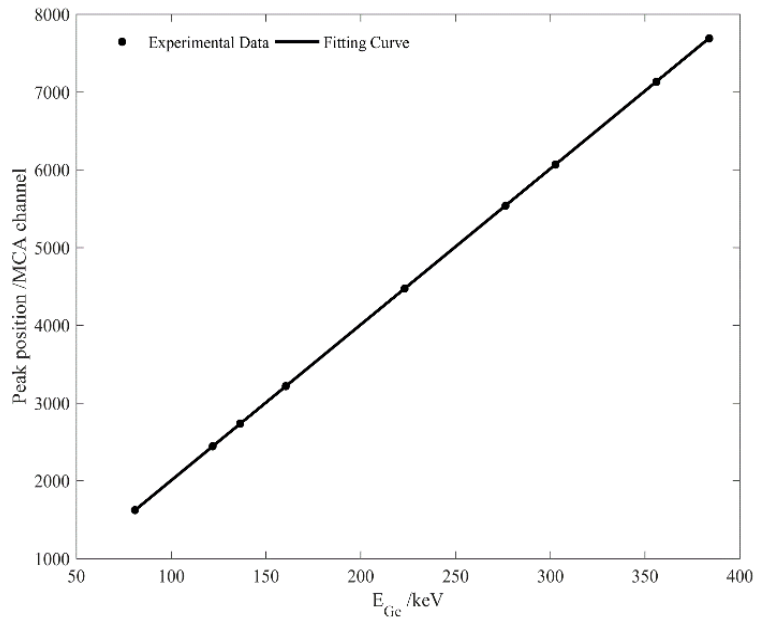
FWHM=1.67keV
@1.332MeV (Co-60)



FWHM=0.62keV
@122.06keV(Co57)

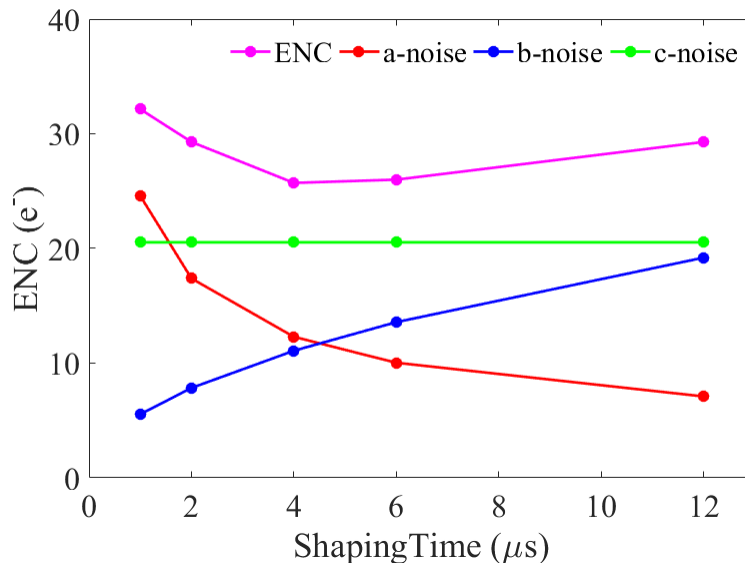


530eV FWHM @ 81keV



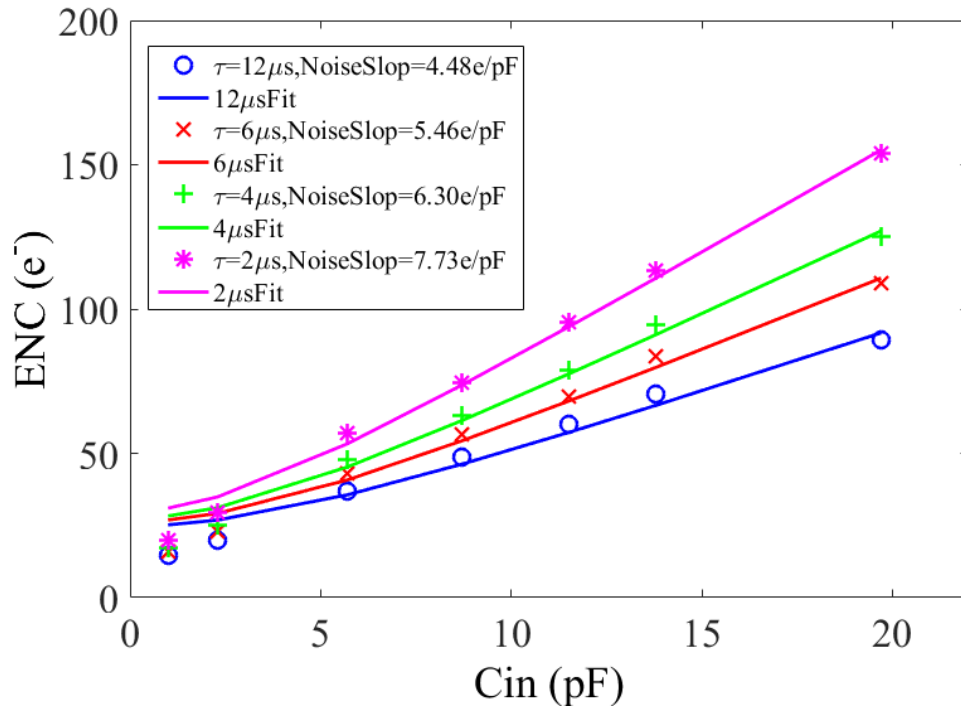
INL < 5.5×10^{-5}

- Noise analysis:
 - Pulser: ENC = 26 e rms (183 eV FWHM)
 - Baseline: ENC = 23.6 e rms (165 eV FWHM)
- Flicker noise contribution: 21 e rms



$$C_{det} \cong 1pF , I_{leak} \cong 10pA$$

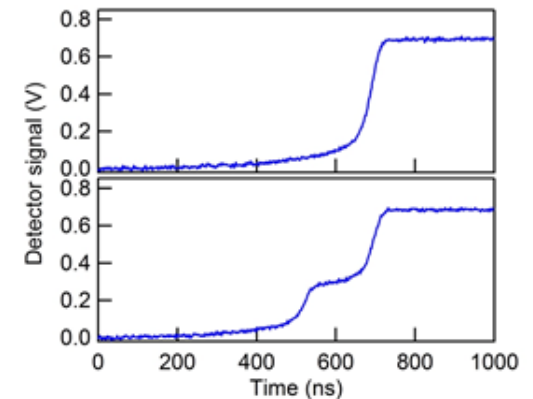
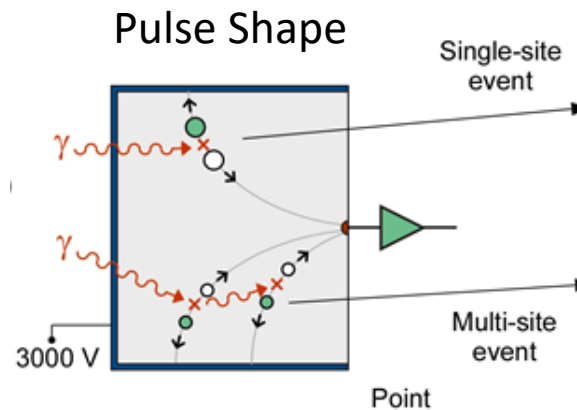
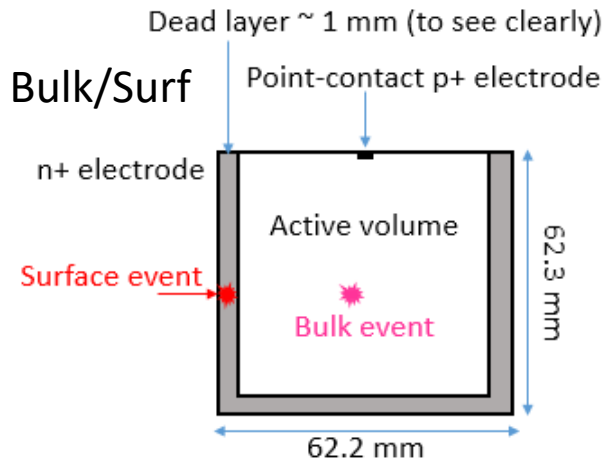
- Dielectric loss noise from Rogers 4350B substrate



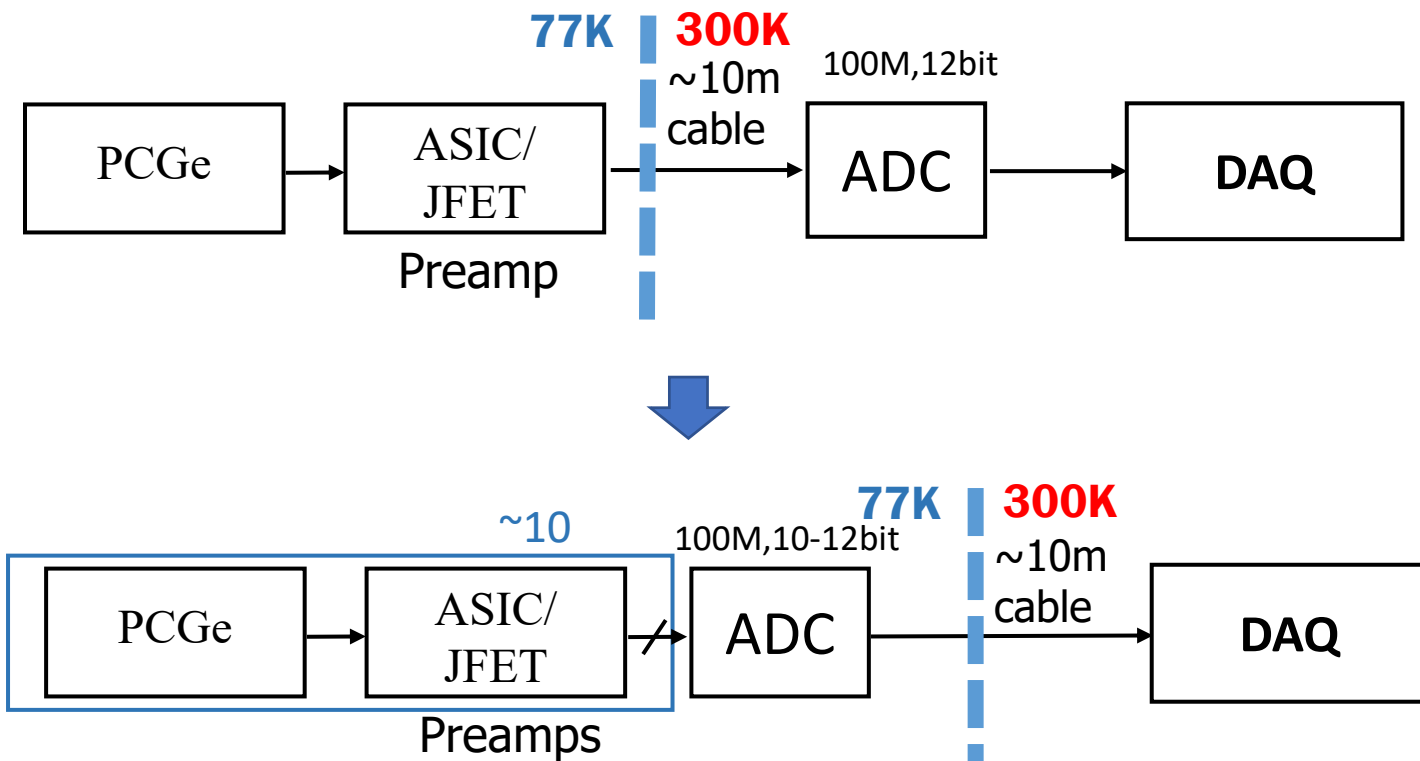
$$ENC_D = \sqrt{2.4kTDC_D} \sim 19.2e @ D = 0.0037, C_D = 1p$$

Cryogenic Waveform Sampling

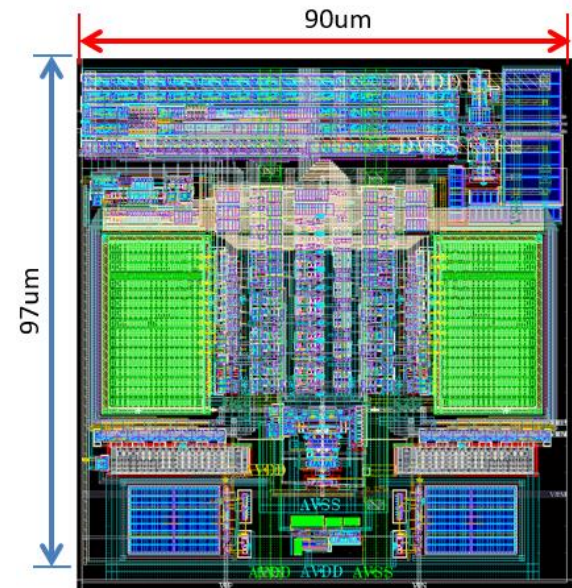
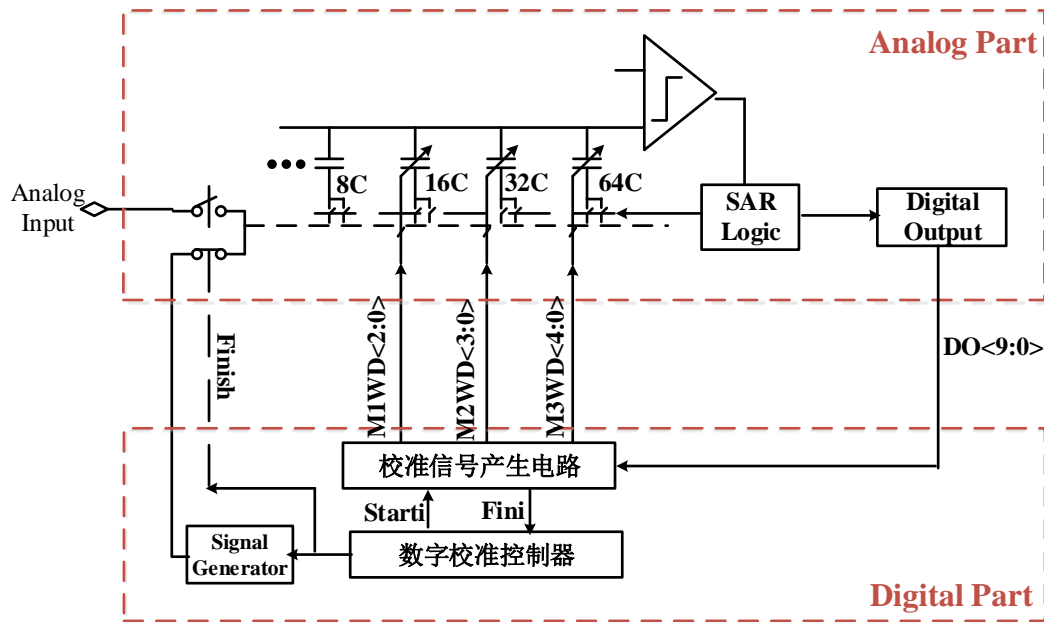
- Digital signal processing are used for HPGe detector signal processing
- Usually need 100MSPS, 12+ bit sampling and digitization



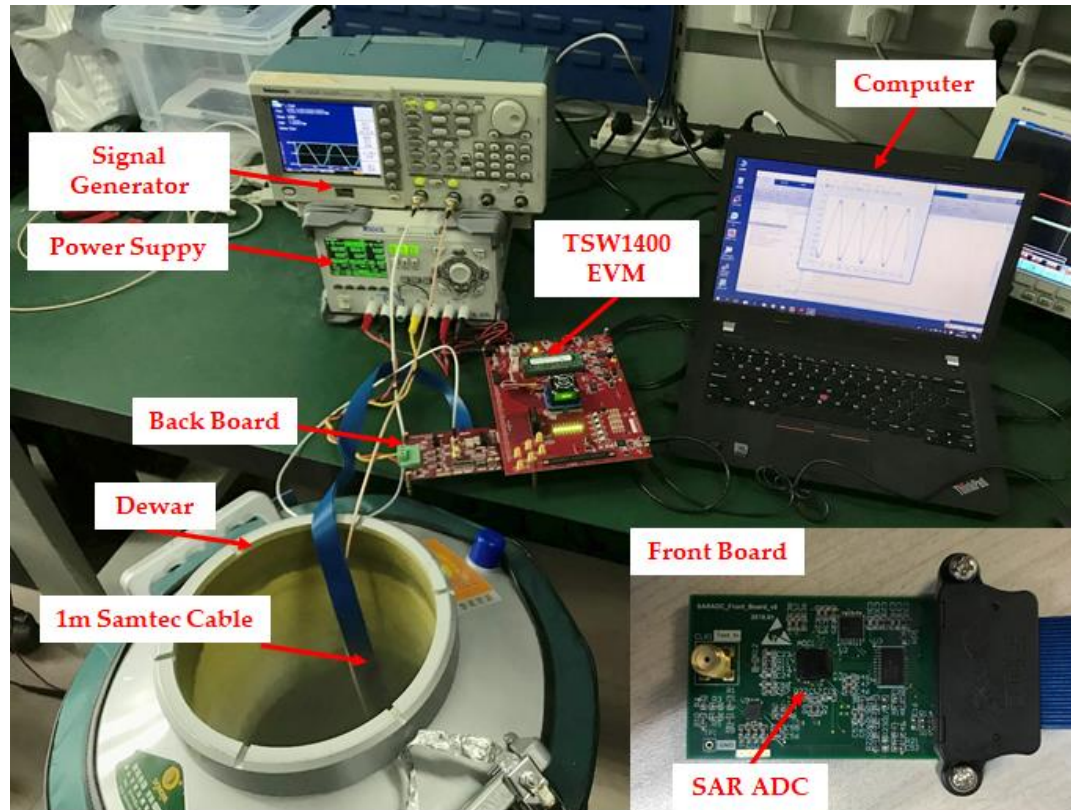
- Cables may contribute significant background for large scale HPGe detector array



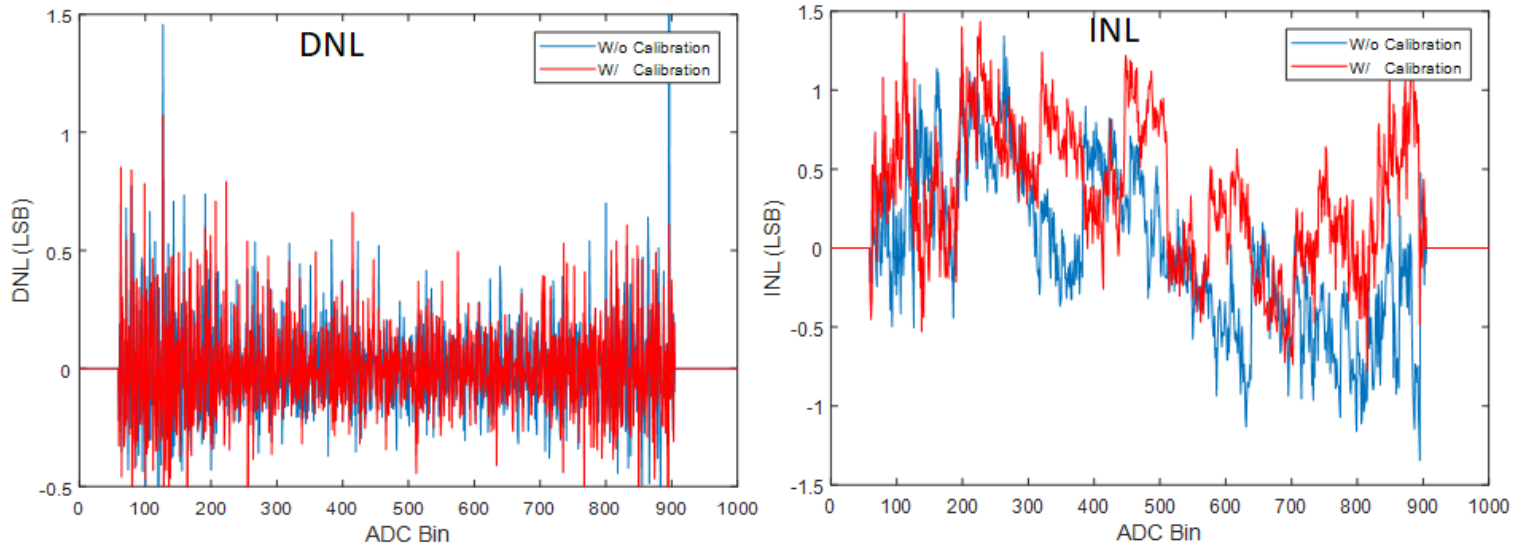
- An ultra-low power SAR-ADC in 65nm process developed by IME Tsinghua



- Cryogenic test setup



- Test results (preliminary)
 - Clock **50MHz**, 0.7V; Input Sine Wave, **2.4MHz**



	RT	LN	RT	LN
	w/o Calibration	w/o Calibration	w/ Calibration	w/ Calibration
ENOB	9.01	8.73	9.09	8.79

Summary

- R&D Progress on CDEX readout electronics:
 - A low noise CMOS CSA working at 77 K has been successfully developed for HPGe detector for CDEX
 - A low mass front-end electronics based on the ASIC has also been developed and tested with a large volume (0.5 kg) home made HPGe detector
 - Cryogenic performance of a waveform sampling SAR ADC has been characterized and shows great potential for large scale HPGe detector array readout
- Towards custom designed readout electronics for CDEX-100
 - Summarizing R&D options → TDR
 - Building small scale of prototypes

THANKS