粒子物理前沿卓越创新中心
第四届青年骨干评审

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中科院高能所
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Contributions to the CEPC R&D

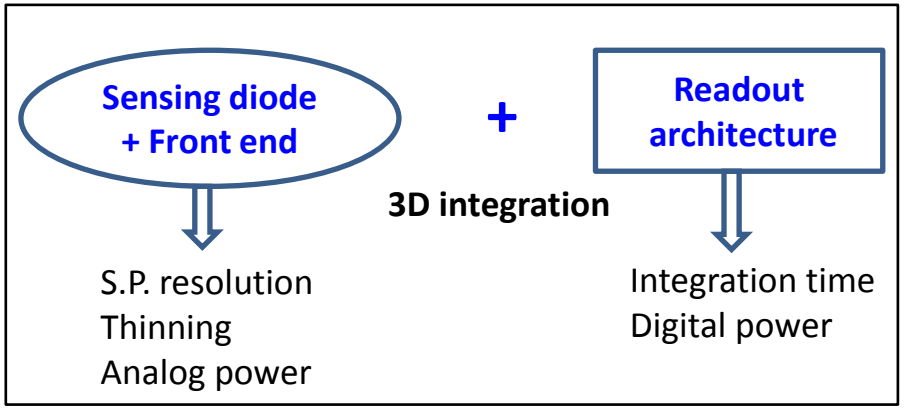
1. Development of CMOS pixel sensor
   - MOST国家重点研发计划 (2016-2021)
   - R&D roadmap
   - CDR editor

2. SOI R&D for CEPC vertex
   - NSFC面上项目（2016-2019）
   - Chip thinning down to 75 μm
   - Single point resolution 2.3μm

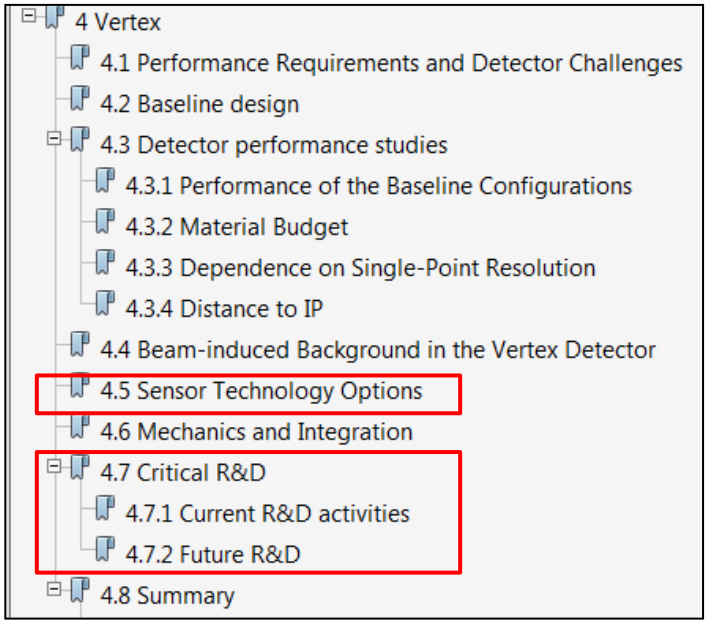
3. Development of SOI technology
   - NSFC面上项目（2014-2017）
   - Synchrotron beam test

Contributions to the CEPC R&D (1)

- Development of CMOS pixel sensor
  - MOST国家重点研发计划 (2016-2021)
  - R&D roadmap
    - Coordinate design force to solve critical issue
  - CDR editor
    - Feedback from mini-review in Nov.



R&D roadmap proposed at CEPC workshop Wuhan, Apr. 2017



Chapter of Vertex in CEPC CDR

Contributions to the CEPC R&D (2)

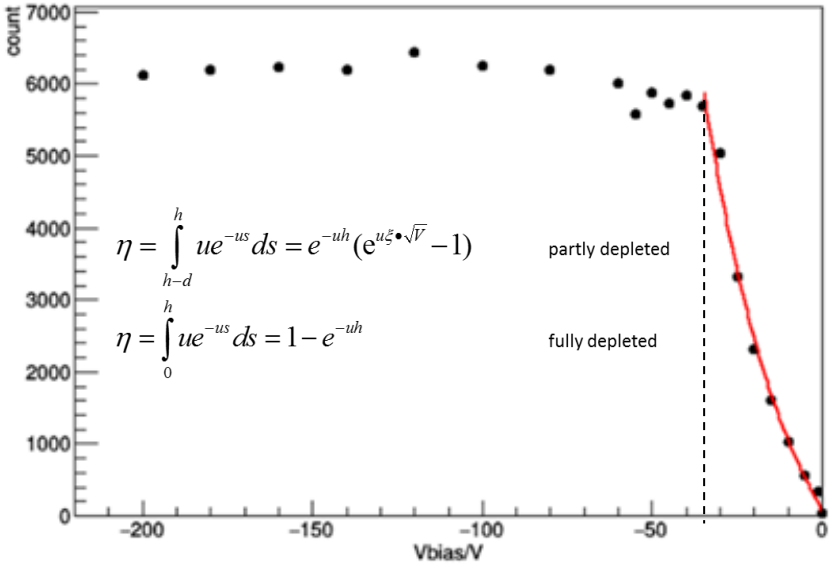
- SOI R&D for CEPC vertex.
  - NSFC面上项目（2016-2019）
  - Chip thinning down to 75 μm
  - Single point resolution 2.3μm

ALICE/ITS upgrade芯片 | CEPC芯片

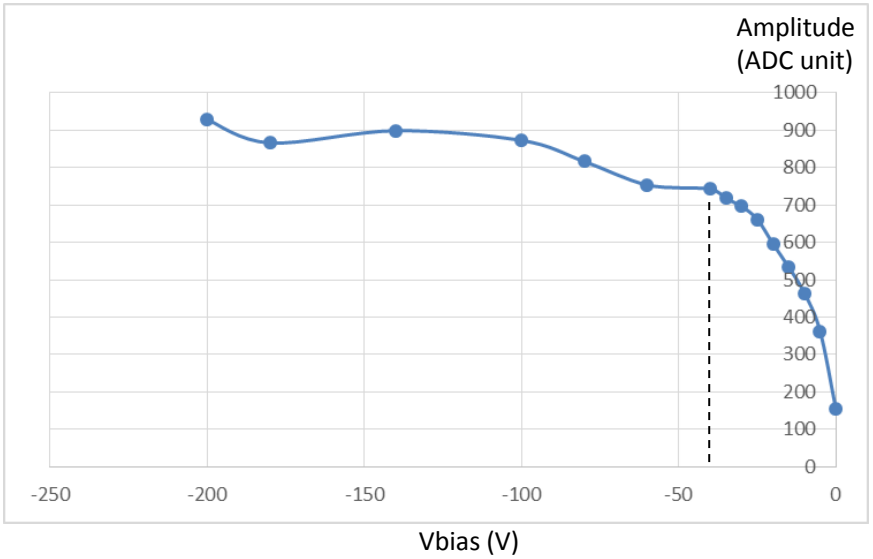
	ASTRAL	ALPIDE	CPV
Process technology	*0.18 μm* CMOS		0.2 *μm* SOI
Readout strategy	Rolling shutter	asynchronous	Rolling shutter
Readout time	20 μs	<2 μs	
Power	85 mW/cm^2	39 mW/cm^2	Analog power < 10 mW/cm^2
Pixel size	*22 × 33 μm^2*	*28 × 28 μm^2*	*16 × 16 μm^2*
Spatial resolution	*≈ 5μm*		Expected < 3*μm*
Total signal for MIP	*≈1200 e$^-$ (20μm* epi-layer partly depleted)		*≈4000 e$^-$* (back thinning to 50*μm*, fully depleted)

Chip thinning

- Thinning and back-side processing via SOIPIX collaboration
  - 75um thin chips wire-bonded at HOME (董静)
  - Full depletion verified



Photon rate vs bias voltage
(^{55}Fe source 5.9keV X-ray)

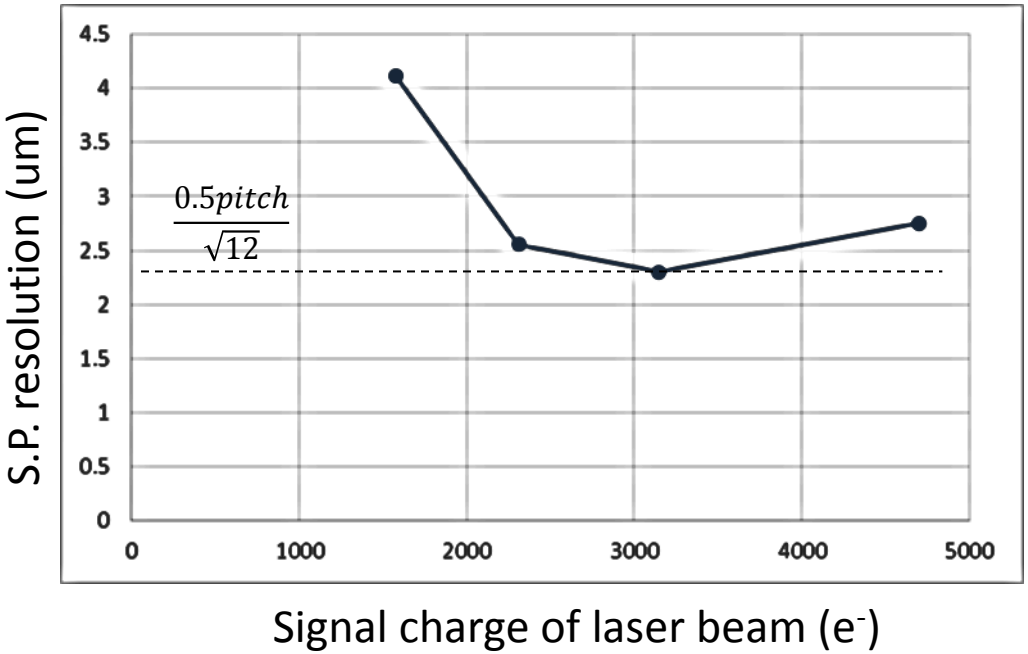


Signal amplitude vs bias voltage
(1064nm Laser pulse)

Single point resolution

- Measured with infrared laser beam
  - 2.3um achieved at the optimum signal/threshold ratio
  - To be presented at HSTD11&SOIPIX2017, Dec. 10-15, 2017

S.P. resolution measured with fixed threshold ~ 100e$^-$



Contributions to the CEPC R&D (3)

- **Major contribution** to the development of SOI technology.
  - NSFC面上项目（2014-2017）
  - Synchrotron beam test in Dec. 2016, data analysis finished in 2017
  - **A summary paper to be submitted to RDTM**

国外同行Takaki Hatsui (spring-8)对相关工作的评价：

发件人: "Takaki Hatsui" <hatsui@spring8.or.jp>
发送时间: 2016年12月9日 星期五
收件人: yplu@ihep.ac.cn
抄送:
主题: On your paper on double SOI

Dear Yunpeng Lu,

I have read your interesting paper appeared in NIMA Vol 831.
The noise of 113 e-rms with beautiful S curve is the **milestone** in SOI process.

Congratulations!

Best regards,

Takaki

Selected publication and talks

[1] Y. Zhou, **Y. Lu***, et al., 2017 **JINST** 12 C01037

[2] Study of SOI pixel for the vertex, **CEPC workshop, Wuhan**, April 19-21, 2017

[3] An SOI pixel sensor with in-pixel binary counter, **TIPP, Beijing**, May 22-26, 2017

[4] **Overview of SOI development**, **invited** by CEPC international workshop, **Beijing**, Nov. 6-8, 2017

[5] A prototype SOI pixel sensor for CEPC vertex, presented by Z. Wu, accepted as oral presentation, **HSTD11&SOIPIX2017 joint workshop,** Okinawa, Japan, Dec. 10-15, 2017

[6] Performance evaluation of an SOI pixel sensor with in-pixel binary counters, presented by L. Song, accepted as oral presentation, **HSTD11&SOIPIX2017 joint workshop**, Okinawa, Japan, Dec. 10-15, 2017

Plan for next year

- Test of CMOS pixel sensors
  - Chips designed in 2015/2017
  - 所创新项目结题
  - MOST国家重点研发计划中期考核

- CMOS/SOI Design & submission in 2018
  - One submission to be secured
  - Average submission interval: 2years -> 1year

致谢

- 感谢欧阳群研究员
- 感谢核探测与核电子学国家重点实验室

- 感谢评委给我展示自己的机会！