“粒子物理前沿”卓越创新中心
年度考评汇报

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清华大学

12/1/2017

概要

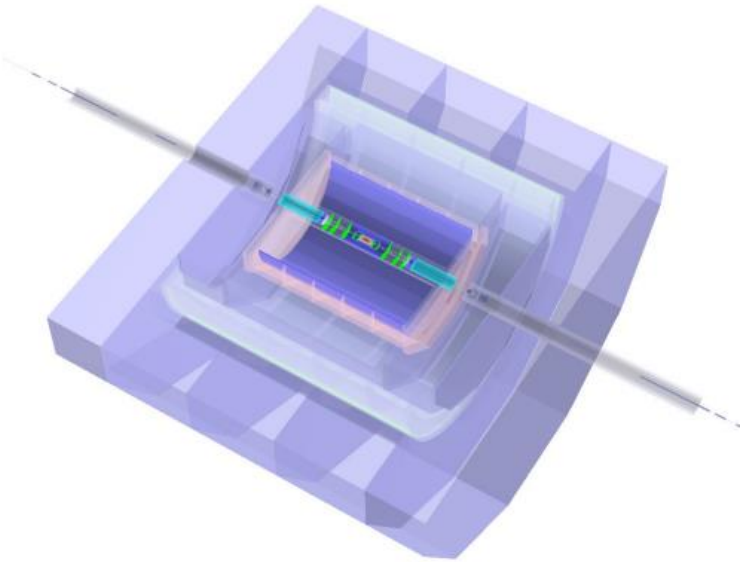
- 个人基本情况
- 学术研究
  - 低功耗高集成度大型TPC读出ASIC芯片研制
  - 高纯锗探测器低温低噪声低本底前端电子学
  - 用于PET/TOF-PET的SiPM读出ASIC芯片研制
- 发表论文与承担项目

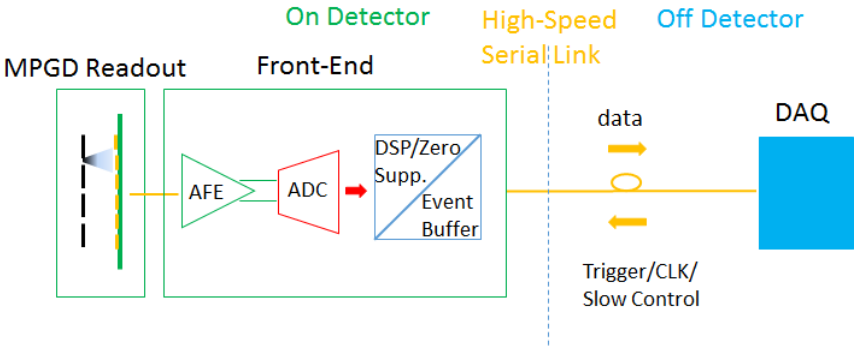
个人基本情况

- 工作情况：
  - 清华大学工程物理系，副教授
  - 主要从事用于粒子物理实验和辐射成像的核电子学技术研究，重点是核电子学专用集成电路（ASIC）
- 教育经历：
  - 2002-2005: Ph.D, Engineering Physics Tsinghua University
  - 2000-2002: Master of Engineering, Quantum Engineering and System Science, University of Tokyo
  - 1995-1999: Bachelor, Engineering Physics, Tsinghua University

学术研究：TPC读出ASIC

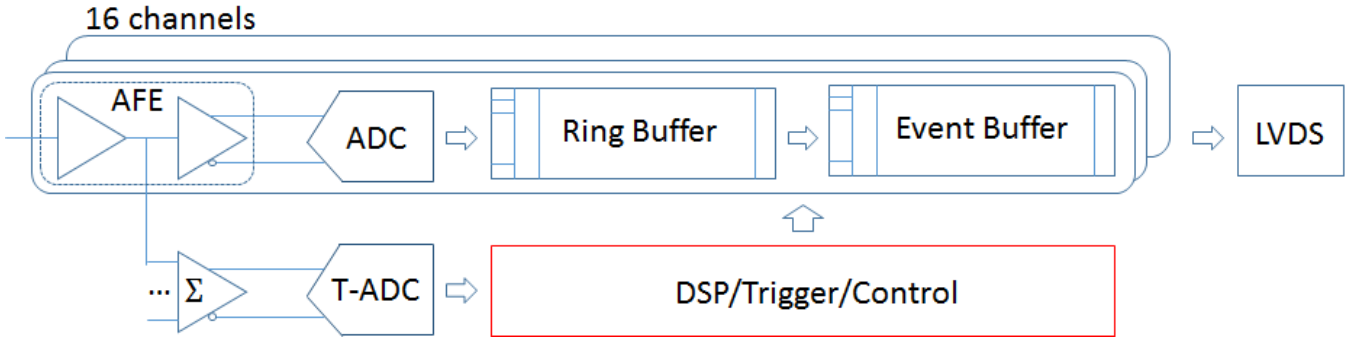
- 低功耗高集成度大型TPC读出ASIC芯片研制





Total number of ch.		1 million per endcap
AFE	ENC	500 e @ 10pF input cap.
	Gain	~10 mV/fC
	Shaper	CR-RC
	Peaking time	~100 ns
ADC	Sampling rate	≥20 MSPS
	Resolution	10 bit
Power consumption		≤5 mW per channel
Output data bandwidth		200 Mbps × Occu. per ch
Channel number		32
Process		TSMC 65nm LP

TPC读出芯片结构和指标

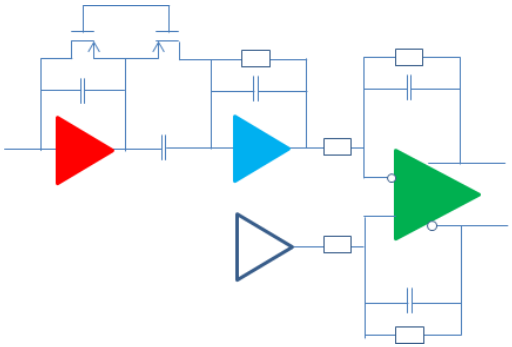


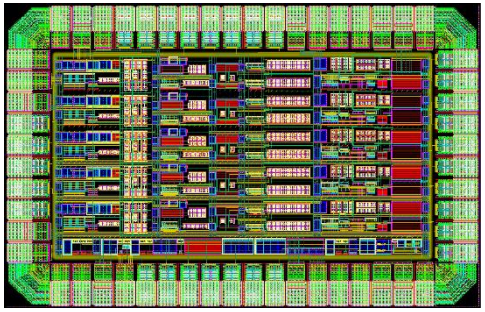
AFE	
Signal Polarity	Negative
Detector Capacitance	5-20pF
Shaper	CR-RC
Shaping Time	160ns
ENC (Equivalent Noise Charge)	<500e @ 10pF
Dynamic Range	120fC
Gain	10mV/fC
INL (Integrated Non-Linearity)	<1%
Crosstalk	<0.3%
Power Consumption (AFE)	<2.5mW/ch

ADC	
Input Range	-0.6V ~ 0.6V diff.
Resolution	10bit
Sampling Rate	40MSPS
DNL	<0.65LSB
INL	<0.6LSB
SFDR @ 2MHz, 40MSPS	68dBc
SINAD	57dB
ENOB	>9.2bit @ 2MHz
Power Consumption (ADC)	<2.5mW/ch

TPC读出芯片设计进展

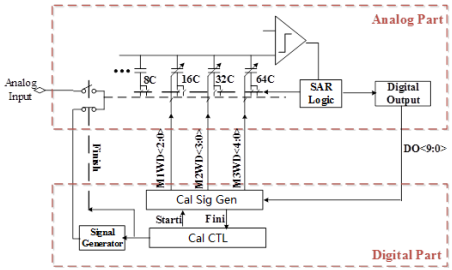
模拟前端
1.93mW/ch (sim.)

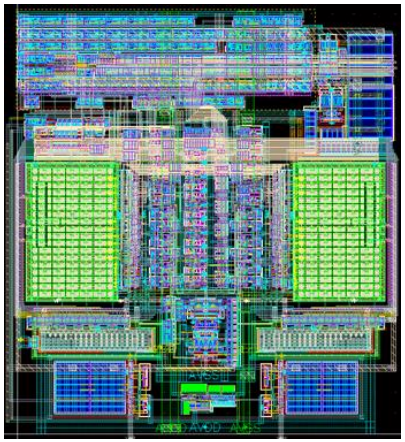




1320umx 838um

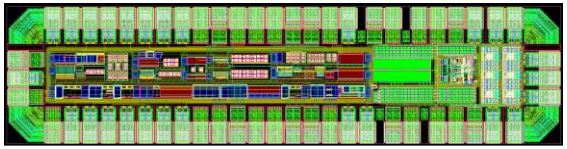
SAR-ADC:
0.55mW/ch (sim.)





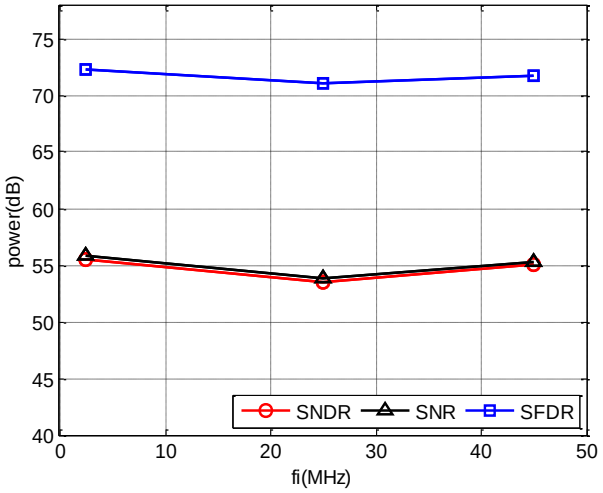
90umx 97um

完整通道的前端



1800umx 440um

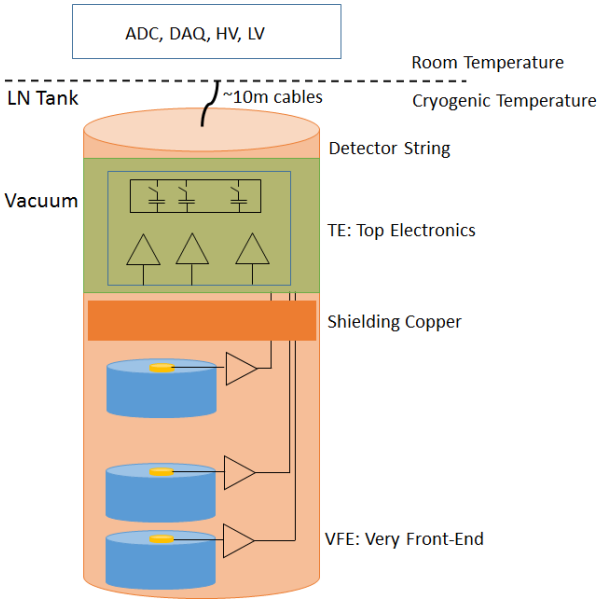
0.7mW @ 100MSPS, ENOB=8.8bit

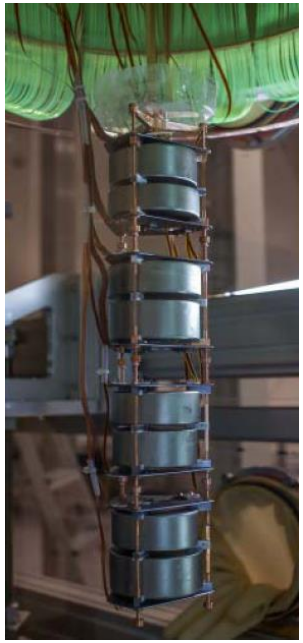


ADC动态特性测试

学术研究：高纯锗前端电子学

- 高纯锗阵列探测器低温低噪声低本底前端电子学研制

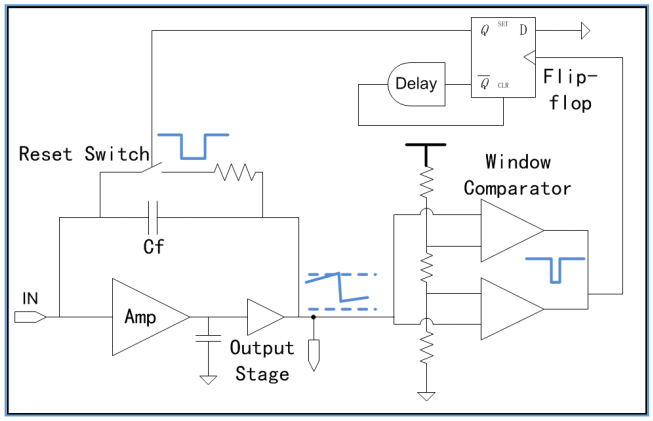


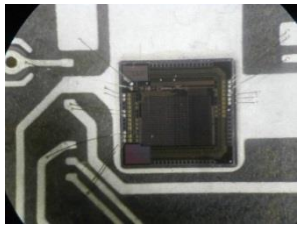


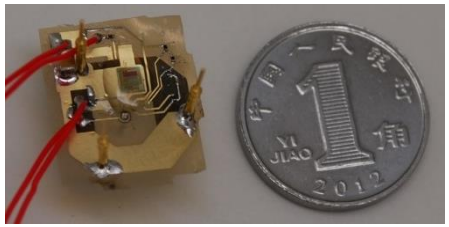
商业探测器系统不可能同时兼顾低噪声和低本底两个极端需求，开展用于暗物质探测实验的大规模高纯锗阵列探测器研制必须立足于自主研发

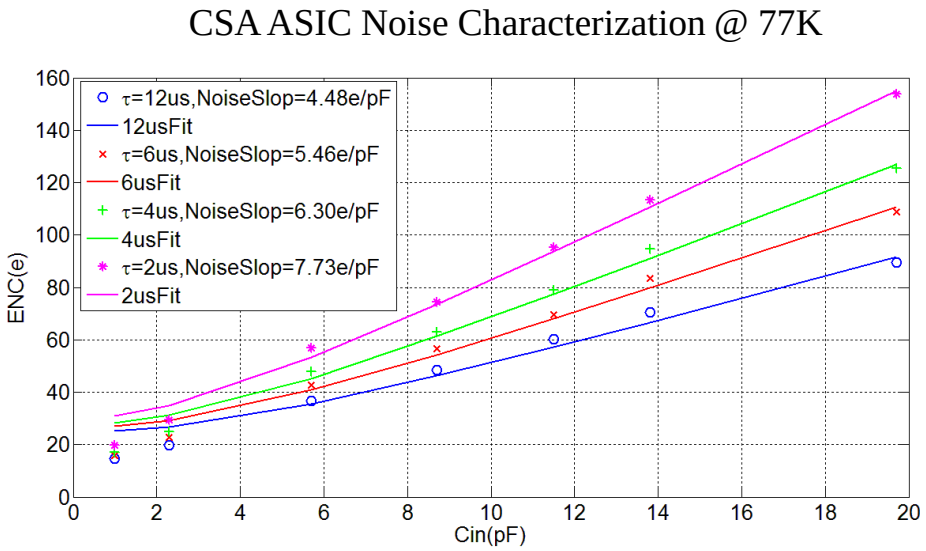
高纯锗前端电子学结构

- CMOS ASIC前放
- 低物质量PTFE前端电路板



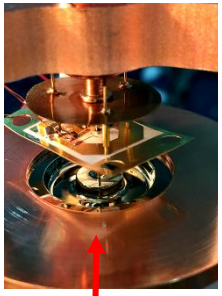


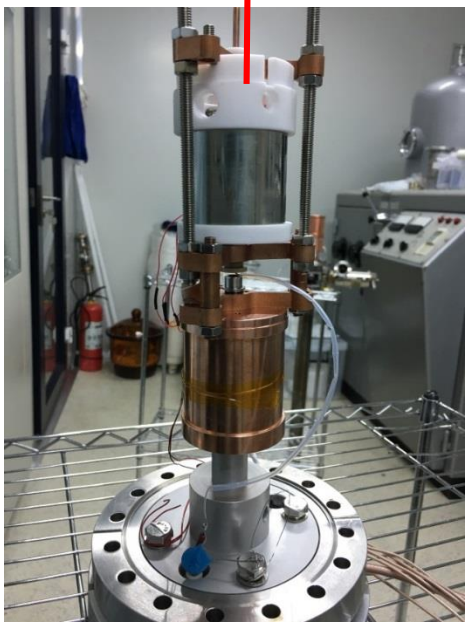


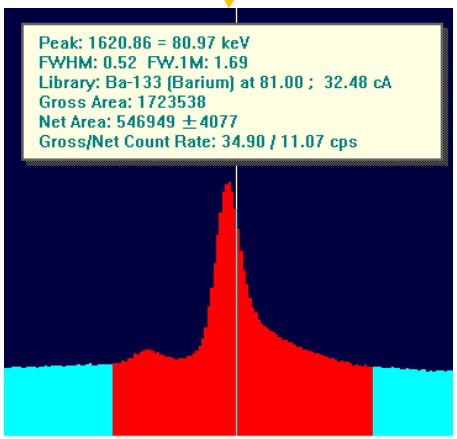


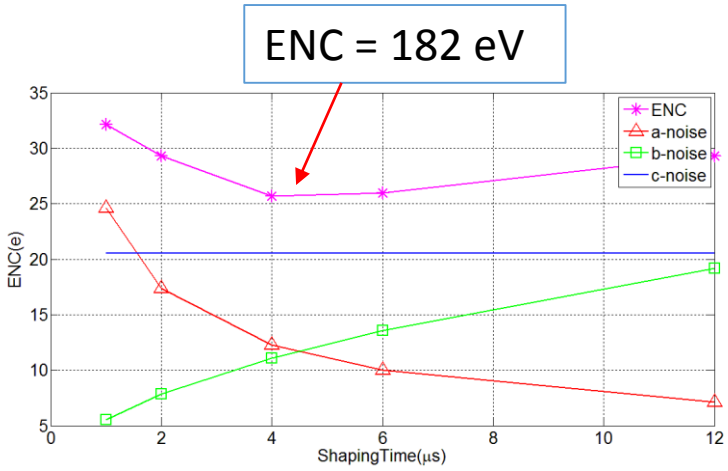
高纯锗前端电子学进展

- 与0.5kg高纯锗探测器联调测试









学术研究：SiPM读出ASIC

- 用于PET和TOF/PET的SiPM探测器读出ASIC芯片研制

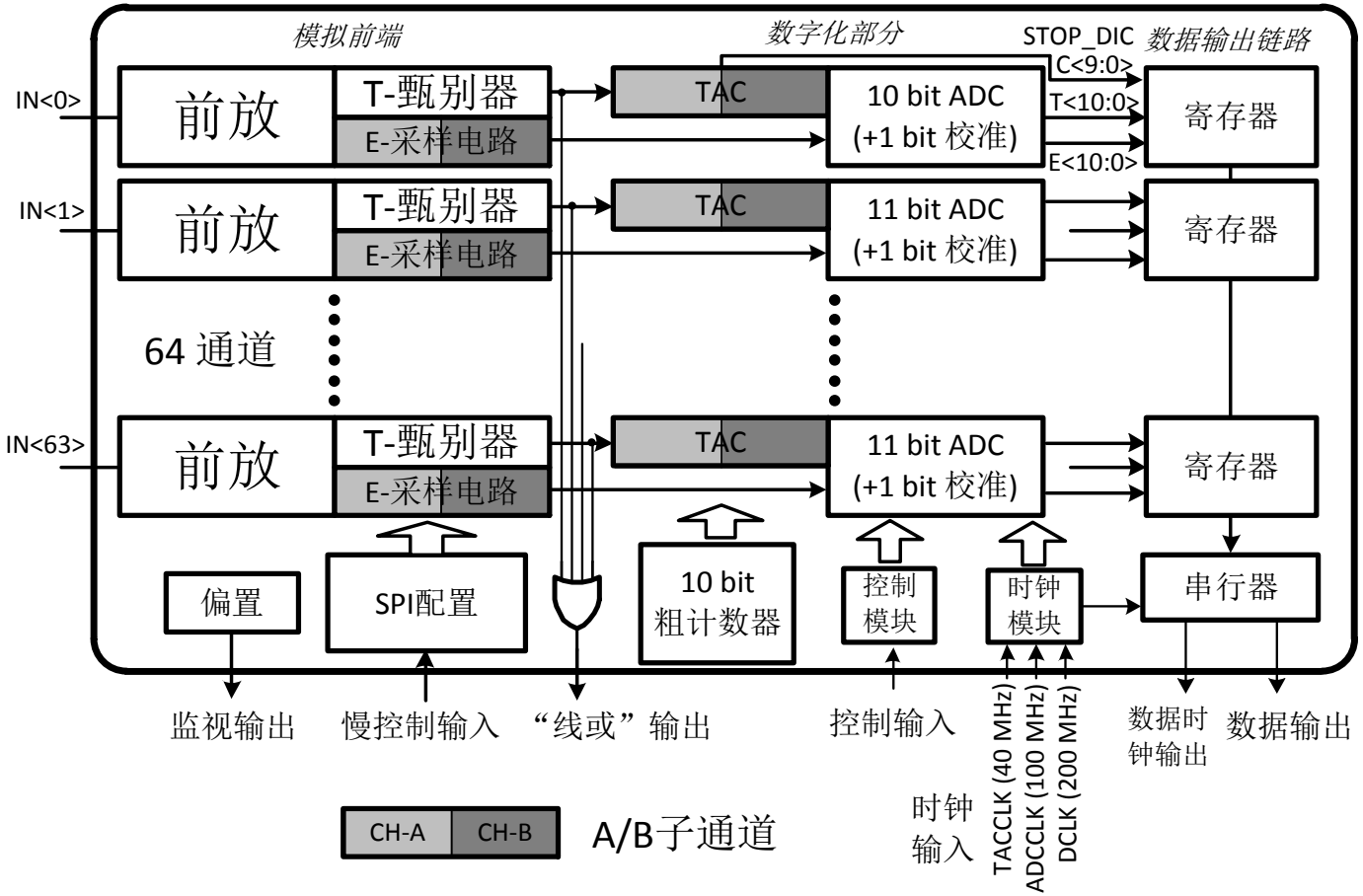
优势

- 尺寸小，“像素化”读出，排布灵活
- 响应速度快(<100ps rms)
- 工作电压低(<100V)
- 对磁场不敏感（PET-MRI融合系统）

缺点

- 输出通道数多（100ch/cm^2）
- 输入电容大（10~100pF）
- 温度敏感
- 暗计数率高(~100kHz/mm^3)
- 其他非理想因素干扰（饱和、串扰等）

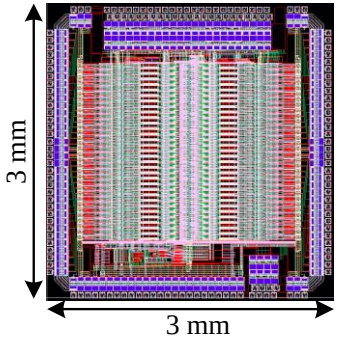
SiPM读出ASIC芯片结构

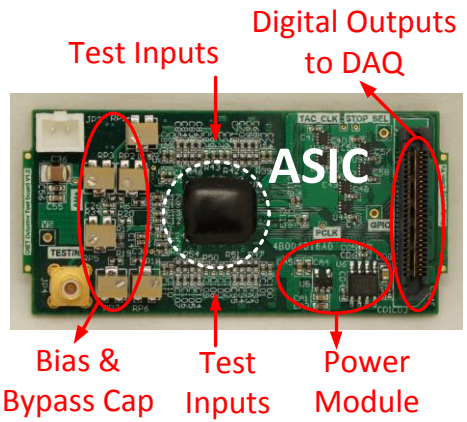


- 64通道SiPM信号→
  - 10+1 bit 能量E
  - 10 bit粗计数C
  - 10+1 bit TAC值
  - \+ “线或”输出（用于触发、总计数率测量）
- 能量、时间信息并行采集。
- 200 MHz 串行化数据输出
- A/B 子通道工作在乒乓模式
- 功耗：5.2 mW/通道（测量值）

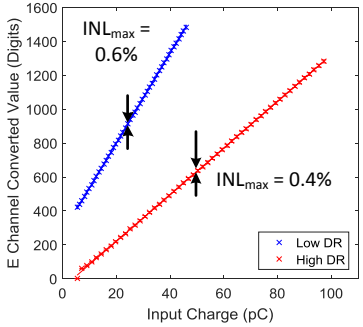
SiPM读出ASIC芯片进展

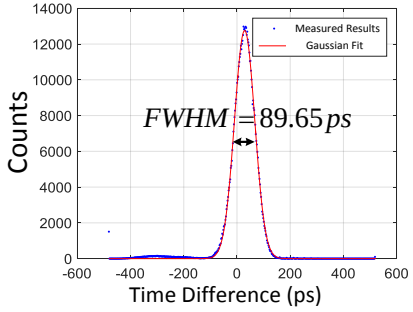
芯片与测试系统



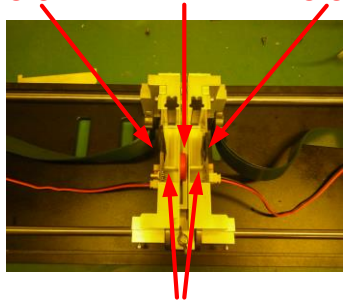


信号发生器测试结果

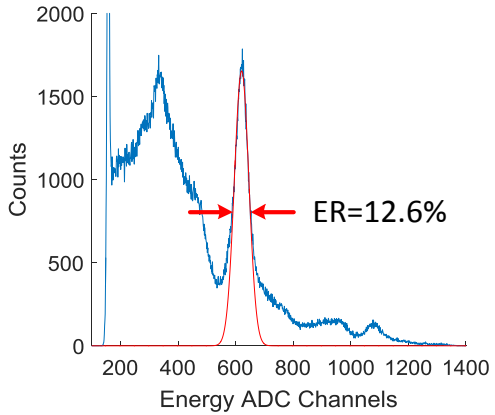


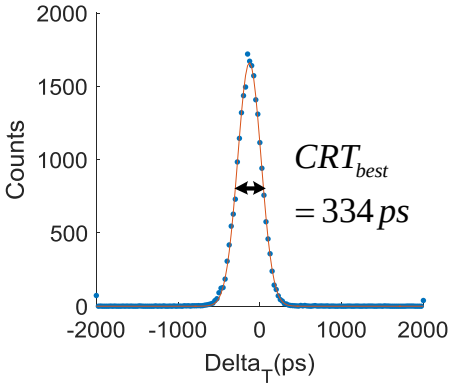


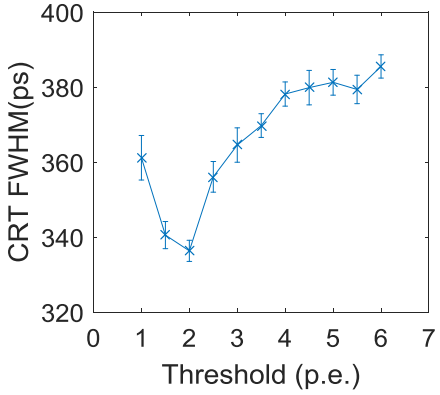
LYSO晶体测试结果



LYSO (2mm x 2mm x 11mm)
SensL® FJ-30035 SiPM







发表论文和承担项目

- 发表论文：3篇SCI

  [1] Zhu X, Deng Z, Chen Y, et al. Development of a 64-Channel Readout ASIC for an 8x8 SSPM Array for PET and TOF-PET Applications[J]. IEEE Transactions on Nuclear Science, 2016, 63(3): 1327-1334.

  [2] Zhang H Y, Deng Z, Liu Y N. Non-ideal effects of MOS capacitor in a switched capacitor waveform recorder ASIC [J]. Chinese physics C, 2016, 40(7): 076102.

  [3] Yuan Z X, Deng Z, Wang Y, et al. CAD-II: the second version current-mode readout ASIC for high-resolution timing measurements[J]. Journal of Instrumentation, 2016, 11(07): P07013.

- 承担项目：3项

  [1]“低温辐射探测器CMOS集成前端电路设计研究”，自然科学基金面上项目，96万，2014.01-2017.12

  [2]“高能环形正负电子对撞机相关的物理和关键技术预研究”子课题，重点研发计划，160万，2016.07-2021.07

  [3]“高纯锗阵列直接探测暗物质实验”子课题，重点研发计划，789万，2017.07-2022.06