Chapter 4 Vertex

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Nov. 10th , 2017 Beijing

CEPC detector CDR mini-review

Contents:

Detector Requirements

- impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta} (\mu m)$$

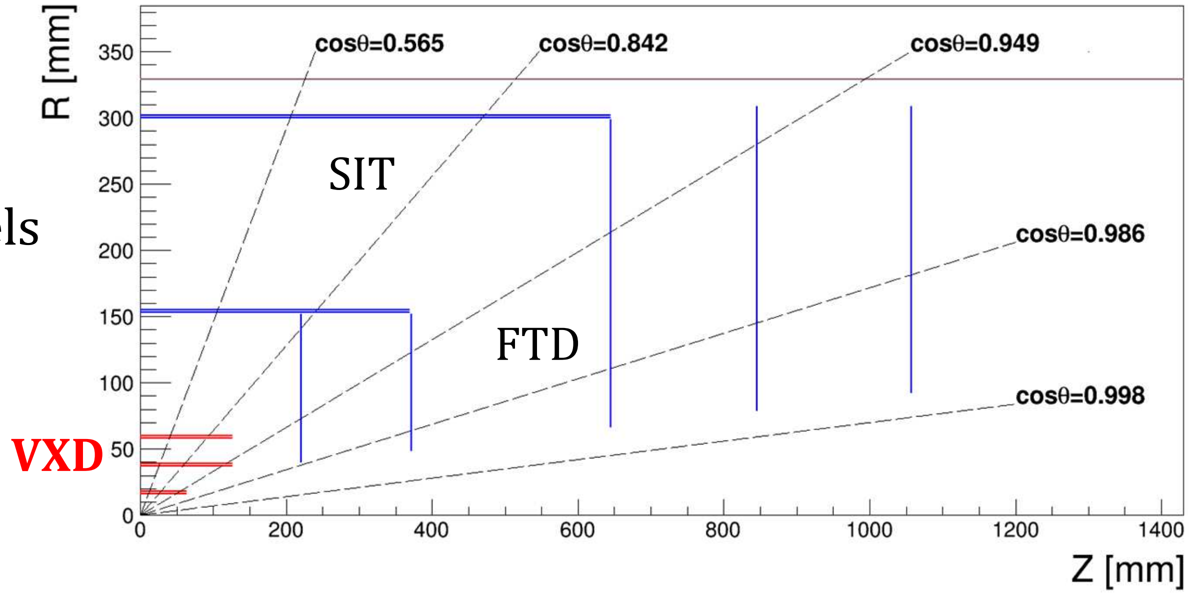
- Detector system requirements:
  - σ_{SP} near the IP: *<3 μm* → ~16μm pixel pitch
  - material budget: *≤ 0.15%X_0/layer* → power consumption < 50mW/cm^2 , if air cooling used
  - first layer located at a radius: *~1.6 cm*
  - pixel occupancy: *≤ 1 %* → ~ μs level readout

Target: fine pitch, low power, fast pixel sensor + light structure

Baseline Detector Layout

<u>VXD</u>:

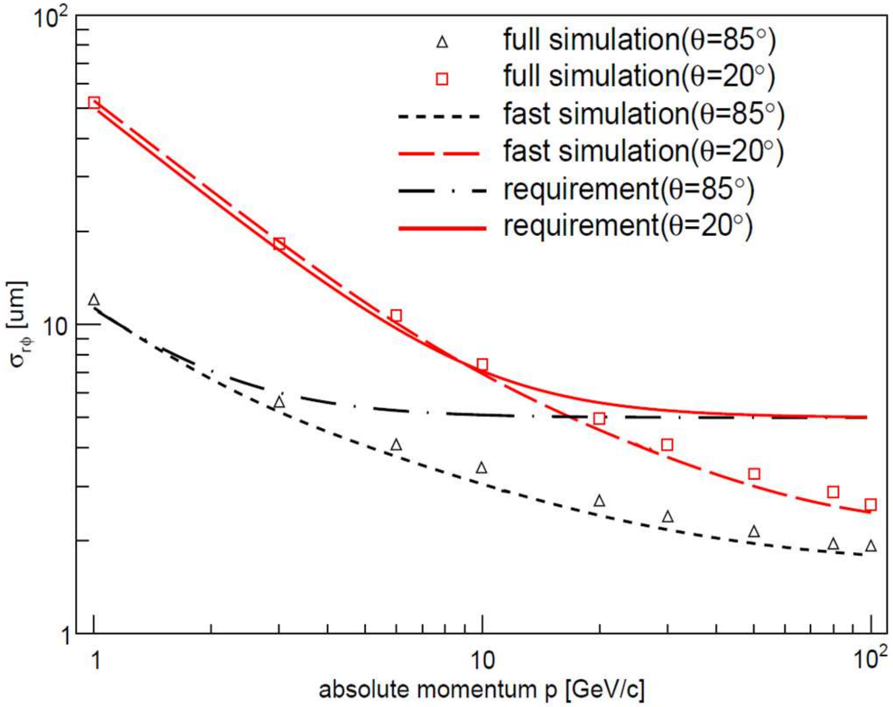
- ILD like layout
- 3 layers of double-sided pixels
- σ_{SP}=2.8μm, inner most layer
- Polar angle θ~15 degrees



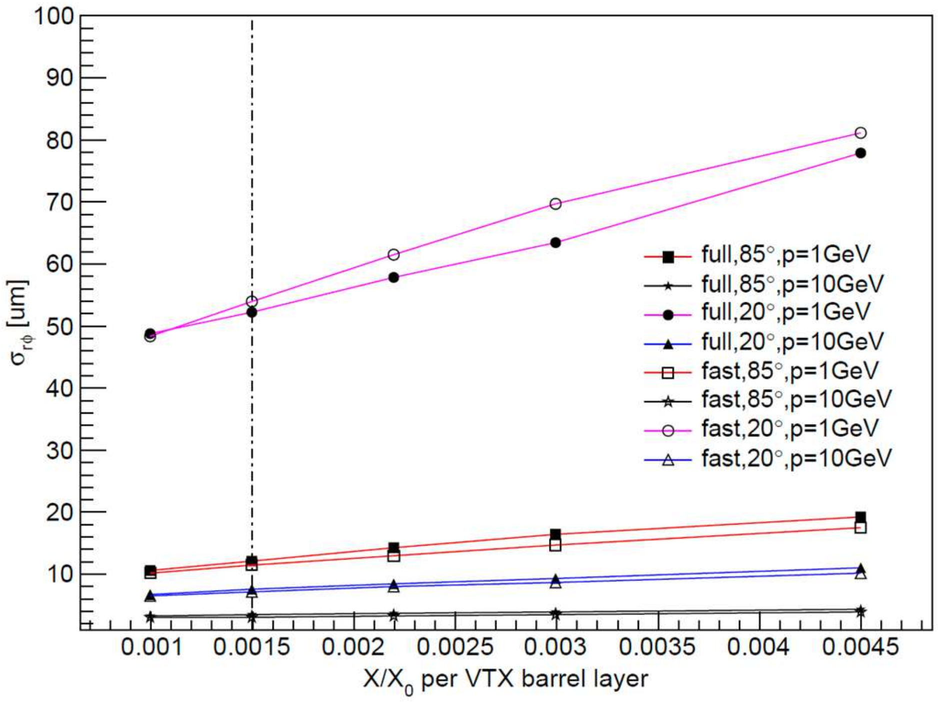
VXD parameters

	R (mm)	|z| (mm)	|cos θ|	σ_{sp} (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	20
Layer 2	18	62.5	0.96	6	1-10
Layer 3	37	125.0	0.96	4	20
Layer 4	39	125.0	0.95	4	20
Layer 5	58	125.0	0.91	4	20
Layer 6	60	125.0	0.90	4	20

Performance Studies

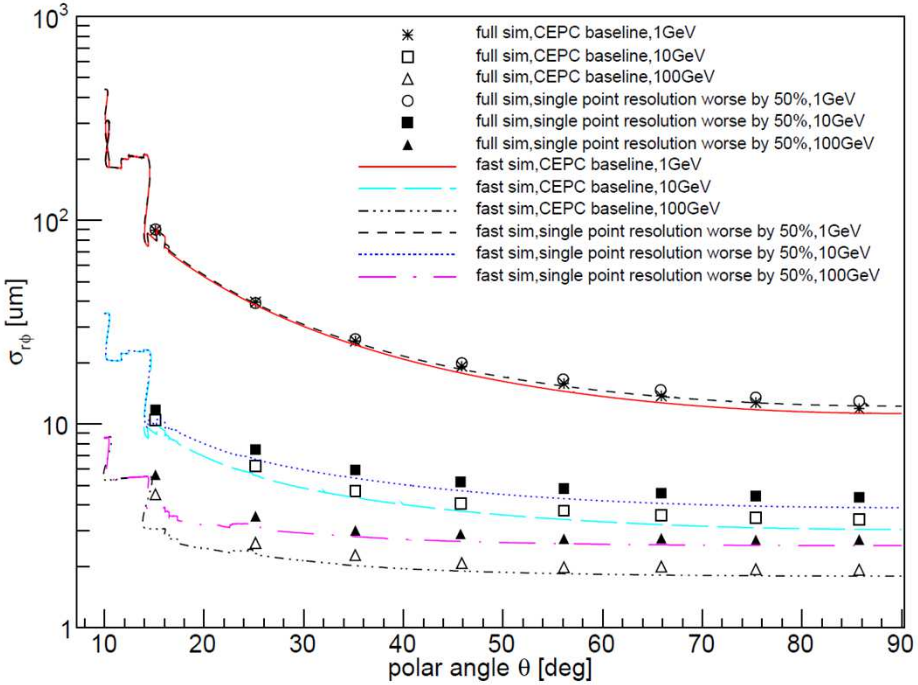


Baseline

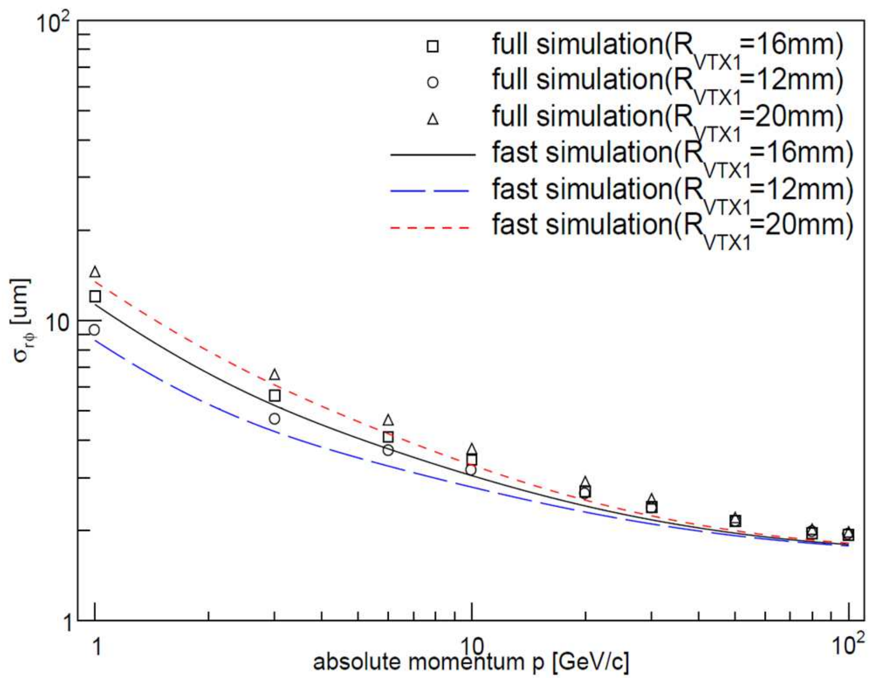


Material budget

Performance Studies



Single point resolution



Distance to IP

Beam-Induced Backgrounds (to be updated)

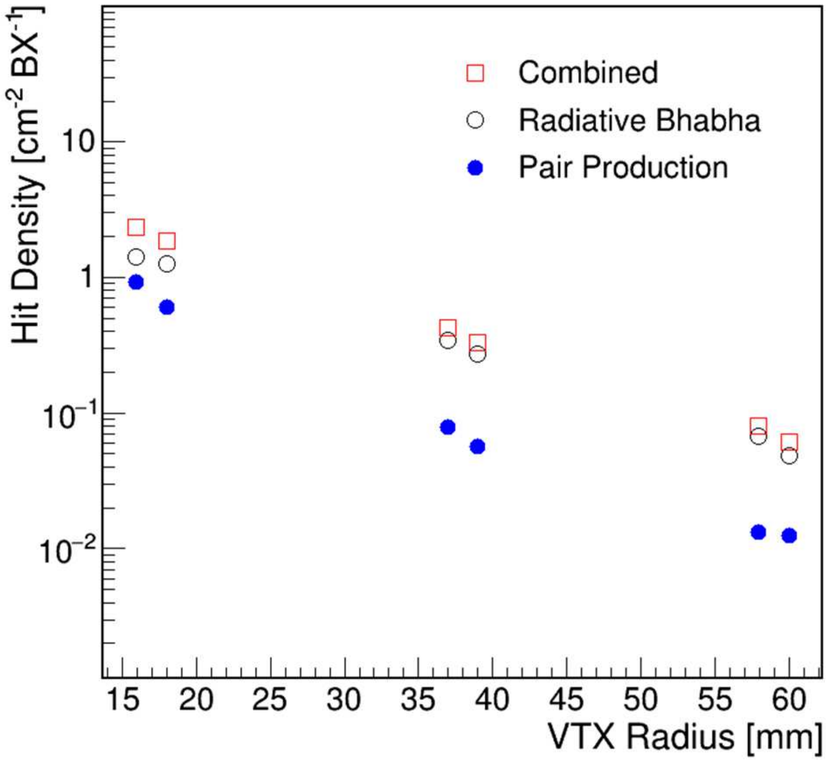
- **Radiation level**
  - TID ~2.5 MRad / year
  - NIEL ~10^{12} 1MeV n_{eq} / (cm^2 year)

  (safety factor: 10)

- **Hit density** ~2.5 hit cm^{-2} BX^{-1}

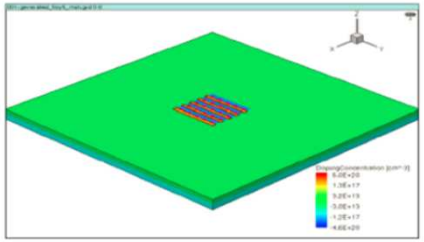
  → detector occupancy: <1%

  by estimating tolerable hit density, with a safety factor of 10 included

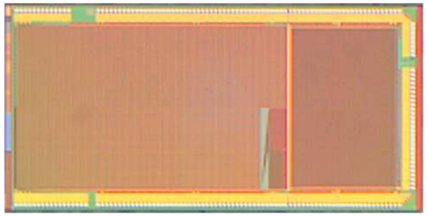


CMOS Pixel Sensor R&D Activities

- **Sensor design & TCAD simulation**
  - Different sensor diode geometries, epitaxial-layer properties and radiation damage



- **First submission in Nov. 2015**
  - Exploratory prototype, analog pixel, rolling shutter readout mode
  - Sensor optimization and radiation tolerance study
  - sensing node AC-coupled to increase biased voltage



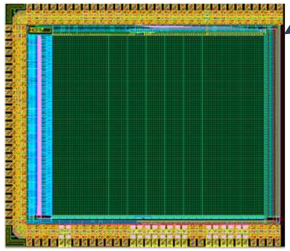
- **Second submission in May 2017**
  - Tow prototypes with digital pixels (in-pixel discriminator)
  - Tow different readout schemes: rolling shutter & asynchronous

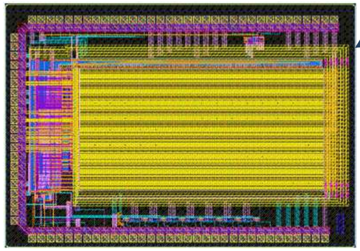
Design goals

Spatial resolution $5\ \mu m$

Integration time $< 10\ \mu s$

Power consumption $< 80 mW/cm^2$





SOI Pixel Sensor R&D Activities

- **First submission (CPV1) in June 2015**
  - 16*16 μm with in-pixel-discrimination
  - Double-SOI process for shielding and radiation enhancement
- **Second submission (CPV2) in June 2016**
  - In-pixel CDS stage inserted
  - To improve RTC and FPN noise
  - To replace the charge injection threshold

CPV2 performance

- *Thinned down to 75um thick*
- *Temporal noise ~6e$^-$*
- *Threshold dispersion (FPN) ~114e$^-$*
- *Single point resolution measurement under infrared laser beam*

Future R&D

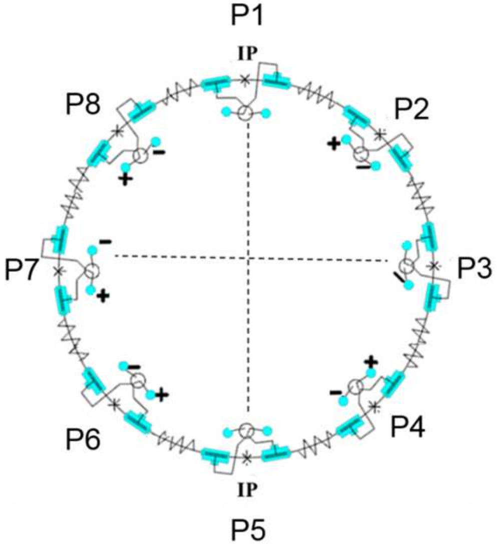
- Pixel pitch shrinkage
- Novel readout scheme
- Radiation hardness
- Light structure

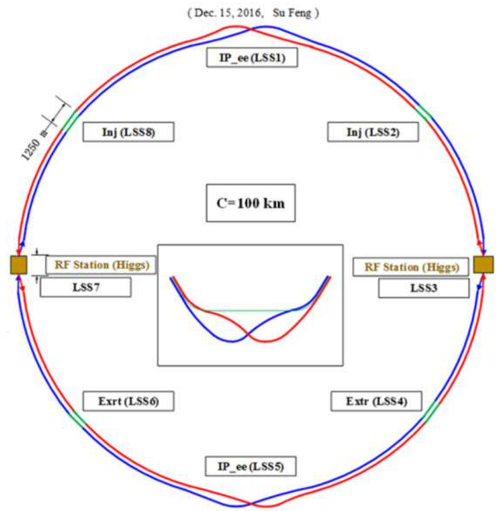
Thank you for your attention!

CEPC and Its Beam Timing

Circular e^+e^- Higgs (Z) factory **two detectors, 1M ZH events in 10yrs**

E_{cm}≈240GeV, luminosity ~2×10^{34} $cm^{-2}s^{-1}$, (1×10^{34} $cm^{-2}s^{-1}$ at the Z-pole)





Single Ring - 54Km

- **Baseline design in pre-CDR**
- Bunch number 50
- Colliding every 3.6μs, continuously

  →Power pulsing not applicable

Fully Partial Double Ring - 100Km

- **Baseline design in CDR**
- Bunch number 286 (half ring)
- Bunch spacing 0.537μs

Reference: CEPC Accelerator CDR - Status, J. Gao, Workshop plenary talk

R&D activities

Initial sensor R&D targeting on

- *Pixel single point resolution <3- 5μm*
- *Power consumption at the current level <100mW/cm²*
- *Integration time 10-100μs*

➢ CMOS pixel sensor (CPS)-funded by MOST and IHEP

TowerJazz CIS 0.18 μm process

➢ SOI pixel sensor- funded by NSFC

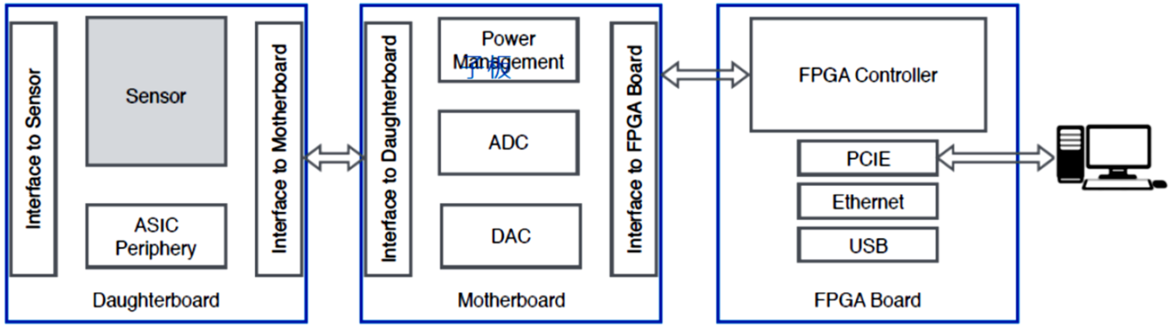
LAPIS 0.2 μm process

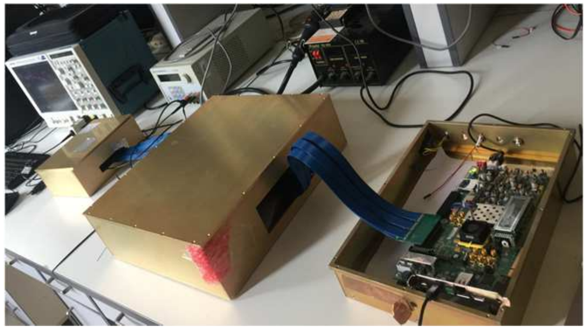
1st CPS Prototype Characterization

- **Test system being developed**

  Prototype analog readout → Daughter-board → ADC sampling by mother-board

  – Two versions of daughter-board designed and fabricated
  – Single analog readout channel verified with oscilloscope
  – ADC debugging in progress



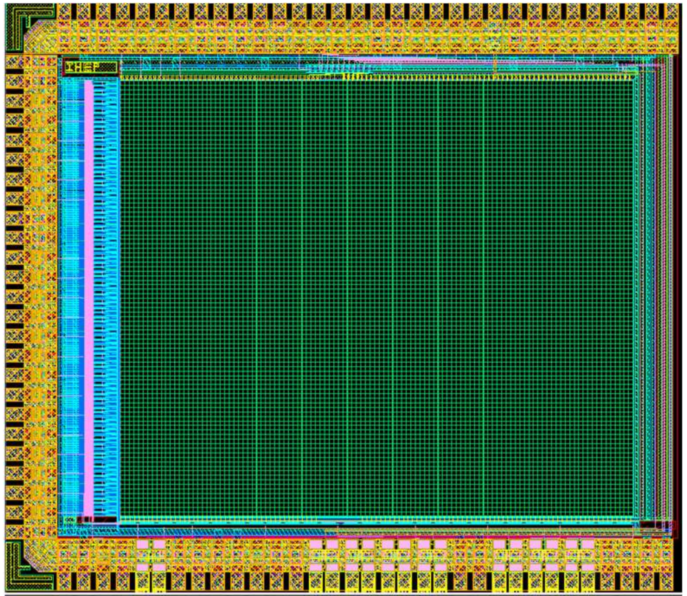


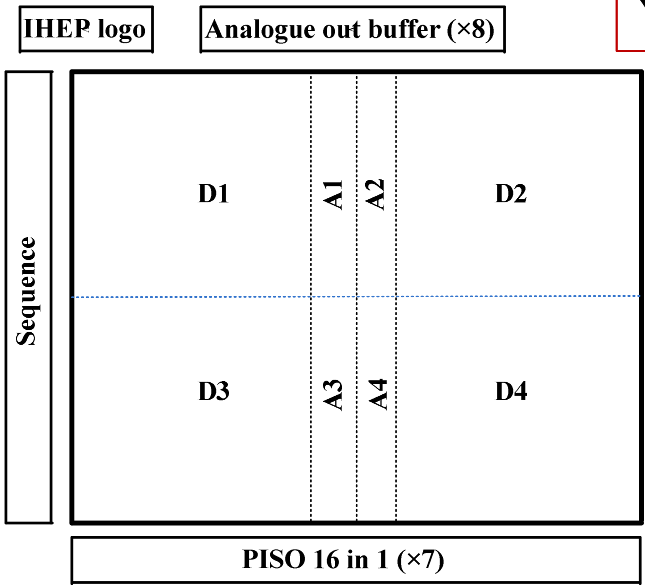
WANG Ke, WANG Na et al.

SHI Xin, Kiuchi Ryuta et al.

2nd CPS Submission: Rolling-shutter Mode

Y. Zhou (IHEP)





Two different pixel versions:

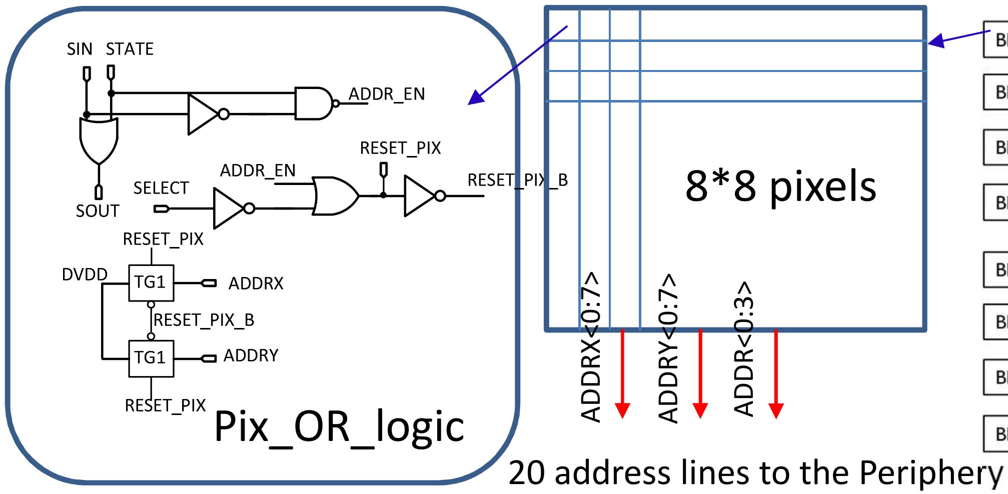
- Pixel size: 22μm×22μm
  → 65% of ASTRAL chip
- Same amount of transistors;
- Offset cancellation technique;
- Version 2 has higher signal gain, but suffers "more" from "Latch" input voltage distortion.

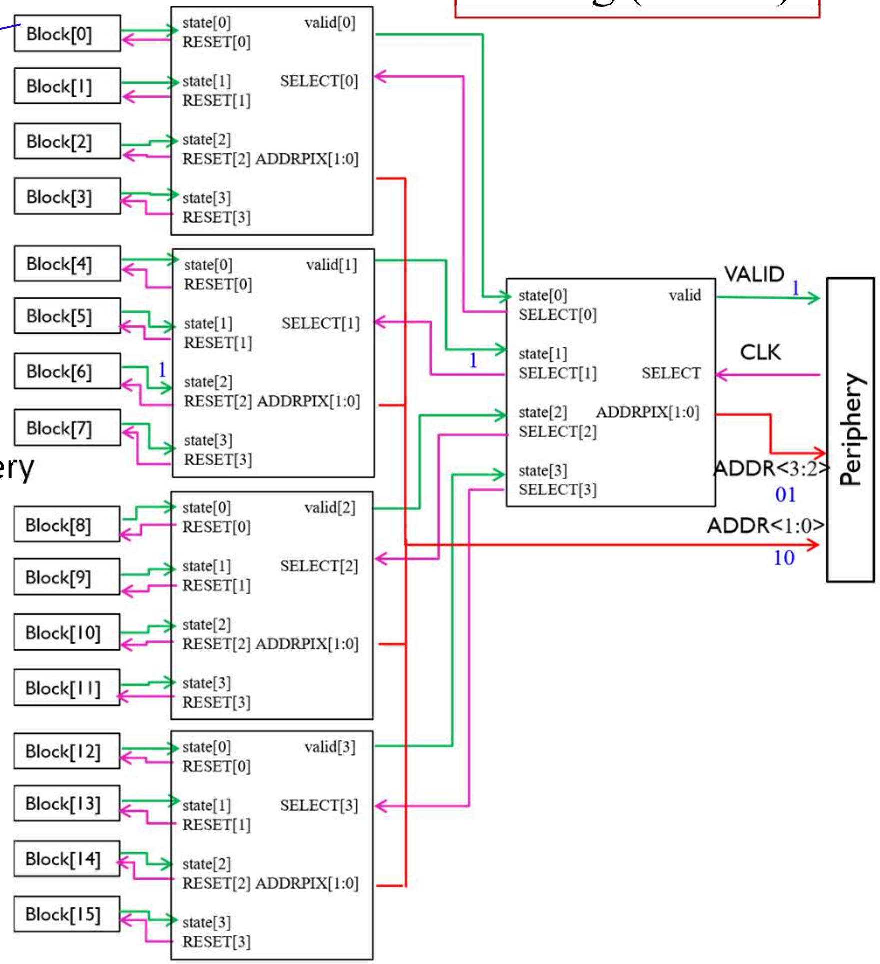
Chip features:

- 3×3.3 mm^2
- 96×112 pixels with 8 sub-matrix
- Processing speed: 11.2μs/frame with 100 ns/row
- Output data speed: 160 MHz
- Power: 3.7μA/pixel (14.4 mW/cm^2 @pixel matrix)

2nd CPS Submission: Asynchronous Mode

P.Yang (CCNU)





Matrix readout architecture:

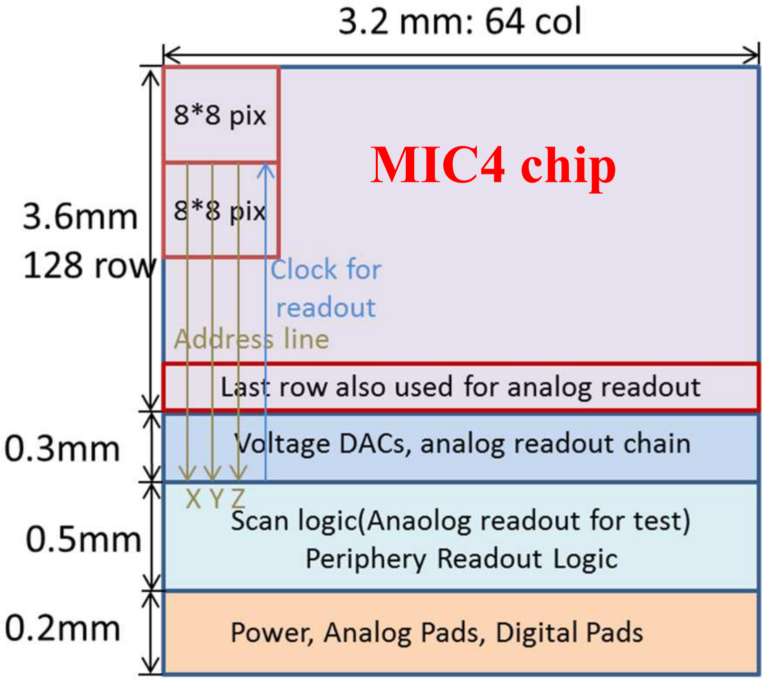
- **AERD (Address-Encoder and Reset-Decoder)** many connection lines occupy larger area than the logic circuit itself
- **OR gate chain:** speed is limited with the number of the chain pixels
- **Combine these two solutions:** 64 pixels as a group using OR gate chain, groups using AERD structure to readout

2nd CPS Submission: Asynchronous Mode

Y. Zhang (IHEP) & P.Yang (CCNU)

front-end I: Same structure as ALPIDE chip

- ENC: 8 e^-
- Power cons.: 61 nA/pixel
- Threshold: 140 e^-
- Peaking time < 1 us
- Pulse duration < 3 μs



front-end II: CSA based front-end circuit

- Pixel size: 25×25 μm^2
- ENC: 24 e^-
- Power cons.: 50 nW/pixel (8 mW/cm^2 @pixel matrix)
- Threshold: 170 e^-
- Peaking time < 500 ns @ Qin < 1.5 ke^-
- Pulse duration < 9.4 μs @ Qin < 1.5 ke^-

- 3.2 × 3.7 mm^2
- 128 × 64 pixels
- Integration time: < 5 μs/10 μs
- Power consumption: < 80 mW/cm^2
- Chip periphery
  - Band gap
  - Voltage DAC
  - Current DAC
  - Matrix configuration
  - LVDS
  - Custom designed PADs

CEPC CDR Parameters

beta_y=2mm

D. Wang

	Higgs	*W*	*Z*
Number of IPs		2	
Energy (GeV)	120	80	45.5
Circumference (km)		100	
SR loss/turn (GeV)	1.68	0.33	0.035
Half crossing angle (mrad)		16.5	
Piwinski angle	2.75	4.39	10.8
N_e/bunch (10^{10})	12.9	3.6	1.6
Bunch number	286	5220	10900
Beam current (mA)	17.7	90.3	83.8
SR power /beam (MW)	30	30	2.9
Bending radius (km)		10.9	
Momentum compaction (10^{-5})		1.14	
β_{IP} x/y (m)		0.36/0.002	
Emittance x/y (nm)	1.21/0.0036	0.54/0.0018	0.17/0.0029
Transverse σ_{IP} (um)	20.9/0.086	13.9/0.060	7.91/0.076
ξ_x/ξ_y/IP	0.024/0.094	0.009/0.055	0.005/0.0165
RF Phase (degree)	128	134.4	138.6
V_{RF} (GV)	2.14	0.465	0.053
f_{RF} (MHz) (harmonic)		650	
Nature bunch length σ_z (mm)	2.72	2.98	3.67
Bunch length σ_z (mm)	3.48	3.7	5.18
HOM power/cavity (kw)	0.46 (2cell)	0.32(2cell)	0.11(2cell)
Energy spread (%)	0.098	0.066	0.037
Energy acceptance requirement (%)	1.21		
Energy acceptance by RF (%)	2.06	1.48	0.75
Photon number due to beamstrahlung	0.25	0.11	0.08
Lifetime due to beamstrahlung (hour)	1.0		
F (hour glass)	0.93	0.96	0.986
L_{max}/IP (10^{34}cm^{-2}s^{-1})	2.0	4.1	1.0