CDR on Silicon Tracker

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- Introduction
 - Main task: Improving tracking efficiency and precision
 - Additional functionalities: field distortion, detector alignment, time-stamping, dE/dx
 - Material budget control (o _{1/Pt} equation)

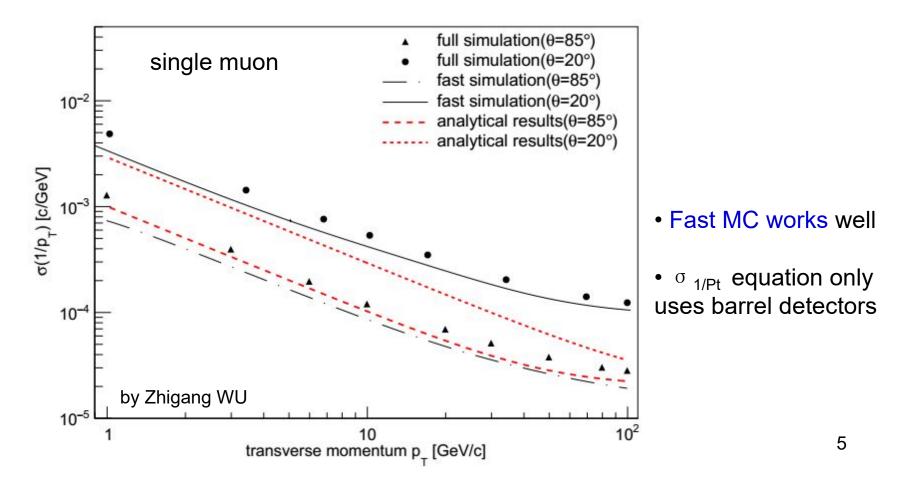
$$\sigma_{1/p_{\rm T}} = a \oplus \frac{b}{p \sin \theta} \quad [\,{\rm GeV^{-1}}]$$

- Baseline design
 - Detector layout (2 SIT + TPC + 1 SET, 5 FTD ETD?)
 - fast simulation (LDT toy MC) & full simulation (tracking performance section)

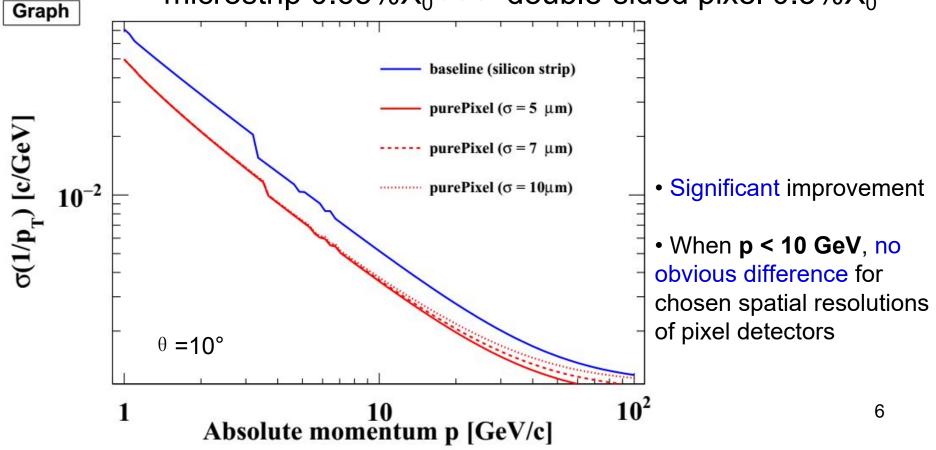
- Sensor tech. & Front-End electronics
 - silicon microstrip sensor
 - 10x10 cm², pitch 50 μm σ_{sp} < 7 μm, thickness ~ 200 μm
 - Front end electronics board (amplifying,shaping,ADC, zero suppression, sparcification..)
 - silicon pixel sensors
 - e.g., CMOS pixel sensors (CPS), σ_{sp} < 7 µm, thickness ~ 50 µm
 - Front end electronics on sensor

- Powering and cooling
 - powering: DC-DC converters
 - cooling: silicon micro-channel
- Mechanics and integration
 - Carbon-fibre Reinforced Plastic material
 - laser monitoring systems for pre-alignment
 - Liverpool Univ.(GAO yanyan) will cooperate on this part

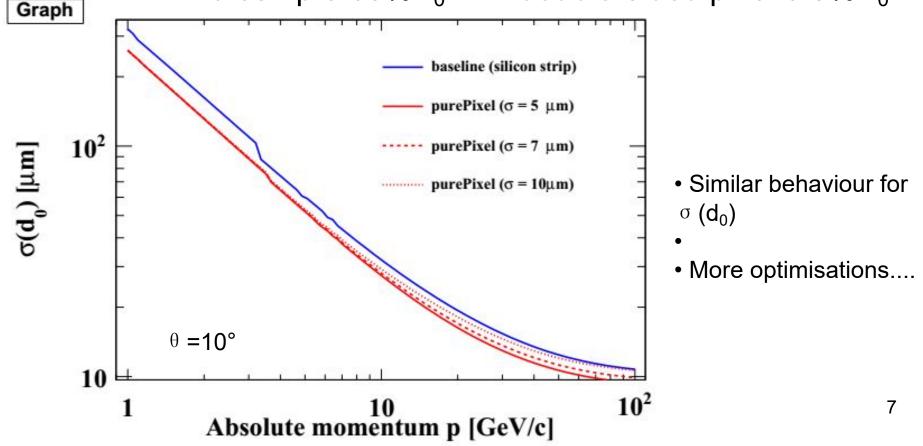
• Tracking performance (baseline design)



- Tracking performance (baseline vs pure pixel)
 - microstrip $0.65\%X_0 >>>$ double-sided pixel $0.3\%X_0$



- Tracking performance (baseline vs pure pixel)
 - microstrip $0.65\%X_0 >>>$ double-sided pixel $0.3\%X_0$



- Critial R&D
 - pixelated strip sensors using CMOS tech.
 - p⁺-on-n silicon microstrip sensors (slim-edge)
 - Front-end electronics (low power consumption, low noise, ...)
 - Efficient powering and CO2 cooling (low material budget)
 - light but stiff mechanics
 - Detector layout optimisation

Thank you