Monolithic Active Pixel Sensors on high resistivity substrates: status and perspective

Angelo Rivetti

INFN-Sezione di Torino

Outline

- Motivations
- Project and goals
- Results from small test structures
- Outlook

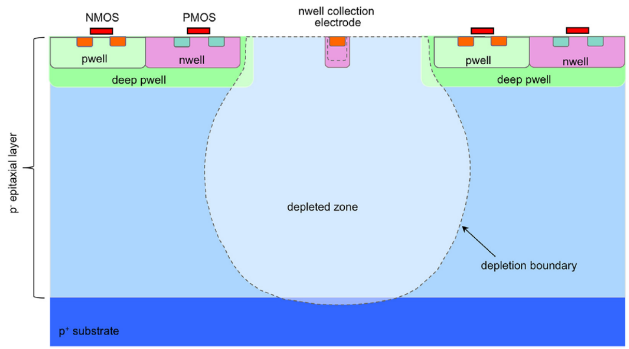
Monolithic CMOS Pixel Sensors

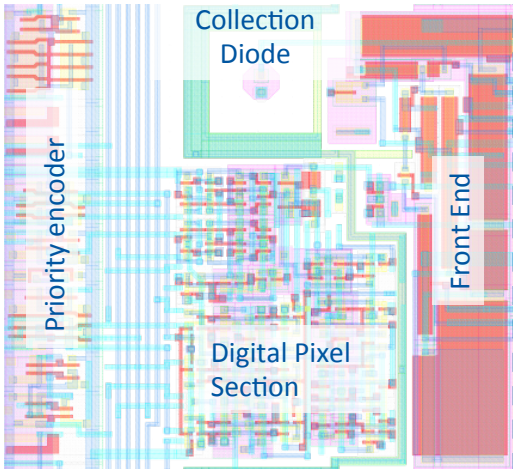
- Sensor and readout electronics share the same wafer
- Lower cost and increased reliability on assembly and production of detectors:
  - no need for costly fine-pitched flip-chip assembly
  - less (failing) connectors and lower material budget
  - use 8" wafers (CMOS fab): reduced cost per sensor
- Thanks to the reliability of IC-grade CMOS fabrication plants
- Typical production rate: 40.000 wafers/month $\rightarrow$ 800 m^2/month of working silicon
- Excellent opportunity for customisation (speed vs power trade-off)
- Perspective of using silicon pixel detector where never before

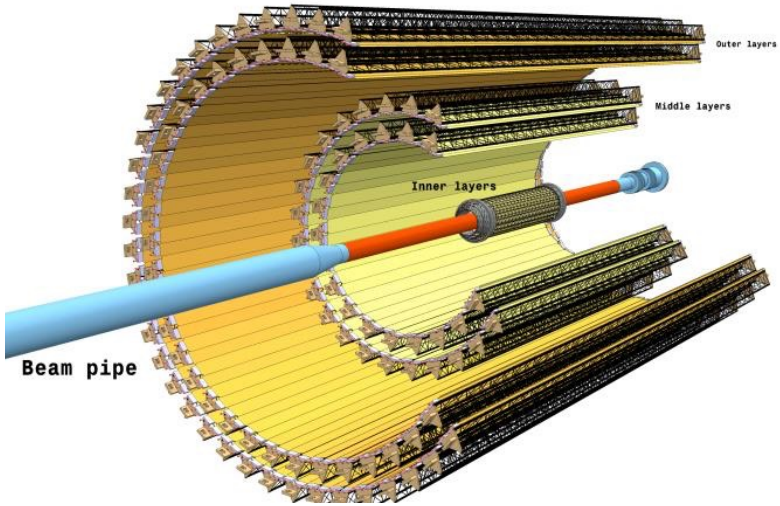
Experiment-grade CMOS sensors

- Quadruple well available by most CMOS sensor vendors
- Full CMOS electronics in pixels established → sparsified readout
- Sensors for the ALICE ITS upgrade in TJ 180 nm

  W. Snoeys: https://indico.ihep.ac.cn/event/6618/session/9/contribution/79/material/slides/0.pdf







Trends in radiation CMOS sensors

- A lot of interest in fully depleted MAPS.

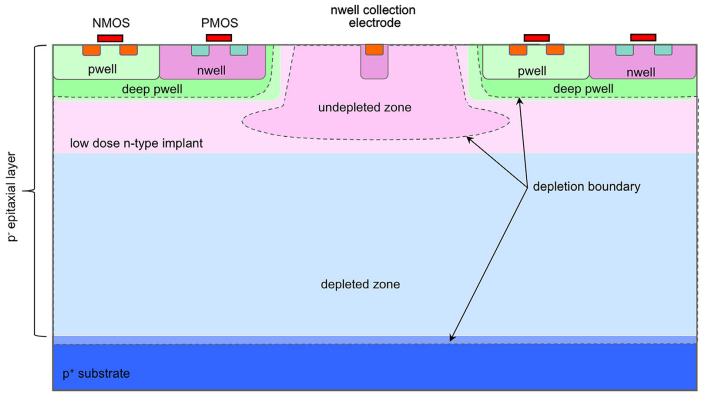
  Fast charge collection by drift:
  - ⋆ Better radiation hardness
  - ⋆ Improved timing
- Deeper collection depth
  - ⋆ Better SNR
  - ⋆ Lower analog power

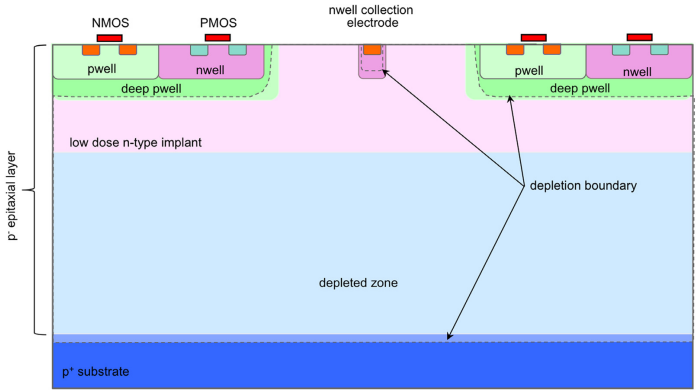
- Example: 150 μm depletion, 5 fF collection capacitance $\rightarrow \frac{Q}{C} \approx 0.4$ V
  $\rightarrow$ could be detected by an inverter (zero analog power!)
- Analog power can be limited by time resolution
- Digital power determined by rate

Example of DMAPS

- Modification of the TJ process used in ALPIDE

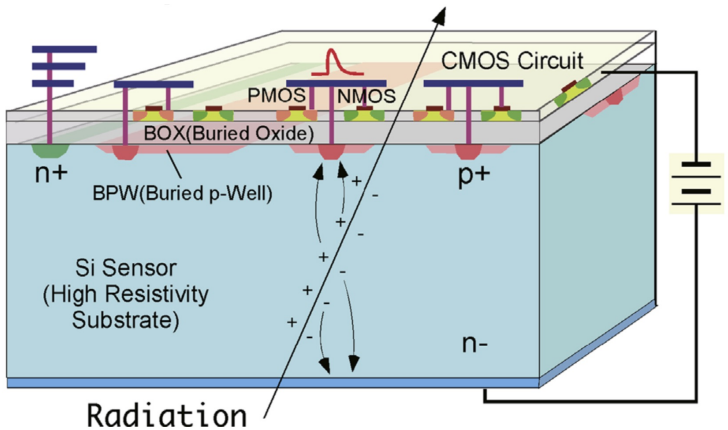
  W. Snoeys et al., NIM A871 (2017) pp. 90-96





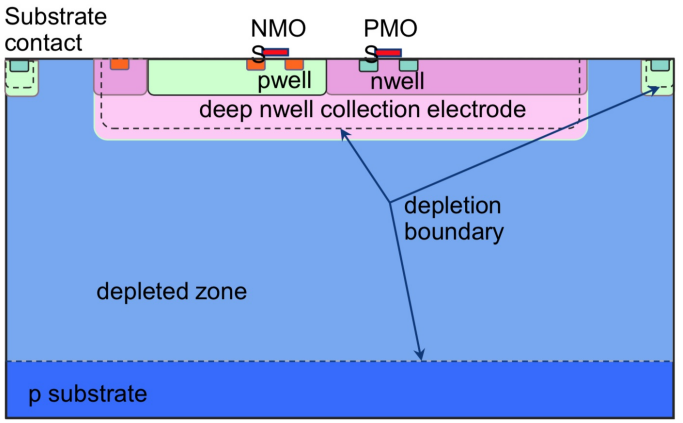
- SOI pixels

  T. Miyoshi et al., NIM A824 (2016) pp. 439-42



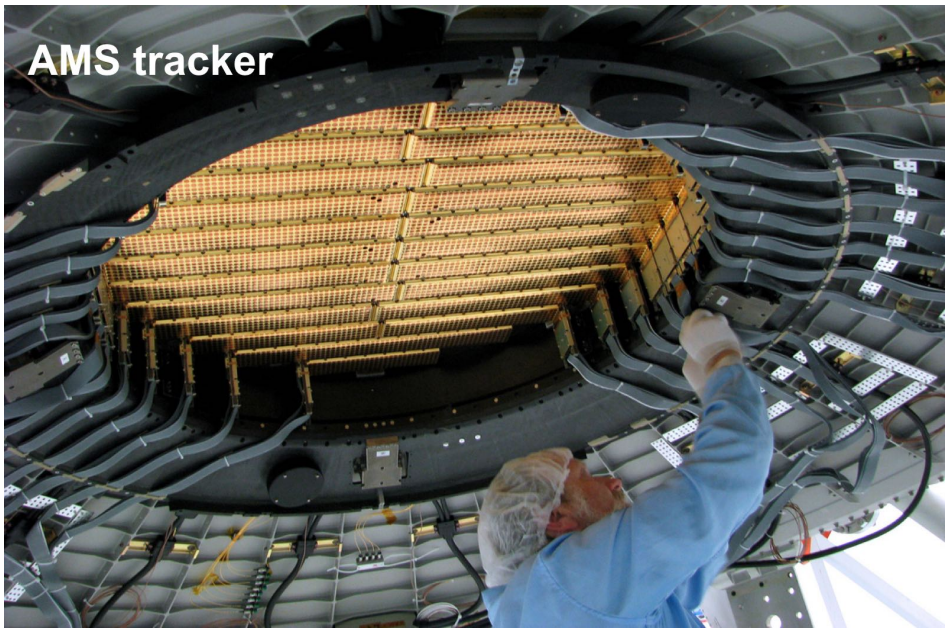
- HV-CMOS

  N. Wermes NIM A824 (2016) pp. 483-86



Monolithic CMOS pixel sensors in Space

Low power, reliability & small pixels (< 50 μm)



- ↪ Not much room for heavy magnets in space experiments!
  - ◇ Extra-small pixels to achieve the target tracks resolution
  - ◇ No much room for power supplies also: ultra low power definitely a must!
  - ◇ Extreme reliability in harsh operational conditions

⋆ **Monolithic CMOS pixel sensors are a good choice to meet these goals!**

Opportunities for CMOS sensors

- CMOS radiation sensors are relevant for many applications, but..

	Scalable to large area architecture	**Extra low-power mode**	**Fully depleted sensor (sensitivity)**	**Fully depleted sensor (speed)**
High Energy Physics	Scale economy in large detectors	Reduced material budget (no cooling)	dE/dx capability (equival. to Si-strips)	Cost-effective timing layers, pile-up reduction
Space applications	Reliability for space-born large detectors	High spatial resolution space-born detectors		
X-ray and UV Imaging	Reduced dead area in imaging panels		Broad spectrum imaging (0.5 eV to 10 keV)	Counting mode possible
Medical imaging and tracking	Self-supporting sensors to avoid scattering			Accurate timing for PET, particle tracking matching

- ⋆ There is not an optimal electronics design that can serve all applications
- ⋆ There isn't even an unique sensor optimization
- ⋆ What about sensor technology?

A versatile technology

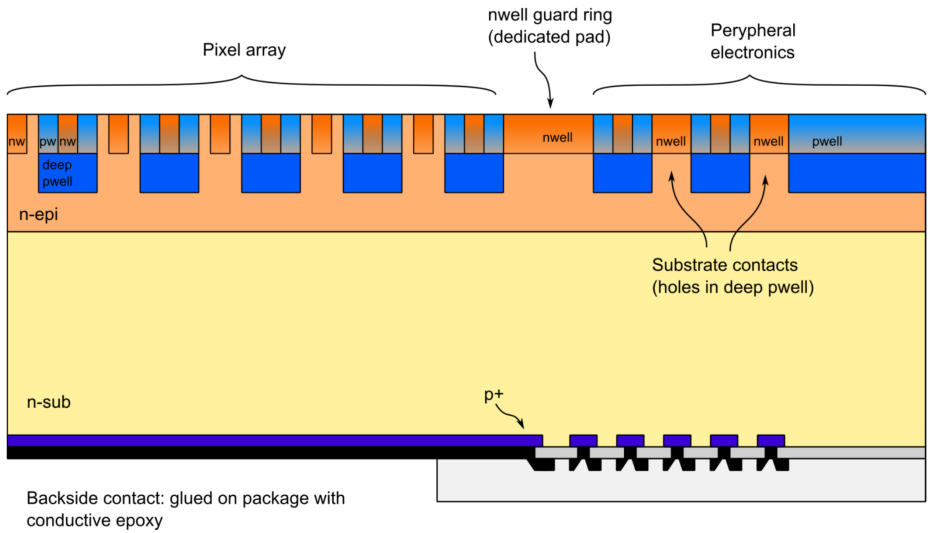
It would be interesting to have a sensor platform that allows for:

- ⋆ Active sensor thickness in the range 50 μm to 500 μm or more;
- ⋆ Operation in full depletion with fast charge collection only by drift;
- ⋆ Small charge collecting electrode for optimal signal-to-noise ratio;
- ⋆ Scalable readout architecture with ultra-low power capability (O(10 mW/cm2));
- ◇ **Easy compatibility with standard CMOS fabrication processes**

The ARCADIA project @ INFN

Advanced **R**eadout **C**MOS **A**rchitectures with **D**epleted **I**ntegrated sensor **A**rrays

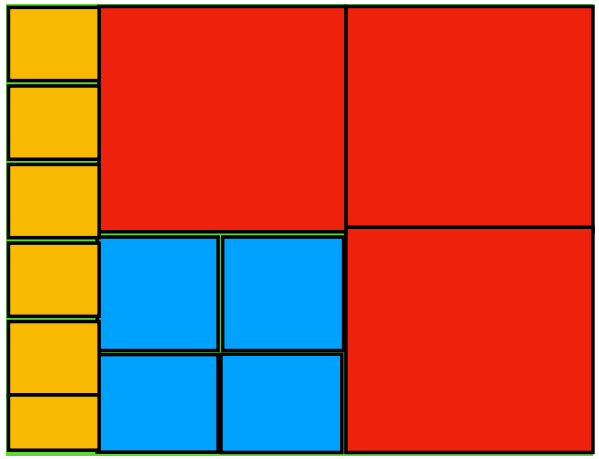
- Goal: full depletion in 100-500 μm.
- Technology: 110 nm CMOS technology, high-resistivity bulk
- Both NMOS and PMOS transistors
- Custom backside process developed (collab. LFoundry)
- The depletion starts from the backside
- At the backside, the main diode is surrounded by a guard-ring
- Pixel capacitance lower than 20 fF



ARCADIA: System-grade Demonstrator

Engineering run by summer 2020

- Pixel size between 10 μm and 100 μm;
- embedded electronics with sparsified readout;
- binary readout modality for maximum rate capability, or
- analogue sampling on-pixel, digitisation on periphery;



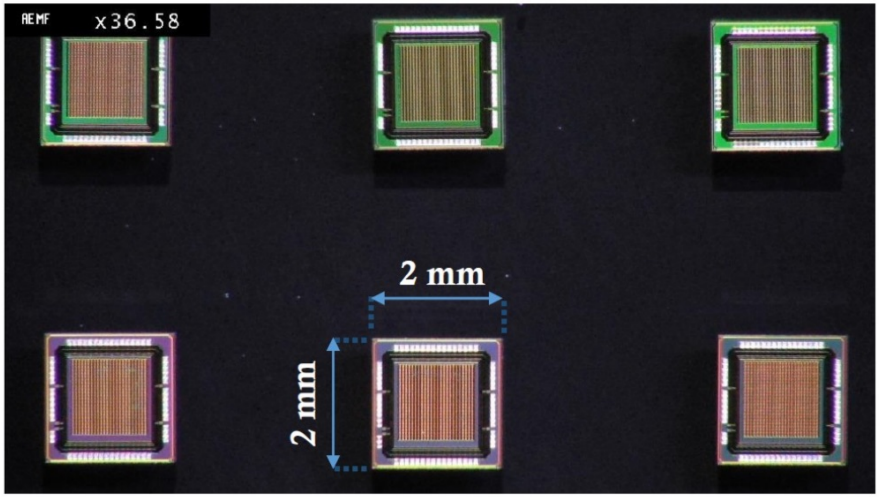
- data-driven readout and low-power digital architecture for data and control signal transmission;
- modular architecture for a straightforward scaling of the design to a reticle-size sensor

SEED Project - INFN CSN V

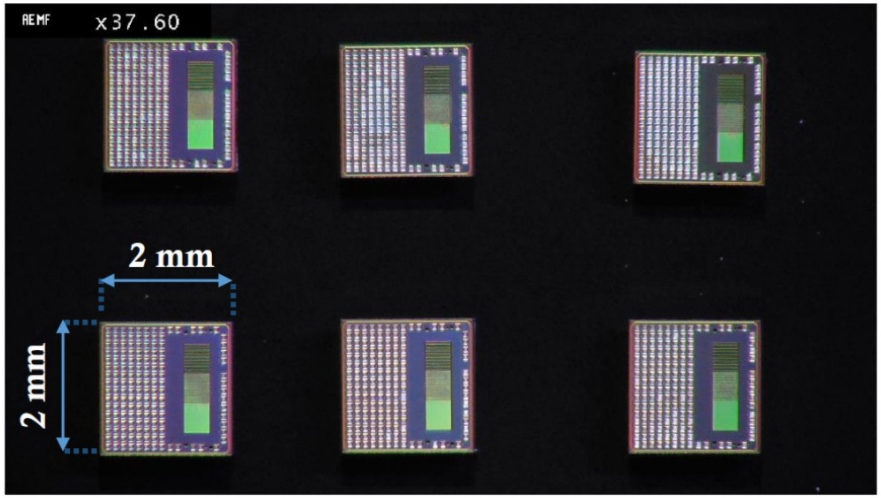
- **SEED : Sensor with Embedded Electronics Development**
- Goal: fully depleted monolithic pixel sensor
- Good timing resolution O(ns)
- Integrated CMOS pixel electronics
- Process development with an industrial partner: **LFoundry**
- INFN Divisions: Torino, Padova, Trento, Frascati, Perugia
- INFN-LFoundry patent pending

First silicon prototyping

Complete monolithic sensor



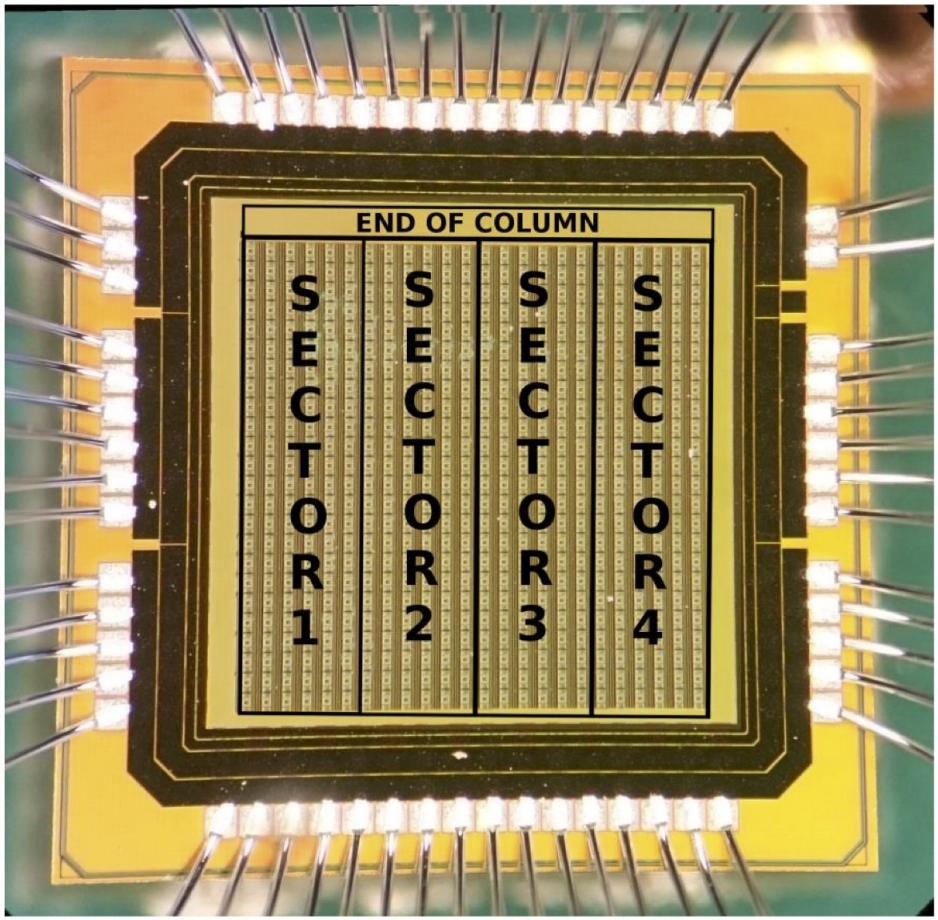
Test chip



Technology	110 nm double side CMOS technology
Metal layers	6
Size	2 X 2 mm^2

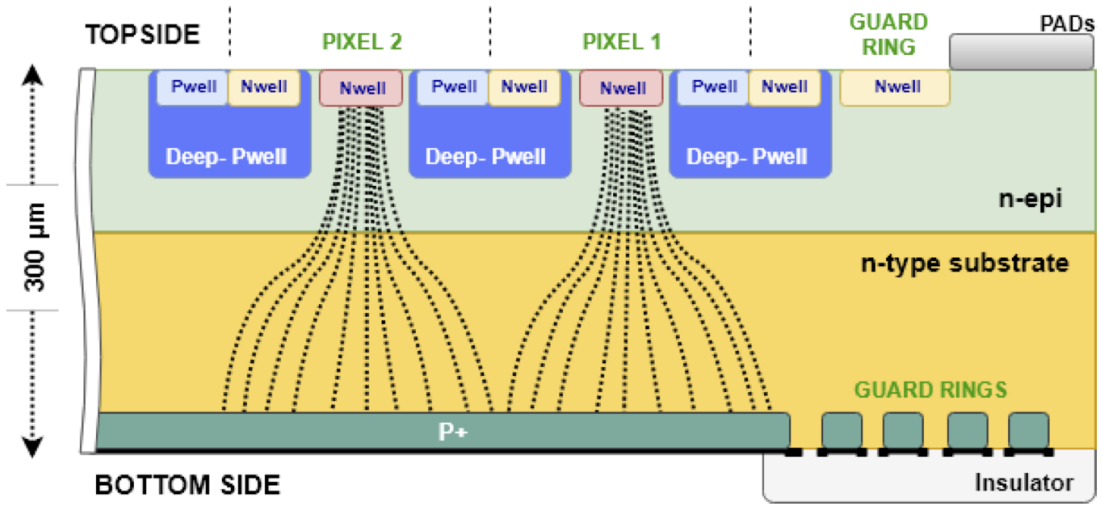
- Wafers with small different epitaxial layer thickness have been used for the production

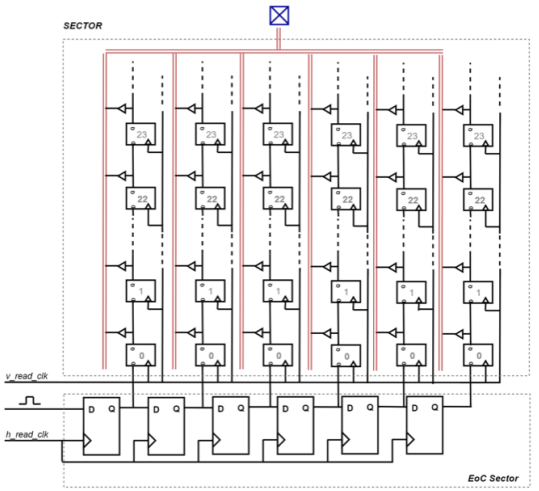
The MATISSE Demonstrator

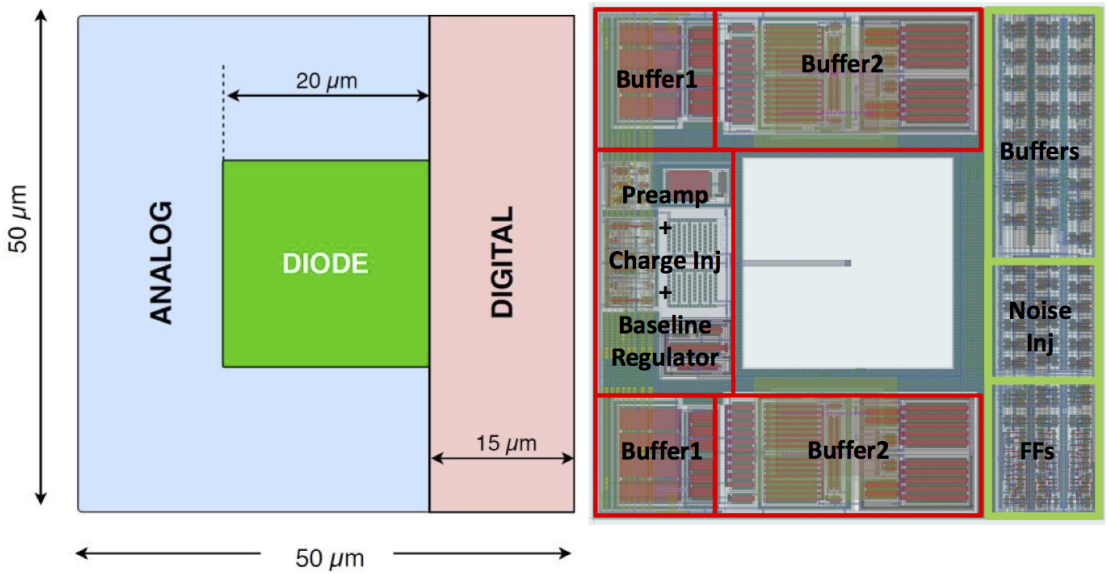


- Monolithic sensor with embedded CMOS electronics.
- Compatible with a standard CMOS process flow
- matrix of 24 x 24 pixels organised in 4 sectors
- Analog readout with CDS
- 2x2 mm^2 die, VDD=1.2V

Sensor architecture





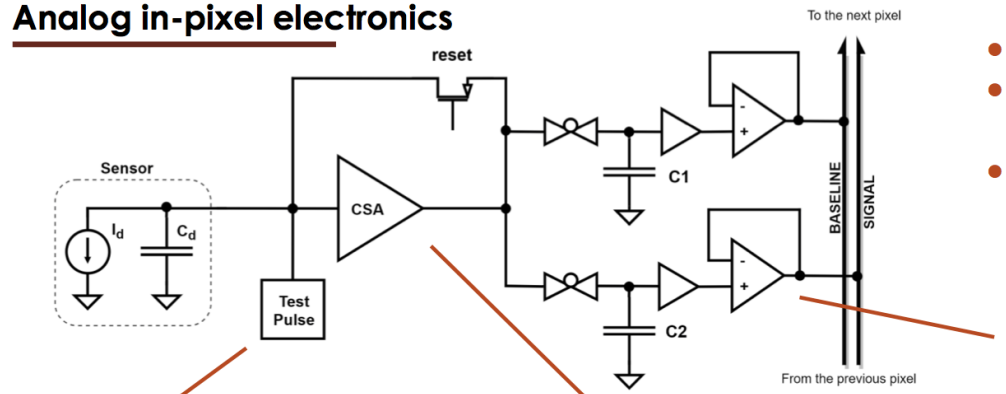


Sensors with Embedded Electronics Design (SEED)

Supported by INFN R&D Committee

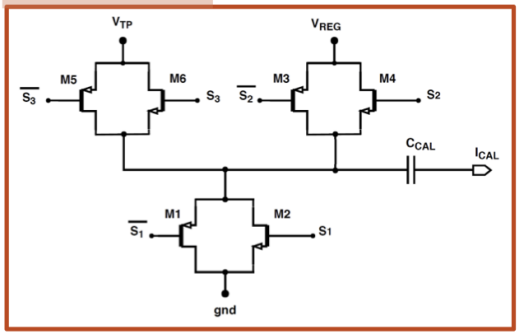
In-pixel electronics

Analog in-pixel electronics

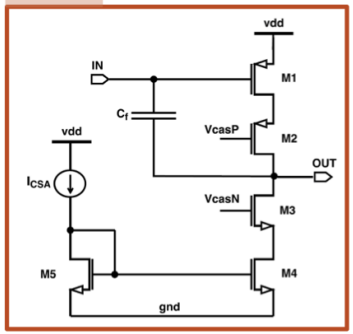


- Analog gain = $1/C_f$
- Analog buffer based on a switched o amp amplifier → high dynamic range
- The calibration system: test pulse injection and baseline regulation

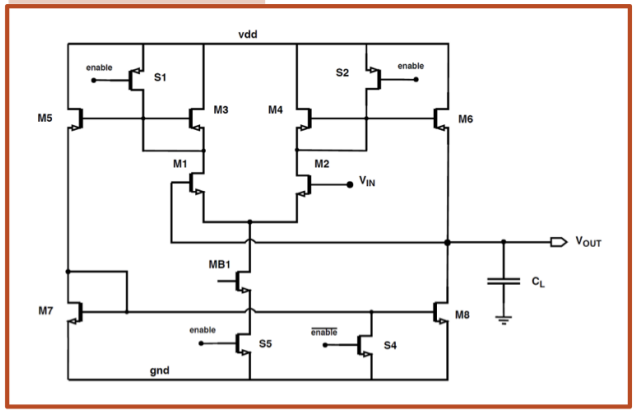
Calibration



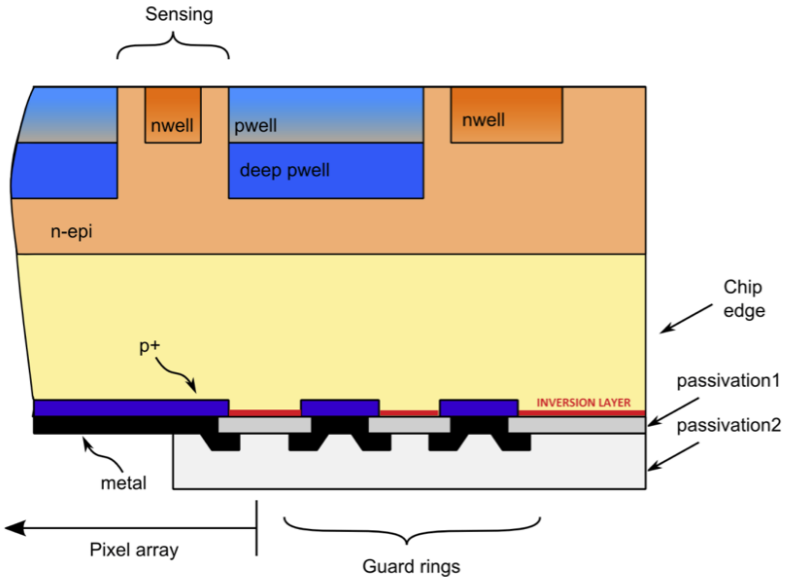
CSA

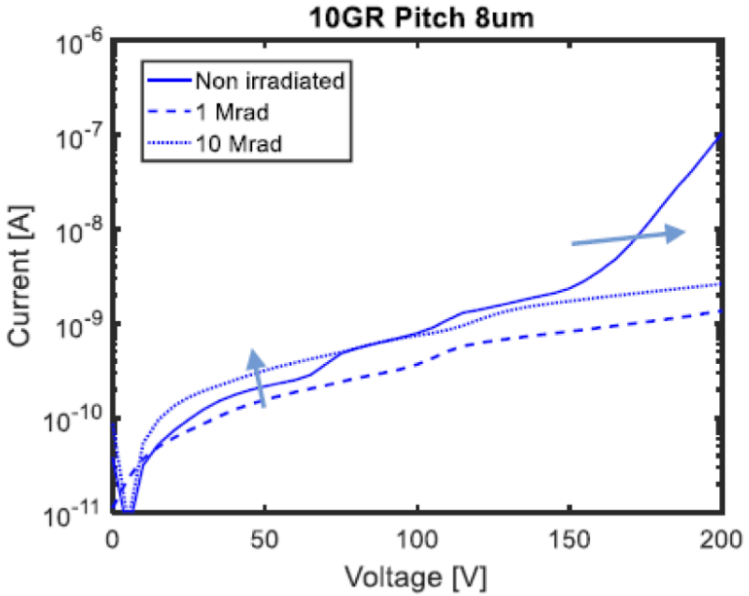


Analog buffer



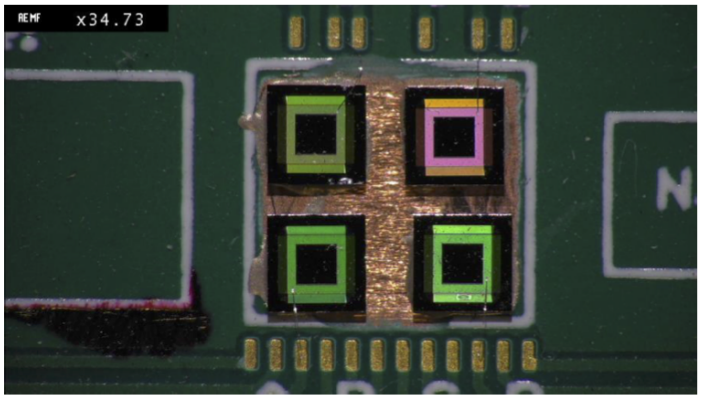
Depletion studies: test structures



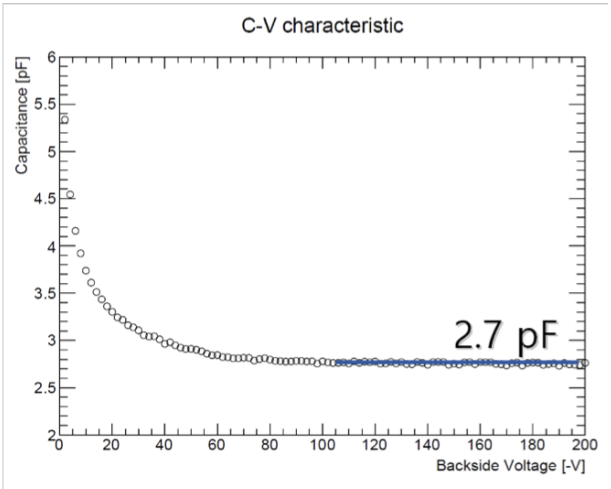


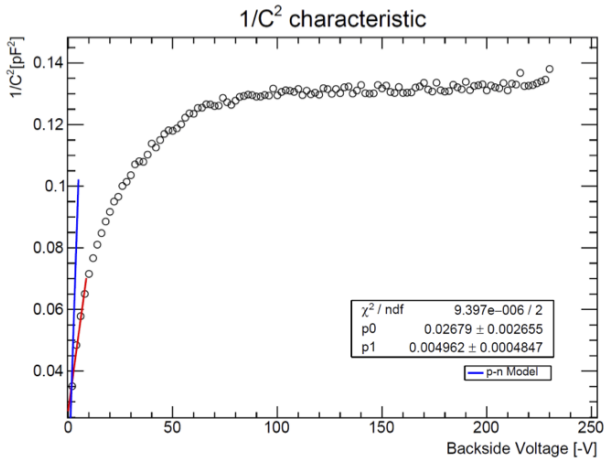
- Several test structures with different guard-ring design
- Inversion layer may compromise guard-rings
- Can be partially cured with irradiation
- Cause understood and fixed in the next release just delivered by the foundry

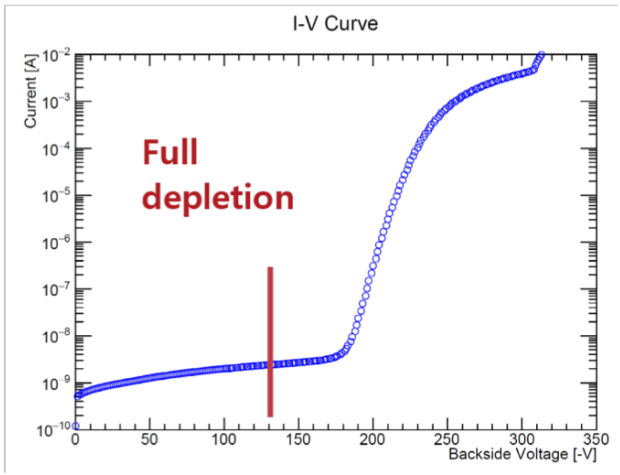
Depletion studies: matrix



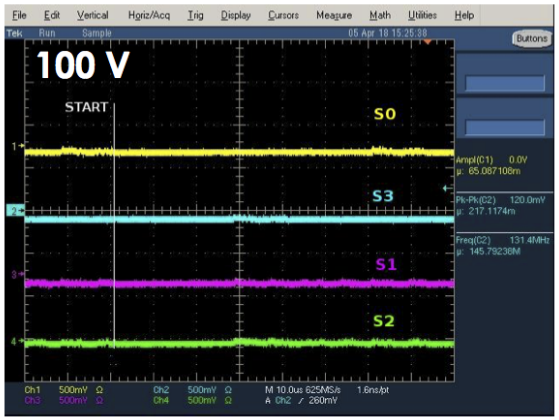
- In full depletion, total matrix capacitance is 2.7 pF
- I-V cure: few nA up to 180 V
- Maximum voltage before breakdown 240 V

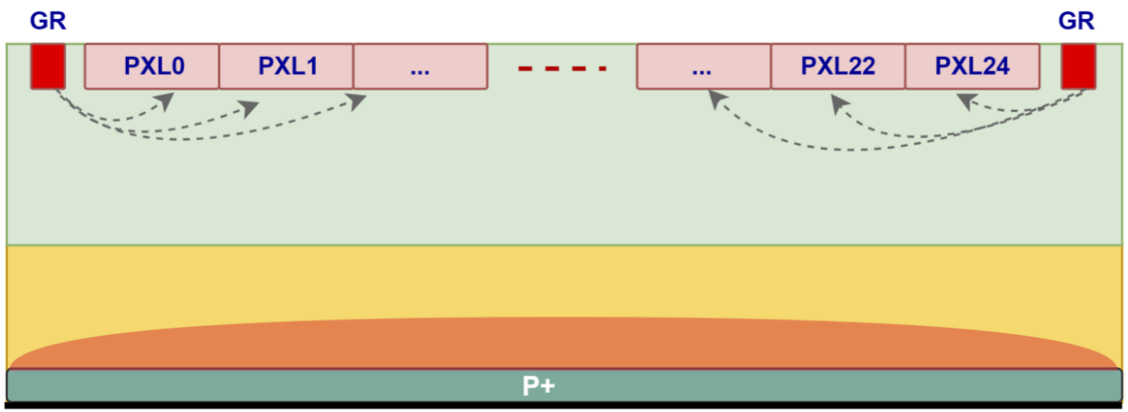


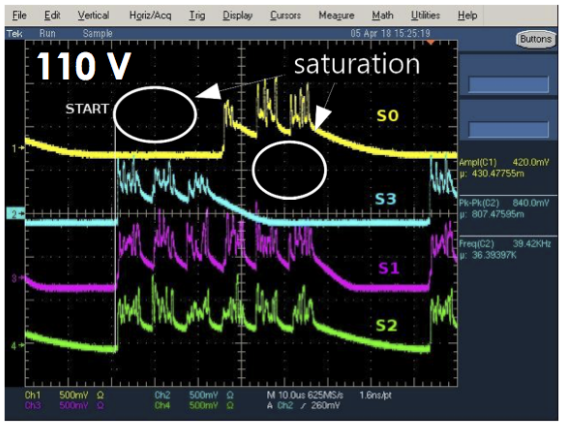


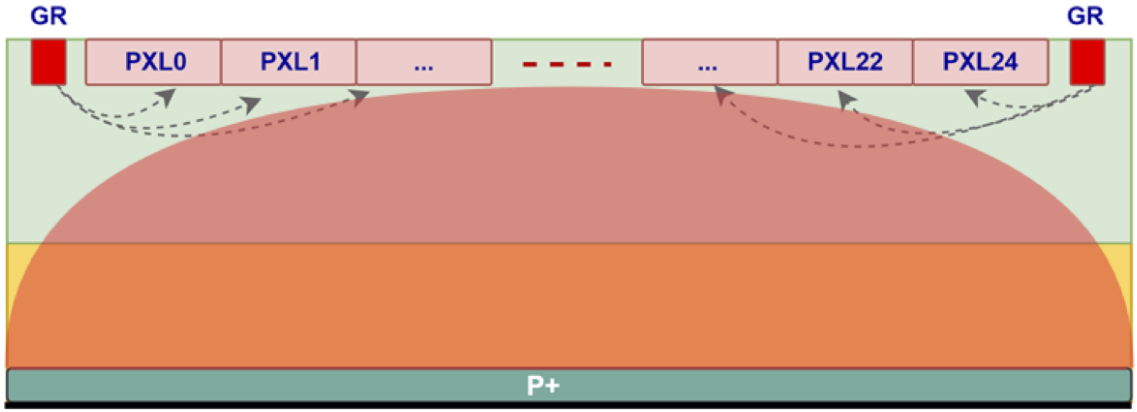


Depletion at work-1

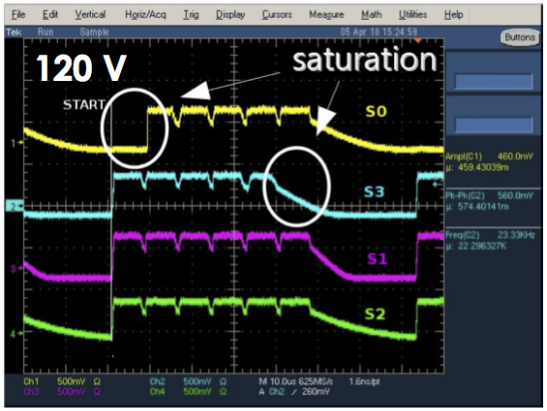


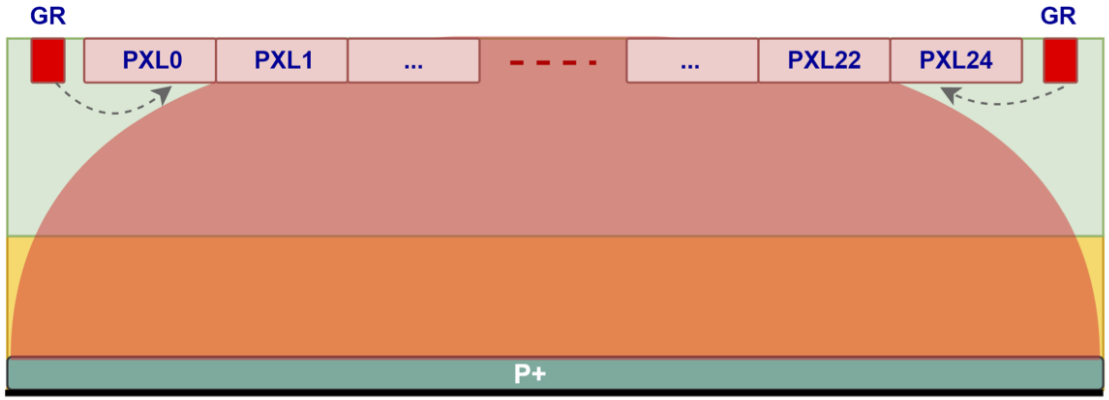


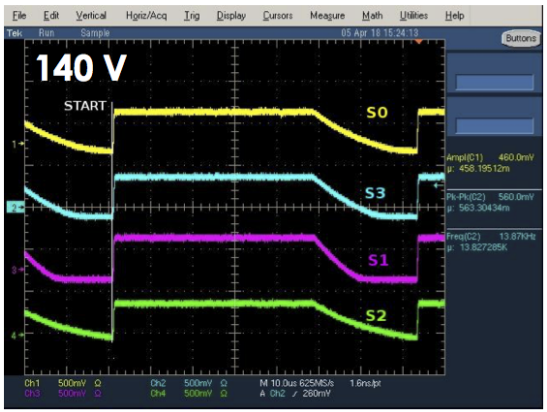


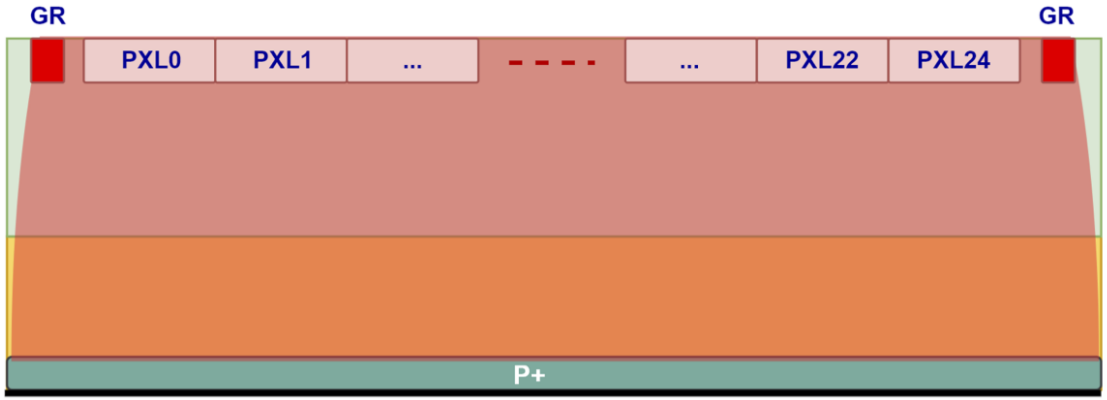


Depletion at work-2

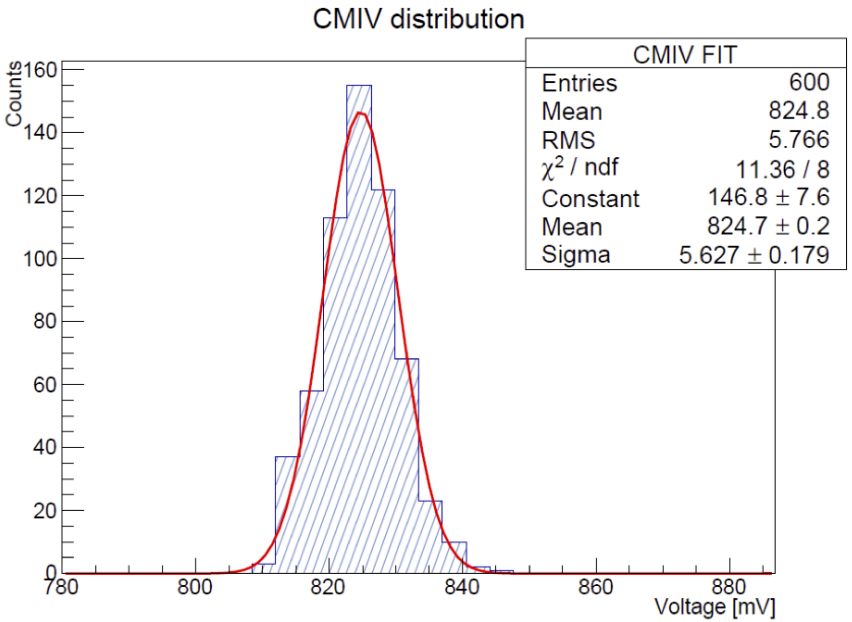


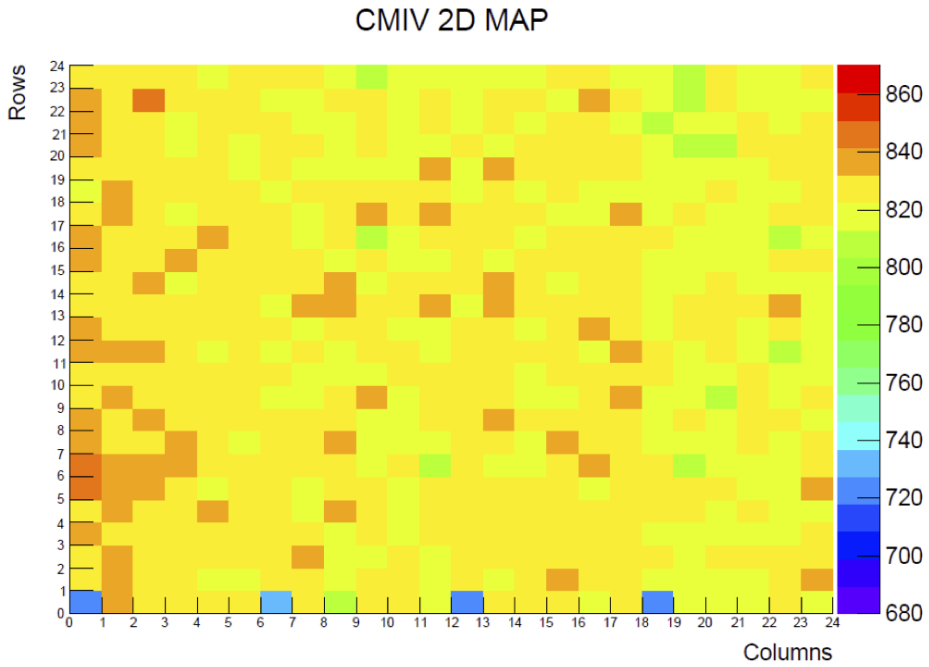


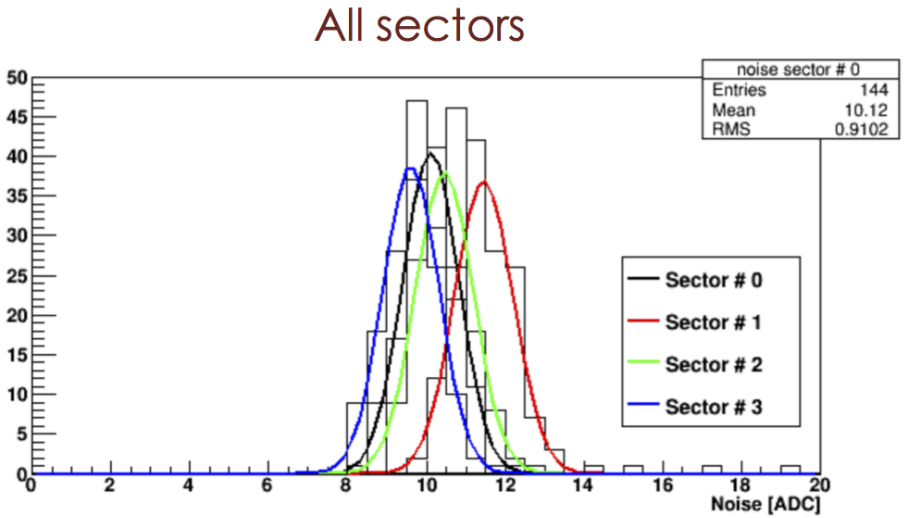


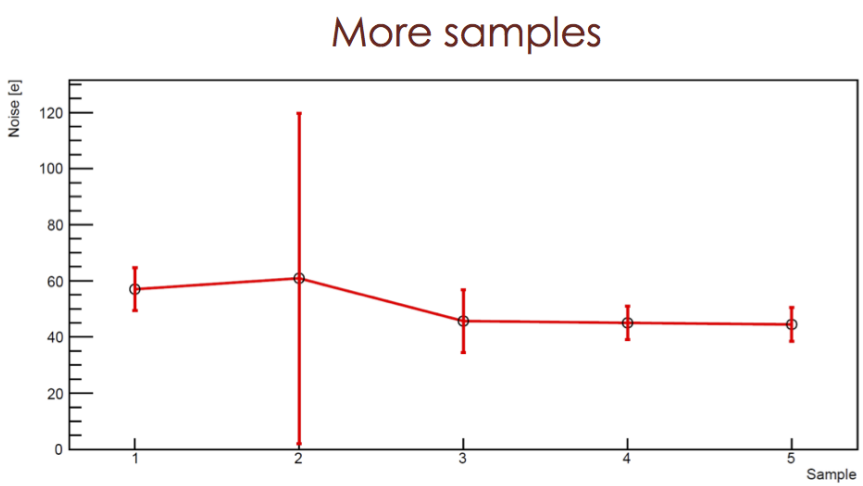


Uniformity

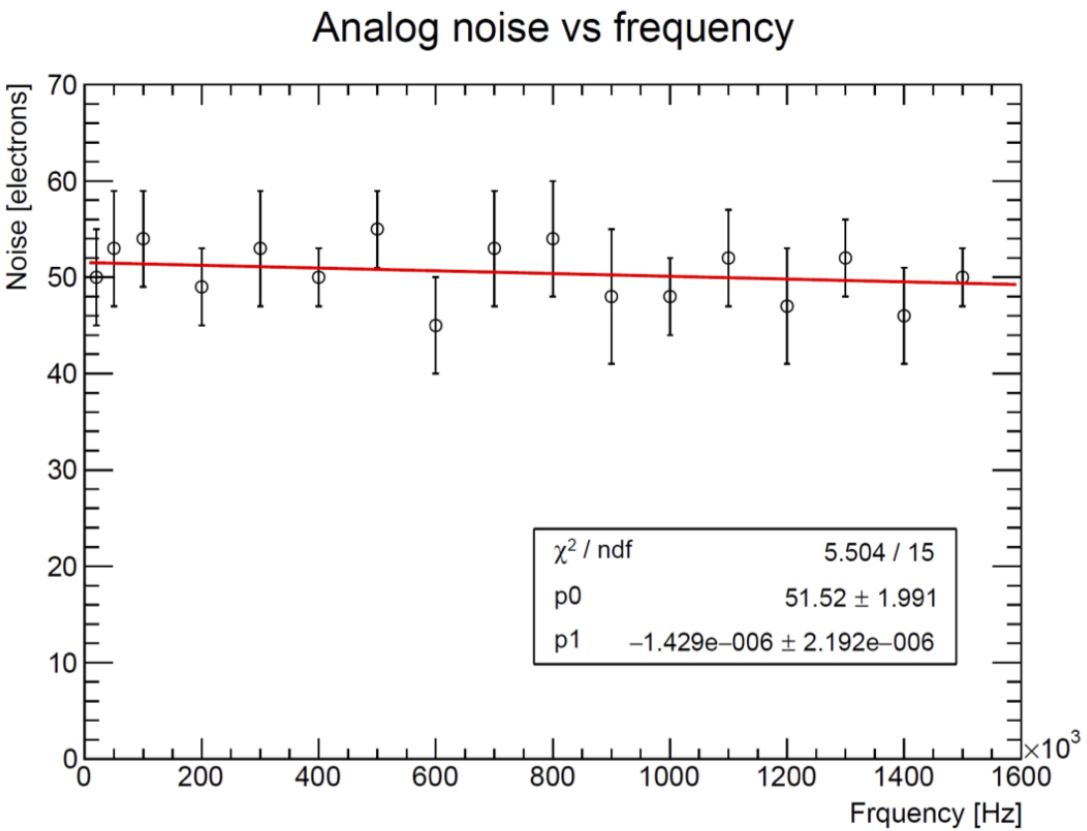

CMIV distribution
CMIV FIT
Entries 600
Mean 824.8
RMS 5.766
χ^2 / ndf 11.36 / 8
Constant 146.8 ± 7.6
Mean 824.7 ± 0.2
Sigma 5.627 ± 0.179
Counts
Voltage [mV]


CMIV 2D MAP
Rows
Columns


All sectors
noise sector # 0
Entries 144
Mean 10.12
RMS 0.9102
Sector # 0
Sector # 1
Sector # 2
Sector # 3
Noise [ADC]


More samples
Noise [e]
Sample

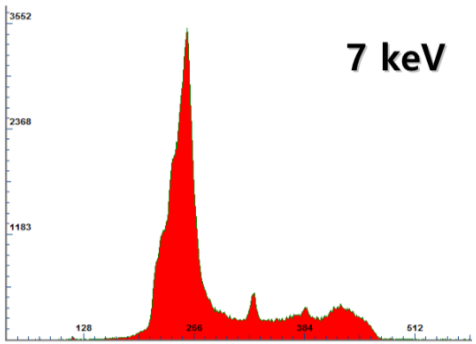
Digital (non) interference

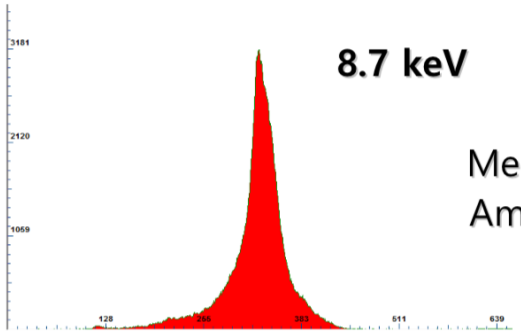


- Very good isolation between analog and digital circuits

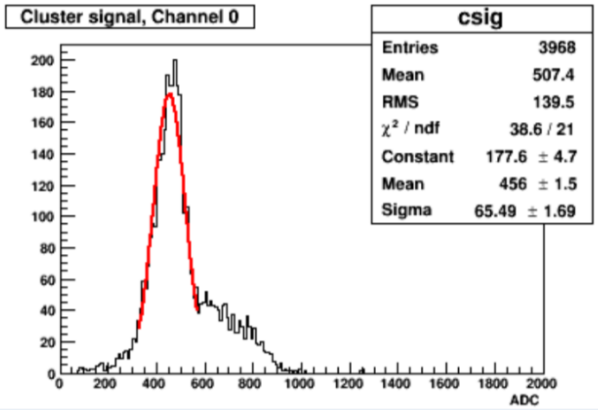
With X-Ray...

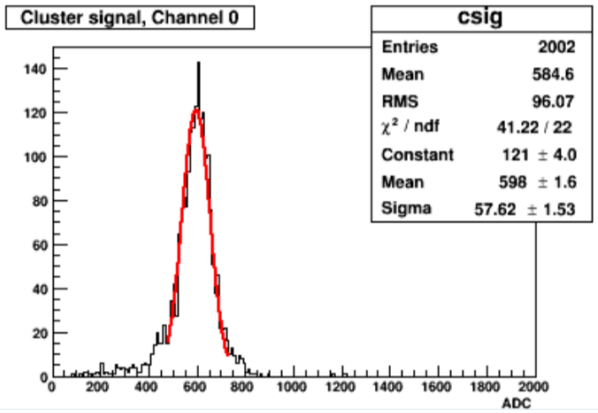
- Calibration made by means of the facility for total dose RP-149 Semiconductor Irradiation System.
- A monochromator has been used to get a monochrome spectrum.
- Two different energies selected: 7 KeV and 8.7 KeV.





Measured with the Amptek XR-100CR

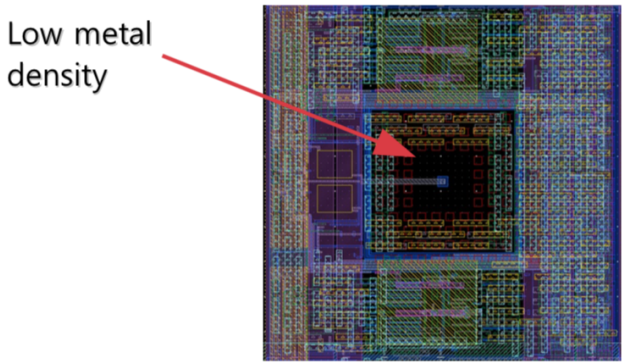




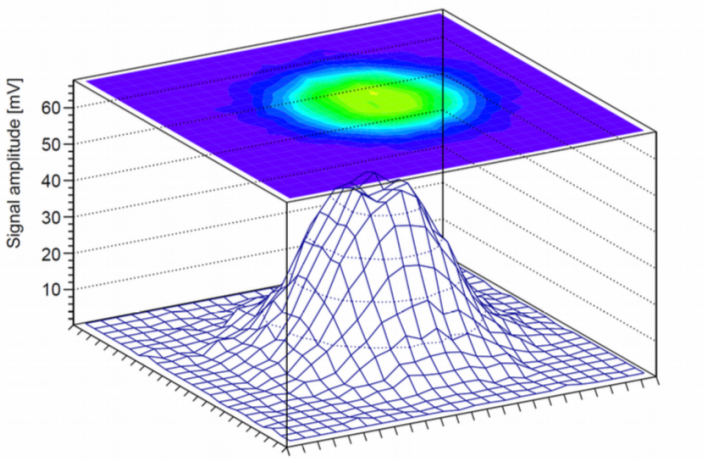
Measured with MATISSE

...and laser

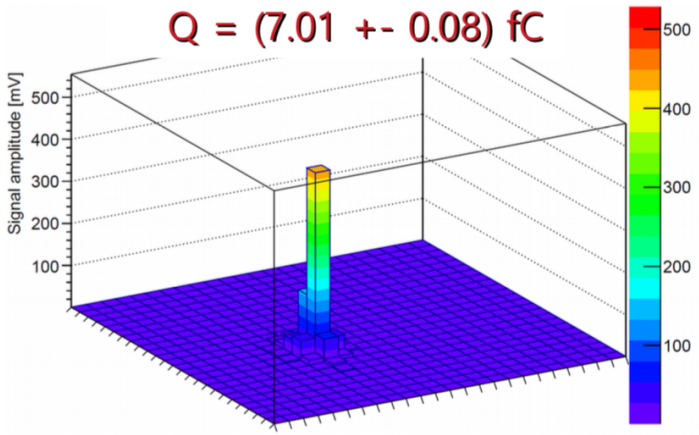
- The metal fillers of the channel has been designed so that left free the pixel centre for optical measurements.
- A laser of with a **wavelength 1060 nm** has been used for the measurements
- The laser spot has been focused up to reach a diameter 8 um
- Laser sent to 16 pixels in the matrix



Non focused pulse



Focused pulse



Outlook

- R&D effort on DMPAS taking momentum within INFN
- Direct cooperation with a silicon foundry
- Large scale demonstrators planned for mid-2020
- Take as much profit as possible for the existing in the meanwhile

The team

Bologna, Milano, Padova, Perugia, Pavia, TIFPA, Torino

A. Gabrielli, D. Falchieri, G. D'Amen, F. Alfonsi, N. Giangiacomi, A. Cervelli, A. Andreazza, M. Caccia, R. Santoro, A. De Angelis, P. Giubilato, J. Wyss, A. Candelori, R. Rando, D. Bastieri, G. Ambrosi, P. Placidi, D. Passeri, L. Servoli, A. Scorzoni, G. Traversi, L. Ratti, C. Vacchi, L. Gaioni, S. Noli, L. Pancheri, G.-F. Dalla Betta, A. Ficorella, M. Zarghami, M. Favaro, R. Iuppa, P. Zuccon, F. Nozzoli, B. Di Ruzza, E. Ricci, M. Rolo, R. Giampaolo, A. Rivetti, S. Beole', R. Wheadon, F. Tosello, N. Demaria, A. Di Salvo, G. Dellacasa, M. Mandurrino

Backup Slides

Segmentation

$$ENC \propto v_n \frac{C_d}{\sqrt{T_p}} \qquad v_n = \sqrt{\frac{4\gamma k_B T}{g_m}} \qquad I_C = \frac{I_D}{2\mu C_{ox} \frac{W}{L} \phi_T^2}$$

- For the same ENC

$$C_D \to C_D/2 \Rightarrow I_D \to I_D/4$$

- Difficult to beat pixels in binary mode