Tungsten – silicon electromagnetic calorimeter

R&D status

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Sampling ECAL calorimeter projects based on silicon diodes ..

ILC - (ILD or SID)

- a duty cycle of about 1% on electronics … no need for active cooling
- a readout every 500 ns
- 26 layers for 24X0 , cost estimation made by experts : cheaper than CMS ECAL

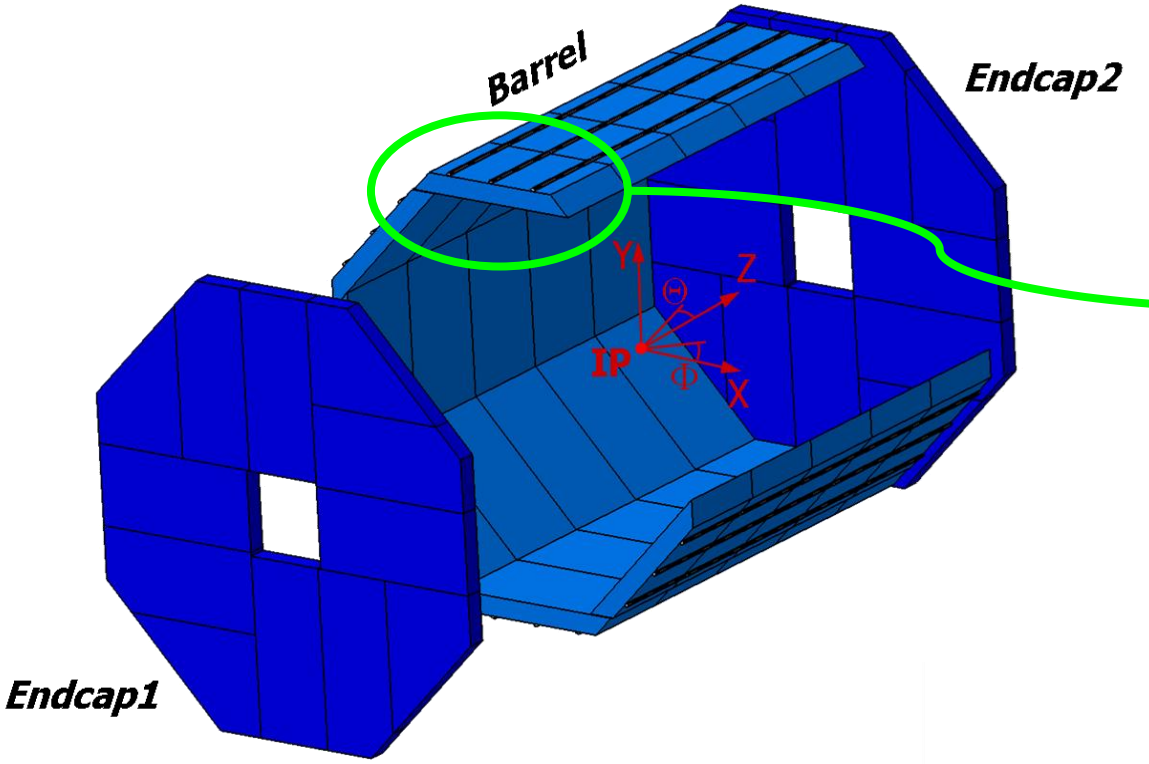
CMS HGCAL

- Readout every 25 ns, active cooling , large number of layers
- High level of radiation (10^{16} n/cm²/year) … variation of the gain of the diodes
- pile-up mitigate the power of PFA

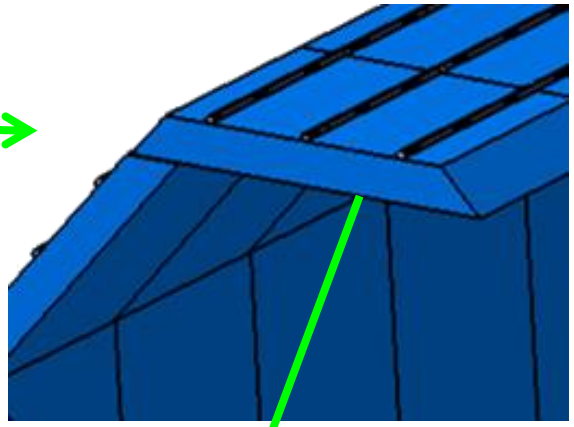
CEPC

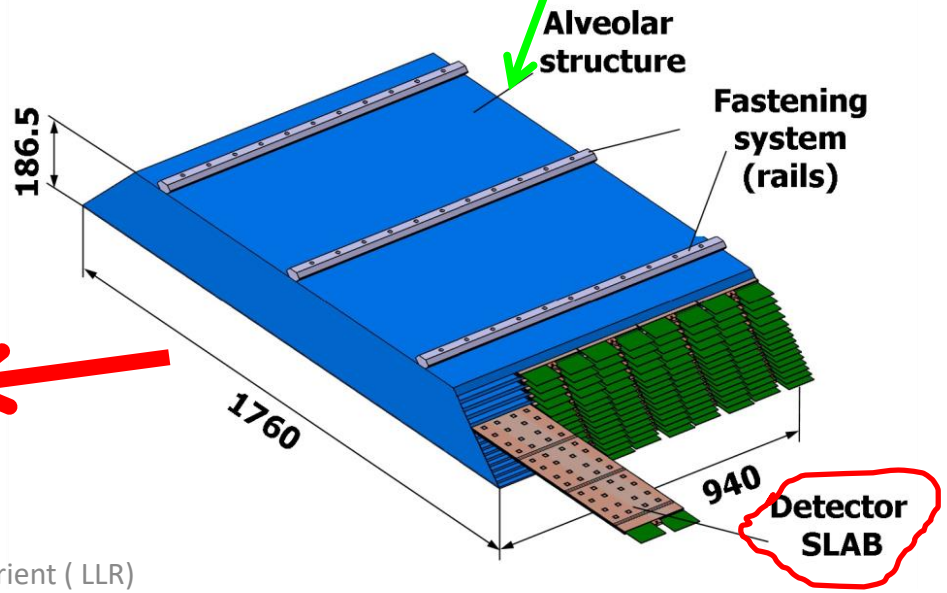
- Readout every 25 ns (hypothesis)
- No problem of radiation
- Need active cooling (It allows pixels size of 6x6 mm – see my presentation at CEPC workshop 2017)
- Small pixel allows time measurement /particle (like in ATLAS or CMS)
- Small pixel allows to run at Z Pole (occupancy)

ECAL GEOMETRY

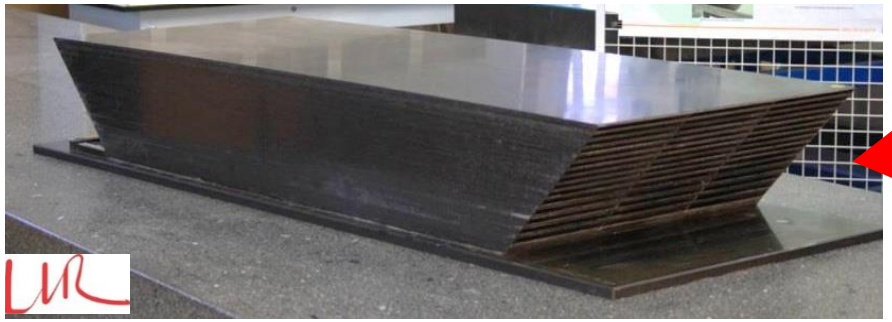


No DEAD ZONE !!!



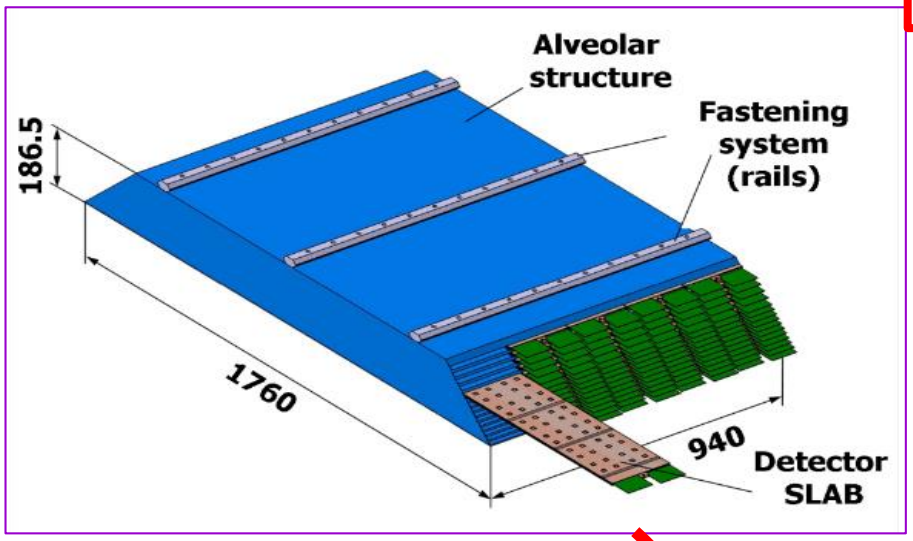


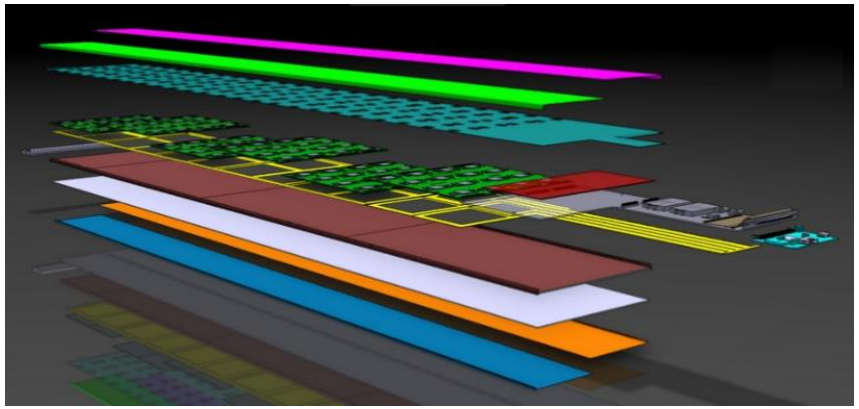
Carbon fiber –Tungsten structure with Alveola to slide in the active layers.

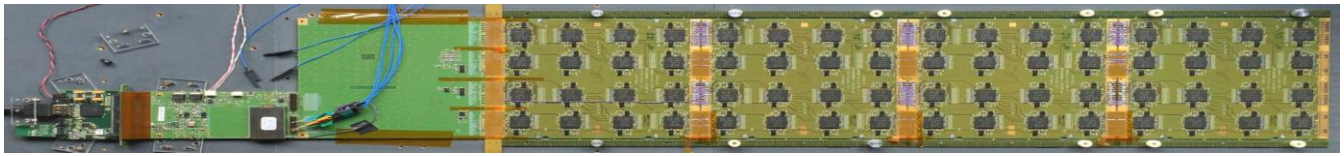


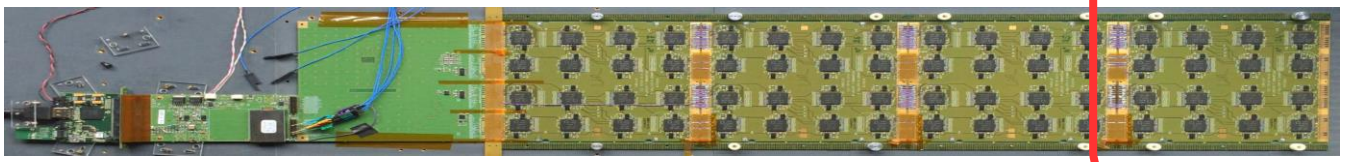
Geometry could be the one of ILD

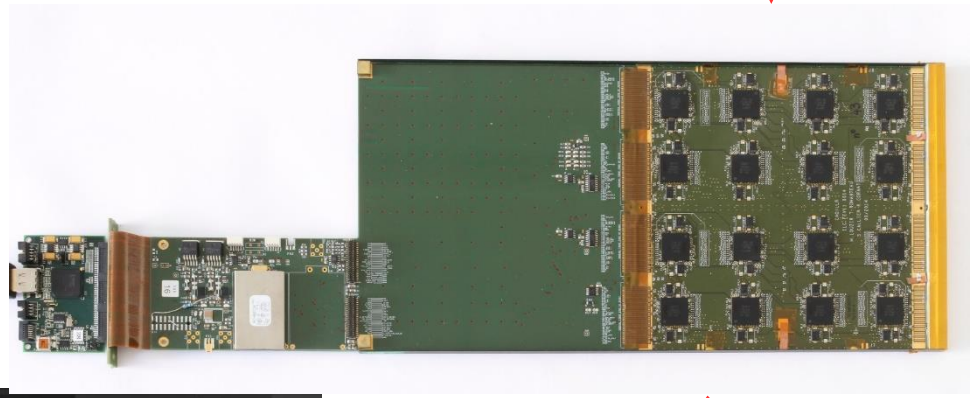
20 to 30 readout layers and
20-24 Rad. Length within thickness<20 cm

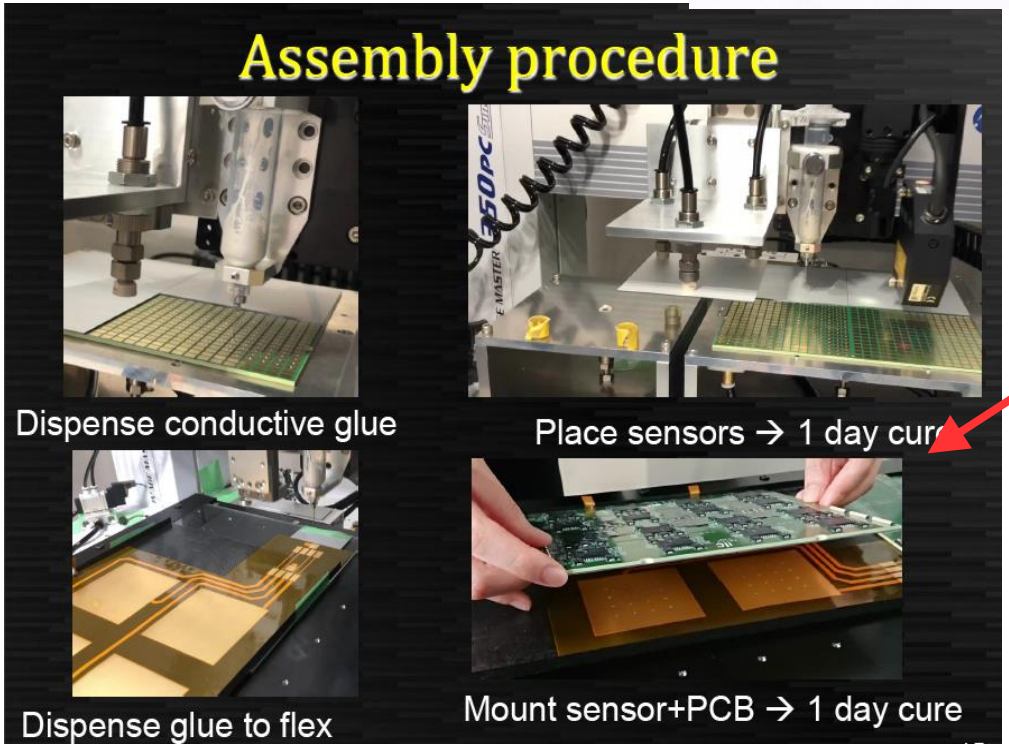






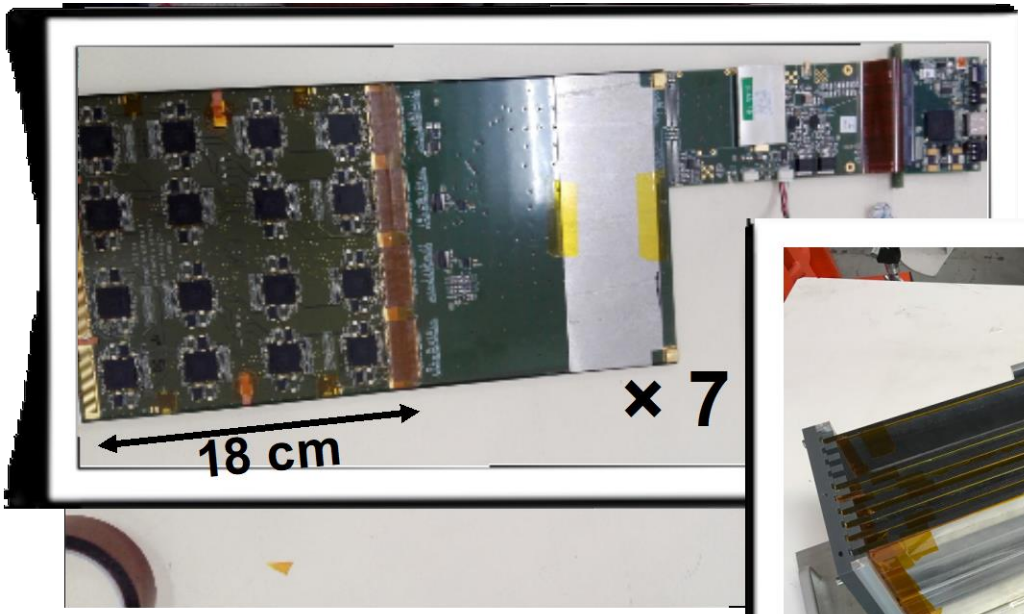


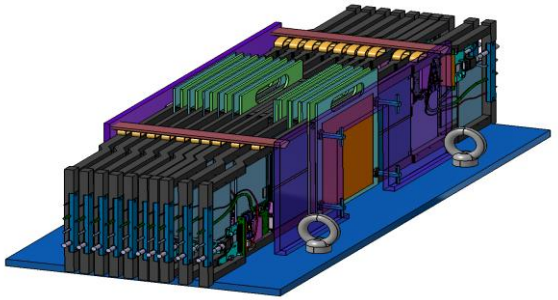


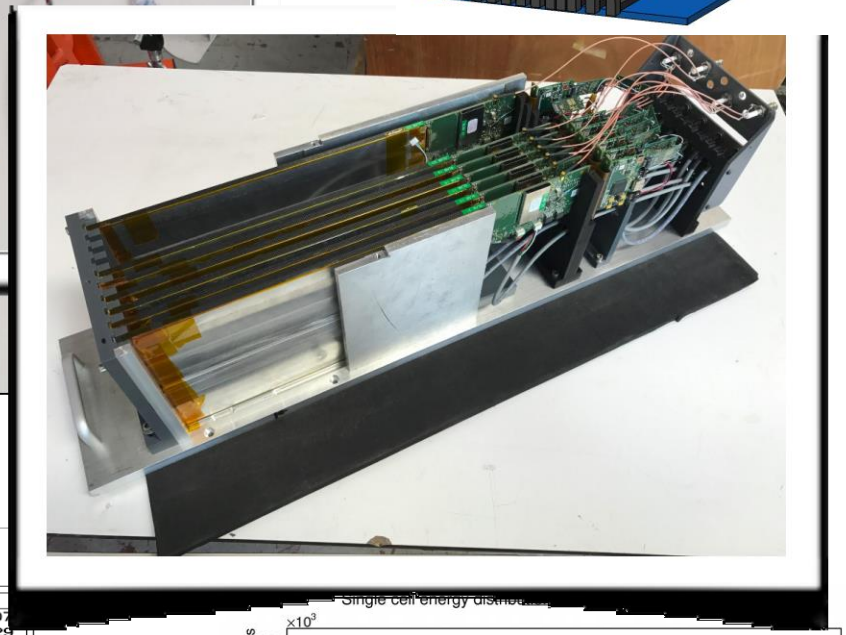


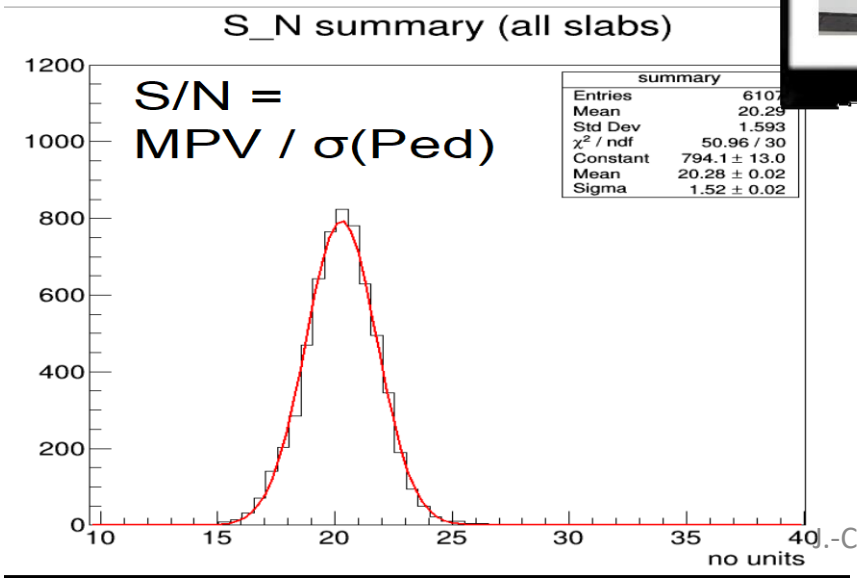
- Wafers glued on one side of PCB
- VFE asics on the other side

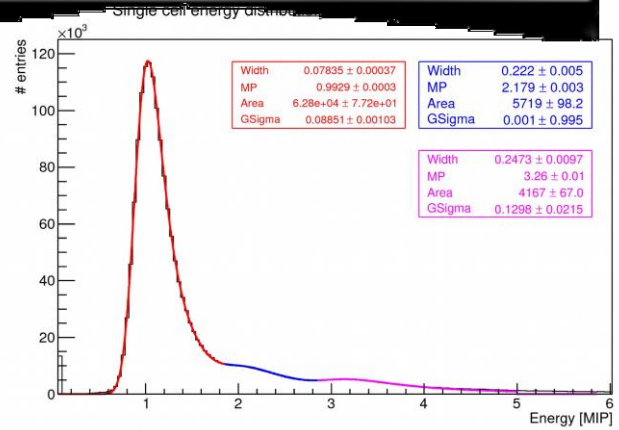
Detector test





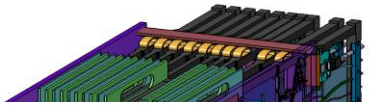


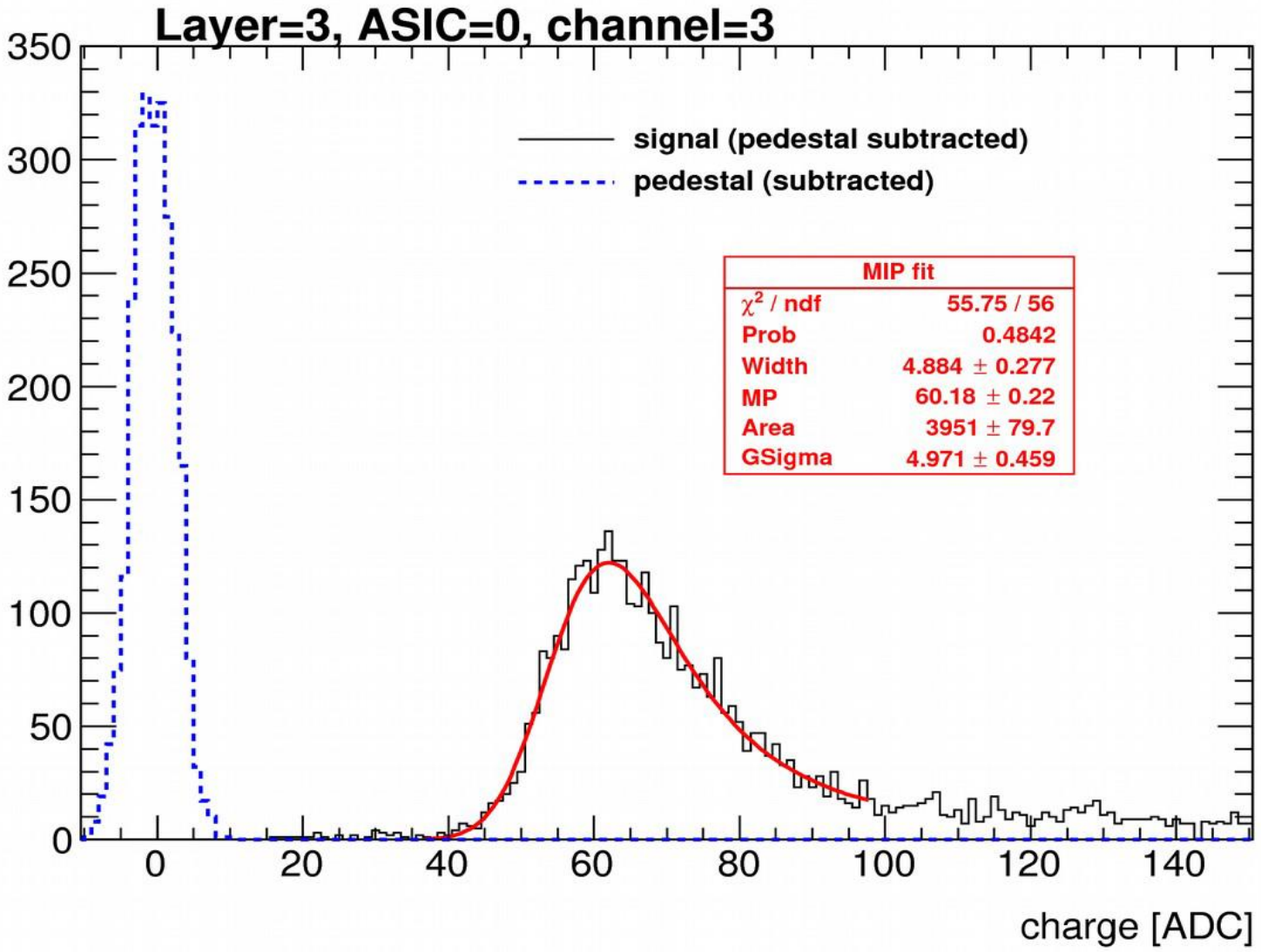


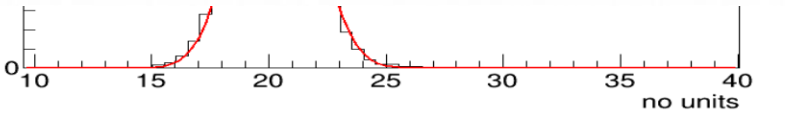


Cumulated « Mip » spectrum in 3GeV e-

Detector test





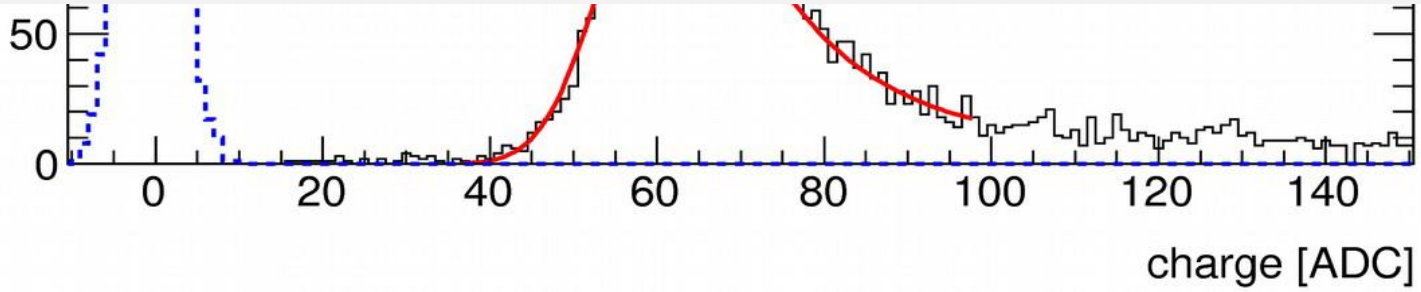


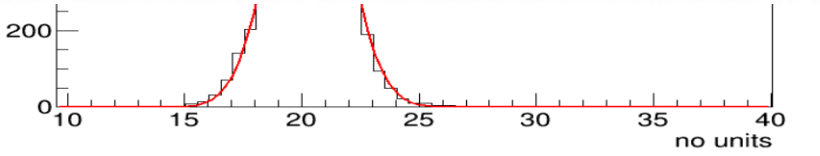
Cumulated « Mip » spectrum
in 3GeV e-

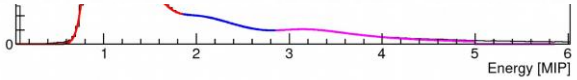
Detector test

When compare to scintillators based ECAL….
It explains partially our choice

Yes, scintillators ECAL is possible,
but it seems more difficult to tune

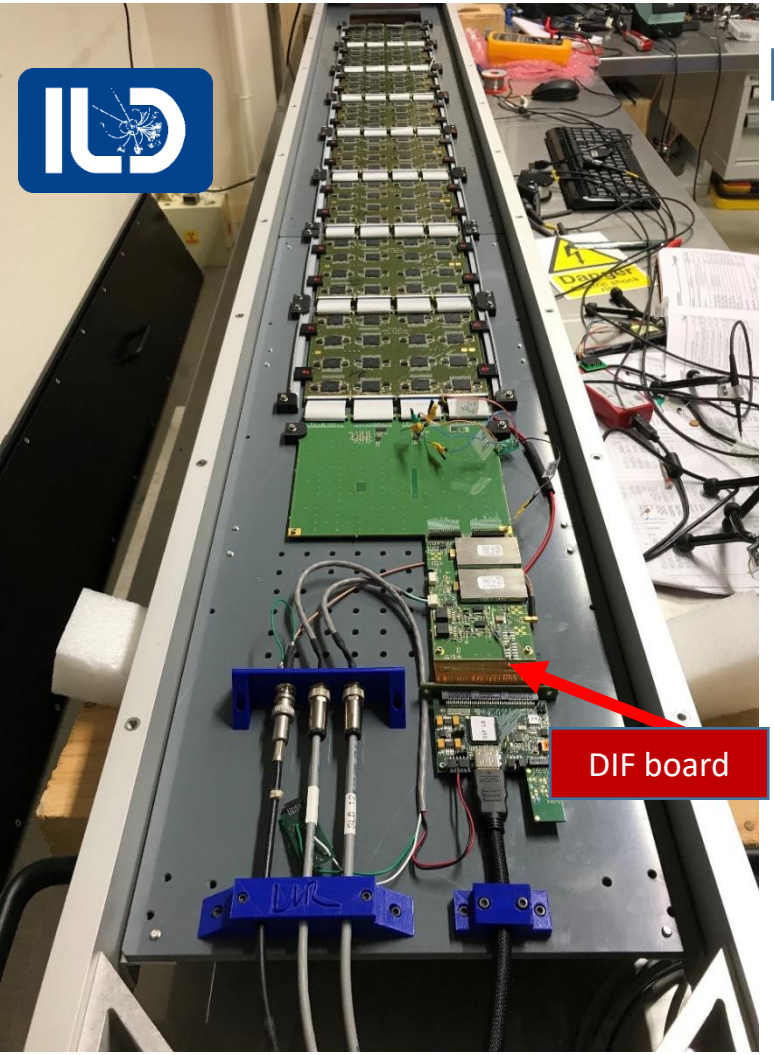




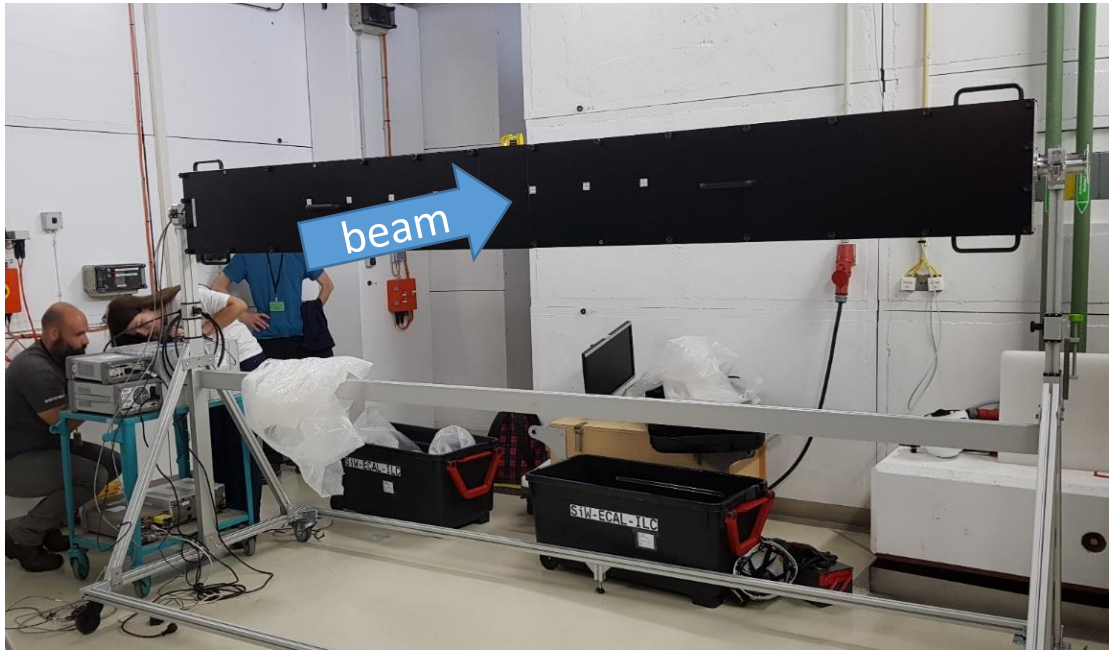


Cumulated « Mip » spectrum
in 3GeV e-

Detector test , long slab



Test Beam DESY July 2018



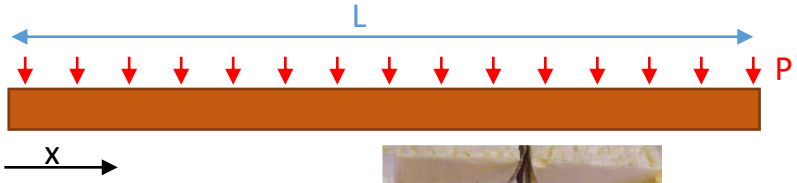
1.6m long , almost the full scale for the final detector

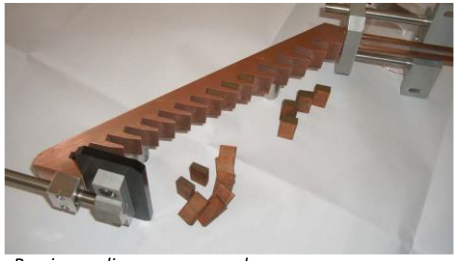
Analysis on going

About Cooling (not in ILC, but for CEPC, FCCee or CLIC)

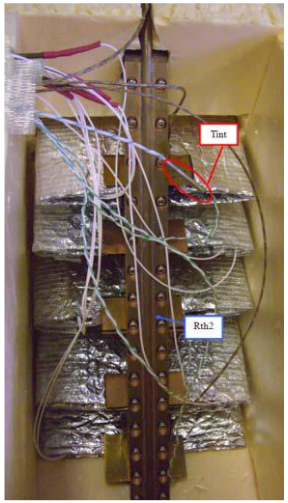
R&D using CMS studies (Thanks to Th. Pierre-Emile from CMS-LLR group)

Passive cooling



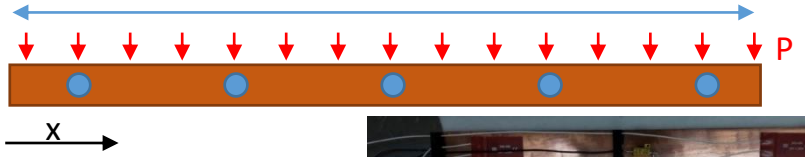


Passive cooling ramp example

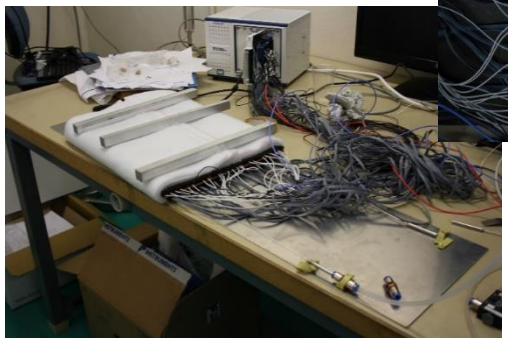


Passive cooling ramp set up test

Active cooling

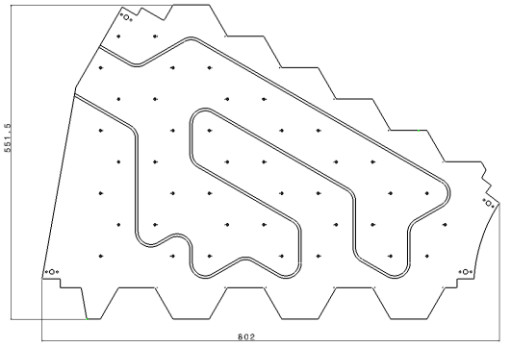


Active cooling test layout (400mm x 300mm x 3mm thick copper plate with 1,8OD pipes embedded)



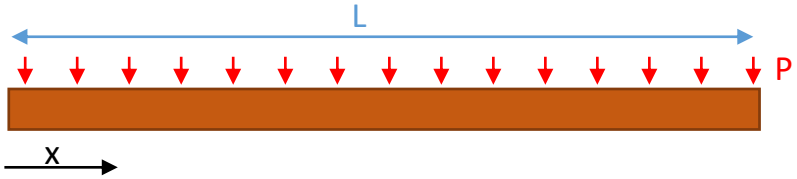
Active cooling set up test with water at room temperature

Cooling test



Copper plate prototype dimensions information

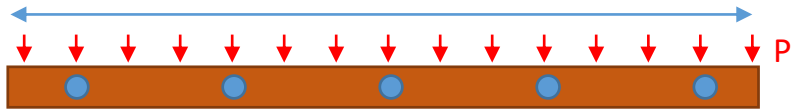
Passive cooling



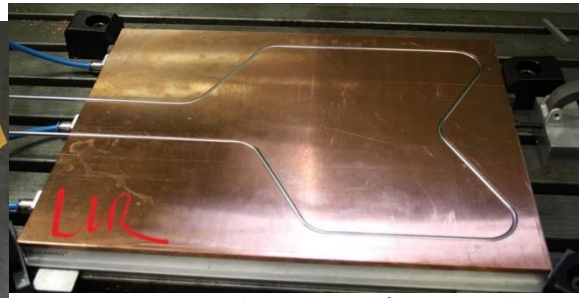
Passive cooling ramp set up test on a 3 layers prototype

- *Passive cooling can lead to more compact solutions depending on the total power to extract and the acceptable temperature gradient*

Active cooling



Pipe insertion on a cooling prototype

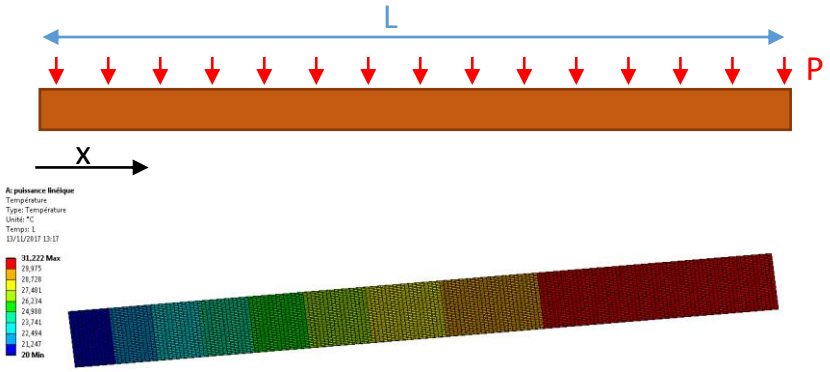


Pipe insertion on a cooling prototype for FEA correlation

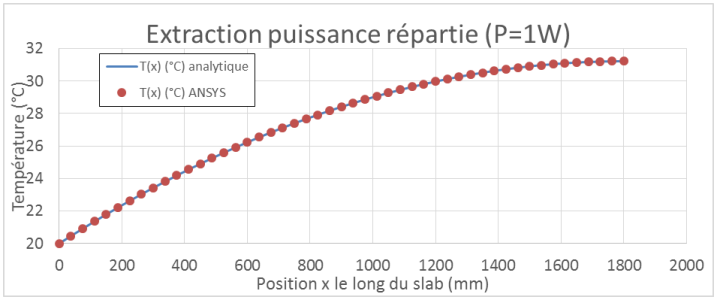
- *Active cooling improves thermal field distribution and can extract much more heat*
- *It requires a qualified pipe insertion process*

Cooling test

Passive cooling

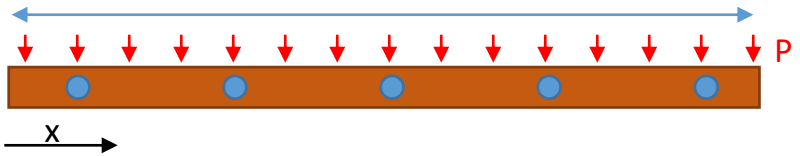


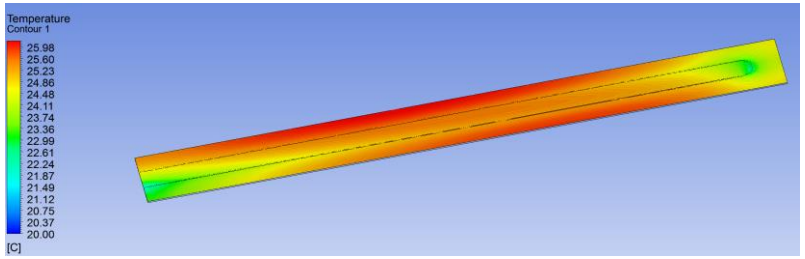
Thermal static FEA analysis thermal field example using ANSYS with 1W extracted



Comparison between thermal static analysis and theoretical approach

Active cooling

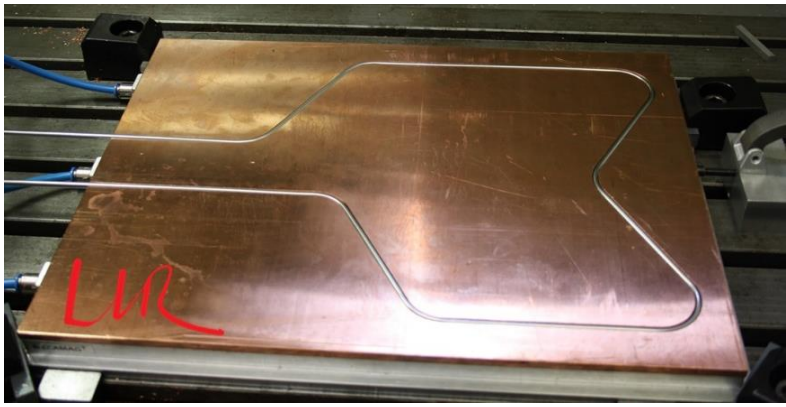


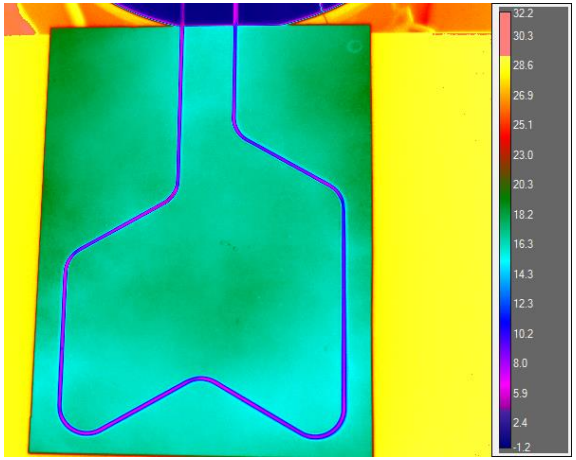


Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe

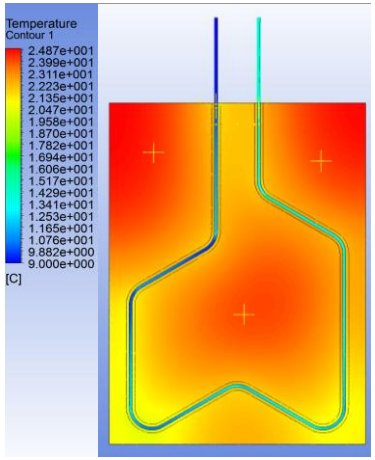
Cooling test

Active cooling pipe insertion test with cold water

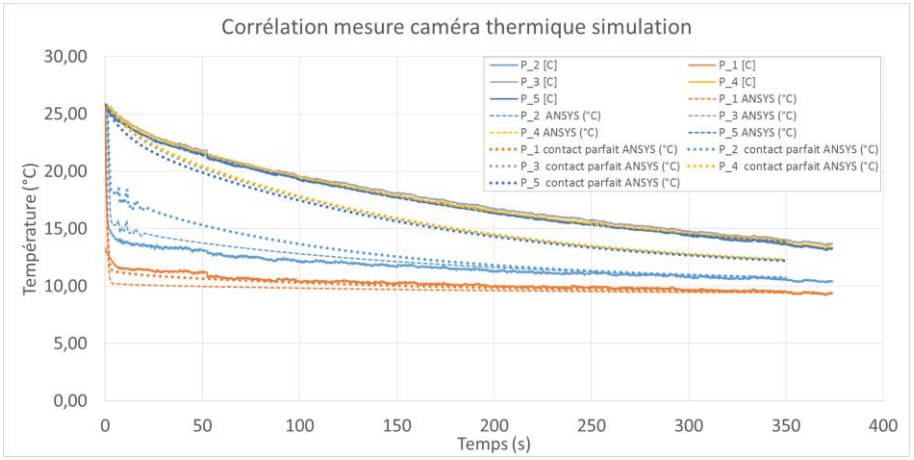




Thermal field registered with an IR camera



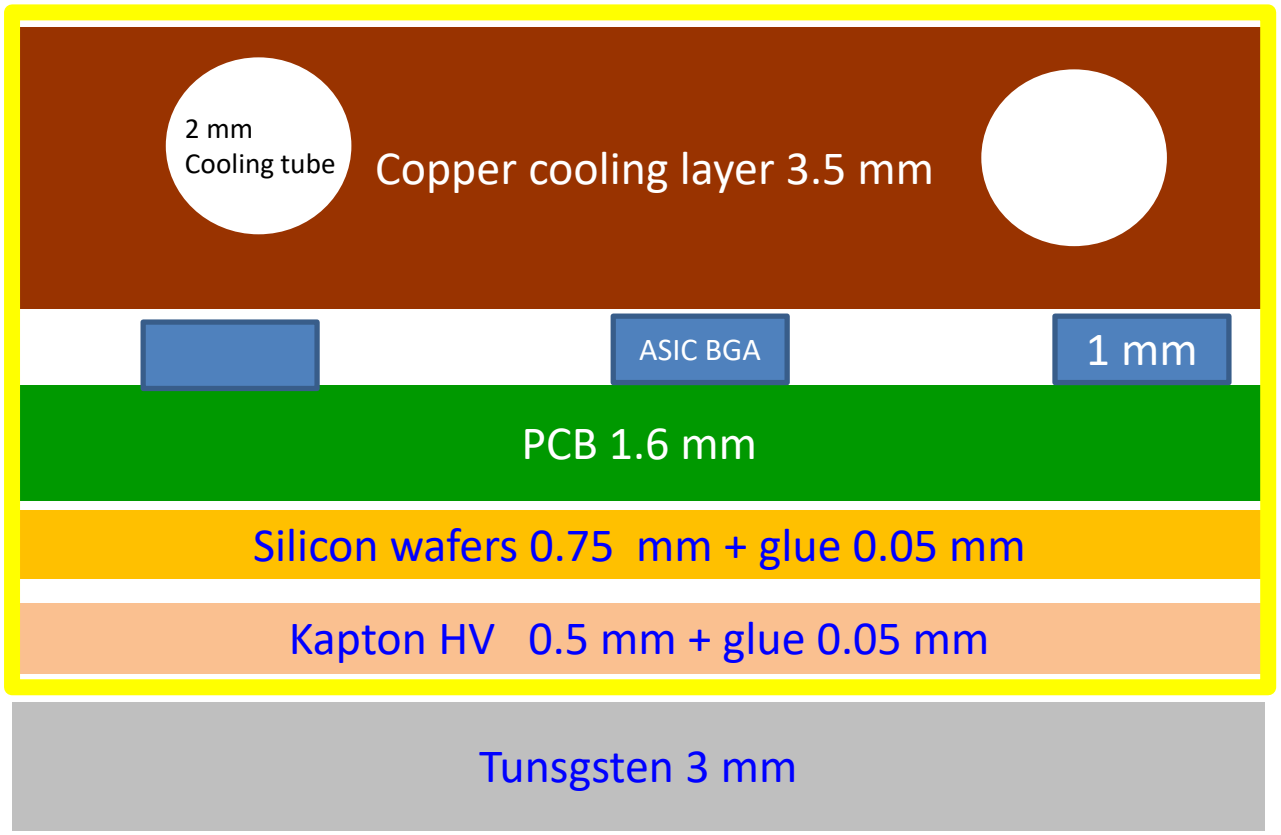
CFD correlation results



CFD correlation results

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling

REALISTIC (from CMS studies) cross section of the ECAL with active cooling



All thicknesses are based on prototypes… (from ILD or from CMS)

No extrapolation

On average 9 mm/layer

Happy with all the progresses , BUT

Standing problems

Hardware

- Readout VFE
- Readout at 1.7 m
- Clock distribution
- Signal at long distance
- Aging of the gluing (10 years checked)
- PCB production
- DIF card small size (4x3 cm)
- Power distribution, cooling distribution
- Definition of quality control and test…

Standing problems

Software

- more than 1 PFA reconstruction software
- Automatic calibration
- HL- Zero suppress
- Test beam data analysis
- etc…

Lot of things to do

Near and mid-term future

Full prototype with about 20 layers at the ~~end of~~ 2018 .. mid/end 2019

- Test Beam (Data taking and analysis) 2019-2020
  (No beam at CERN, remains DESY (low energy) or FERMILAB)

- Going from ILC type to CEPC type. Cooling, pixels size, total rad. Length, etc…

- Going from prototype to "full scalable" (we have already 1.6m long detector slab)

- Interact with industry for optimized production and cost (tungsten, silicon, etc…)
  (amazing for me that HPK is the single producer in the world for high resistivity silicon wafers)

Transfer knowledge to students about ultra-granular calorimeter
(there is specific problems to this type of device…. Ask for to CMS ☺/☹)
Important to learn about with real hardware device… HGCAL can tell you

All groups interested , do not hesitate ,
contact us , there are possibles contributions for all type of expertises
brient@llr.in2p3.fr

CONCLUSION

ECAL for e+e- circular collider at 250 GeV

- Ultra granular calorimeter , optimized for PFA, would do the job at CEPC (including EW physics with tau , i.e. Higgs CP violation studies and at Z-pole)

- Active cooling : R&D demonstrate the feasibility

- Large luminosity and large number of pixels leads to a MANDATORY S/N>10 at MIP This condition is fulfilled by ILD prototype, even at 1.6m from readout concentrator

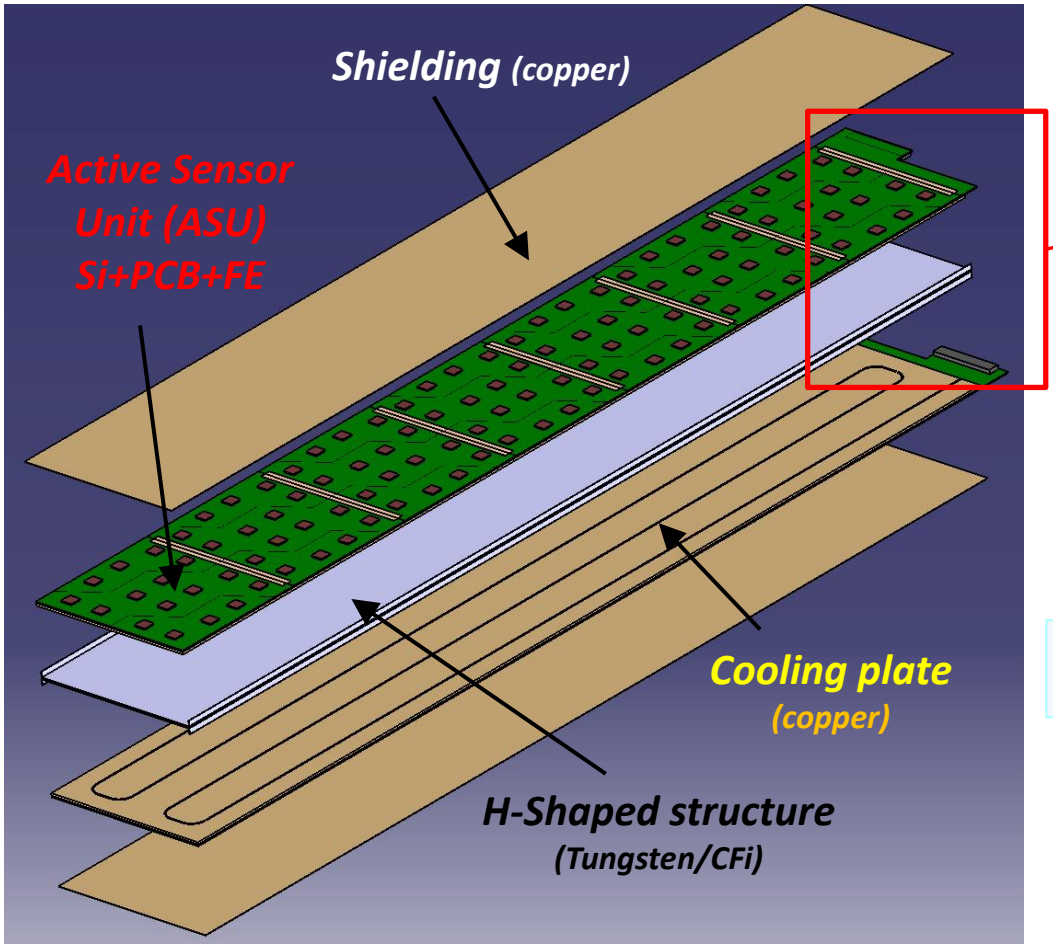
Silicon –tungsten meet the requirements

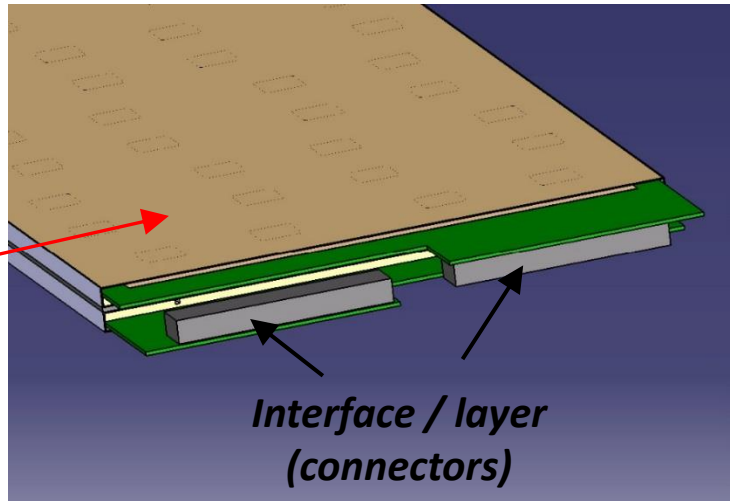
Including the cost … thanks to the upgrade of CMS,ATLAS…. We are talking of about a cost significantly lower than the crystal ECAL of CMS-ECAL….

it is no longer a good reason to say no to silicon

BACKUP

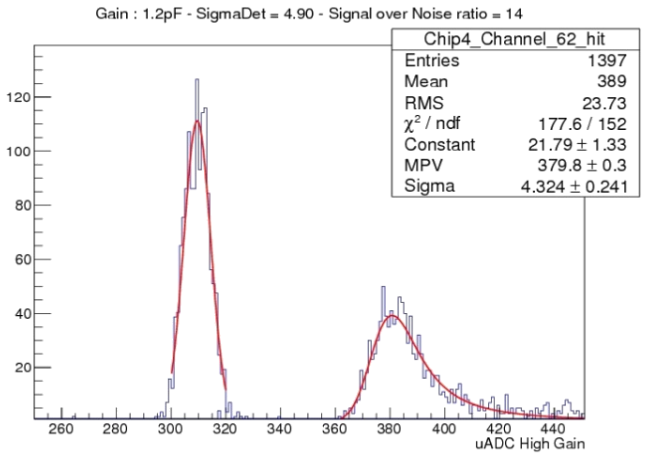
Detector SLAB (exploded view)





Electronics VFE INSIDE

First Test Beam for scalable prototype at DESY - 2012



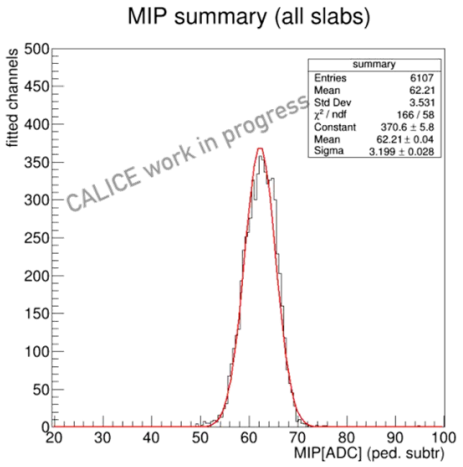
ONE LAYER

S/N ~ 14

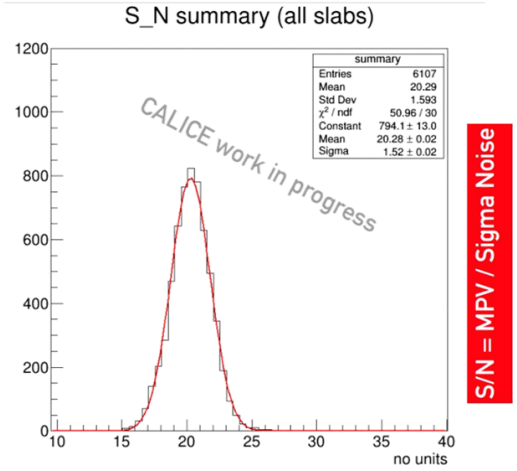
MIP CALIBRATION RESULTS

CALICE ECAL SiW Test Beam at DESY - 2017

- Summary from the MIP fits of the 98% available channels



(MIP position – pedestal position) / pedestal width



S/N = MPV / Sigma Noise

- MPV = 62.2 ADC, sigma= 3.2 ADC (dispersion of 5.1 %)
- S/N = 20.3, sigma = 1.5 (7.4 % dispersion)

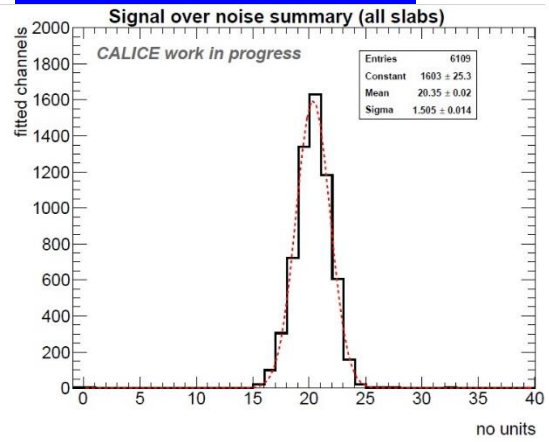
10 LAYERS

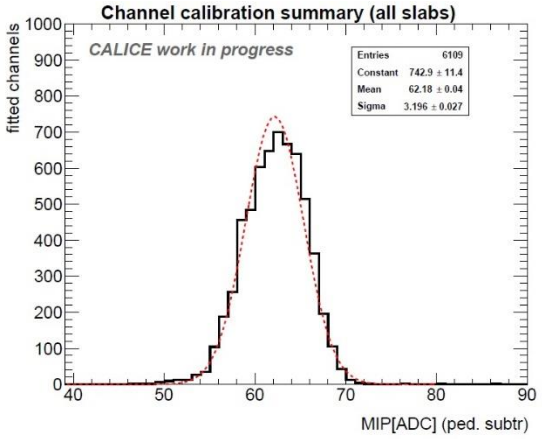
S/N ~ 20

With a large dynamic and a large number of channels, it is important to have a good S/N (in order not to read noise at large, saturating the DAQ)

Test Beam in DESY -2017

Cut at 0.5 mip

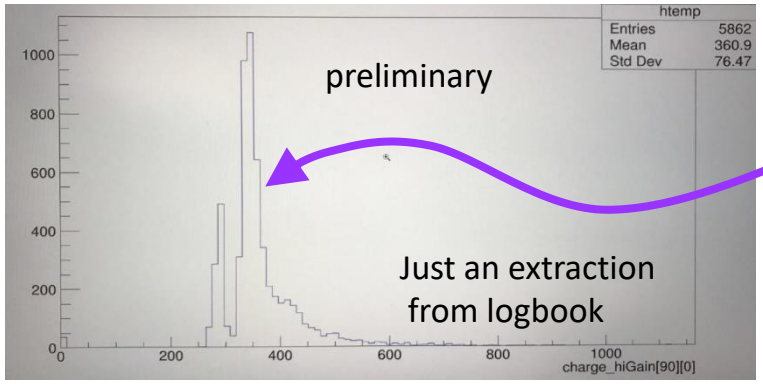




Pixels at <30 cm from DAQ FPGA

Test Beam in DESY – July 2018

Pixels at 160 cm from DAQ FPGA



Landau response to electron mip

3 remarks to conclude

High granularity **ECAL** (longitudinal segmentation and small lateral size) gives you for free (almost free … TOT in ASICS or LGAD diodes)

- BX-ID for neutral (about few ps per shower… limitation from jitter on clock distr.)
- A particle ID for charged tracks (about 5-10 ps , with TOF)

Efficient cost optimization is in progress

Optimisation with the number of Layers, the silicon thickness, a better use of the silicon ingot, the internal radius of the ECAL, etc … about 40% reduction is expected by cost experts with modest impacts on performances (G4 full simulation.. Published in JINST)

The preliminary cost estimate is NOW at the level of 90% of CMS-ECAL

ECAL

Thermal dissipation

level of granularity can be afforded without powerpulsing (like at ILC) ?

- For physics, the smaller is the best (it continue to improve largely even for S_{Pixel}<<Rm)
  BUT for the electronics cost and cooling , … there is some limits

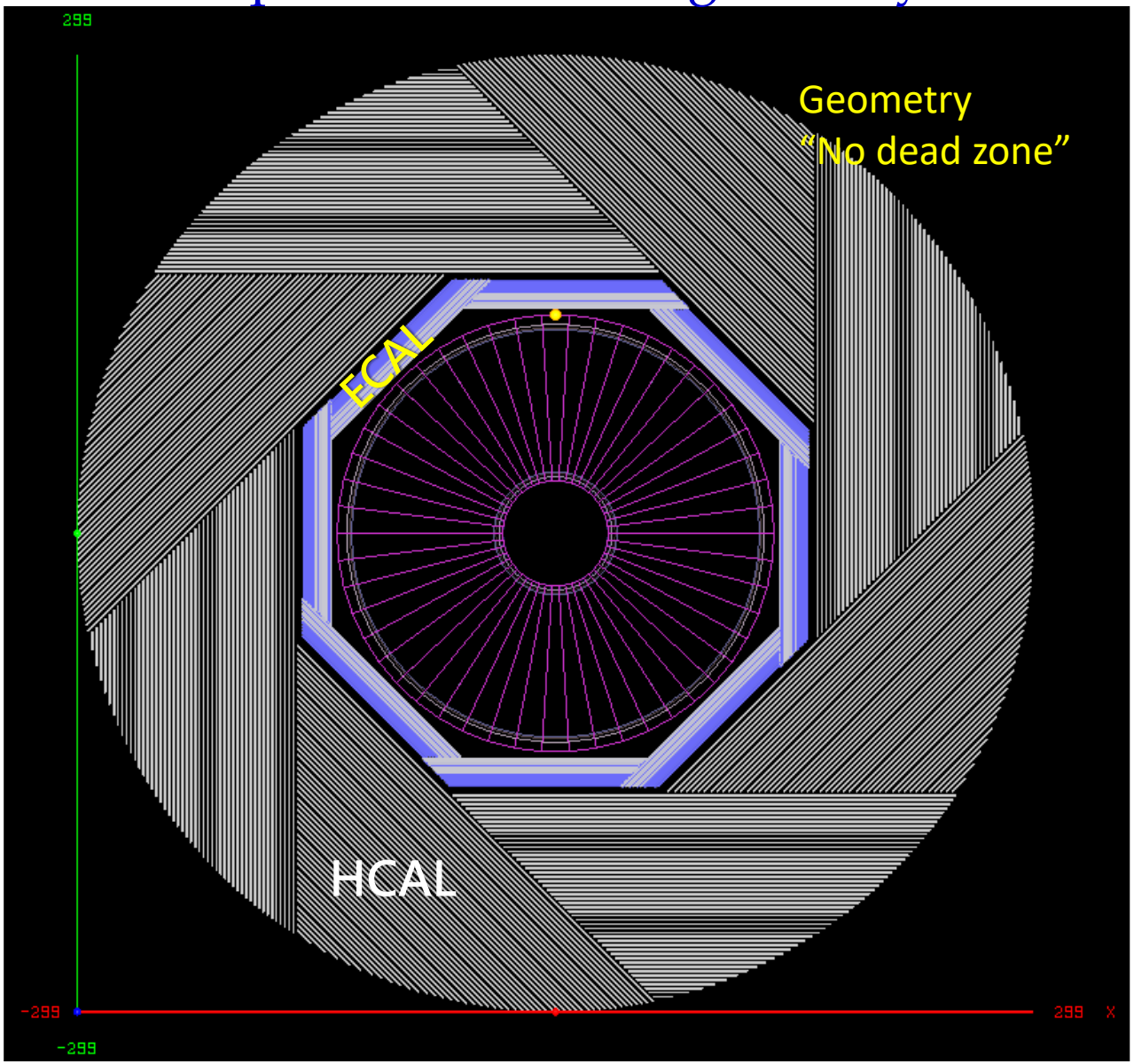
- Readout every 25 ns; no power pulsing
  readout frequency versus ILC x **14** (350 ns to 25 ns)
  conso/cell = 2.8 mW (Analogic part SKIROC2 without PP) +
  2,1 mW (=0,15 x**14** for digital part with readout every 25ns)

  = 5mW …. Propose to use 10 mW/channel (including a safety factor of 2)

- From CMS upgrade project-**HGCAL** , active cooling system can be stabilized in temperature for about 100W/layer, with fluid running in tube inside cooper plate (Rm not so good than ILC… but)

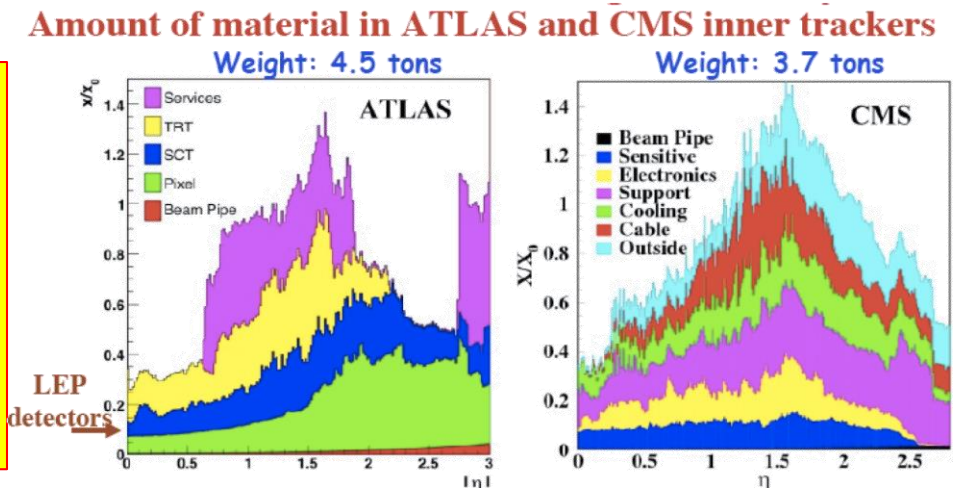
Taking into account the chosen layer size (= 150x20 cm²) and the 100W,
The cooling can afford pixel size of about 0.6x0.6 cm² !!! We have it

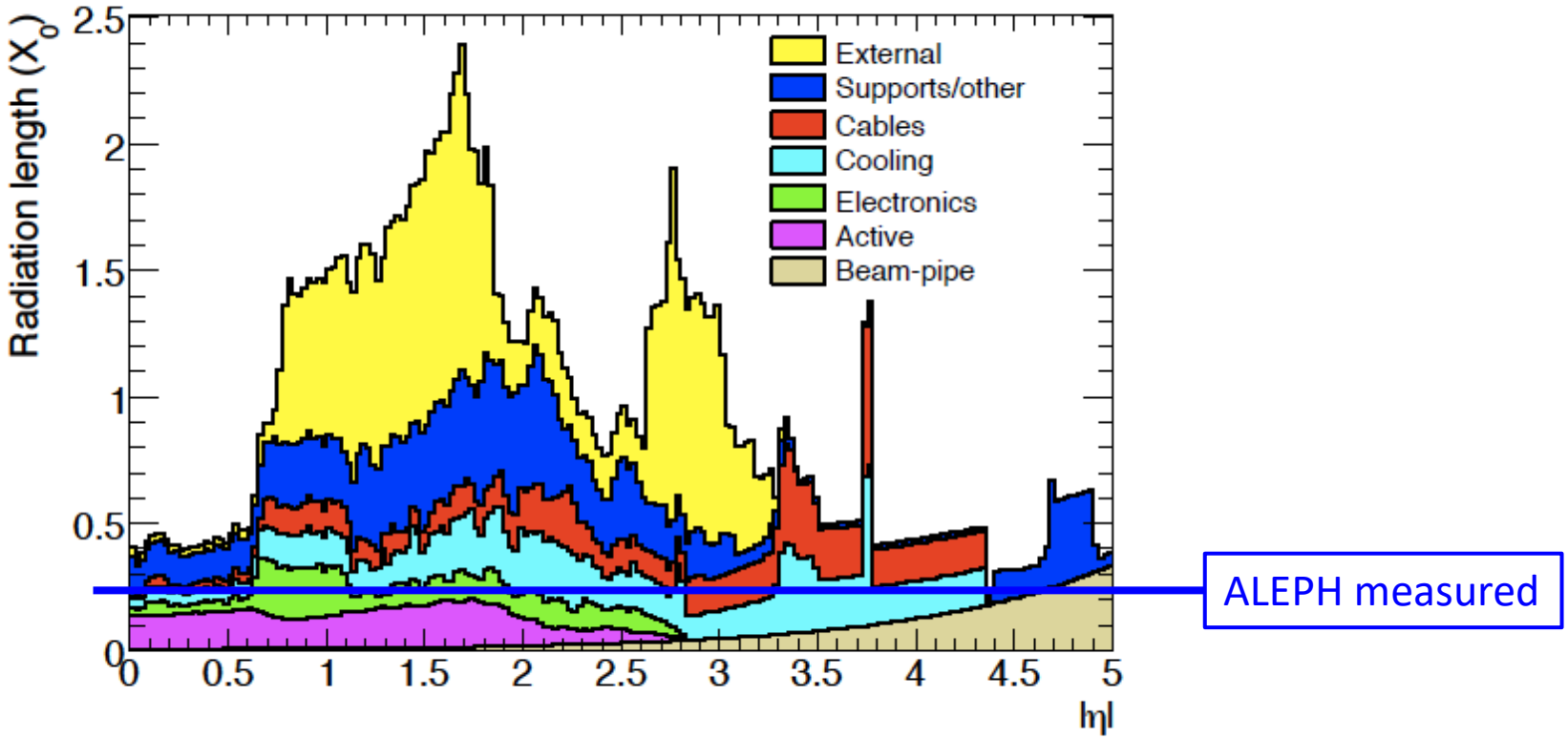
A possible detector geometry



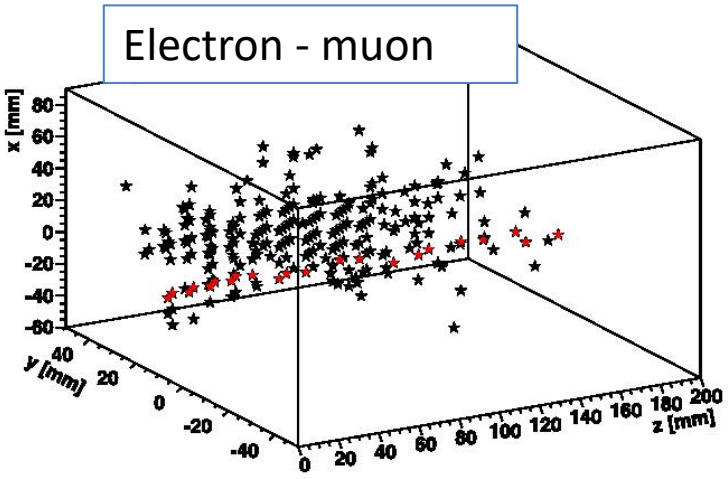
Please don't forget !!

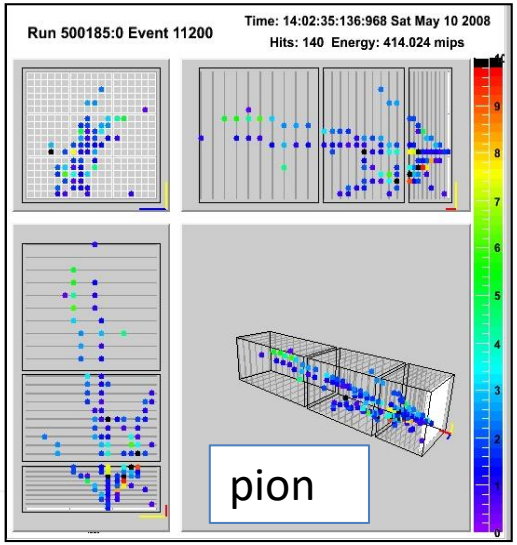
Optimising for a fantastic Vertex and Tracker … and Forgetting the calorimeters

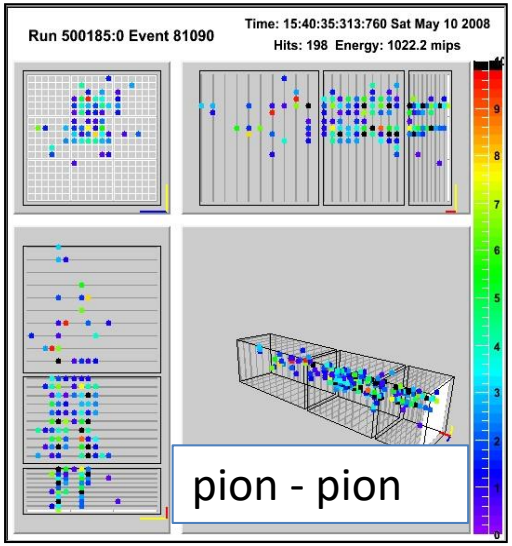


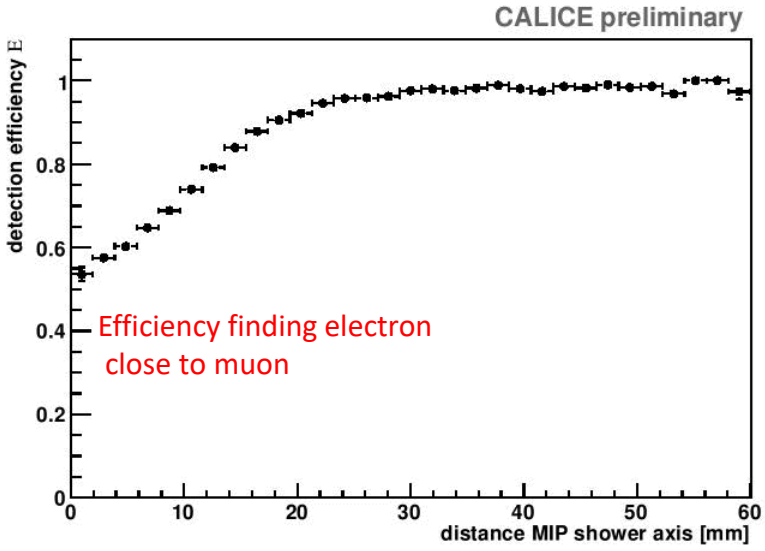


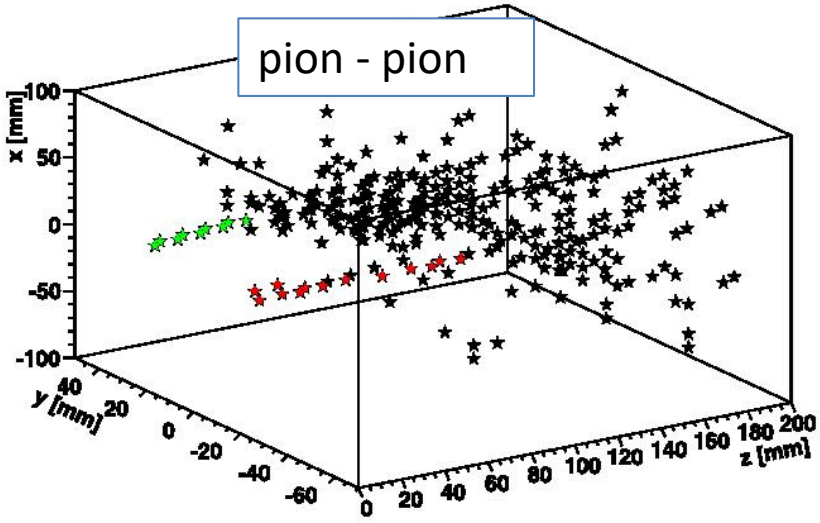
The tests of the camera



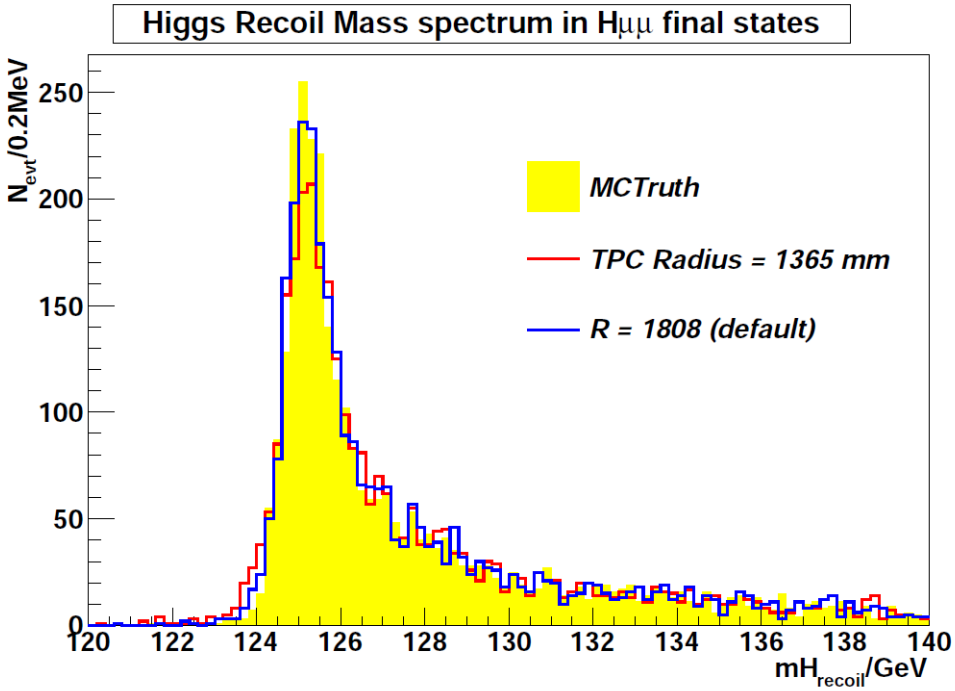


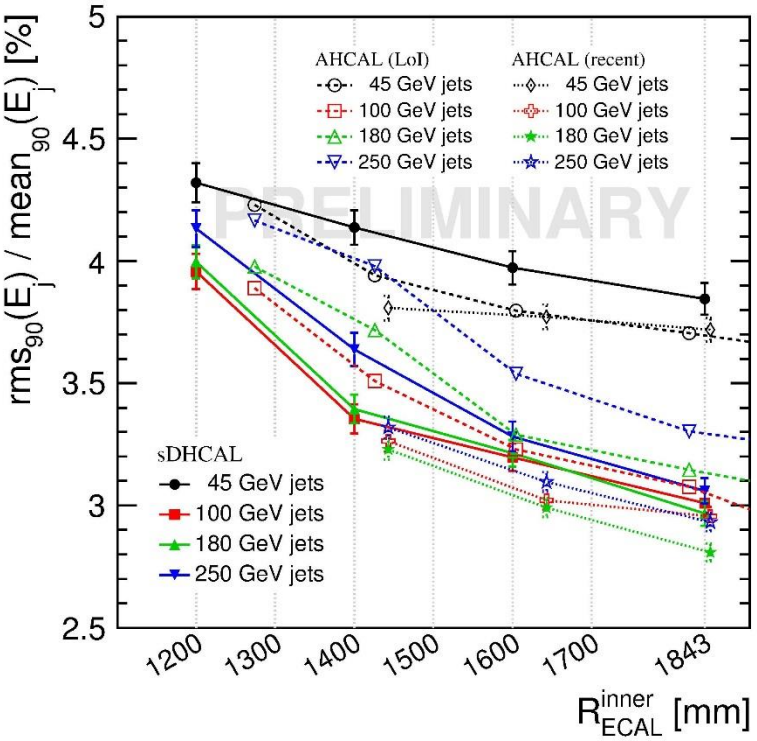


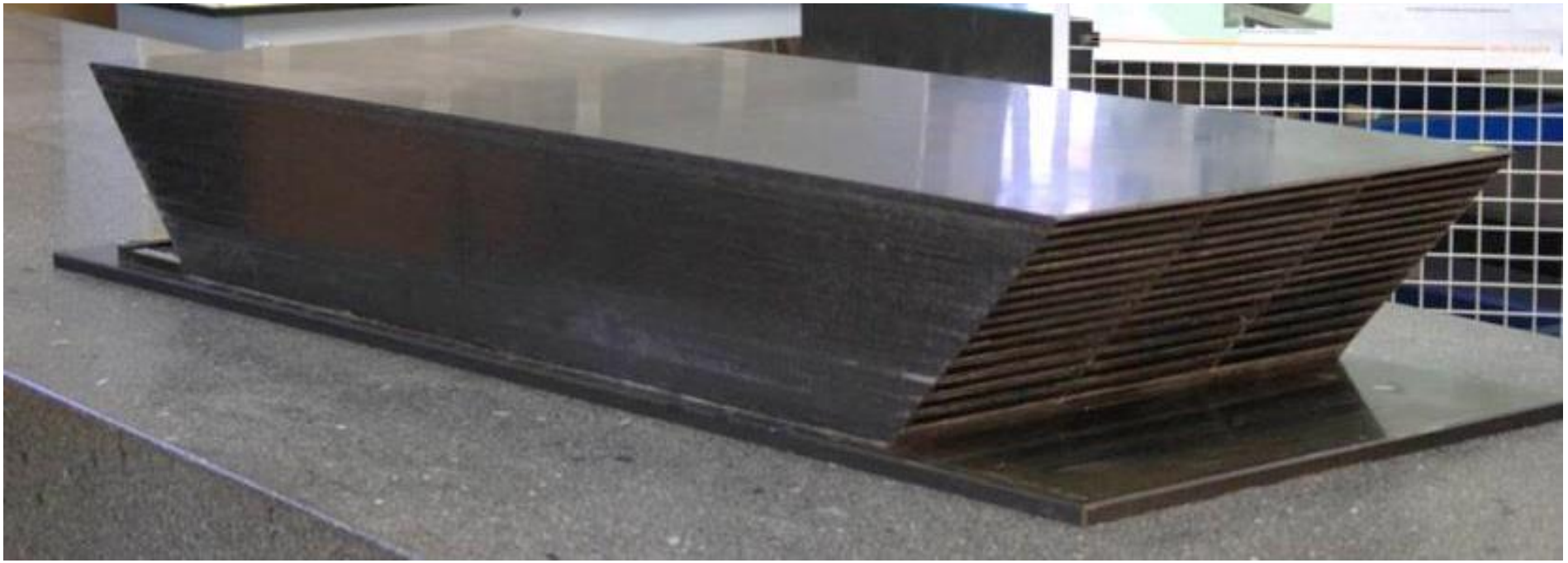


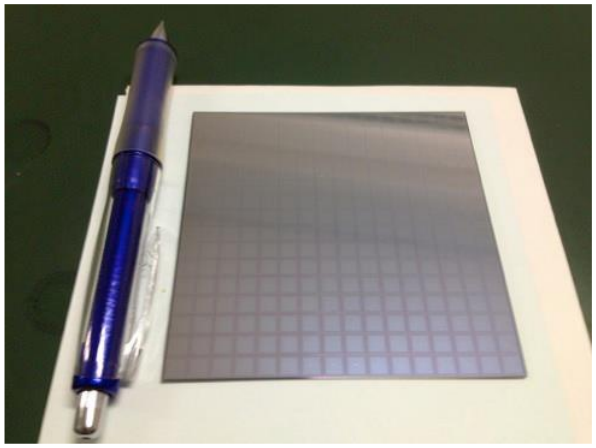


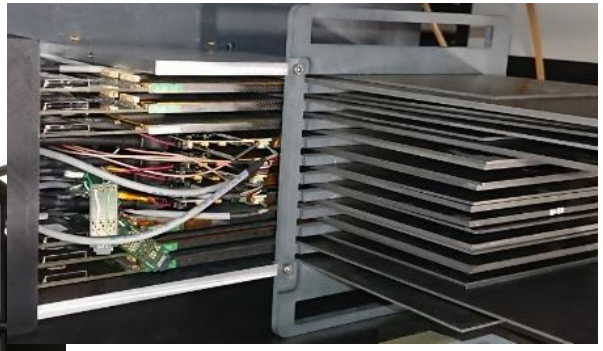
Quantitative test has been published by CALICE (test of PANDORA PFA with TB data)


Higgs Recoil Mass spectrum in Hμμ final states
N_evt/0.2MeV
MCTruth
TPC Radius = 1365 mm
R = 1808 (default)
mH_recoil/GeV

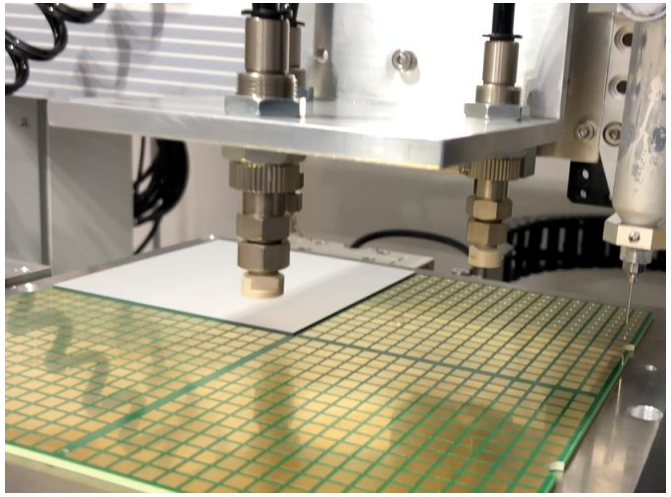

rms90(Ej) / mean90(Ej) [%]
AHCAL (LoI)
45 GeV jets
100 GeV jets
180 GeV jets
250 GeV jets
AHCAL (recent)
45 GeV jets
100 GeV jets
180 GeV jets
250 GeV jets
PRELIMINARY
sDHCAL
45 GeV jets
100 GeV jets
180 GeV jets
250 GeV jets
R^inner_ECAL [mm]







Testing new slabs
in CERN SPS



Intensive study ongoing
mainly on electronics
of large scale
Sensor and readout
concept mature enough

Long-life needed: reliability is crucial

ULTRAGRANULAR CALORIMETER

Requirements

a) Calibration of O(100) millions channels and signal stability (small syst. uncert. needs same response for all collisions)

b) Capability to make zero suppress "in-situ" (we don't want to read empty pixel)

c) Keep S/N ≥ 8-10 at MIP level and coherent noise under control (limitation of the DAQ and it is not interesting to store noisy pixels)

d) Multiplexing for the quantity of signal line out (we don't want to have 100M cables)

e) Power and thermal management due to large number of channels (we don't want to burn our electronics readout)

f) KEEP the COST UNDER CONTROL (we want an affordable cost)

One set of answers

a) Choose stable device (silicon) or control & monitor the signal stability (Scint. or Micromegas)

b) ADC& digital memory in readout chip, close to active layer. Read memories continuously WITH S/N > 8

c) i.e. Silicon PIN diodes …. AC/DC coupling , ground loop … (see later)

d) Large number of Channels/VFE ASIC… (KPIX, SKIROC), but only few readout line

e) reduced the number of channels → the power to dissipate (see later)

f) Reduce the overall surface or use lower cost active device (Micromegas, scintillator)

BUT warning versus point a) and c) . 10 years contacts with producers, defining wafers design which reduce the cost