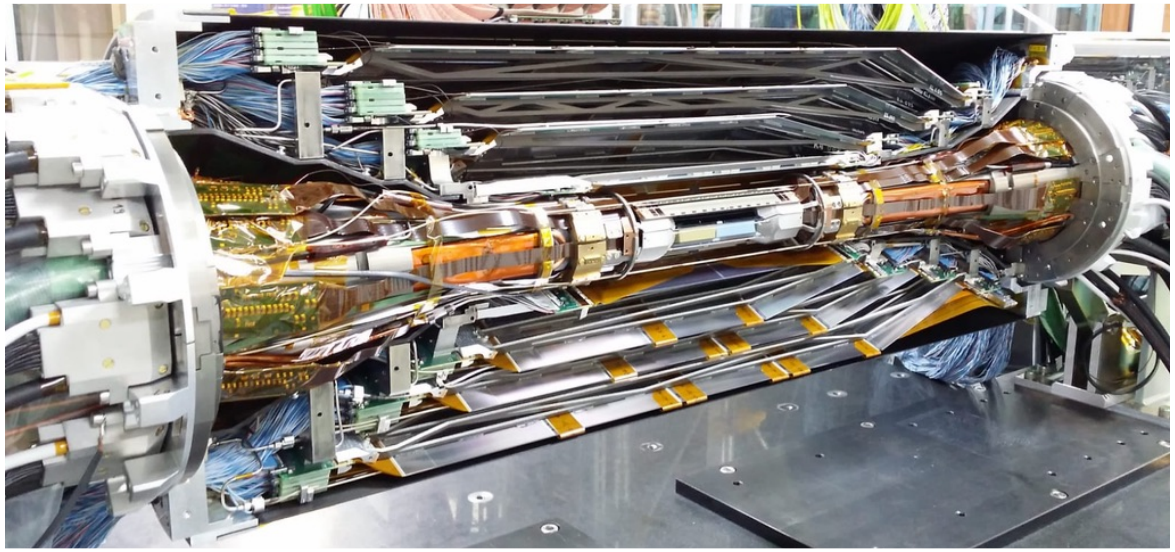


DEPFET active pixel detectors with integrated support and cooling

CEPC workshop, IHEP Beijing, November 2018

Marcel Vos, IFIC, CSIC/UV, Valencia, Spain

Acknowledging contributions and inputs from
L. Andricek, P. Gomis, C. Koffmane, C. Marinas, C. Niebuhr and B. Schwenker, M.A. Villarejo

IFIC INSTITUT DE FÍSICA CORPUSCULAR
CSIC CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS
VNIVERSITAT DE VALÈNCIA
EXCELENCIA SEVERO OCHOA
AIDA 2020

Outline

- DEPFET active pixels: introduction
- Belle II VXD production and installation
- A micro-channel cooling solution for CEPC

marcel.vos@ific.uv.es

Introduction: next-generation pixel detectors

Precision vertexing requires highly integrated devices

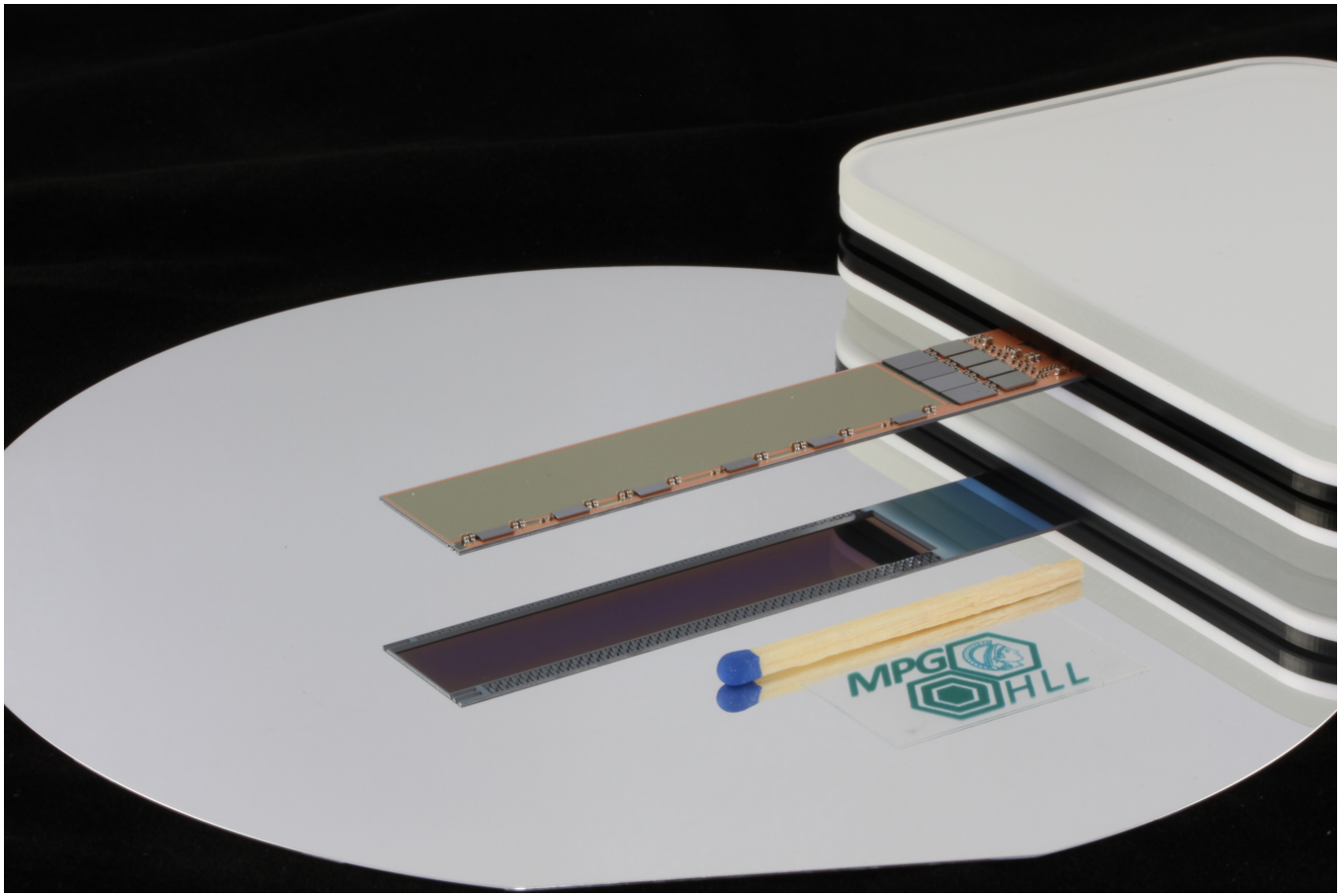
Detector-grade fully depleted silicon sensor

In-pixel FET amplifies signal: thin (50 μm) sensor suffices

read-out electronics:
on the silicon

Power & signal lines:
on the silicon

Support structure:
= the silicon



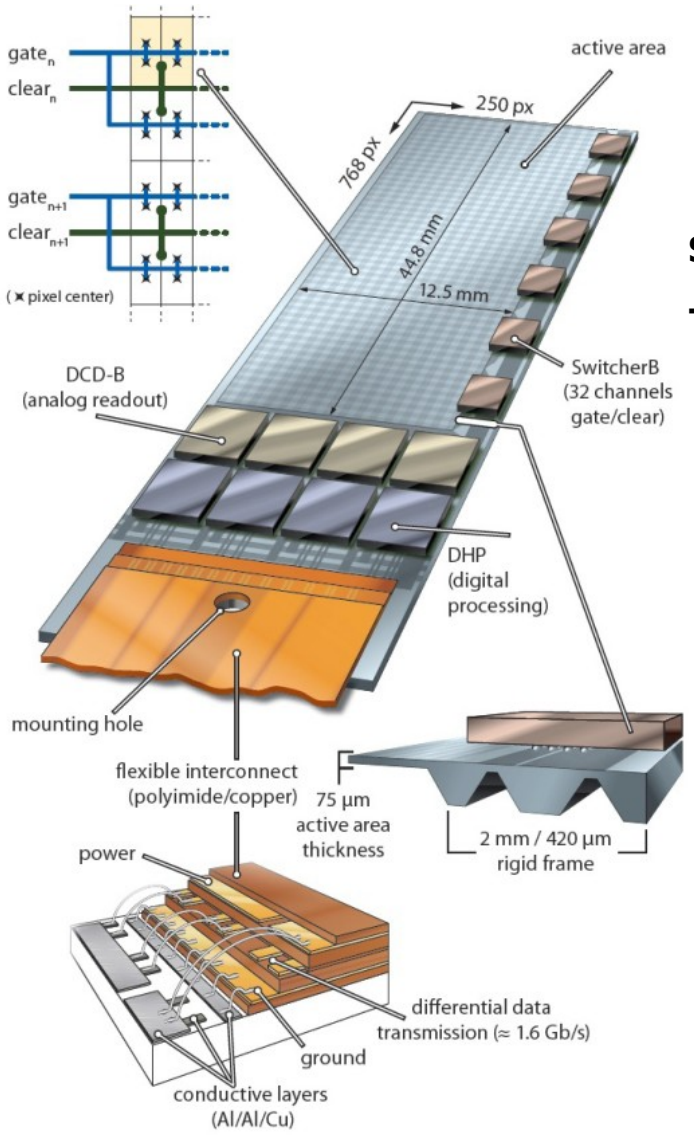
DEPFET PXD all-silicon module

DCDB (Drain Current Digitizer)

Analog front-end & ADC

DHP (Data Handling Processor)

First data compression



SwitcherB

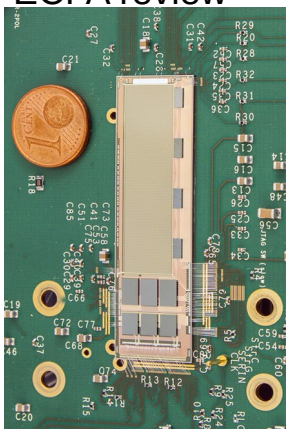
-Row Control

One-slide DEPFET history

"Early days"

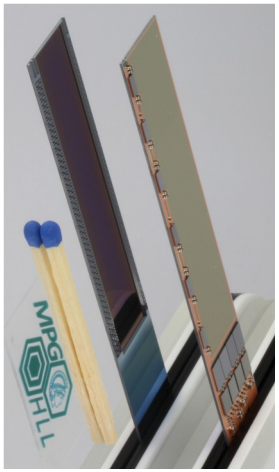
2007-2011
prototypes
O(10^4) pixels

"The most complex piece of silicon in the world", ECFA review



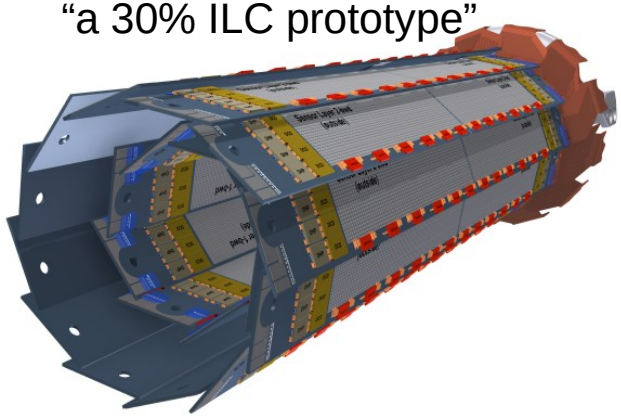
January 2014,
large-scale ladder
DESY TB

"The real thing!"



October 2015,
operational Belle2
ladder

The Belle II VXD
"a 30% ILC prototype"



DEPFET
Active Pixel Detector

Now: installation
Belle II VXD

Belle III PXD

PXD 2020

Physics

Proof-of-principle — Complete demonstrator — A real detector

2002.... 2007.... 2013 2014 2015 2016 2018

LC-specific — ILC approval

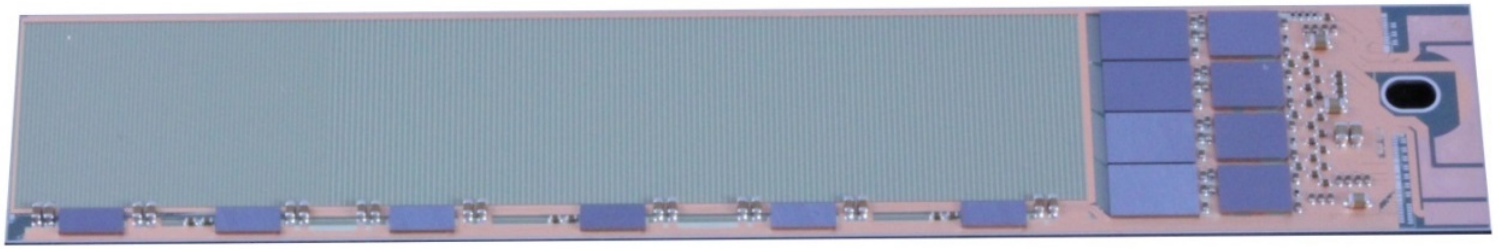
1.5 mm resolution

DEPFET for ILC, IEEE TNS 60

ECFA review:
http://ific.uv.es/~vos/ECFA_DEPFET.pdf

ASICs: production for Belle II

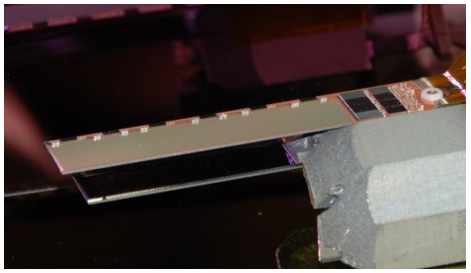
- Drain Current Digitizer DCD (front-end, ADC)
  - **Final chip DCDB4.2, “DCD”**
- Data Handling Processor DHP (data reduction, CMC, off-module driver ..)
  - **Final chip DHPT1.2b, “DHP”**
- Switcher (HV chip for row addressing and Clear)
  - **Final chip SwitcherBv2.1, “SWB”**



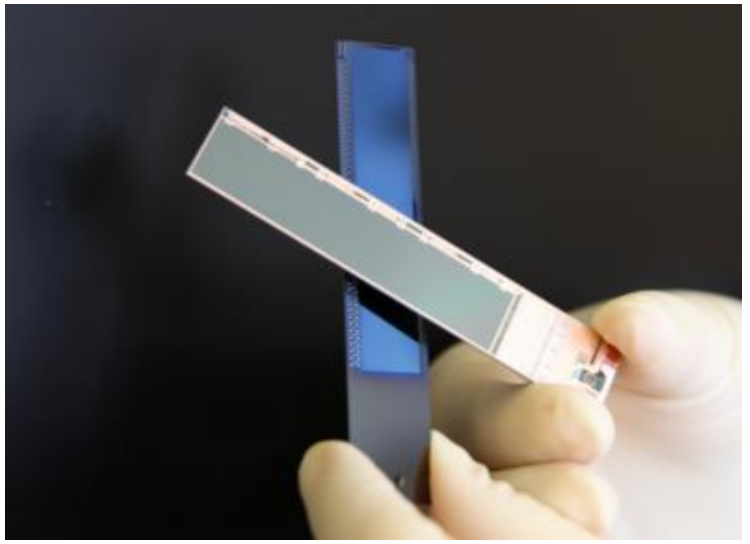
Status at end of 2017: all components ready for module and ladder assembly

PXD9 sensor production

A total of 29 wafers finished



- PXD9-6: 3 wafers pilot run
  - First module assembly, DESY test, gated mode tests …..
- PXD9-7: 4 wafers pre-production
  - Lessons from pilot run implemented (improved periphery routing)
  - Modules for Phase 2 ….



- Main production
  - PXD9-8: 9 wafers
  - PXD9-9: 6 wafers
  - PXD9-10: 7 wafers
- Wafer level tests throughout production cycle
  - after 1st metal → global characteristics, IV
  - after 2nd metal → pixel yield
  - after 3rd metal → periphery

Sensor production yield

Combined	PXD9-6 (3 wafers)			PXD9-7 (4 wafers)				PXD9-8 (9 wafers)								
Wafer arrangement	W30	W35	W36	W31	W37	W38	W40	W32	W33	W41	W42	W43	W44	W45	W46	W47
Inner Forward	G58.4	G98.4	G99	G98.9	G98.4	B98.8	G100	G100	B98.4	G99.5	G99.3	G100	G99	M99.5	G99.5	G99.5
Outer Forward 1	G99.9	G98.4	G99	G98.4	G98.1	B98.4	G99.5	G99.5	G100	G99.5	M100	G100	G100	G99.5	G100	G98.1
Outer Forward 2	G99.5	M99	G99.5	G99	B98.4	B98.4	M99.5	G100	G100	B99.5	M100	B99.5	G100	G100	G99.9	B98.4
Outer Backward 1	G97.5	G88	G98.4	G99.4	G98.4	G97.9	M100	B99	G99.5	B98.4	G99.5	B38.4	G99	B99.5	G99.5	B98.4
Outer Backward 2	G98.6	G96.9	G98.6	G99.5	G99.5	B98.1	G99.9	G100	B99	B98.4	G100	M99.9	G100	G100	G100	B98.4
Inner Backward	G97.9	M100	G99.5	G100	G98.4	G98.4	G100	G100	B98.4	G100	G100	G100	G100	G100	G99.5	G99.5

Combined	PXD9-9 (6 wafers)						PXD9-10 (6 wafers)						
Wafer arrangement	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13
Inner Forward	B95	G99	G99	G99	G99.3	G98.8	B17.9	G99.5	G99.4	G99	G99.3	B100	G99.5
Outer Forward 1	G99.6	G99	B99.2	G99.3	G99.5	G98.9	B37.9	B99	G99	G98.4	G99	G99	G97.9
Outer Forward 2	B98.2	B99	G99.4	B98	G99.3	G97.9	B37.9	G99.5	G99.5	G98.4	G99	M98.9	B98.2
Outer Backward 1	G100	B98.9	G99	M99	G99	G99	B37.9	G99	G99	G98.4	B95.5	G99.5	B98.2
Outer Backward 2	B99	B98.9	B99.4	B99.5	B98.9	B99	B37.9	G99	M99.5	B97.6	B98.8	G99	G98.4
Inner Backward	G94.4	M99	G100	M99.5	G98.4	M99.5	B17.9	B99.5	G100	B99	M98.7	B99	G99

	REQ	G99	G98	G95	M99	M98	M95
Inner Forward	8	17	3	0	1	0	0
Outer Forward	12	26	6	2	3	1	0
Outer Backward	12	22	3	1	4	0	0
Inner Backward	8	13	3	0	3	1	0

G: good
M:Medium
B:Bad
The number behind gives the minimal percentage of live pixels on the sensor

-: same table as after 2nd metal testing

-: 100% yield for thinning and copper process

module and ladder assembly – in a nutshell

1. Flip Chip of ASICs (~240°C)

- DHP/DCD/SWB bumping at TSMC/Europractice/IZM

2. SMD placement (~200°C)

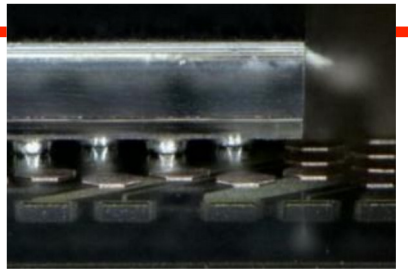
- Passive components at HLL Munich
- **Probe-card test**

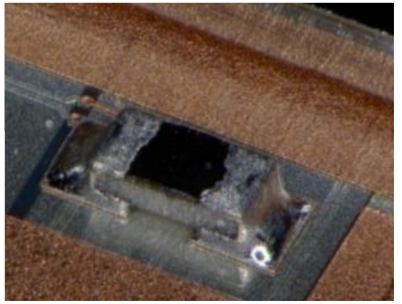
3. Kapton (~170°C) & wire bonding

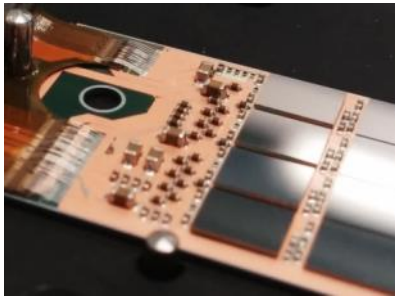
- Kapton attached at MPP Munich
- **Full module characterization**

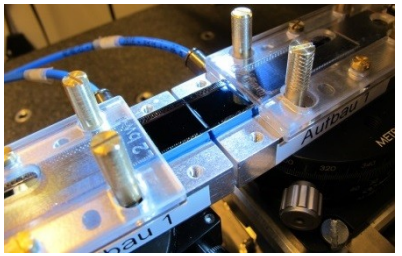
4. ladder gluing (RT)

- Two modules form one ladder, at MPP Munich
- **ladder tests**





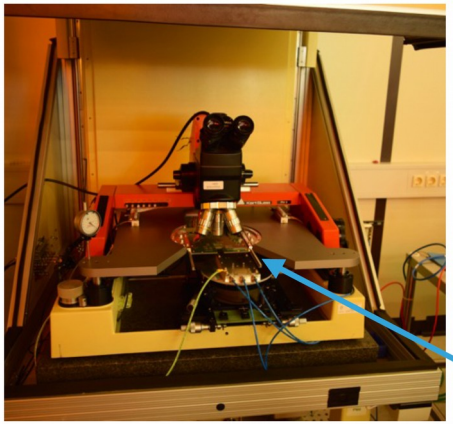




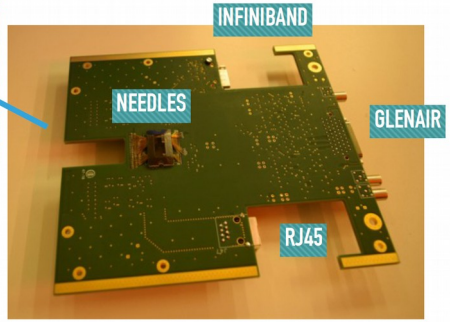
Intermediate module tests

PROBE CARD: ACTUAL HARDWARE

6



- Modules are placed with their base jig on the cooling jig and secured with screws and vacuum under the probe card.
- Through the optical microscope we can align the needles with the module and calibrate at what point the touchdown is performed.



- With the help of the micrometer on the left, we apply the desired overtravel (~40 microns).

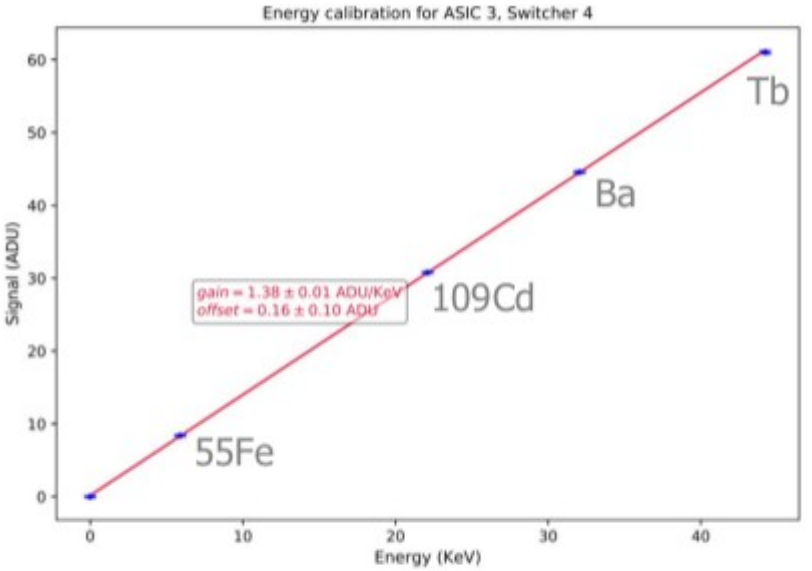
P. Gomis (Pablo.Gomis@ific.uv.es) @ 21st International Workshop on DEPFET detectors and applications - 29/05/2017

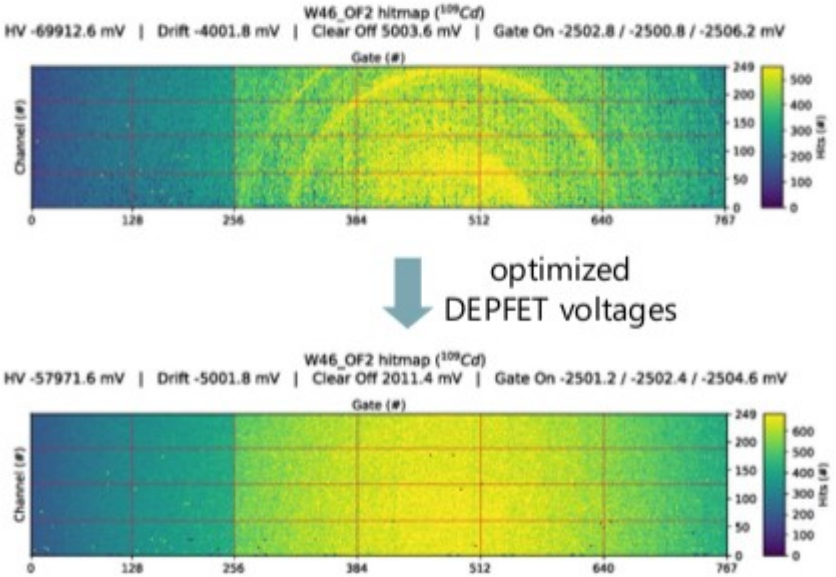
	standard tests			Optional tests			
	Power	JTAG	Boundary	HSL	Analog power	Matrix	Overall
W01_IB							
W02_IB							
W46_IB							
W47_IB							
W44_IF							
W45_IF							
W46_IF							
W47_IF							
W03_IB							
W43_IB							
W44_IB							
W45_IB							
W02_IF							
W03_IF							
W05_IF							
W43_IF							
W09_IB							
W32_IB							
W41_IB							
W42_IB							
W08_IF							
W32_IF							
W41_IF							
W42_IF							

Final module tests

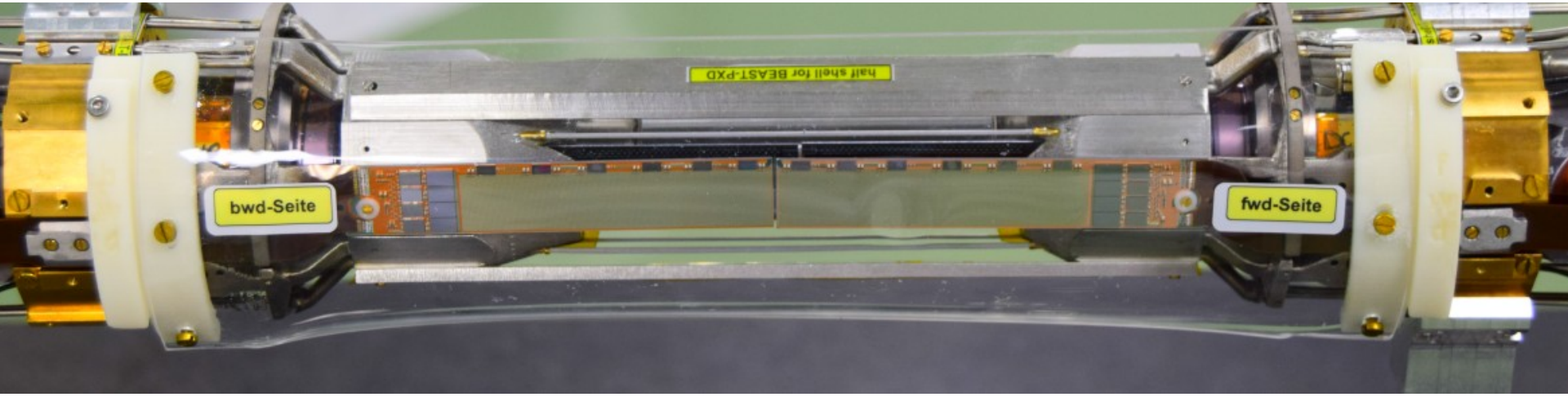
Final module tests
71 modules tested at several sites
- automated standard procedure

Confirm all aspects of operation
→ optimized parameters
→ linear response of the ADC
→ high-speed links of the DHP
→ study signal of radioactive sources
(vs. DEPFET voltages: drift, HV, Clear-Off)





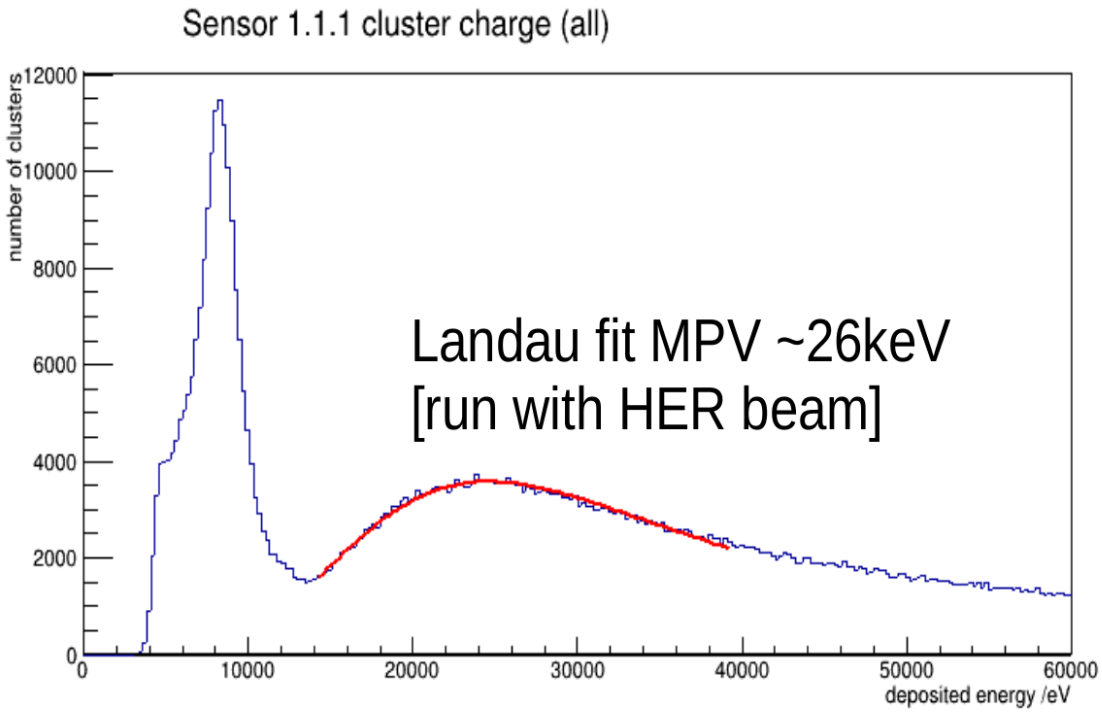
BEAST II – commissioning detector



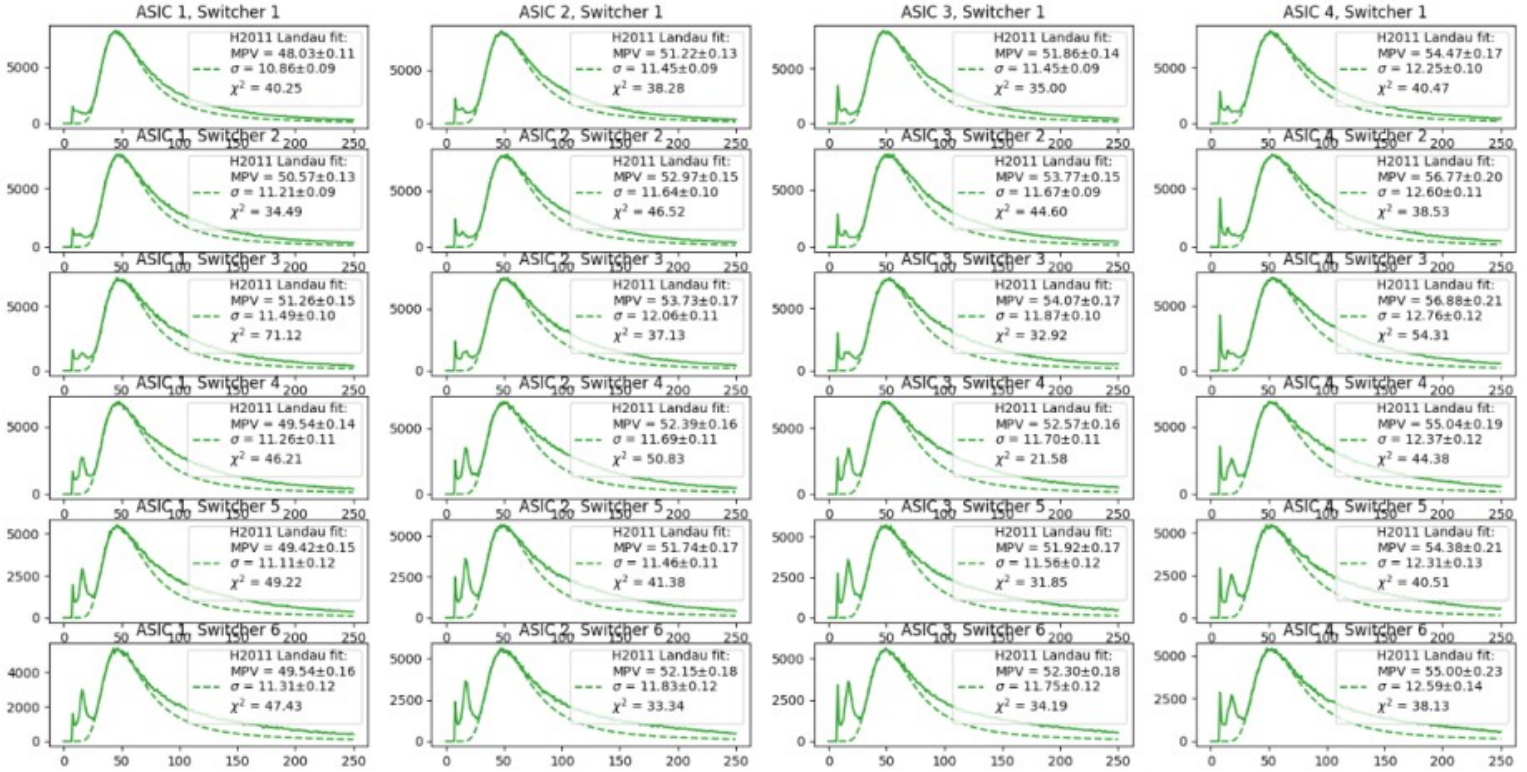
September 2017: installation of DEPFET PXD modules in Belle II commissioning detector

BEAST II

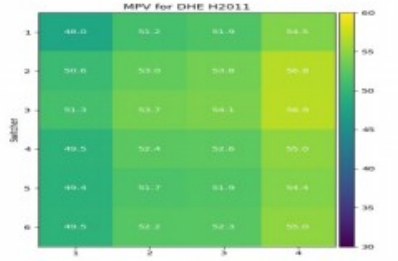
The PXD analogue cluster signal height offers excellent separation between charged particle and photon hits



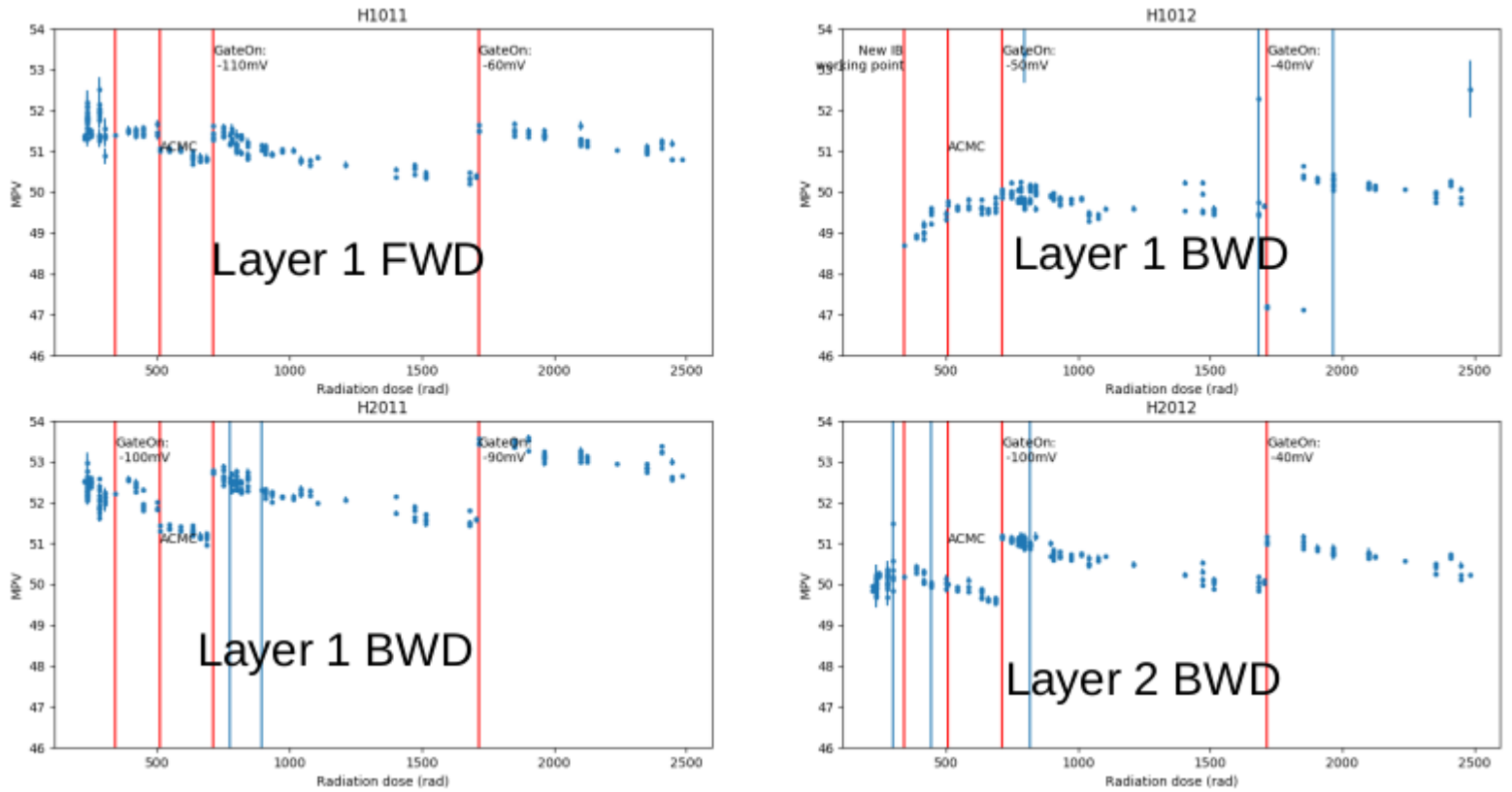
BEAST2: gain uniformity



- Layer 2 FWD sensor split in 24 regions
- All regions show clear Landau peak for charged tracks
- Fitted most probable charge varies on scale ~15% over sensor



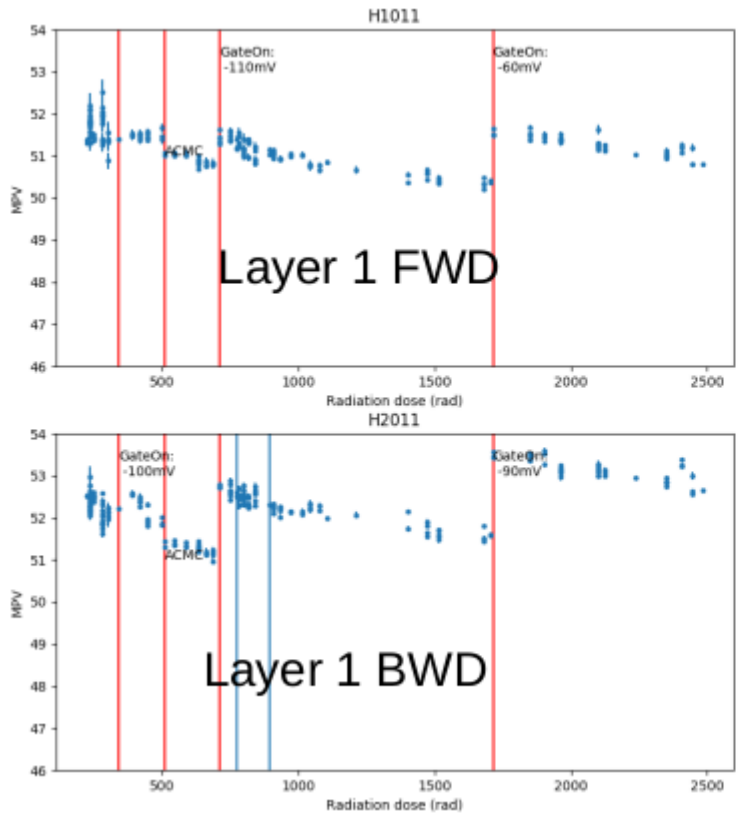
BEAST II: gain vs. dose

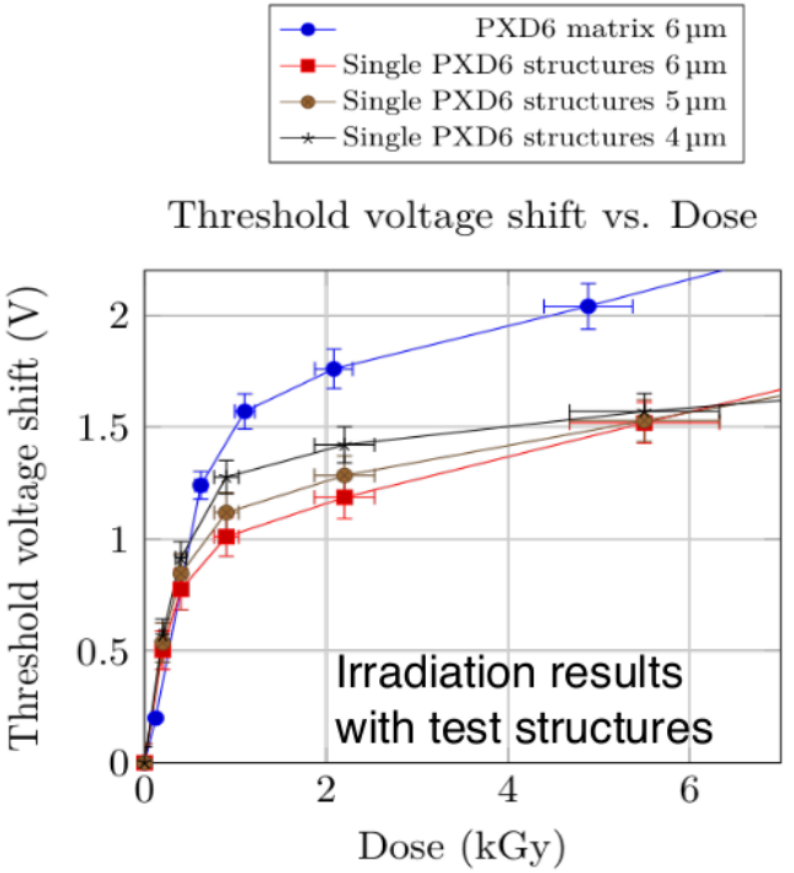


Dose from diamond sensors

- BEAST2 is subjected to significant ionizing dose during phase 2 operation
- gain varies with dose due to threshold shift of in-pixel FET
- diamond sensors indicate 5 krad, threshold shift indicates larger dose
- lost gain is recovered by adjusting Gate-On voltage

BEAST II: gain vs. dose

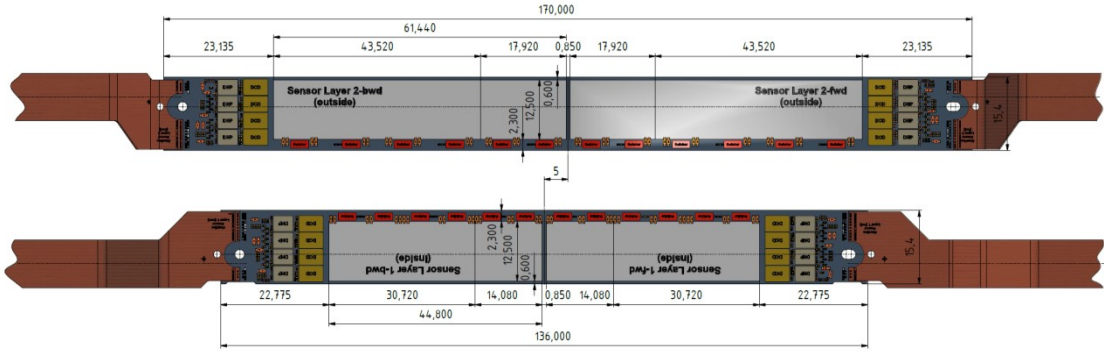




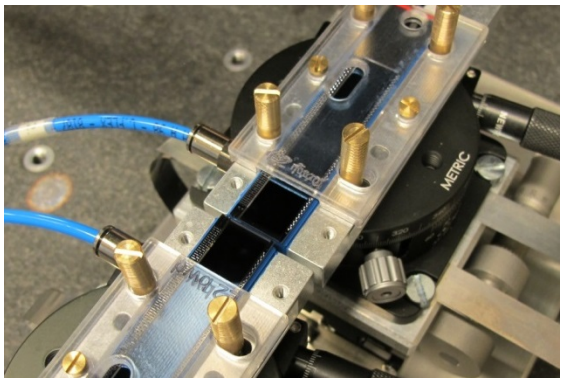
- BEAST2 is subjected to significant ionizing dose during phase 2 operation
- gain varies with dose due to threshold shift of in-pixel FET
- diamond sensors indicate 5 krad, threshold shift indicates larger dose
- lost gain is recovered by adjusting Gate-On voltage

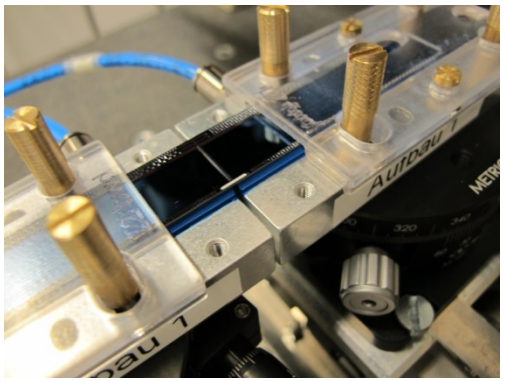
ladder assembly

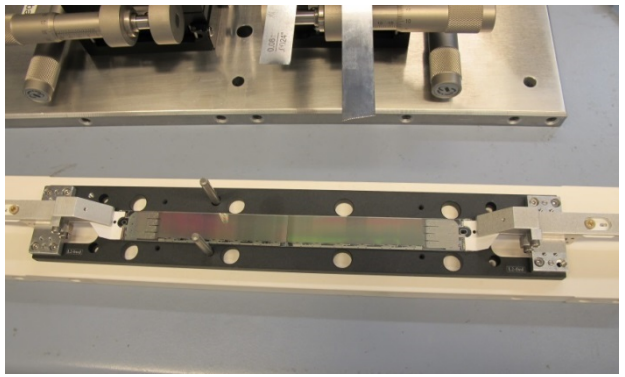
- **four module types**
  - → L1bwd, L1fwd, L2bwd, L2fwd
- **two ladder types**
  - → L1 and L2



- ladder gluing procedure tested on 9 dummy ladders (good results)
- **Many assembled ladders failed on ladder test stand**
  - → shorts due to problems with passivation/cleanliness



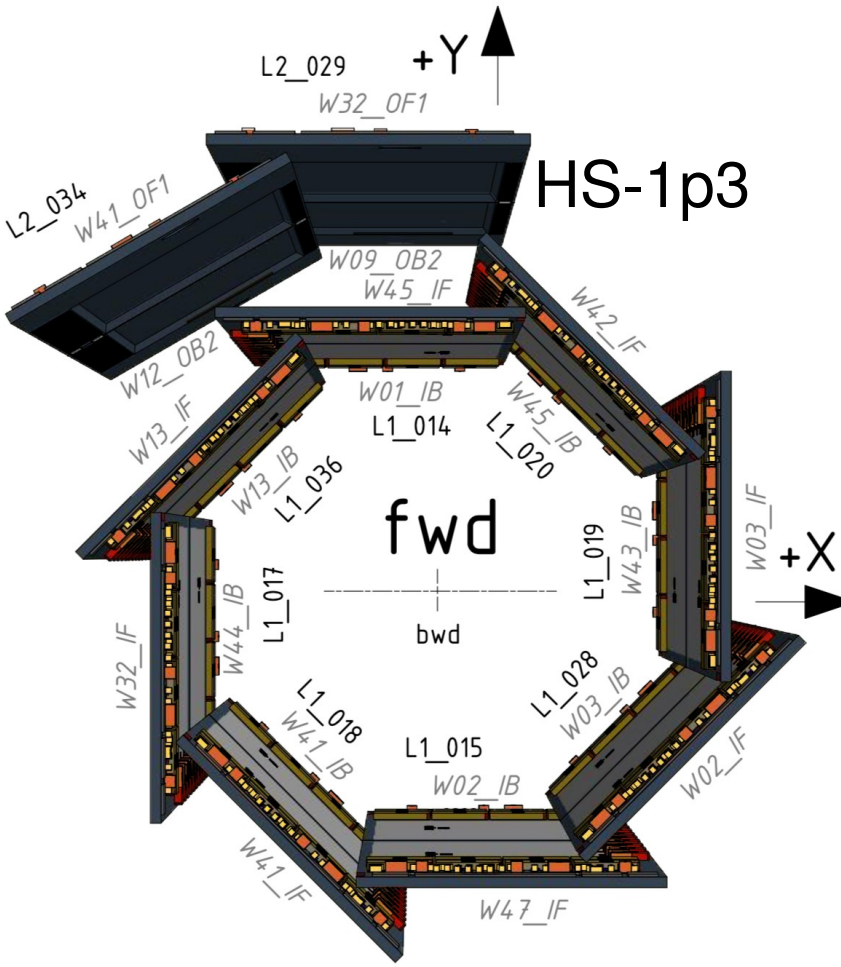




June 2018: descoping decision

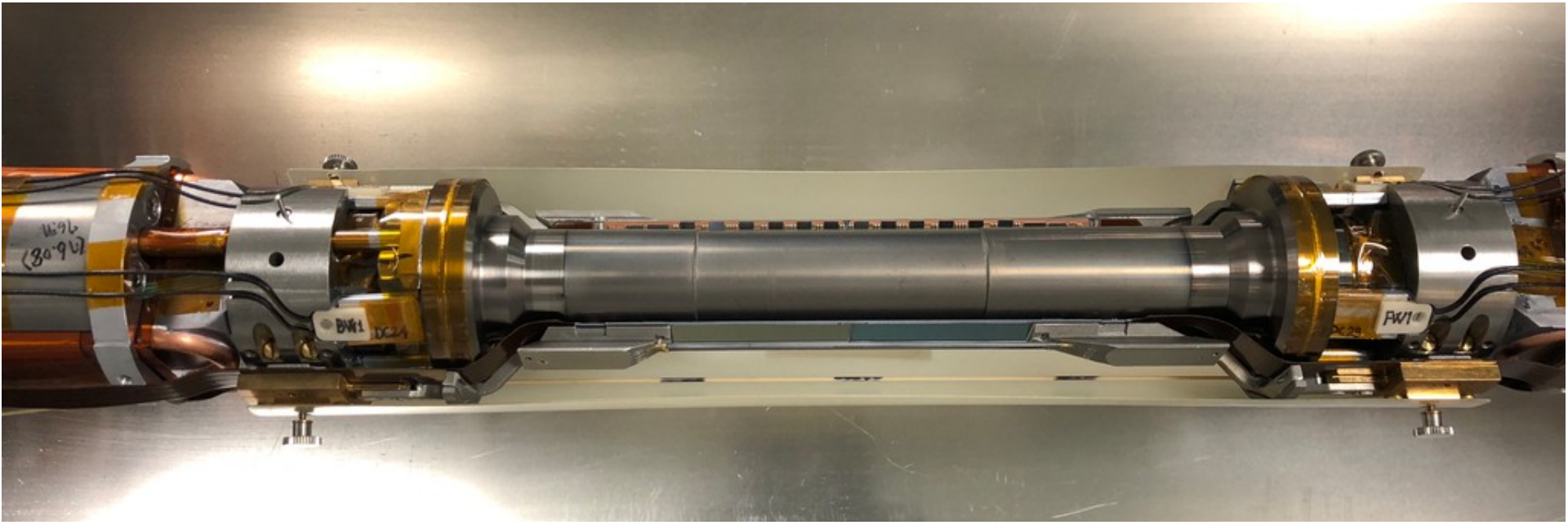
- Due to too high failure rate of ladder glueing process we decided to install a de-scoped PXD in 2018
  - complete L1: 8 ladders
  - partial L2: 2(12) ladders
- Ladder mounting on both PXD half shells
  - HS-2p3 without mylar foil (4 L1 ladders)
  - HS-1p3 with mylar foil (4 L1 + 2 L2 ladders)
- Both half shells commissioned at DESY

PXD for 2019-20

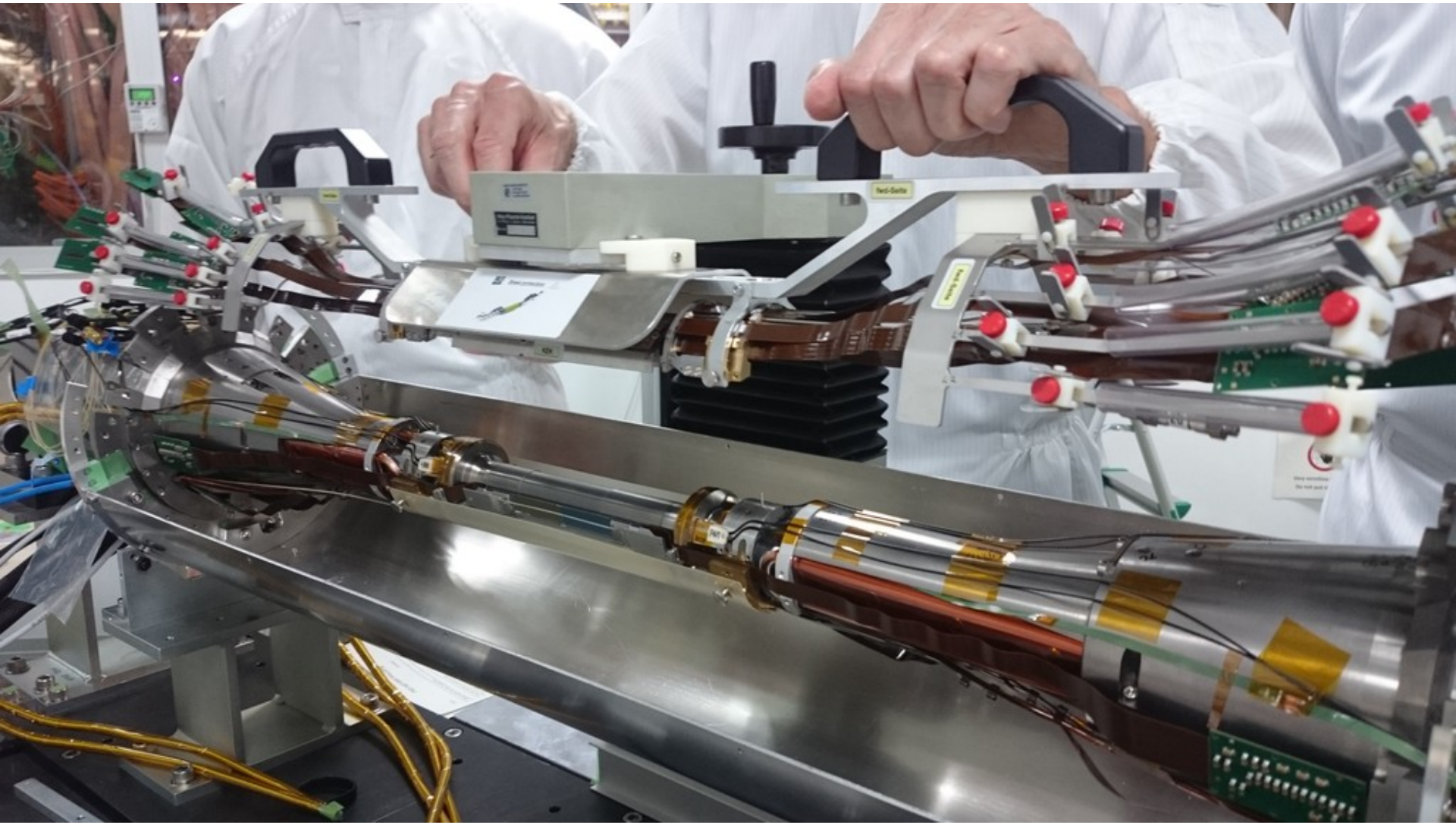


Better than business: the captain's sleeping-cabin

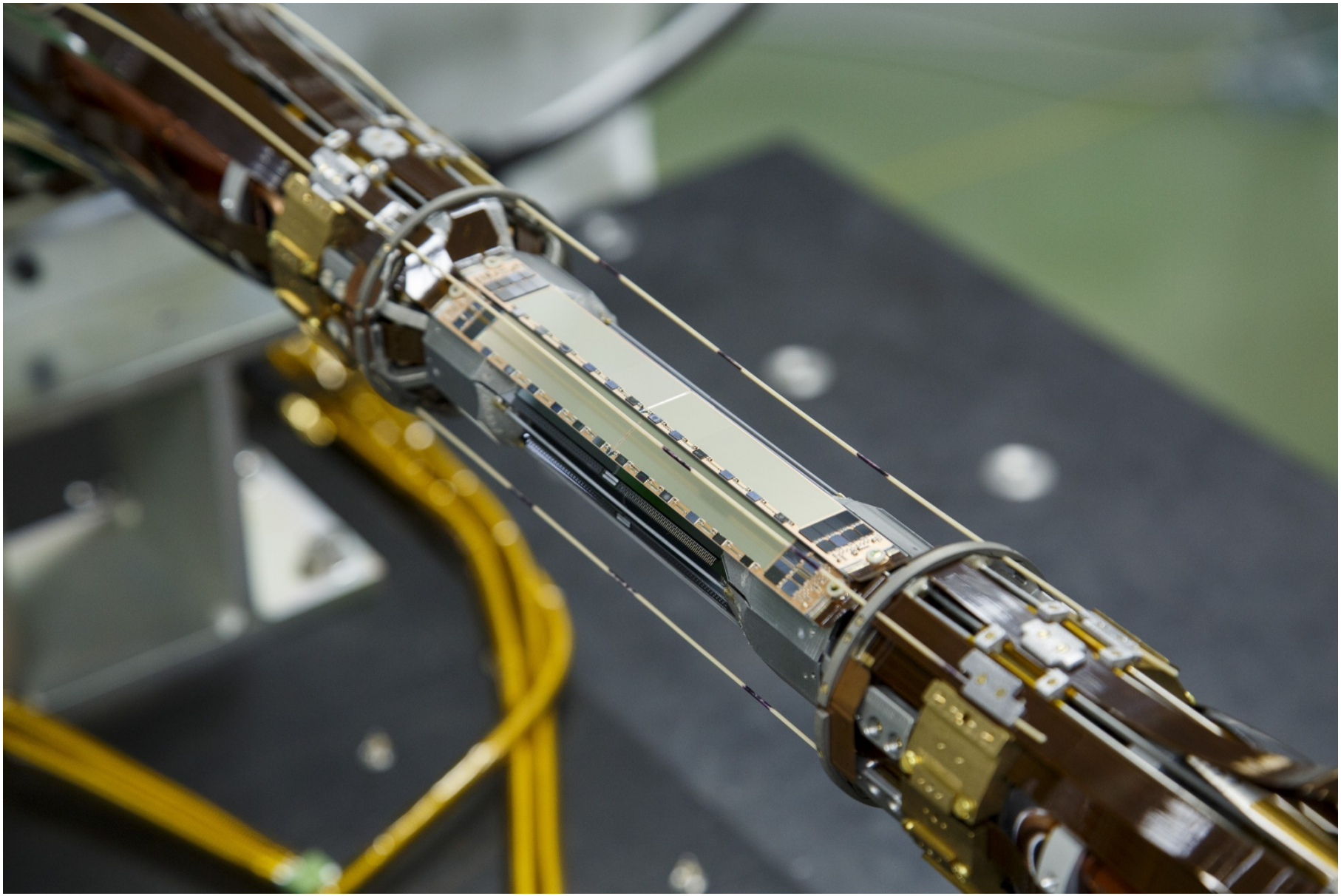
Beampipe & HS-2p3 ready to receive HS-1p3



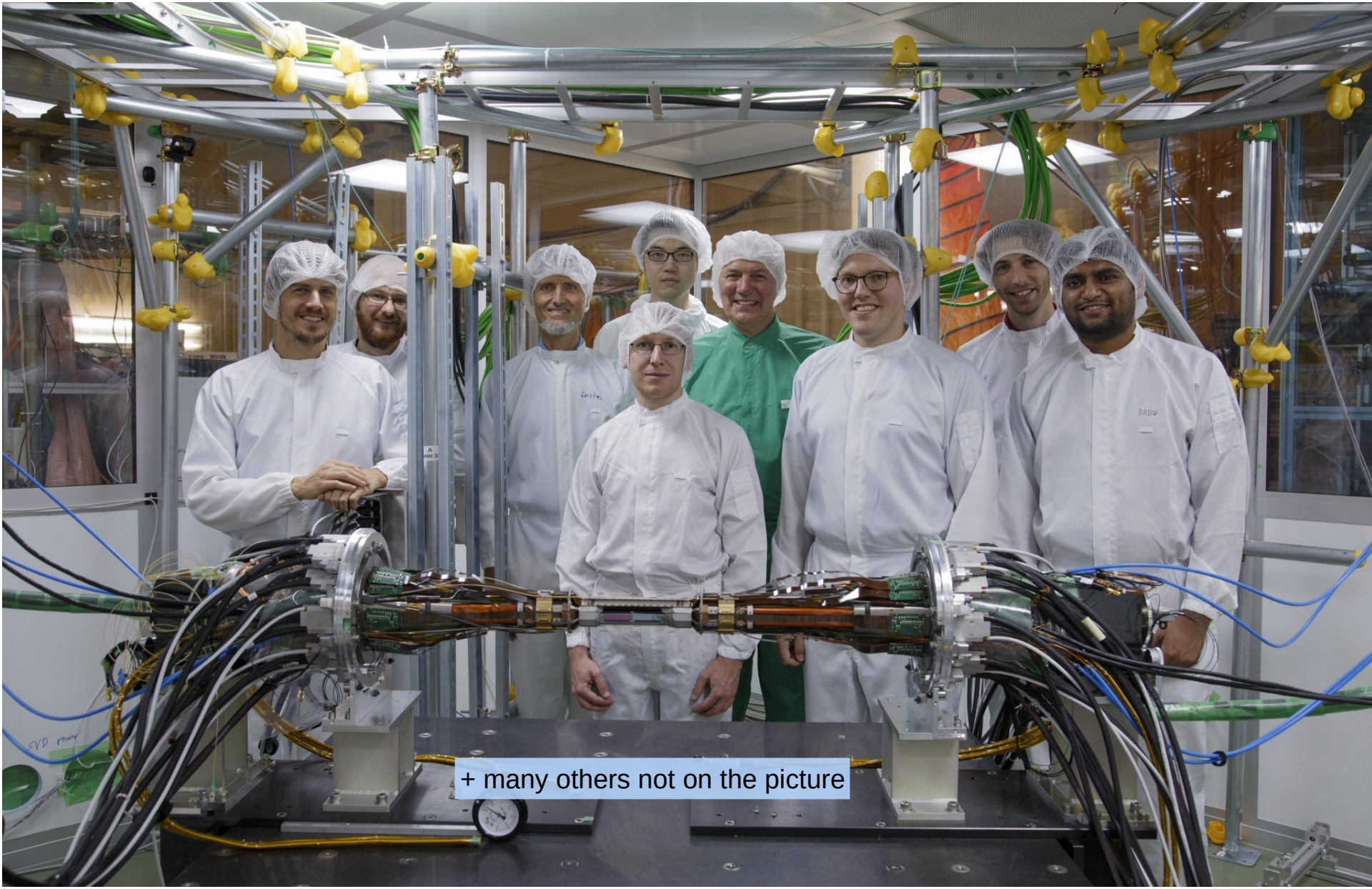
Mounting of HS-1p3 on Beampipe



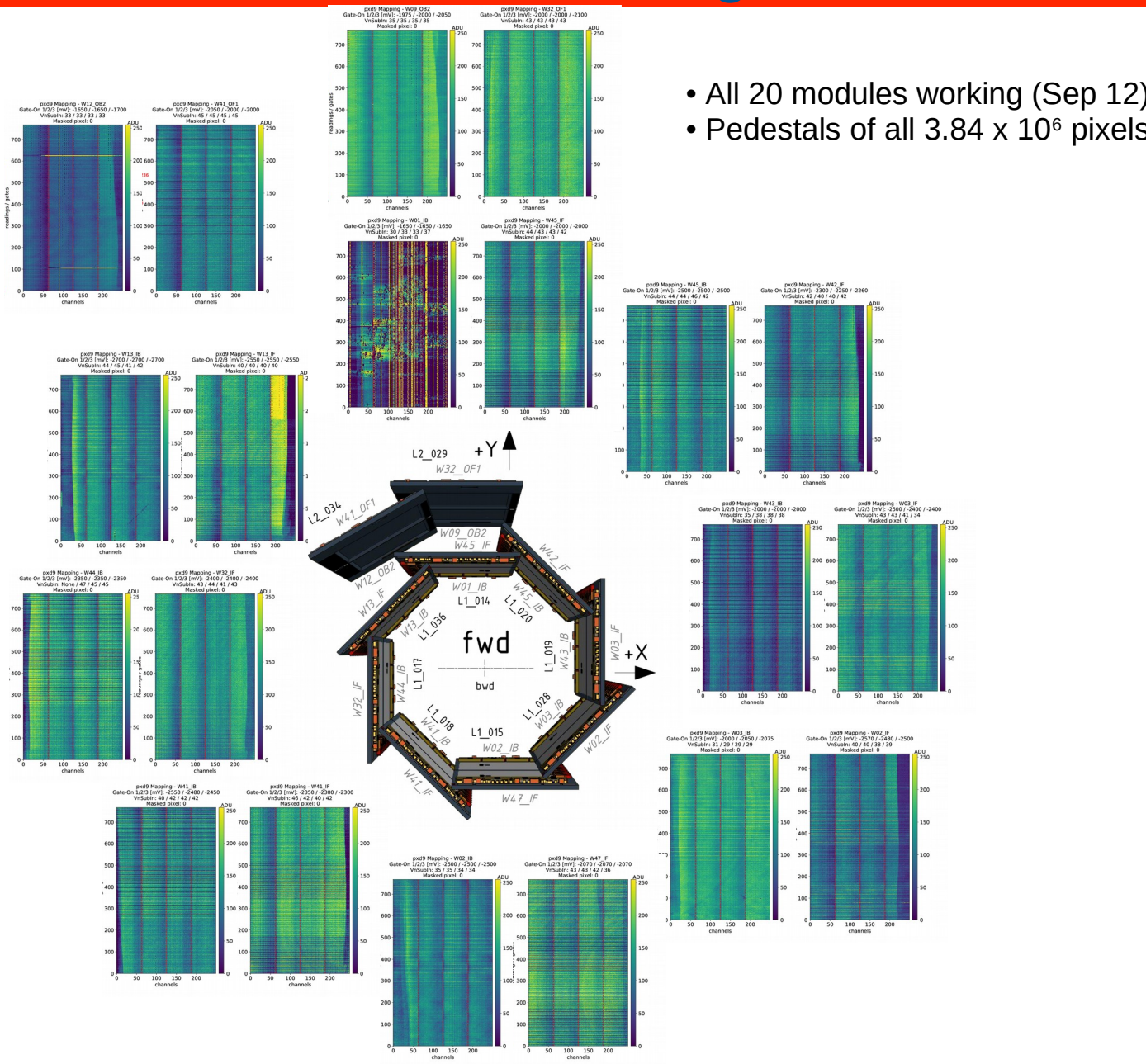
PXD with FOS Fibres Installed



Fully assembled PXD

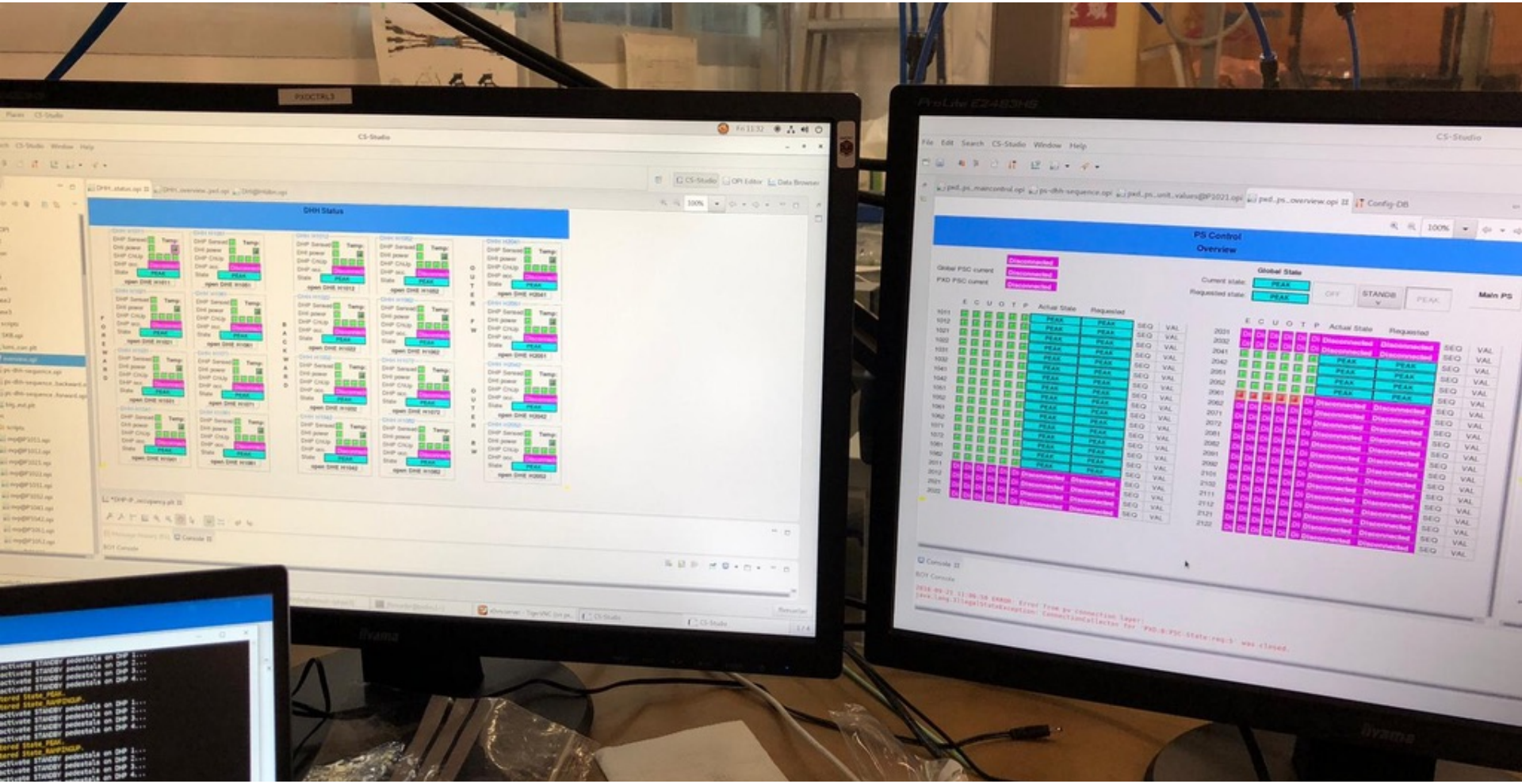


Final PXD Phase 3 Arrangement

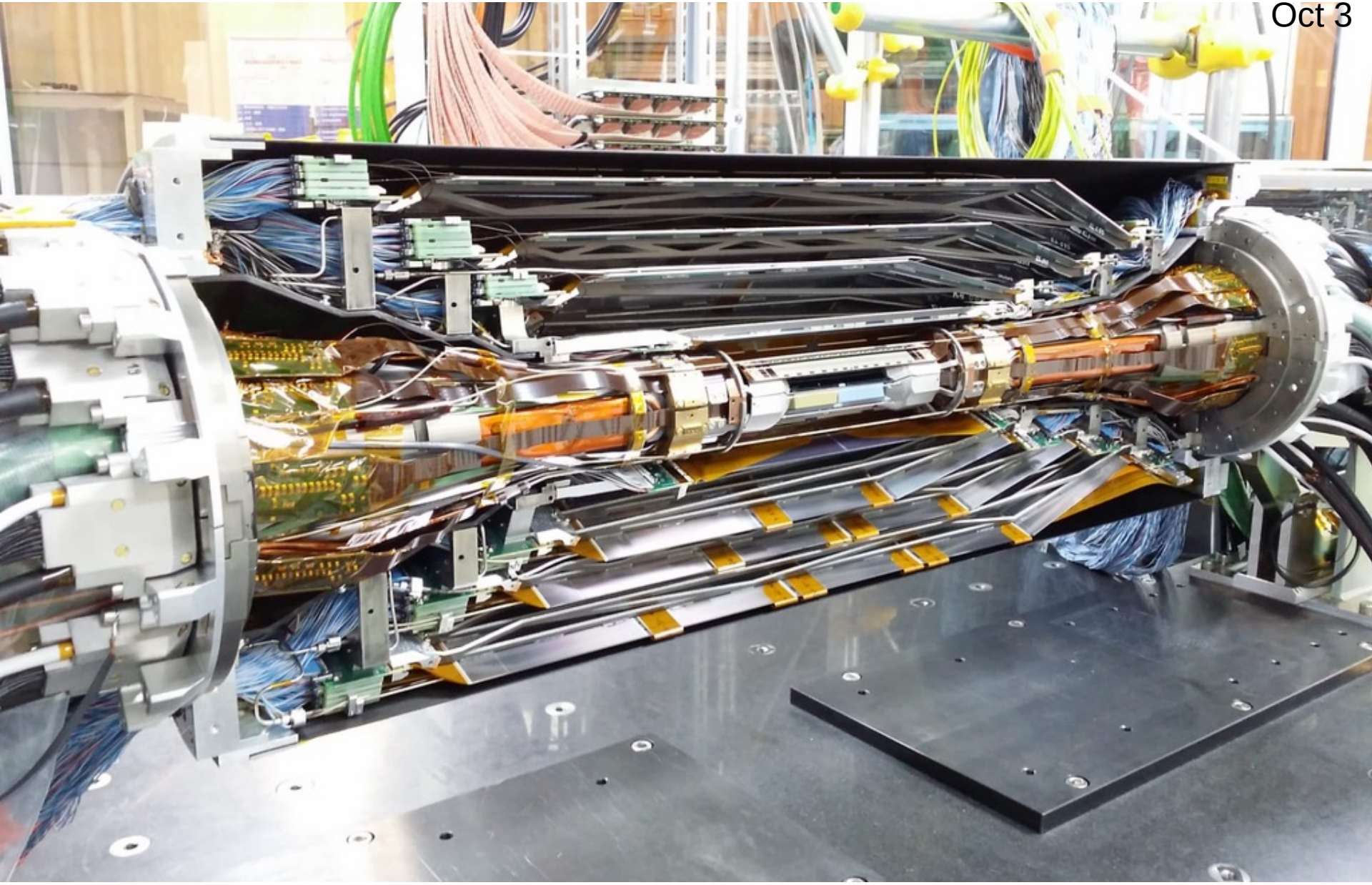


- All 20 modules working (Sep 12)
- Pedestals of all 3.84 x 10^6 pixels

September 21: All 20 PXD Modules Up and Running

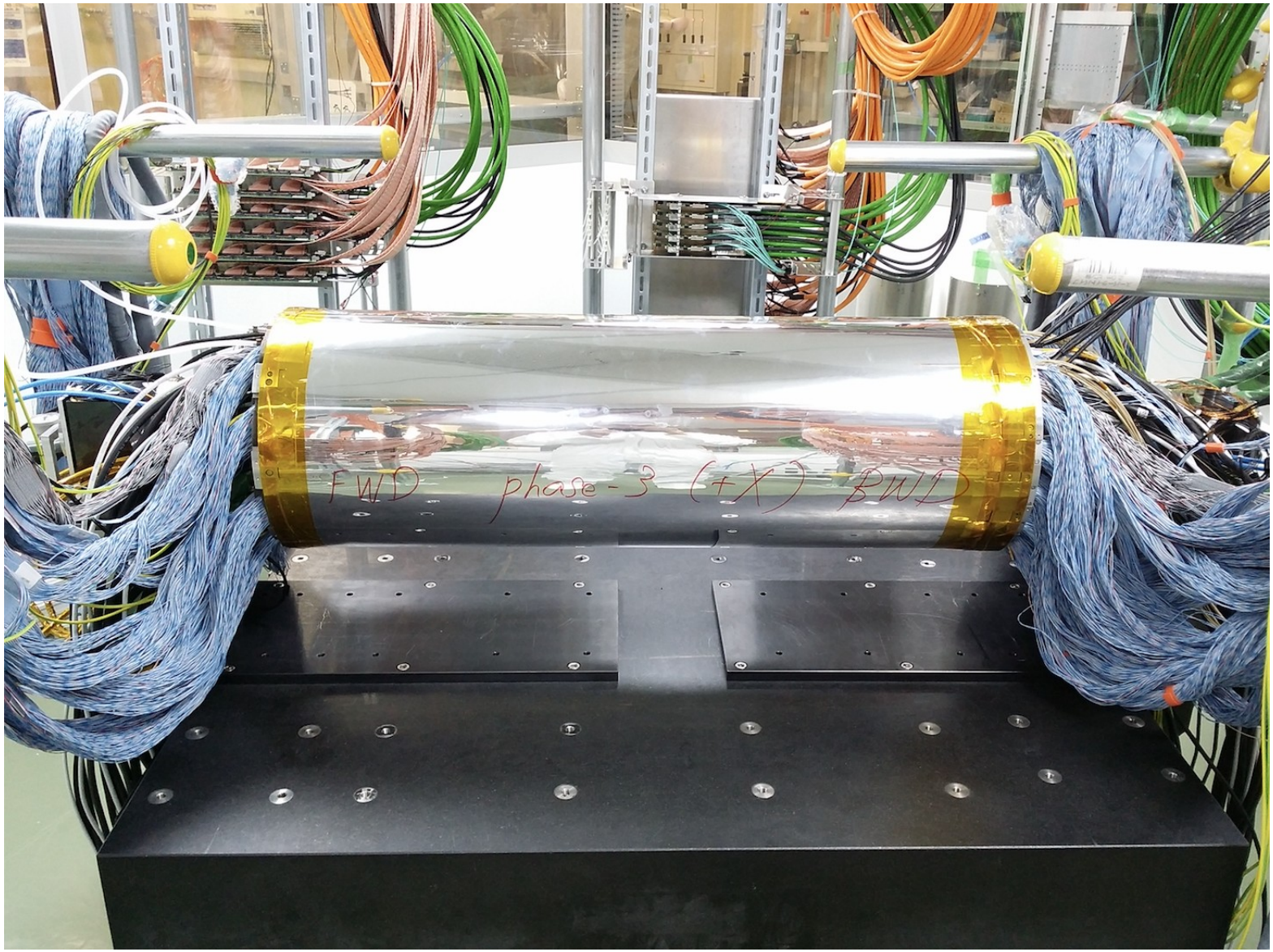


Integrated with SVD!



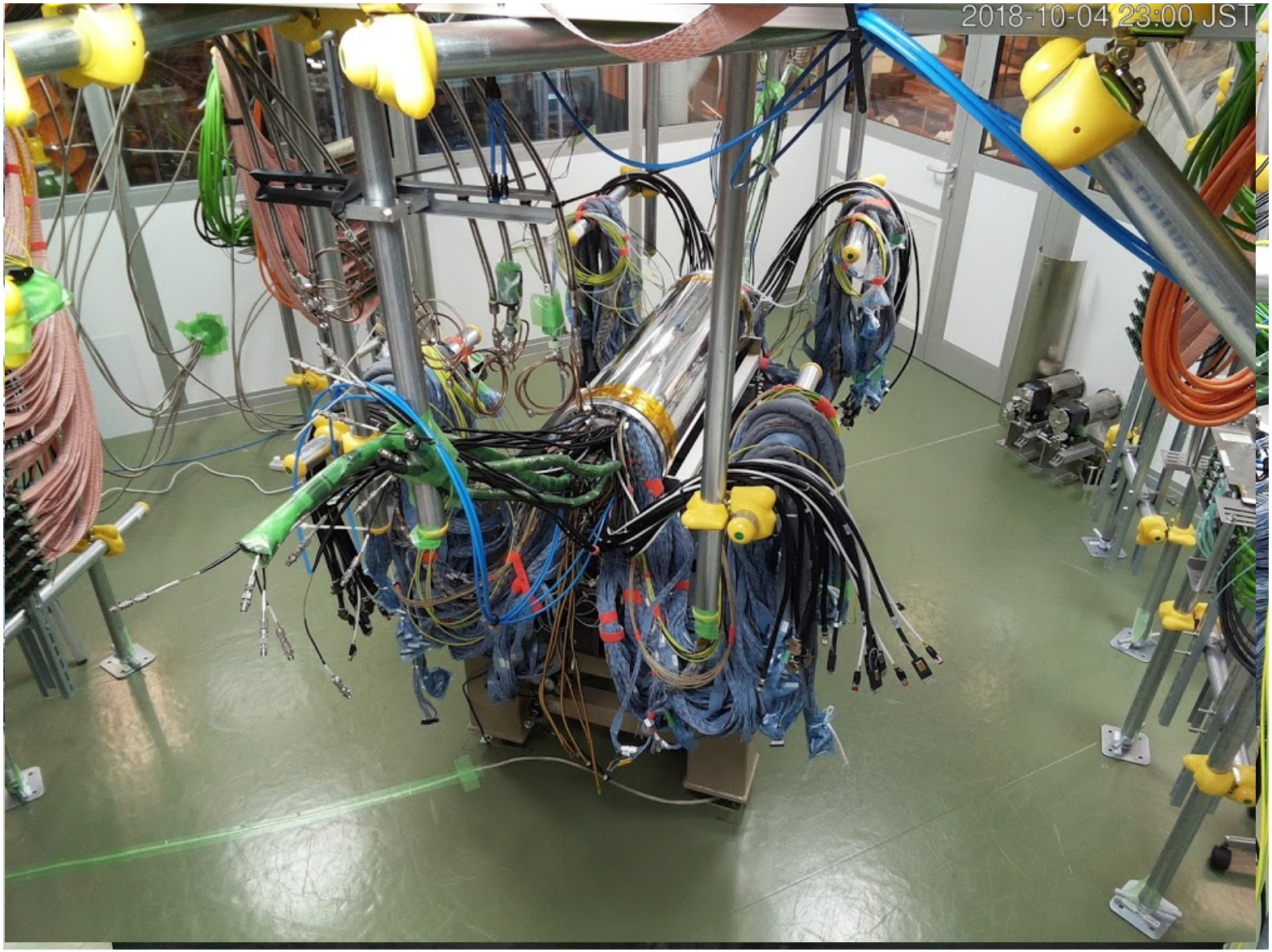
Fully Assembled VXD

Oct 4



Fully Assembled VXD

Oct 4

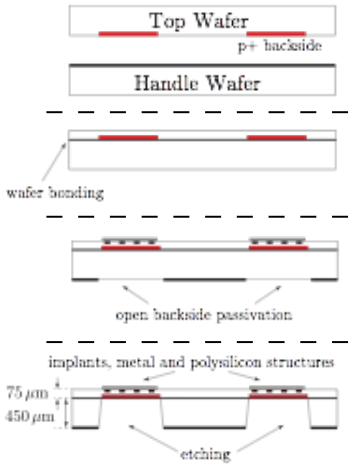


Wafer Production for PXD 2020 at HLL

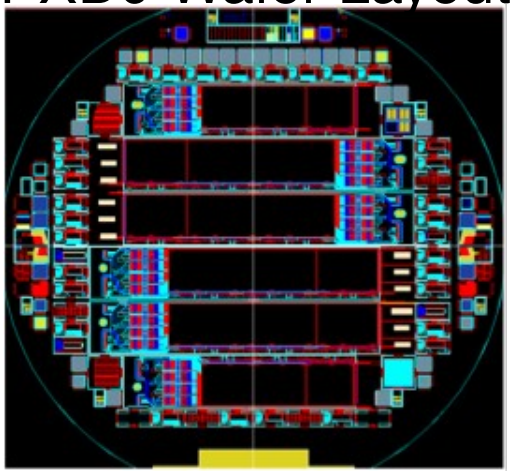
- 2 new PXD production batches
  - PXD9-20 – 7 wafers
  - PXD9-21 – 12 wafers
- Production proceeds in 4 phases
  - 0) oxidation and back side implant
  - 1) poly gates, implants, first contacts
  - 2) two layer Al metallisation, contacts
  - 3) thinning, Cu process, dicing
- Status of production
  - PXD9-20 in phase 1
    - ▶ phase 2 ~ April 2019
    - ▯ phase 3 ~ Summer 2019
  - PXD9-21 in phase 1
    - ▯ 21-Phase 2 ~ Summer 2019
    - ▯ 21-Phase 3 ~ Autumn 2019

Installation of new PXD in summer 2020

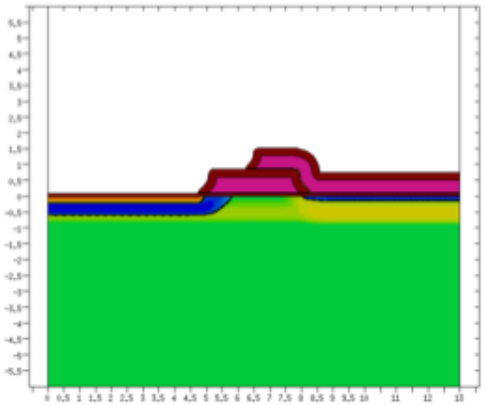
Production phases



PXD9 Wafer Layout

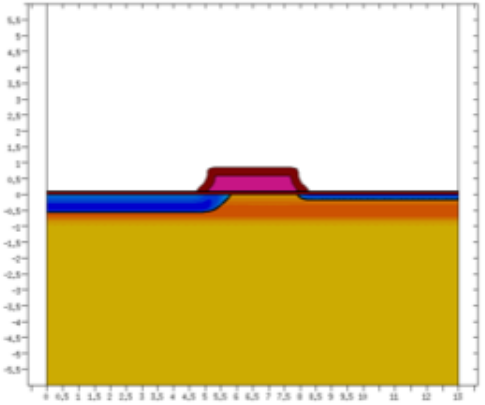


PXD9-20 status



Both poly layers
and all implantations done
→ layer deposition for first contact system

PXD9-21 status

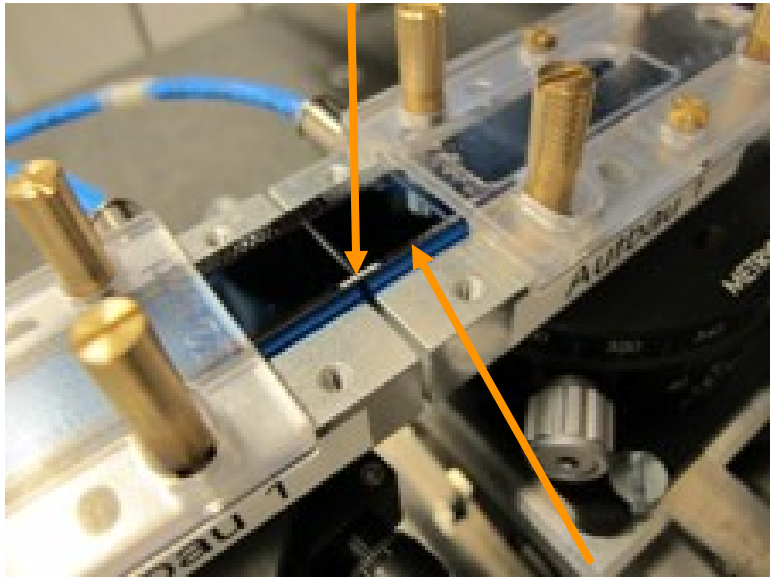


first poly layer finished
→ clear implantation
(3rd of 6 implantations)

New Ladder Assembly Procedure

Old procedure

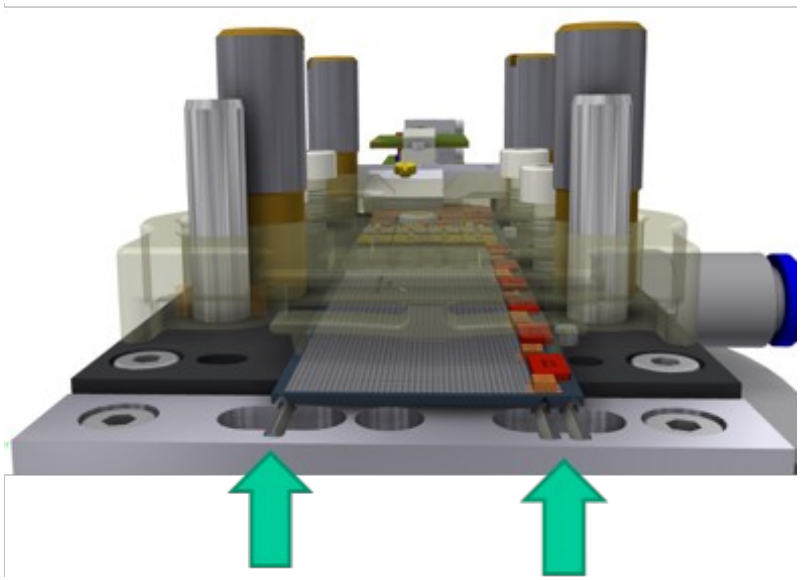
Ceramic stiffeners come from top



Sensor facing down: contact to ceramic jig

Proposed procedure

Sensor facing up: no contact to any jig



Ceramic stiffeners to be lifted from below

- Concept
  - minimize possible impact of remaining dust particle by avoiding any contact to sensor matrix
  - improve cleanliness of environment
  - otherwise change as little as possible to profit from previous learning curve
- Procedure has to be worked out in more detail and needs to be extensively tested and qualified
- Presently setting up an internal review committee

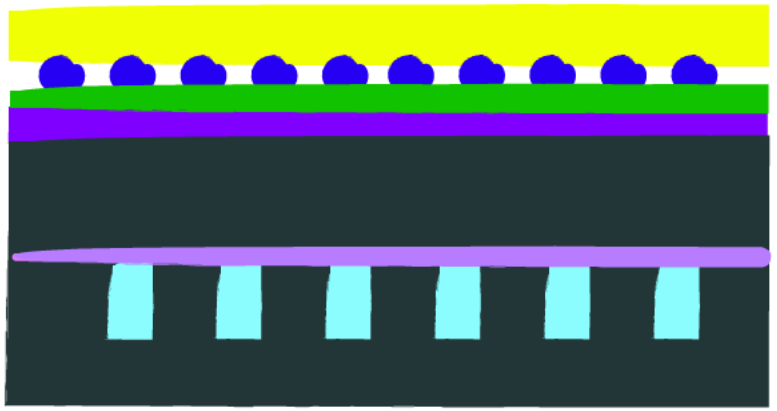
Cooling of silicon detectors

- **Modern strip and pixel detectors have large channel density**
  → high power consumption
- **Sensor temperature must be low and uniform**
  →sub-0 at hadron colliders
- **FE-electronics and sensor are tightly coupled**
  →heat source and cold sensors
- **Minimize material in services and supports**

Micro Channel Cooling

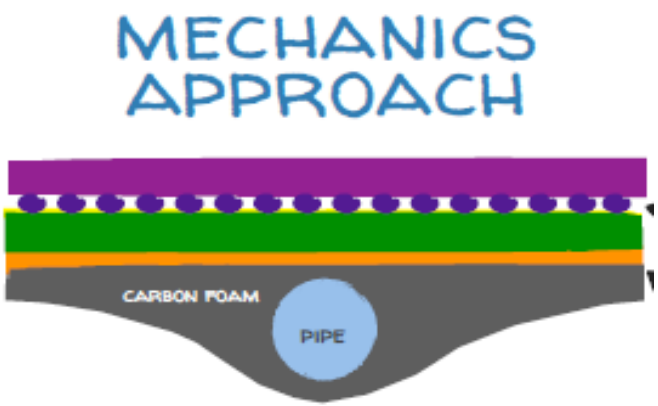
seems the natural solution

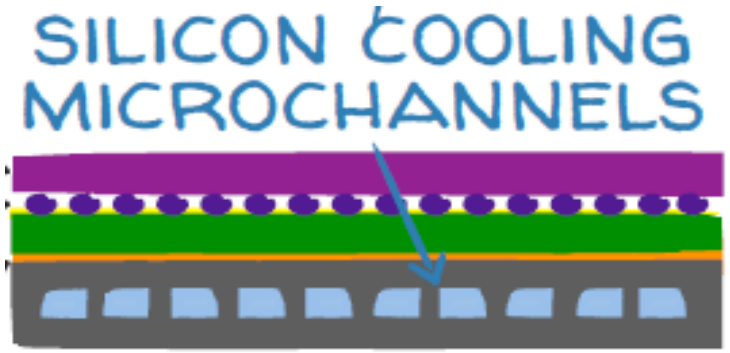
maybe inevitable at a DC machine?



- **Indeed, quite some interest in HEP world**
  - Part of one running experiment (NA62 GigaTracker)
  - Focused R&D ongoing in LHCb for VELO upgrade
  - Exploratory R&D work in ALICE, ATLAS, DEPFET collaborations
  - WP9 of AIDA-2020 provides a forum, “standards” & generic R&D funding

The case for MCC in HEP





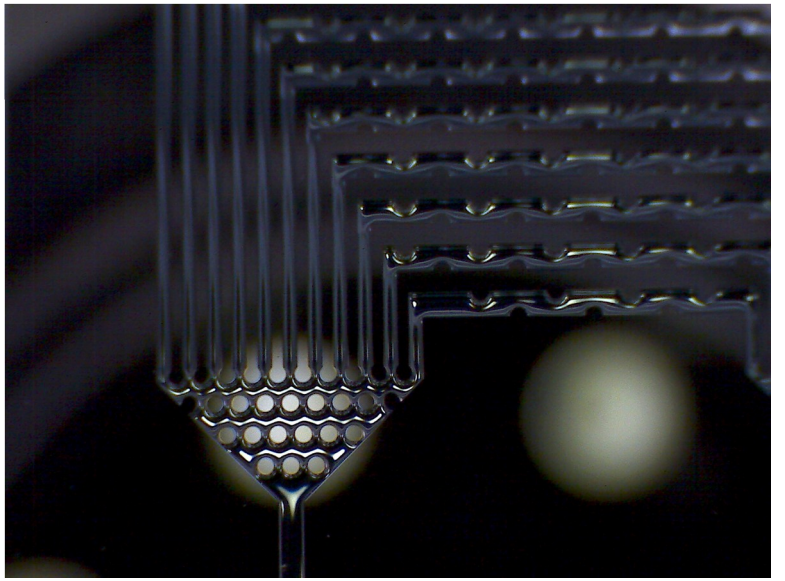
Issues:

→ thermal barriers (glue layers at each interface)
→ material budget (avoid high-Z material)
→ coolant contact area
→ CTE mismatch (cf. ATLAS IBL experience)

Micro-channel cooling, our take...

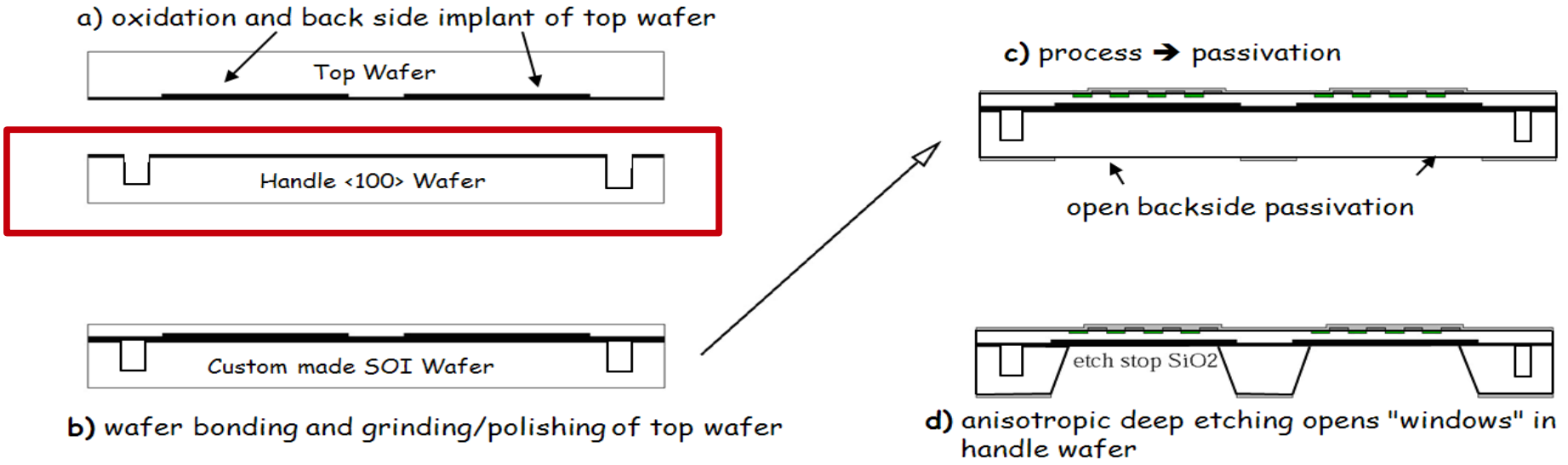
- Liquid cooling provides excellent temperature control, but is too bulky
- DEPFET, with localized power dissipation and SOI process, provides an interesting application → integrate cooling in all-silicon ladder
- Compared to existing effort, aim at relatively high T, low P
- Keep it simple: mono-phase

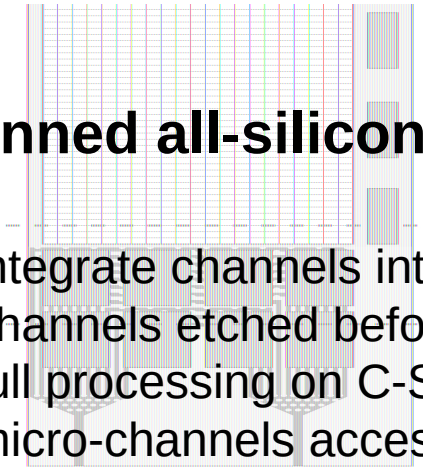
- Small team at University of Bonn MPG-HLL Munich and IFIC Valencia
- Embedded in larger effort AIDA2020 (P. Petagna CERN)



Integrated cooling channels in position-sensitive silicon detectors, JINST 11 (2016) no. 06, P06018
L. Andricek[1], M. Boronat[3], J. Dingfelder[2], J. Fuster[3], I. Garcia[3], P. Gomis[3], C. Lacasta[3], G. Liemann[1], C. Marinas[2], D. Markus[2], J. Ninkovic[1], M. Perelló[3], E. Scheugenpflug[1], M.A. Villarejo[3], M. Vos[3]
[1]MPG Halbleiterlabor Munich, [2]Bonn University, [3]IFIC (UV/CSIC) Valencia

All-silicon ladder with integrated cooling

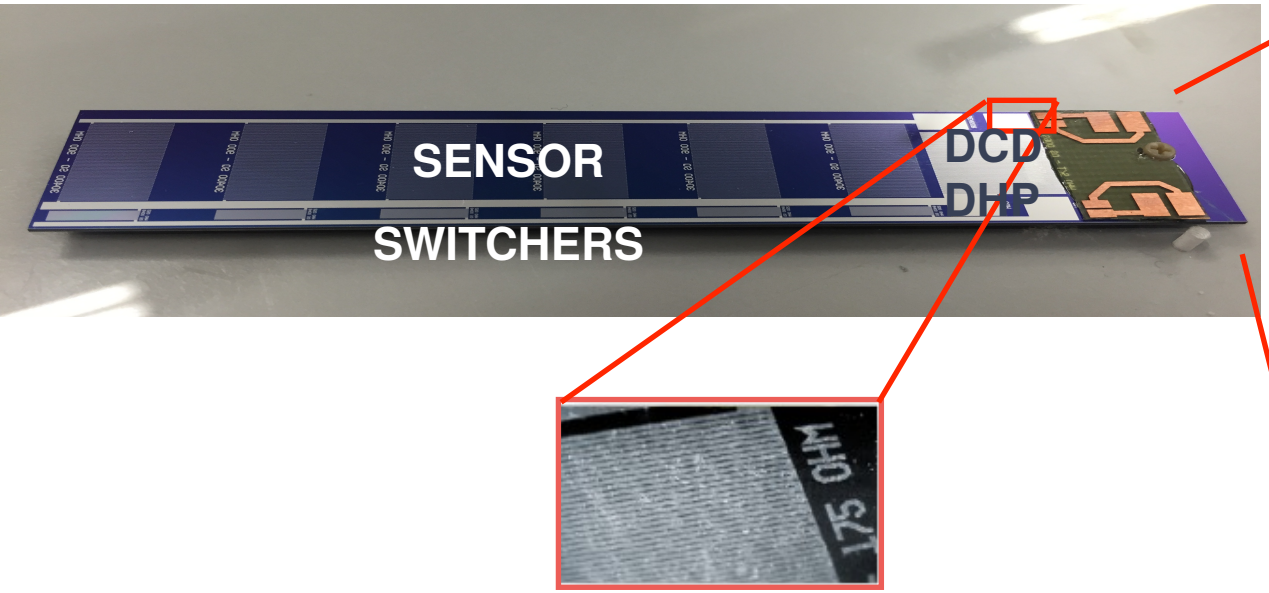


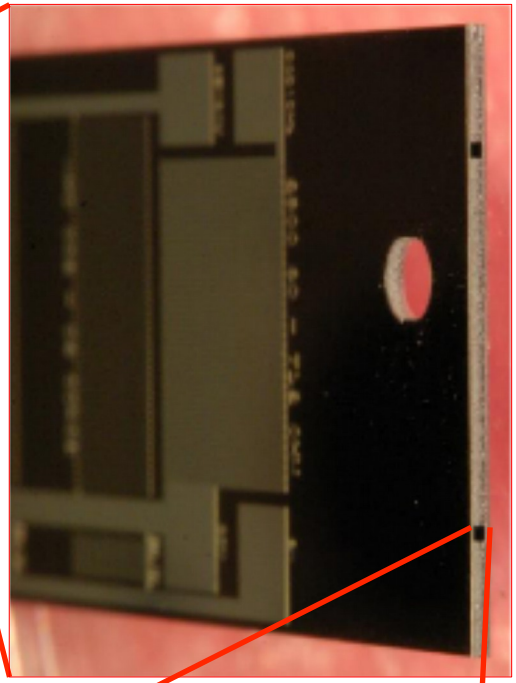


thinned all-silicon module with integrated cooling channels

:- integrate channels into handle wafer beneath the ASICs
:- channels etched before wafer bonding → cavity SOI (C-SOI)
:- full processing on C-SOI, thinning of sensitive area
:- micro-channels accessible only after cutting (laser)

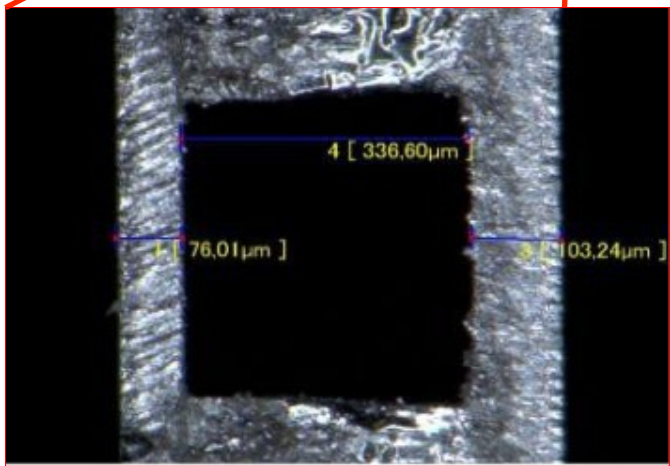
All-silicon ladder with integrated cooling





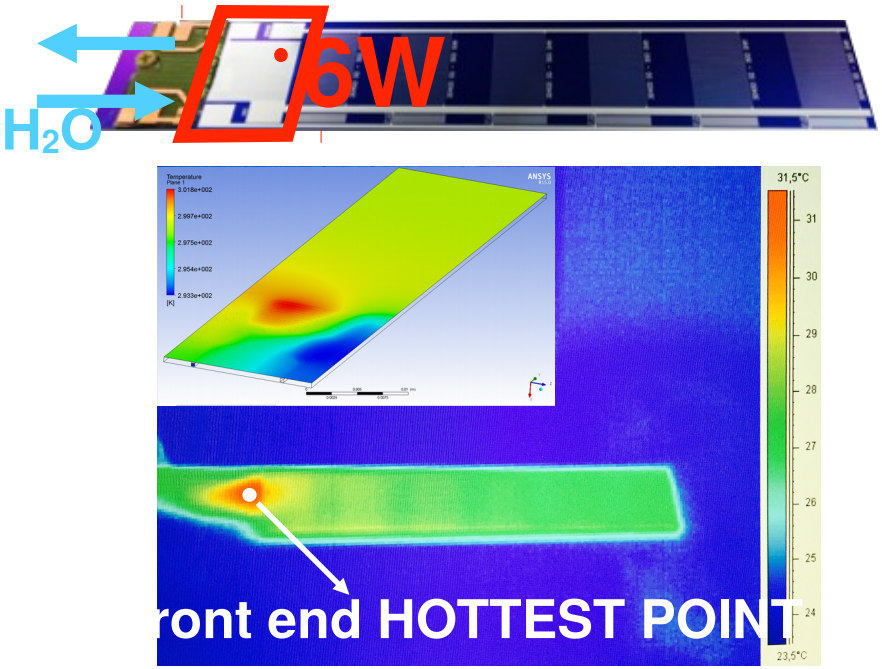
Resistor circuits to mimic DEPFET power dissipation

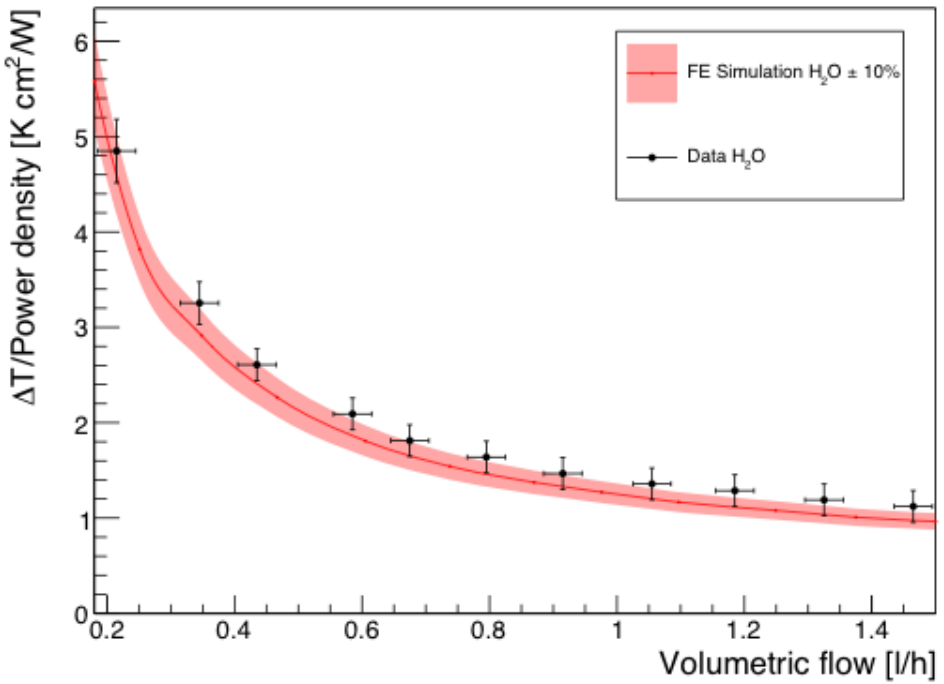
Thermo-mechanical DEPFET half-ladder



Inlet and outlet visible after wafer cutting

Thermal measurements



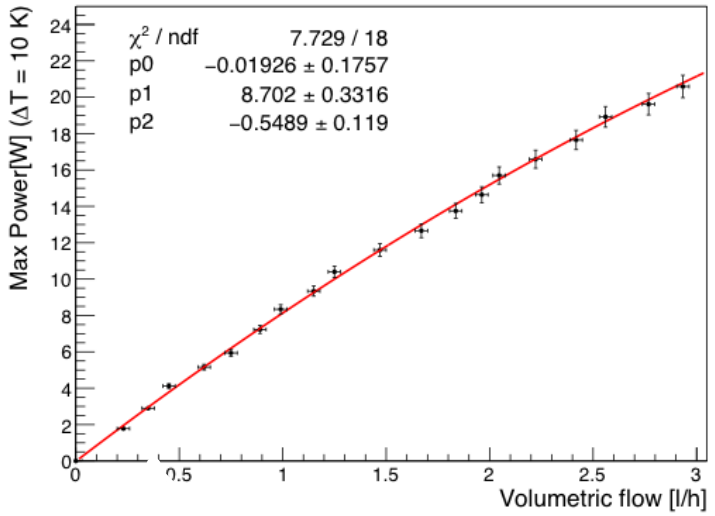


Good agreement with the **FE simulation** within 10%

Thermal figure of merit (temperature gradient/power density) = 1

Other coolants being investigated (C6F14 at CERN)

Thermo-mechanical measurements

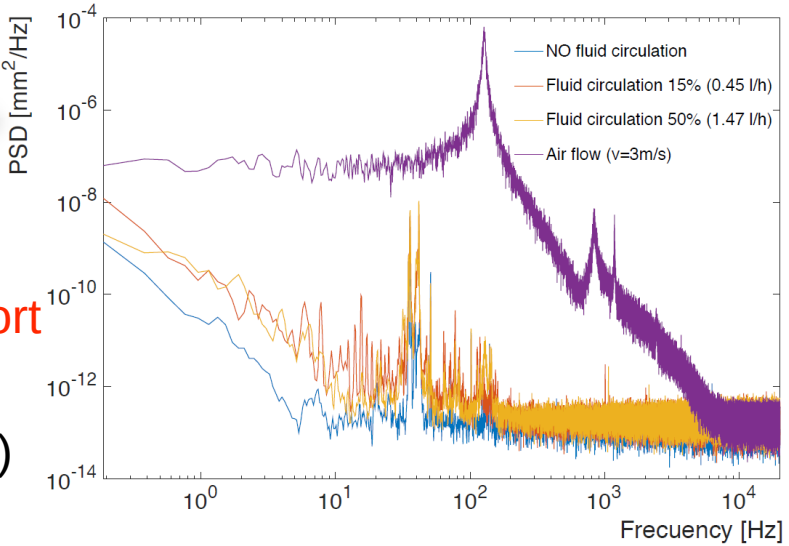


Max. power for a ΔT of 10 ºC vs. coolant flow

- Power density up to 25 W/cm^2
- Continues to improve, flow rate up to 3 l/h
- Low pressure: 0.2 - 1.5 bar

Mechanical stability

- Maximize effects by using single-point support
- Measure position with sub-μm resolution
- Impact of air flow shows sensitivity
- Liquid flow negligible impact (RMS ~ 0.5 μm)



Low pressure mono-phase liquid flow of few l/h removes local heat very efficiently. Insignificant impact on mechanical stability.

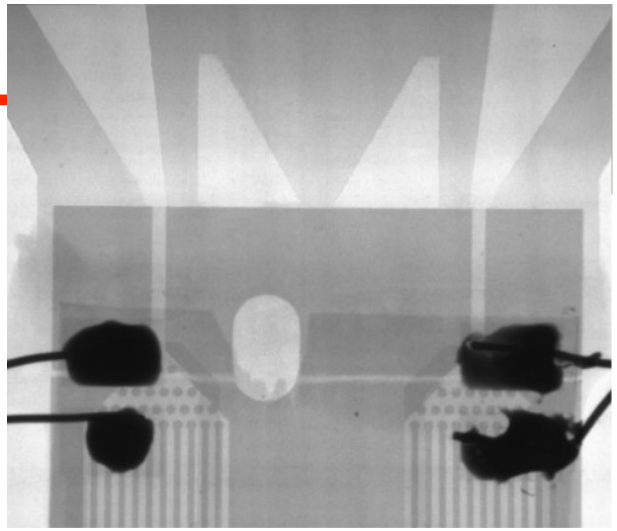
Low-mass in-plane connectors

Low-Z 3D-printed connectors

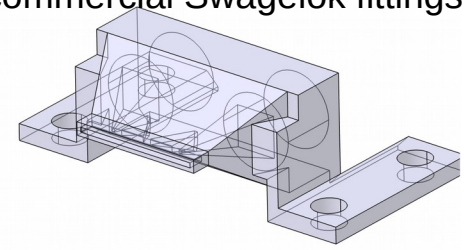
Arbitrary complexity, 30 μm tolerance
→ self-align with silicon channels

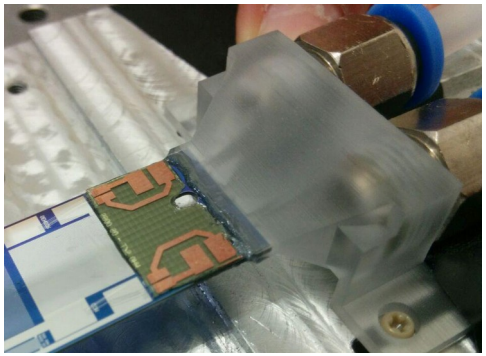
Very rapid prototyping, very cheap

Pressure-tested to >100 bars

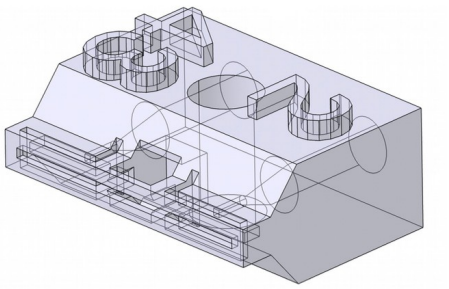


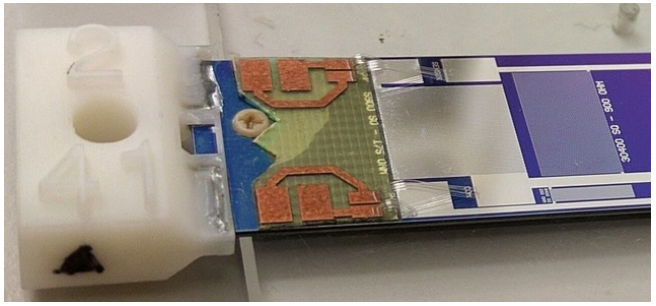
First attempt (0.81% X/X_0)
Mechanical interface to standard commercial Swagelok fittings



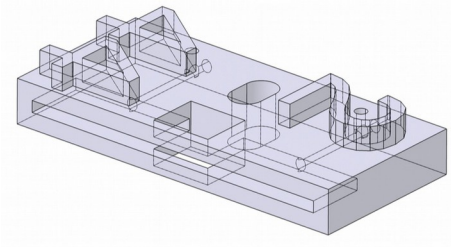


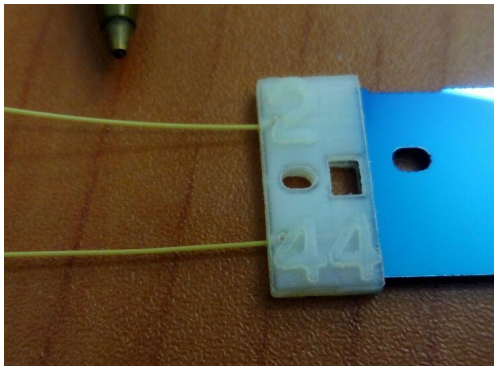
Past (0.21% X/X_0)
Smaller fittings





Present (0.05% X/X_0)
Glue PEEK tubes





Summary

BEAST II successfully operated in SuperKEKB

- Crucial commissioning experience
- Important feedback on background level

Finalized the pixel detector for Belle II

- Second PXD layer descoped due to losses in ladder assembly
- The first DEPFET-based vertex detector!
- PXD+SVD ready for installation and PXD2020 on its way

Micro-channel cooling works!

- Excellent solution for CEPC