Development of a low power TPC readout ASIC in 65 nm CMOS

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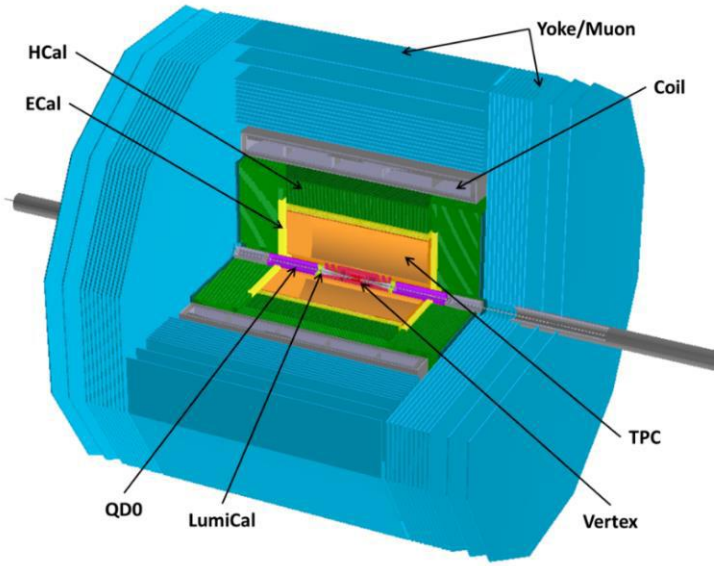
Outline

- Introduction
- ASIC design
- Chip tests
- Summary & Future Plan

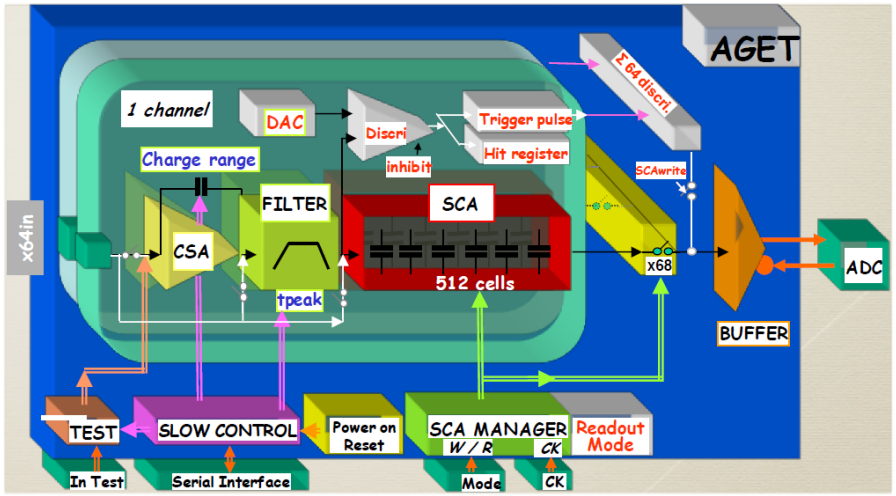
Introduction

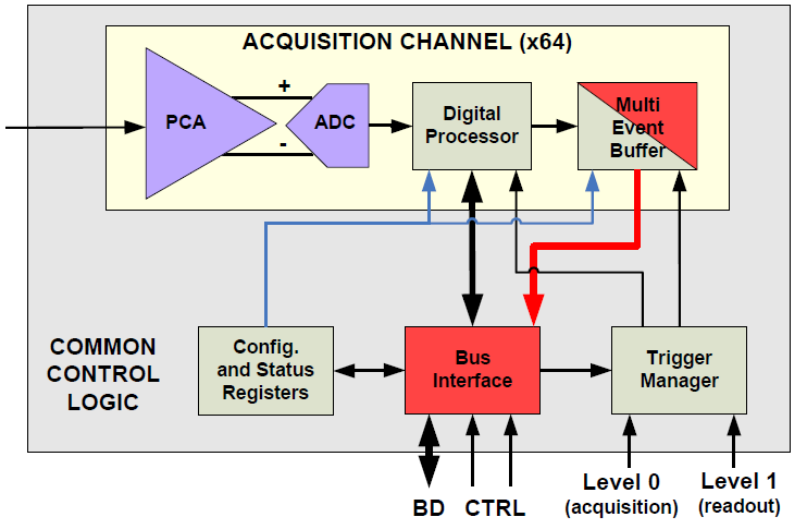
- Time Projection Chamber for CEPC



Momentum resolution (B=3.5T)	$\delta(1/p_t \approx 10^{-4}/GeV/c)$
δ_{point} in $r\Phi$	<100 μm
δ_{point} in rz	0.4-1.4 mm
Inner radius	329 mm
Outer radius	1800 mm
Drift length	2350 mm
TPC material budget	$\approx 0.05X_0$ incl. field cage $< 0.25X_0$ for readout endcap
Pad pitch/no. padrows	≈ 1 mm $\times$ (4~10mm) /≈ 200
2-hit resolution	≈ 2 mm
Efficiency	>97% for TPC only ($p_t > 1GeV$) >99% all tracking ($p_t > 1GeV$)

- Waveform sampling: SCA vs. ADC





- Analog waveform stored in switched capacitor array (SCA), selected output and digitization, APV25、AGET
- Low power, simple circuit
- Low event rate

- Direct waveform sampling ADC, ALTRO、SAMPA
- High event rate
- high power and output data bandwidth

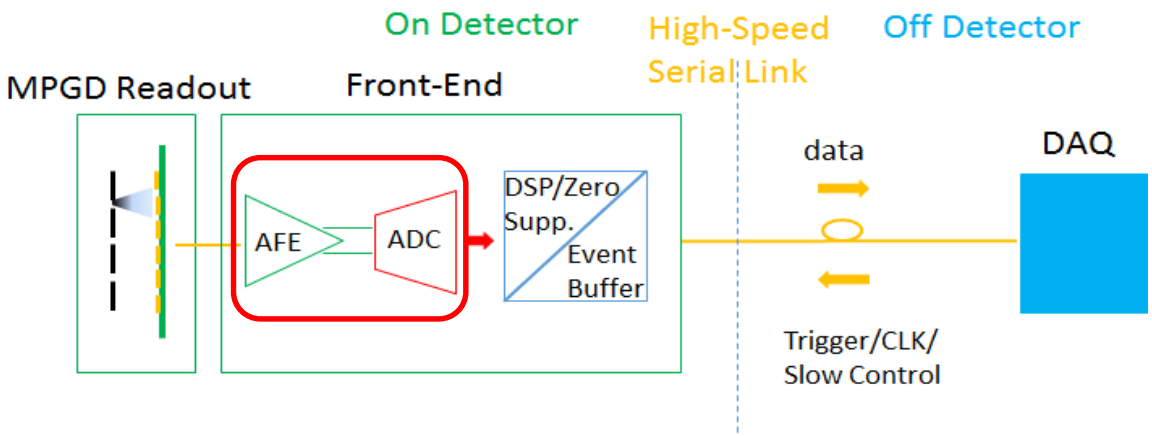
Current TPC readout ASIC

- Small readout pads (~1 mm^2), need ~ 1 M readout channel per endcape
- Working continuously in CEPC, power consumption became a serious issue

	PASA/ALTRO	AFTER	Super-ALTRO	SAMPA
TPC	ALICE	T2K	ILC	ALICE upgrade
Pad size	4x7.5 mm^2	6.9x9.7 mm^2	1x6 mm^2	4x7.5 mm^2
Pad channels	5.7 x 10^5	1.25 x 10^5	1-2 x 10^6	5.7 x 10^5
Readout Chamber	MWPC	MicroMegas	GEM/MicroMegas	GEM
Gain	12mV/fC	18 mV/fC	12-27 mV/fC	20/30 mV/fC
Shaper	CR-$(RC)^4$	CR-$(RC)^2$	CR-$(RC)^4$	CR-$(RC)^4$
Peaking time	200 ns	100 ns	30-120 ns	80/160 ns
ENC	385 e	1000 e	520 e	482 e @ 180ns
Waveform Sampler	ADC	SCA	ADC	ADC
Sampling frequency	10MSPS	25MSPS	40MSPS	20MSPS
Dynamic range	10bit	10bit	10bit	10bit
Power consumption	32mW/ch	6.2-7.5mW/ch	47.3mW/ch	8mW/ch
CMOS Process	250 nm	350 nm	130 nm	130nm

Low power TPC readout ASIC

- Each channel consists of analog front-end (preamplifier and CR-RC shaper), 10b,20-40MS/s waveform sampling ADC and power consumption less than 5 mW/ch
- Low power digital filter and data compression

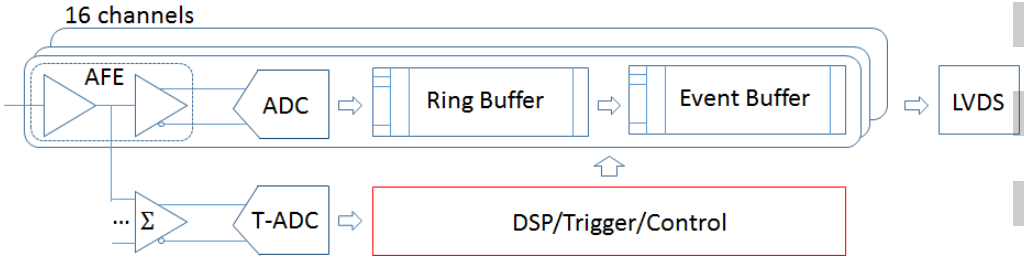


Group members

- ASIC designer:
  - Tsinghua DEP: Zhi Deng, Wei Liu, Feng Liu, Xinyuan Zhao
  - Tsinghua IME: Fule Li, Xian Gu
- Detector and System:
  - IHEP: Huirong Qi group
  - Tsinghua DEP: Yulan Li, Hui Gong

Architecture and Spec.

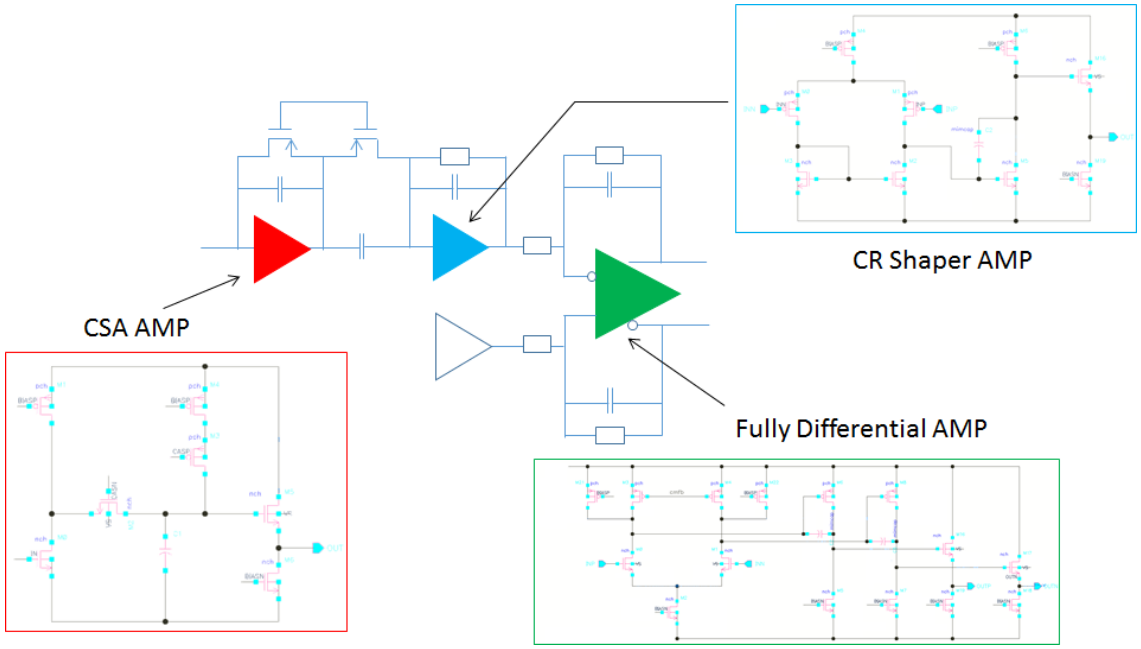
- First prototype:
  - 5 channel AFE
  - Single channel SAR-ADC
  - Full function

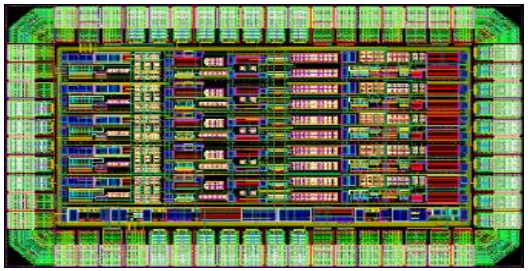


AFE	
Signal Polarity	Negative
Detector Capacitance	5-20 pF
Shaper	CR-RC
Shaping Time	160 ns
ENC (Equivalent Noise Charge)	<500 e @ 10pF
Dynamic Range	120 fC
Gain	10 mV/fC
INL (Integrated Non-Linearity)	<1%
Crosstalk	<1%
Power Consumption (AFE)	<2.5 mW/ch
ADC	
Input Range	-0.6V ~ 0.6V diff.
Resolution	10 bit
Sampling Rate	40 MSPS
DNL	<0.65 LSB
INL	<0.6 LSB
ENOB	>9 bit @ 2MHz
Power Consumption (ADC)	<2.5 mW/ch
Process	65 nm CMOS

Analog Front-end

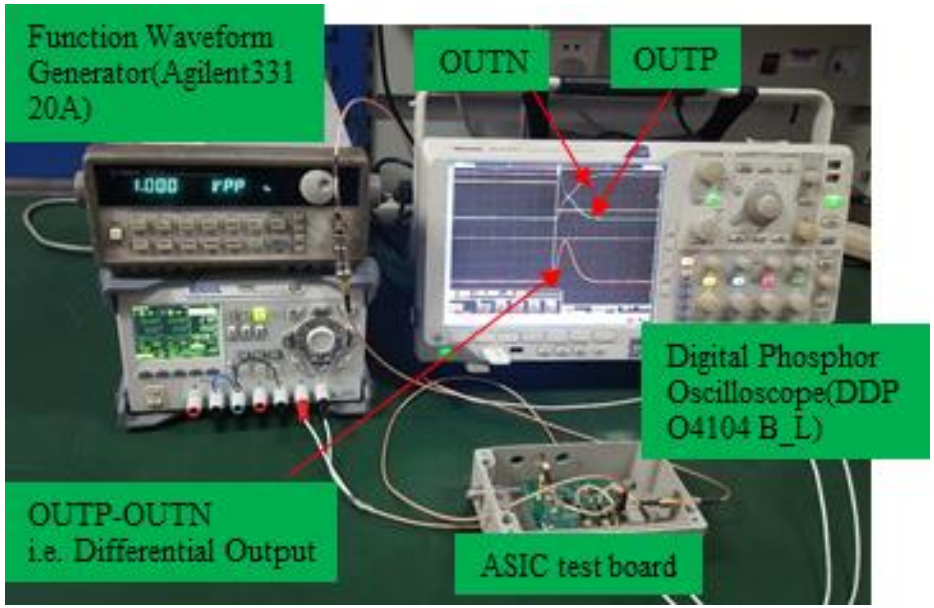
- Schematics and Layout

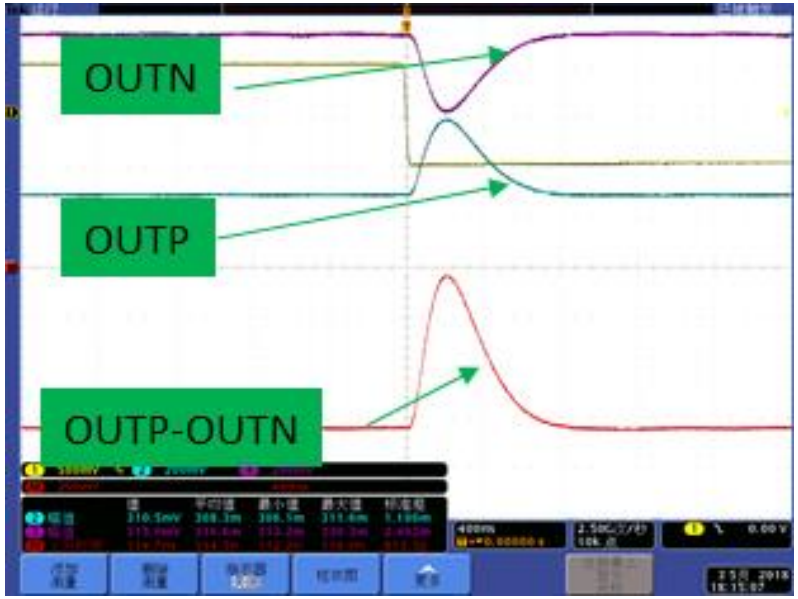




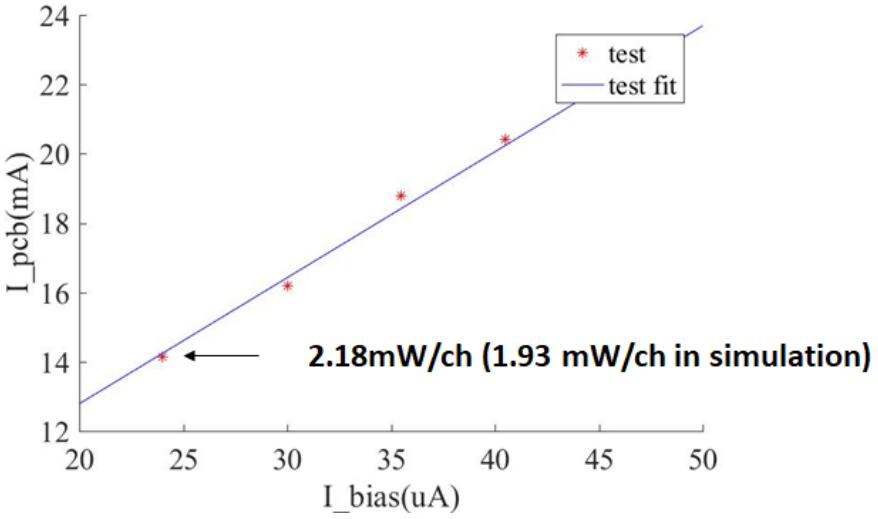
1320um x 838um

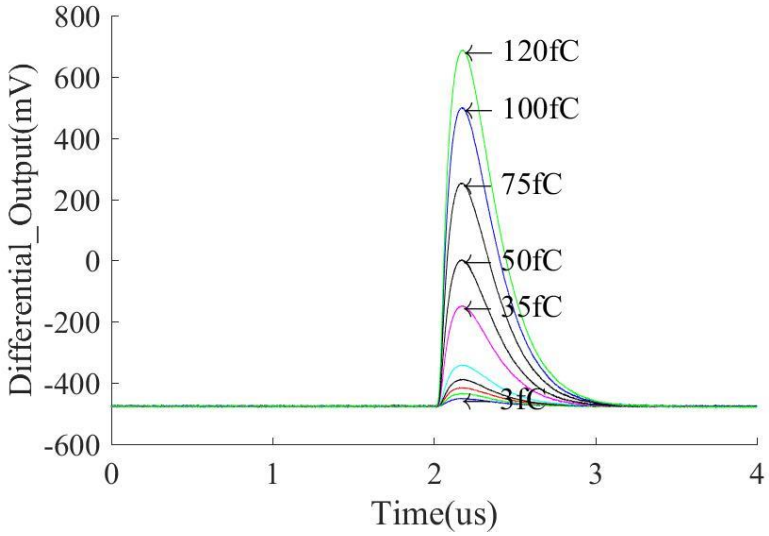
- Test setup

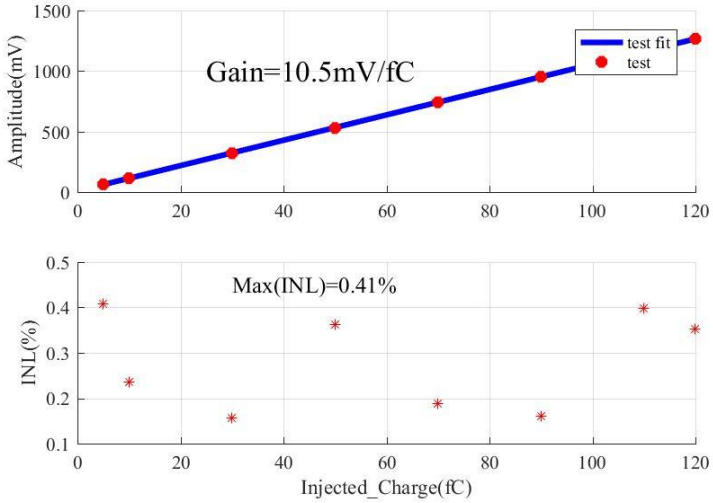

Function Waveform Generator(Agilent33120A)
OUTN
OUTP
Digital Phosphor Oscilloscope(DDPO4104 B_L)
OUTP-OUTN i.e. Differential Output
ASIC test board


OUTN
OUTP
OUTP-OUTN

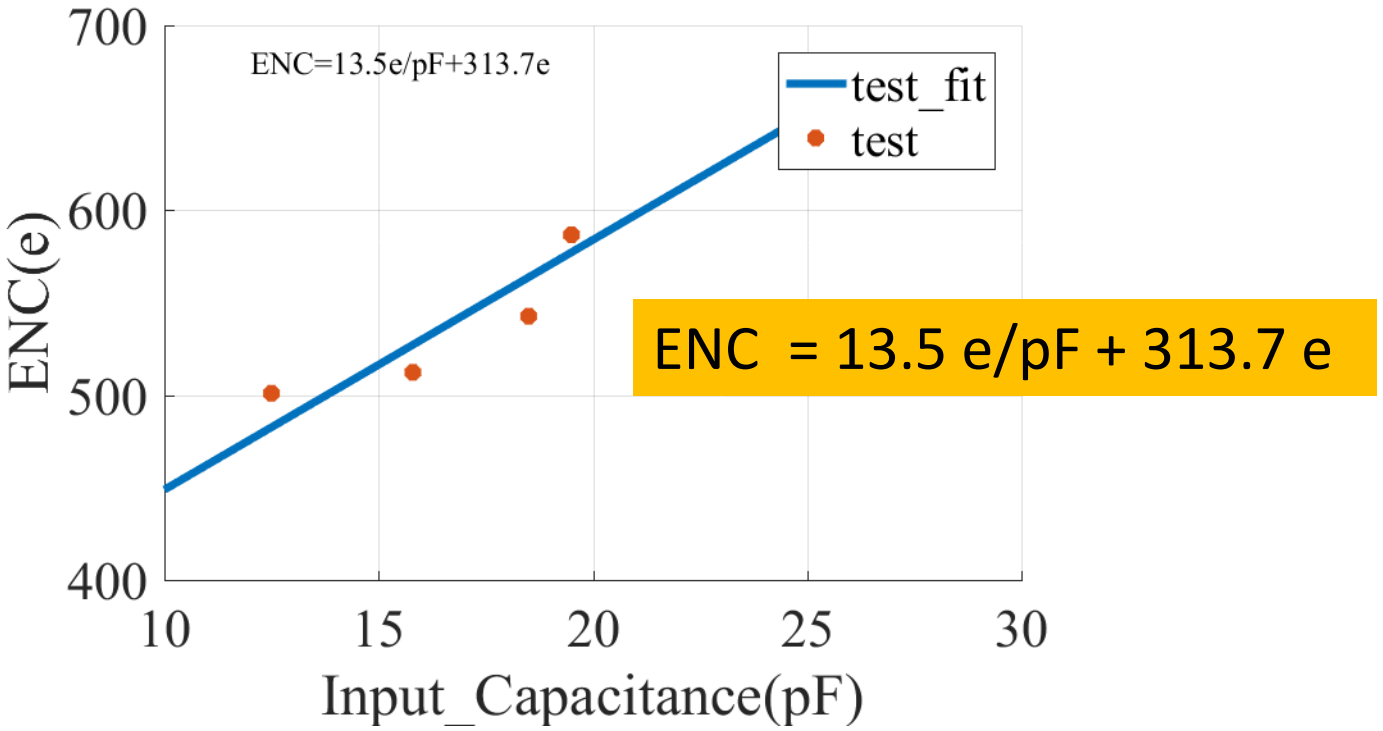
- Power and Linearity







- ENC noise

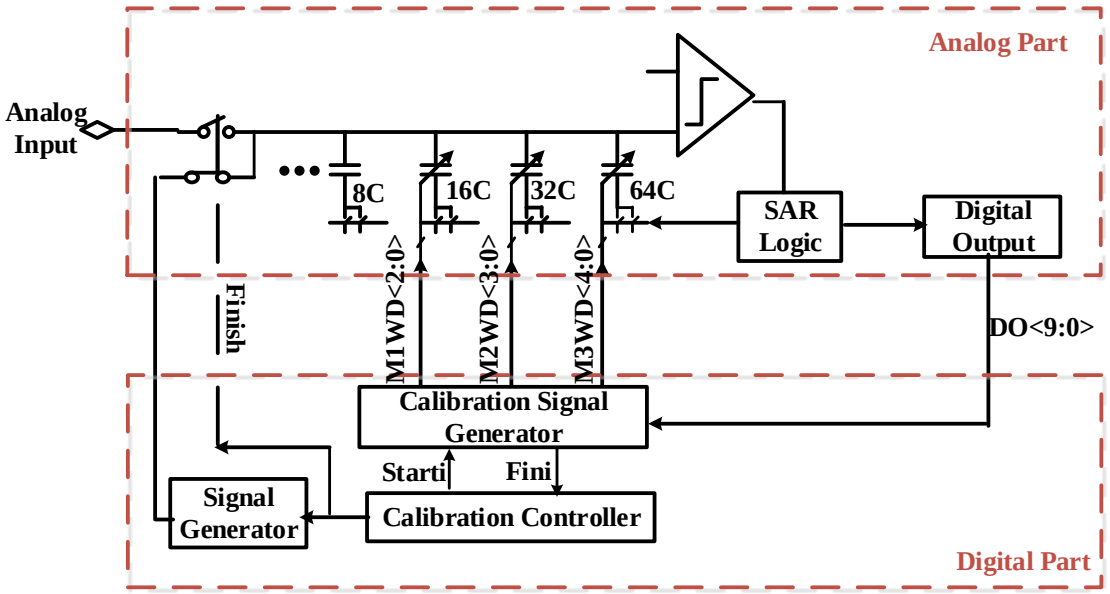


ENC = 13.5 e/pF + 313.7 e

SAR ADC

Design Specification

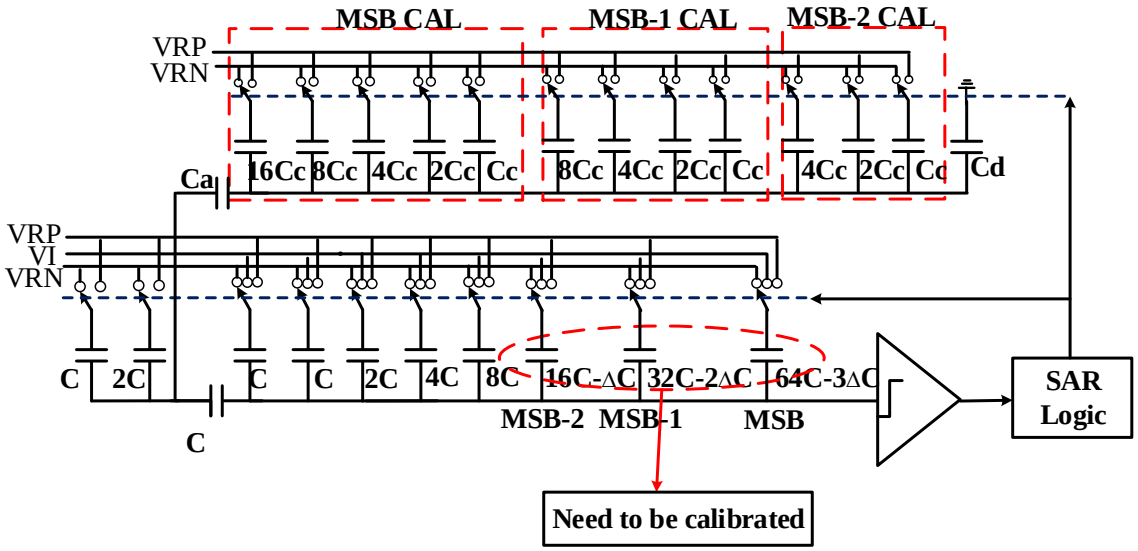
- Sample Rate: 100MS/s
- Resolution:10 bits
- Input capacidence:180fF
- ENOB:≥9bits
- Power Consumption:≤1mW
- Core chip area:≤0.03 mm^2



ADC block diagram

SAR ADC with DAC capacitance mismatch calibration

- ADC Structure

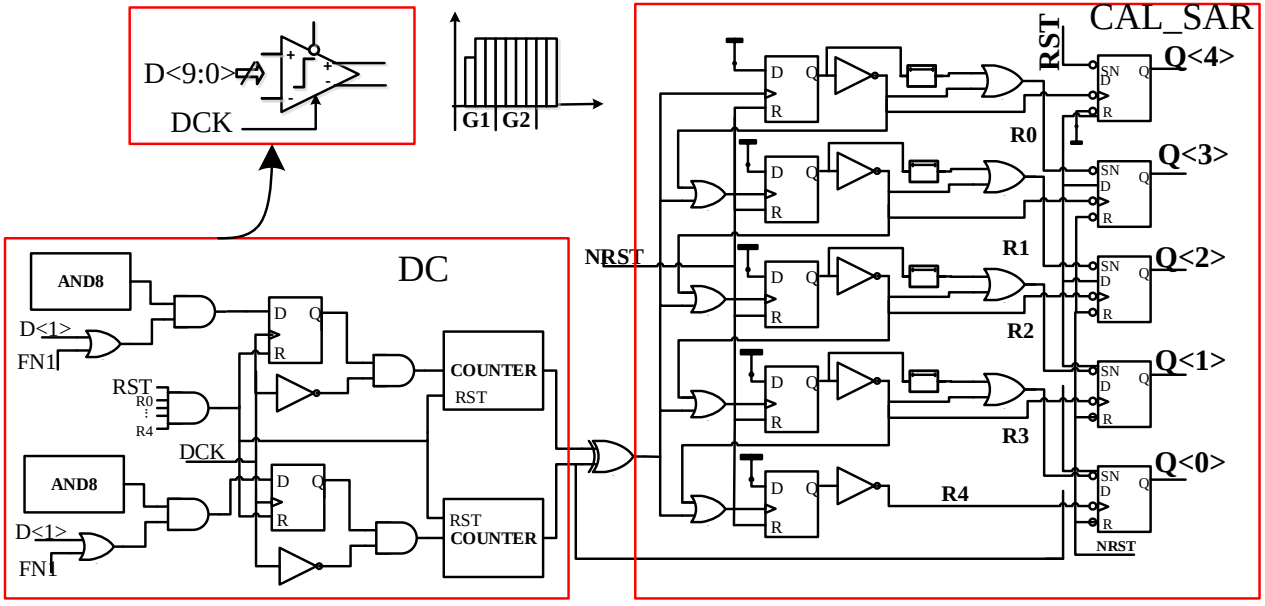


DAC Array ：

- Segmentation DAC array;
- Main DAC + Calibration DAC
- Unit capacitor : 1.4fF;

High speed design:

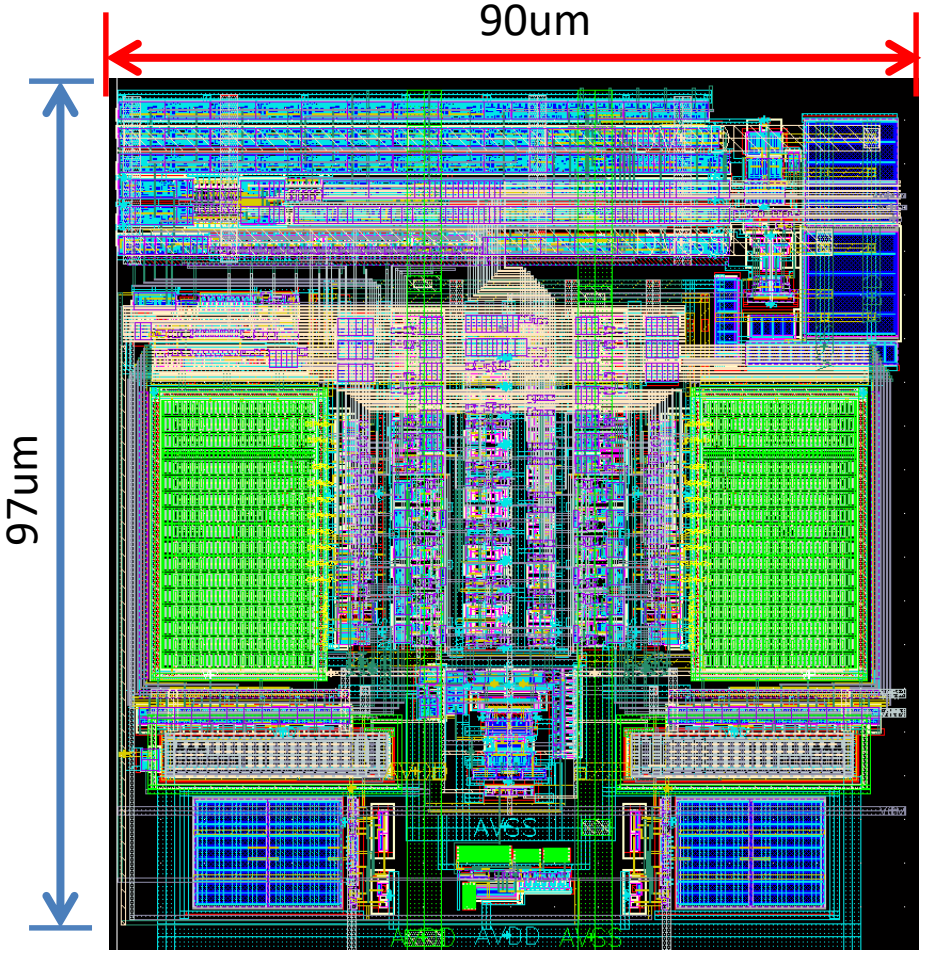
- Asynchronous Clock;
- Split Capacitor Array;
- Dynamic Logic;
- Transparent Latch for fast DAC settling

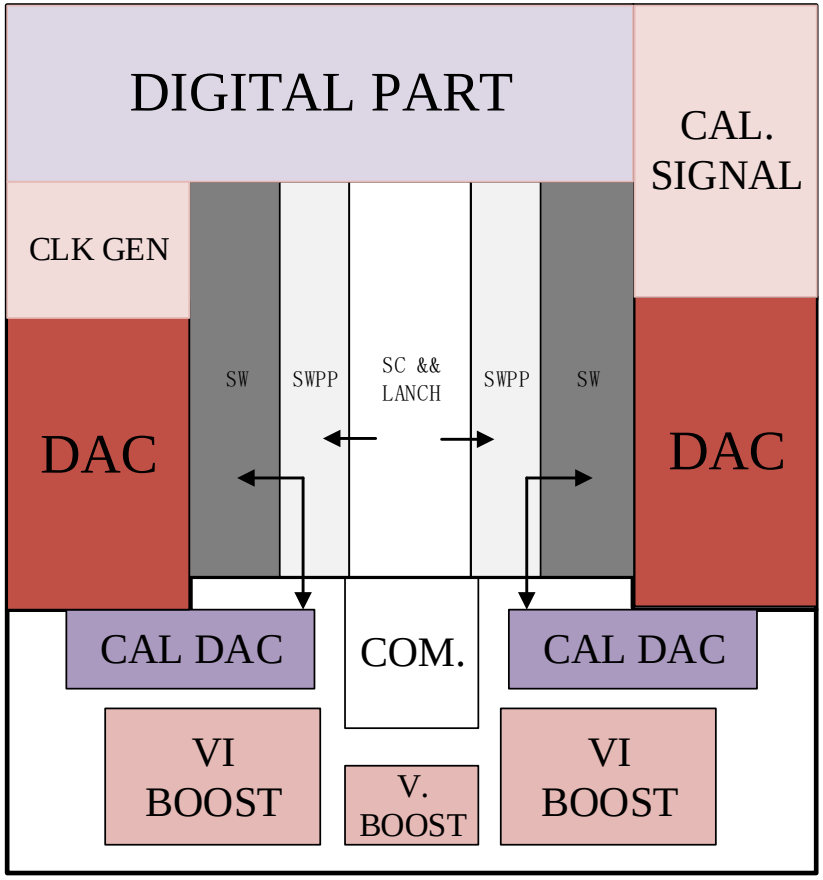


Digital circuits:

- Generate Calibration Configuration bits Q<4:0>;
- Full-custom design;
- BUS architecture and Multiplex circuits to achieve smaller chip area

- ADC Layout


90um
97um
AVSS
AVDD
AVSS


DIGITAL PART
CAL.
SIGNAL
CLK GEN
SW
SWPP
SC &&
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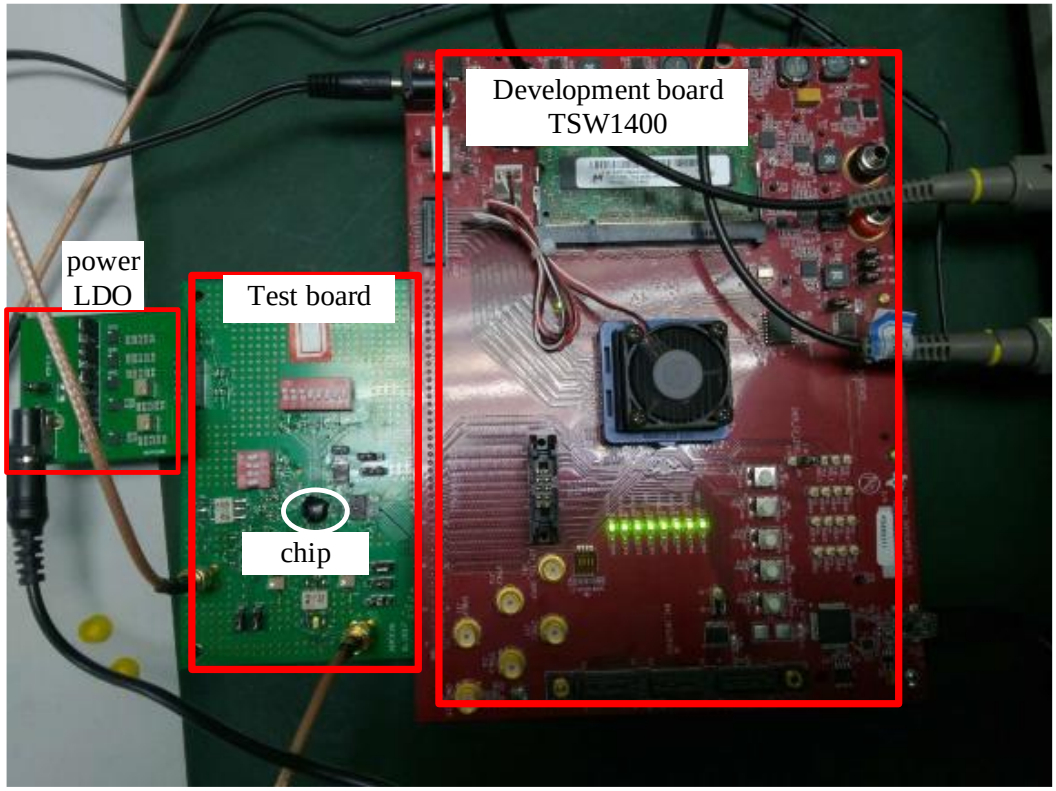
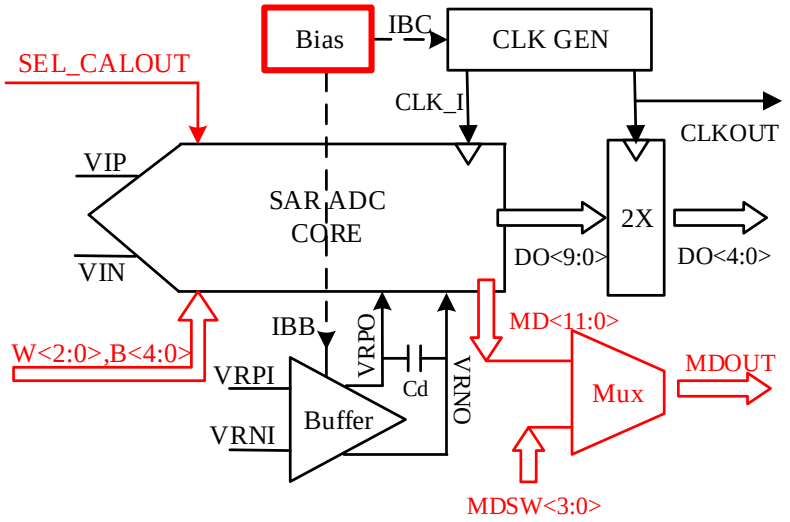
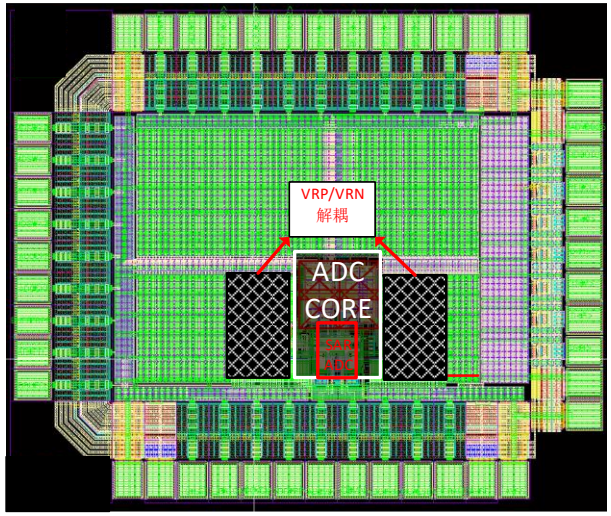
SWPP
SW
DAC
DAC
CAL DAC
COM.
CAL DAC
VI
BOOST
V.
BOOST
VI
BOOST

- Test setup
  - TSW1400EVM

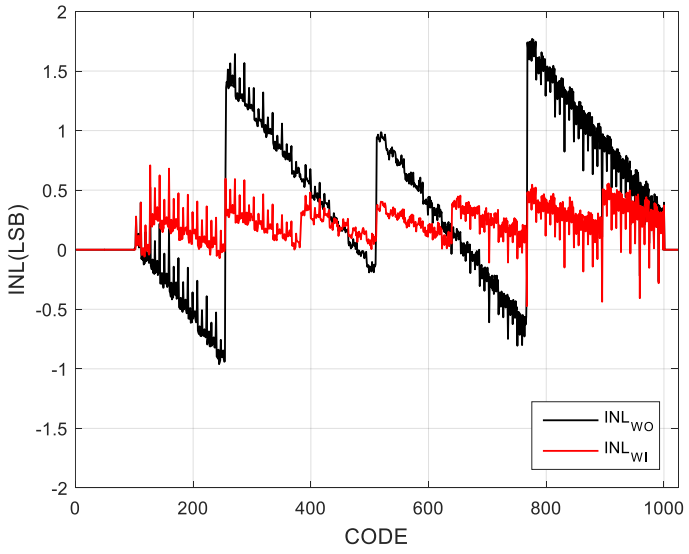


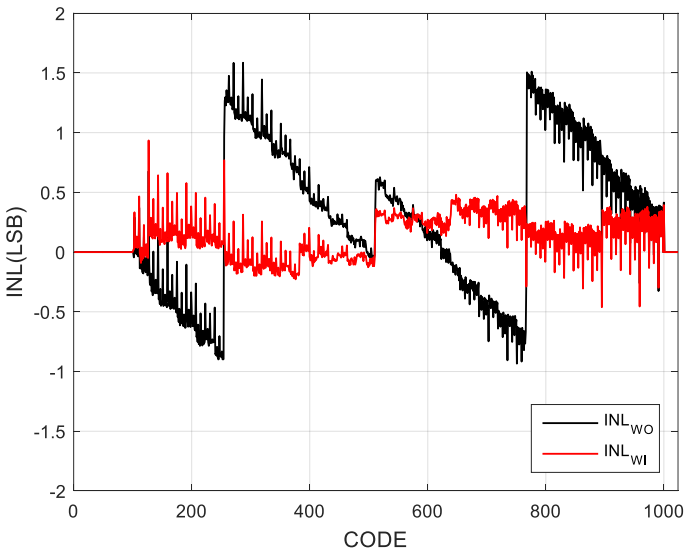




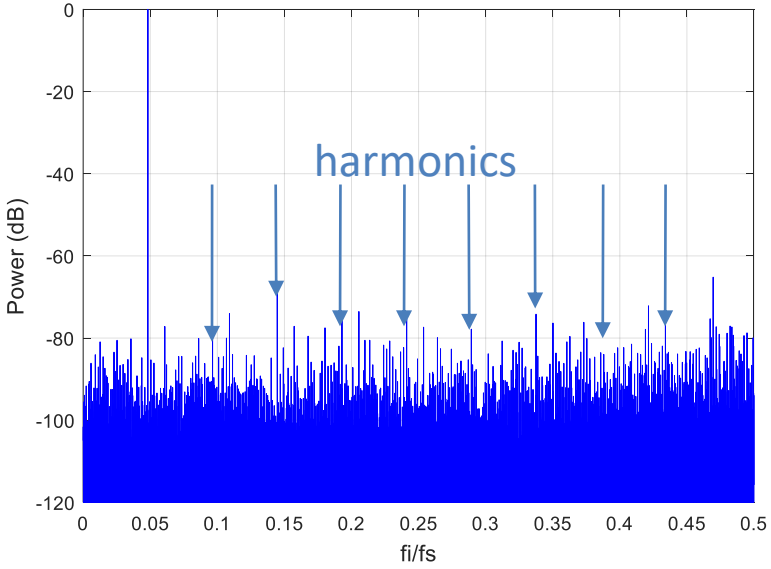
- Linearity @ 50MSPS, 2.4MHz sine input

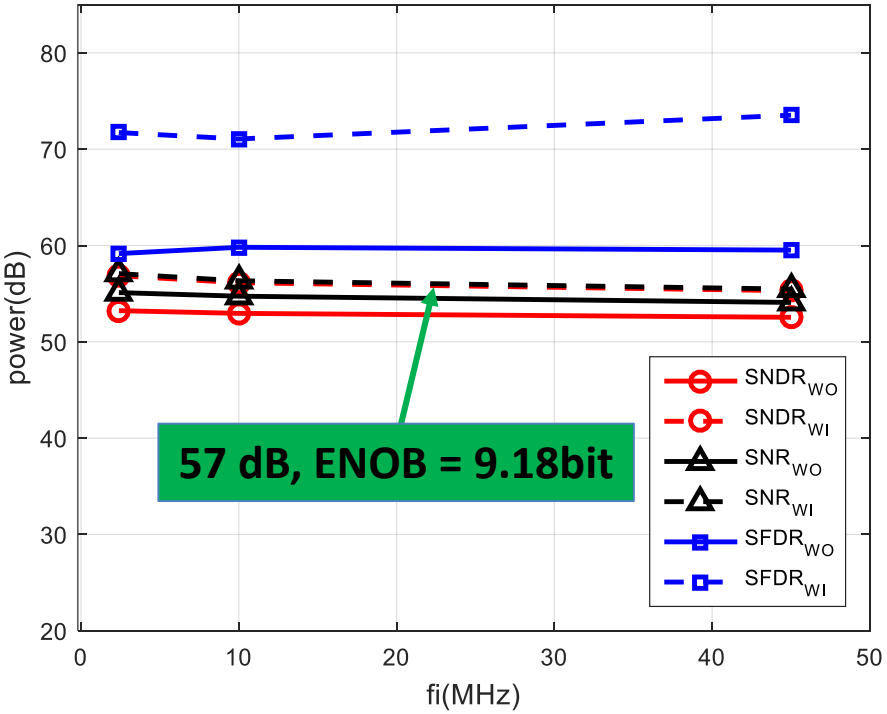
Chip NO.	Without Cali.		With Cali.	
	SNDR (dB)	SFDR (dBc)	SNDR (dB)	SFDR (dBc)
1	54.0	61.4	57.2	79.4
2	53.2	59.2	56.9	71.7





- SNDR @ 50 MSPS sampling rate

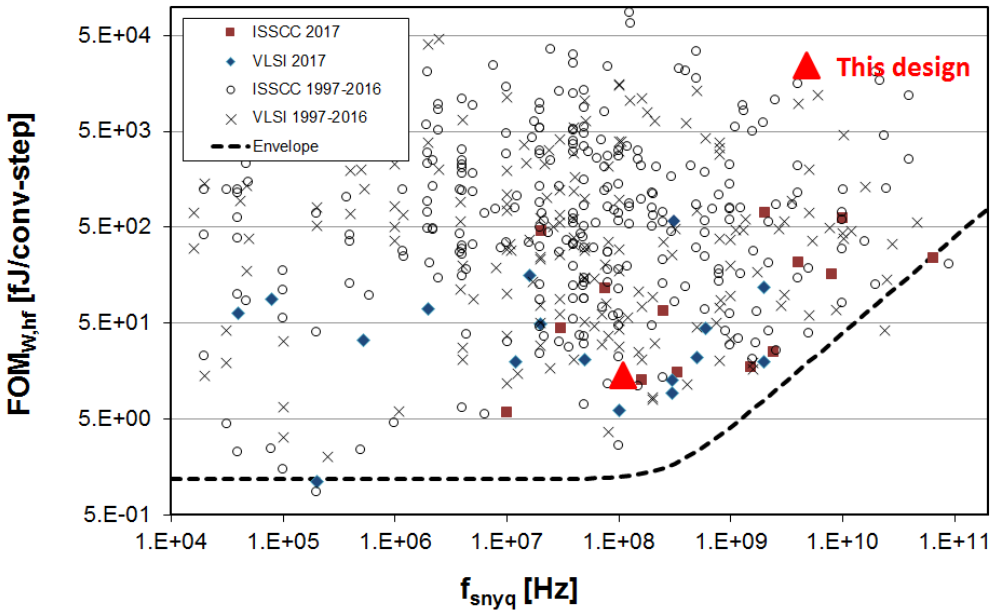




- Power consumption

Module name	Power (mW)
The whole chip	4.0
Reference buffer module	0.25
SAR ADC Core Module	1.0
Other modules (CLK gen.)	2.75

FOM=21.3fJ/conv.

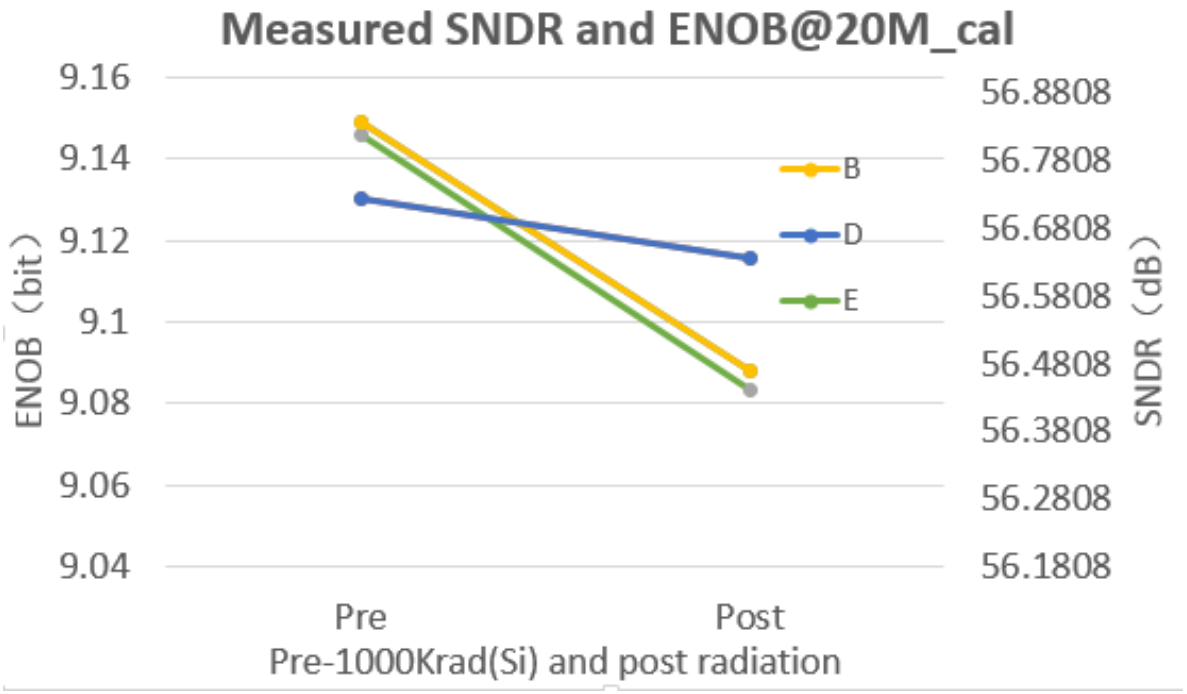


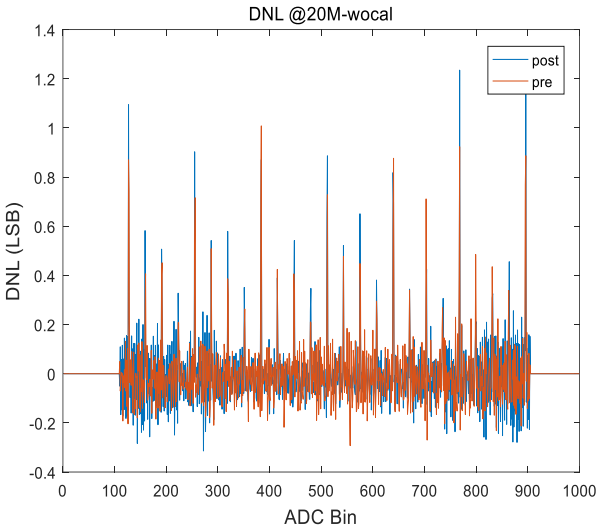
B. Murmann, ADC Performance Survey 1997-2017, [Online].Available: http://web.stanford.edu/~murmann/adcsurvey.html

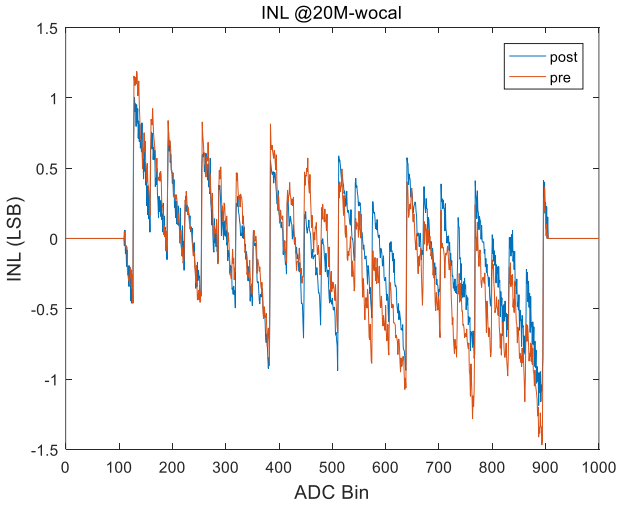
SAR ADC TID Test

- Test setup:
  - Radiation Source: Co-60
  - Does rate: 50rad(Si)/s
  - TID: 1Mrad (Si)
  - Sample no.: 3
  - Chip working condition: CLK=50M, fed with 2.4MHz sine input signal

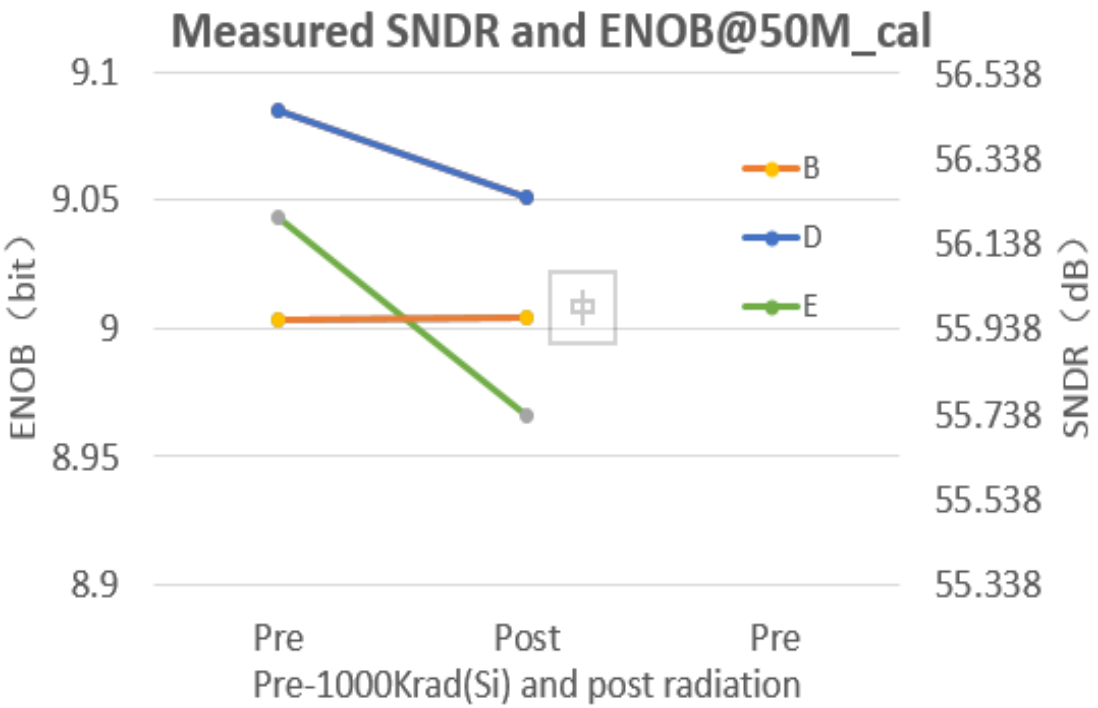
- Performance @ 20 MS/s

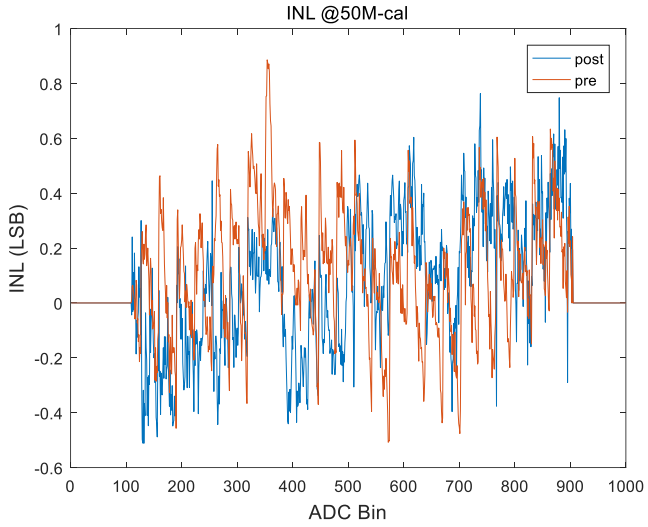


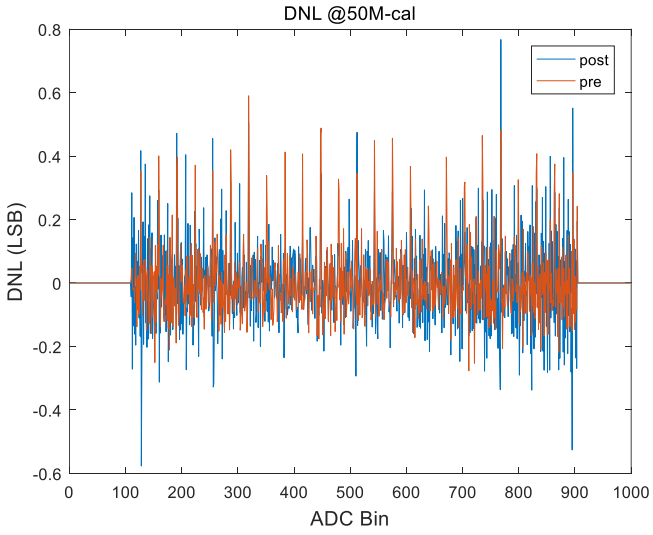




- Performance @ 50MS/s



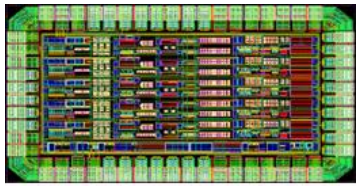




Summary

- A low power TPC readout ASIC are being developed
  - Using more advanced 65nm CMOS process
  - Adopting circuit structure with simple analog circuits: CR-RC shaper and SAR ADC
- Current progress:
  - First prototype chips has been designed and fabricated, The AFE and SAR ADC chips were evaluated and the tested results in good agreement with the specification, with power consumption of 2.18mW and 1mW respectively
  - TID radiation effect for the SAR ADC was also evaluated. No significant performance degradation was observed after 1 Mrad (Si) total ionizing dose radiation

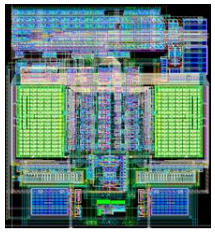
AFE



1320um x 838um

	Specifications	Test Results
Gain	10mV/fC	10.5mV/fC
Dynamic Range	120fC	>120fC
INL	<1%	0.41%
Power consumption	2.50mW/ch	2.18mW/ch
ENC	500e @ 10pF	448e @ 10pF
Xtalk	<1%	<0.36%

SAR-ADC

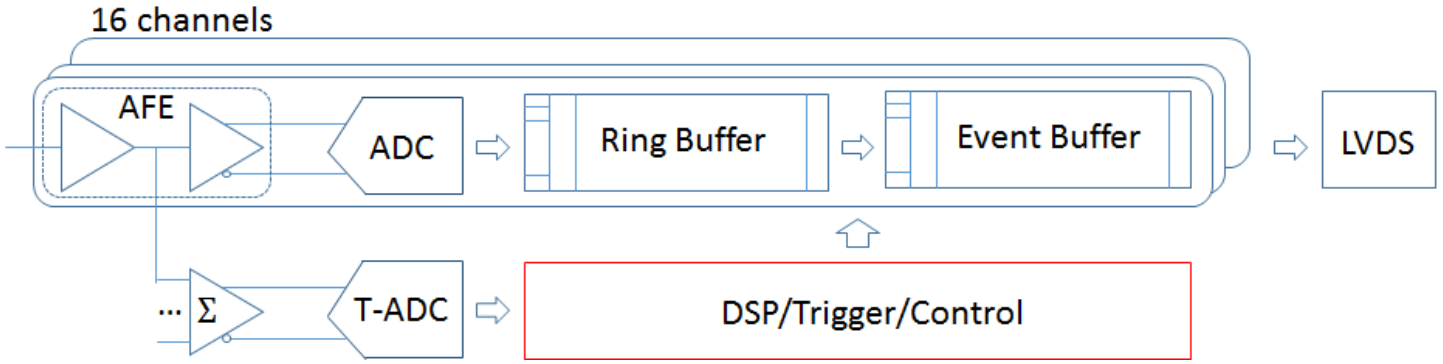


90um x 97um

	Specifications	Test Results
Sampling rate	40 MSPS	50 MSPS
Resolution	10 bit	10 bit
INL	<0.65 LBS	<0.5 LSB
DNL	<0.6 LSB	<0.5 LSB
ENOB	>9 bit	9.18 bit
Power consumption	<2.5 mW/ch	1 mW/ch

Future Plan

- Chip evaluation:
  - Full function prototype chip
  - TID test of the AFE chip
- Chip design:
  - Low power digital filter and data compression
  - High speed serial link
  - 16 channel prototype TPC readout ASIC



Thanks!