



环形正负电子对撞机
Circular Electron Positron Collider



中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Readout of JadePix-1, A Prototype CMOS Pixel Sensor for CEPC Vertex Detector

Jia Tao^{1,2}(reporter), Na Wang^{1,2}, Ke Wang^{1,2}, Liejian Chen^{1,2}, Ryuta Kiuchi^{1,2}, Hongbo Zhu^{1,2},
Ying Zhang^{1,2}, Xiaocong Ai^{1,3}, Yi Liu³, Chenfei Yang⁴, Xin Shi^{1,2}, Zhenan Liu^{1,2}, Qun Ouyang^{1,2},
Xinchou Lou^{1,2}

¹Institute of High Energy Physics, CAS

²State Key Laboratory of Particle Detection and Electronics

³Deutsches Elektronen-Synchrotron DESY

⁴University of Science and Technology of China

CEPCWS2018 Nov 13, 2018 Beijing

Outline



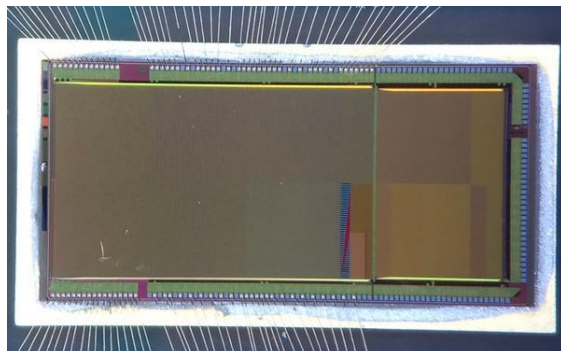
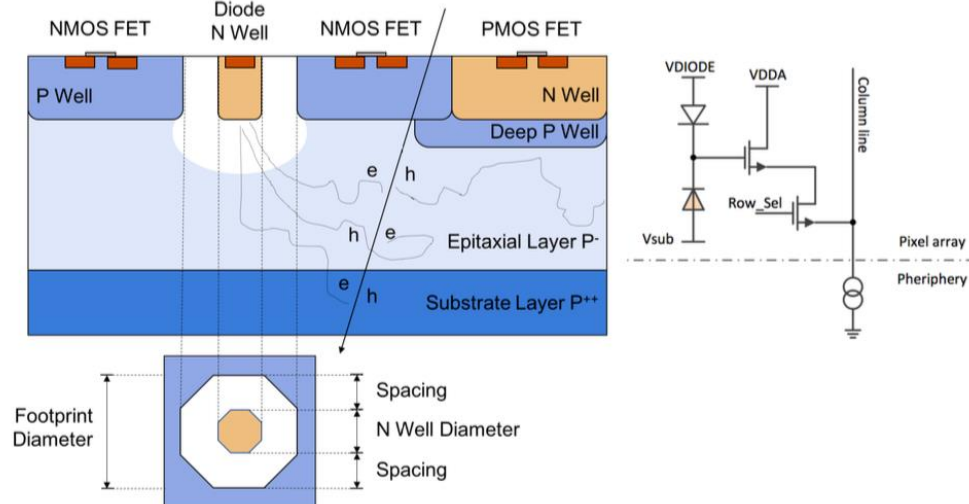
- Background and requirements
- Readout system
- Some test results of JadePix-1
- Conclusion

Background

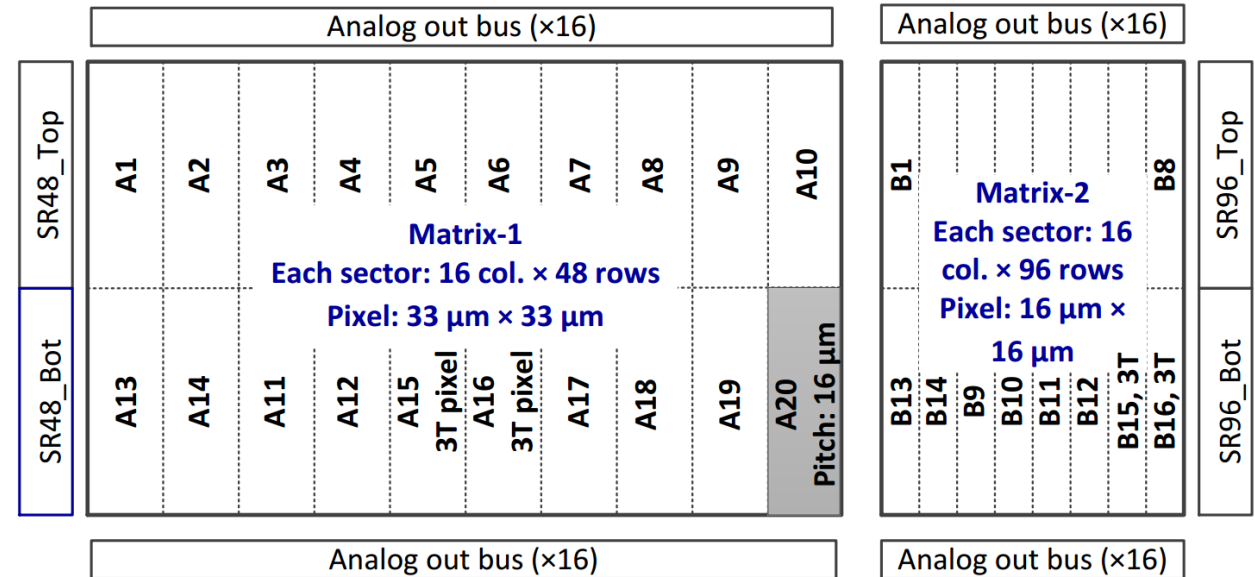


CMOS pixel sensor goals:

- Spatial resolution 3-5 μm
- Power consumption < 100mW/cm²
- Integration time 100 μs



JadePix-1



- TowerJazz 0.18 μm CIS process
- Two independent matrices
 - Matrix-1 16 $\times$ 48 pixel/sector 33 x 33 μm^2
 - Matrix-2 16 $\times$ 96 pixel/sector 16 x 16 μm^2
- Variation of the structure
- Rolling Shutter(in-pixel)——2/4MHz~24 μs /frame
- All channel analog output

Requirements and plan

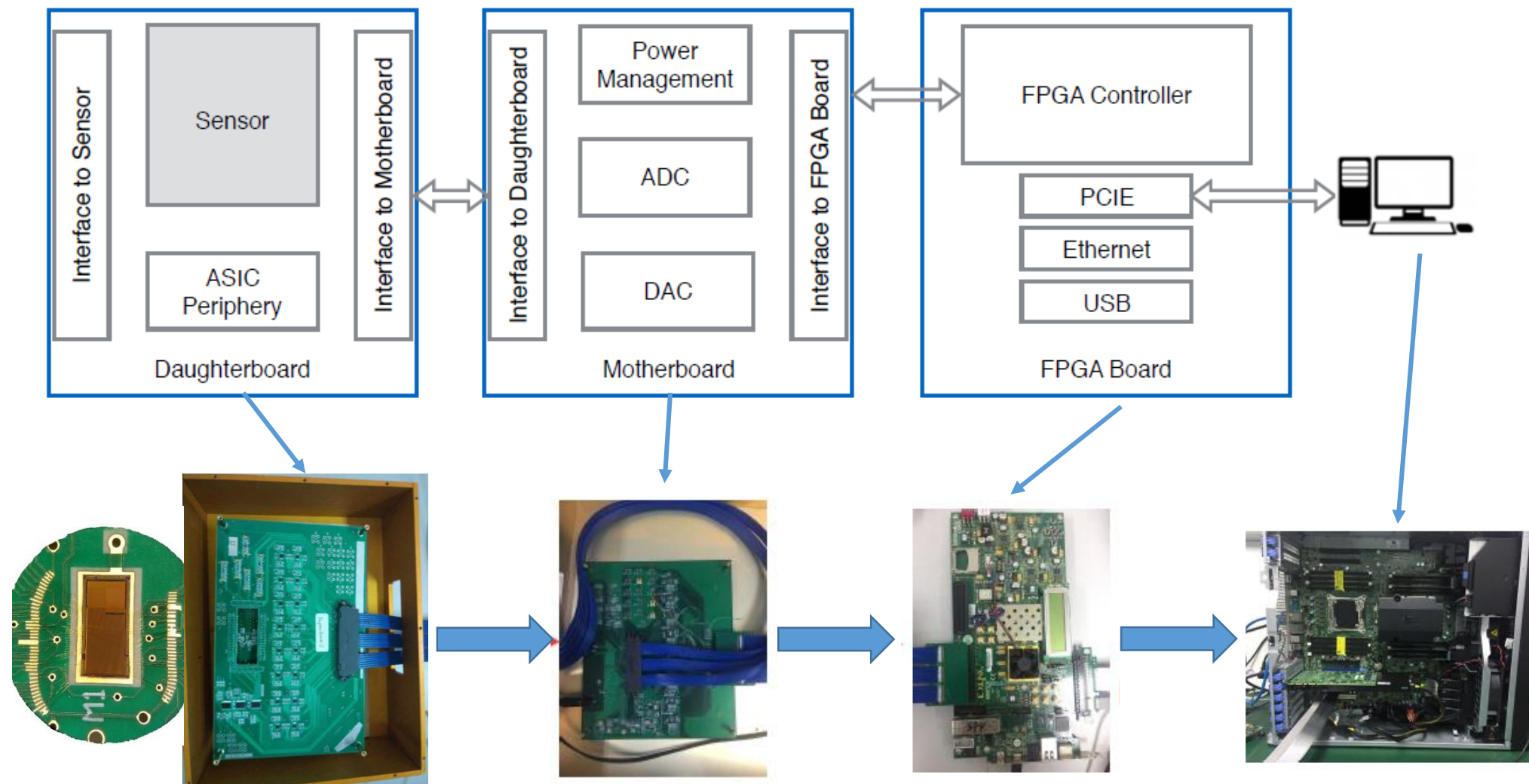


- Small analog signal output — **Amplification + analog to digital conversion**
- $16 \times 48/96$ pixels/sector — **16 channels + readout rolling shutter signals and package into frame**
- High spatial resolution — **Low noise design, noise $< 5e^-$ + correlated double sampling**
- Transmission rate requires 160MB/s — **High speed transmission to host PC**
- Applied to different structure sector — **Integrate all control functions + bonding board**

.....



“Three-Part” structure hardware design



inspired by the Mimosa sensor readout system developed by IPHC

Design of Daughter Board

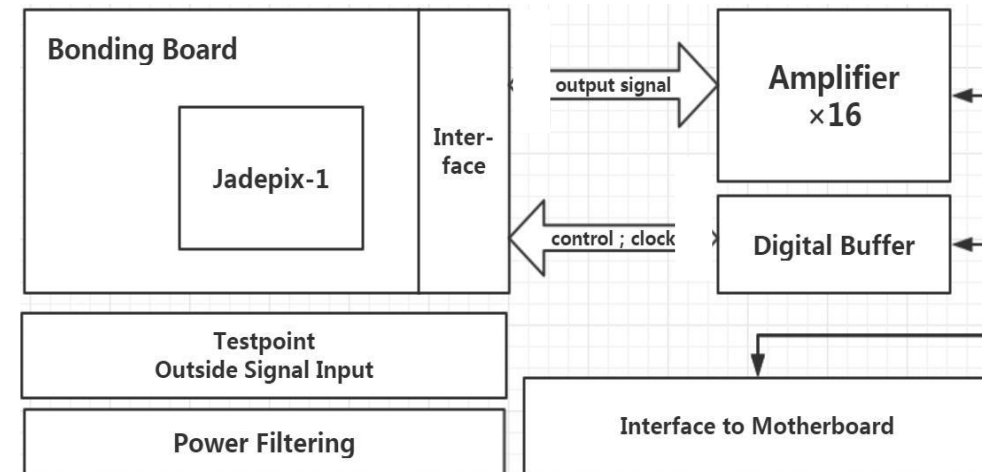


Daughter Board

	10MHz	100MHz
ADA4807	0.59 ENC	1.025 ENC
AD8065	0.82 ENC	1.164 ENC

Noise simulation result for op amp(using Pspice model)
(horizontal: device, Vertical: filter frequency)

The filtering frequency is about 10MHz
Low noise, no significant impact on signal



Architecture diagram of DB

- Daughter Board and Bonding Board are divided
- 16 channels analog signal readout
- 8 times amplification, single signal converted to differential signals
- Enhanced digital signal drive capability by buffer
- Devices are not sensitive to radiation, have long transmission line drive capability and are independent

Drive capability



- Long transmission line: 10 m
- Stable signal when sampling: requires rise time of signal within one-tenth cycle

Slew rate:

$$SR = 2\pi f V_p$$

$$V_p = 500 \text{ mV}$$

<500mV in fact

$$SR = 6.28 \text{ V}/\mu\text{s}$$

$$f = 2 \text{ MHz}, \quad T = 500 \text{ ns}$$

Analog Bandwidth:

$$Tr < 50 \text{ ns}$$

$$Bw = 0.35 / Tr$$

$$Bw \geq 7 \text{ MHz}$$

Current:

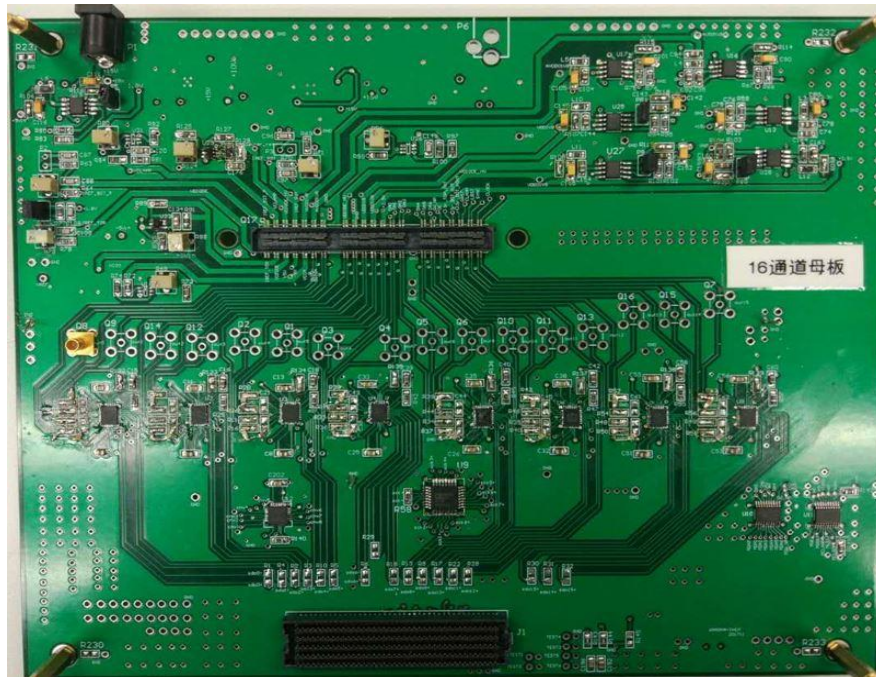
In terms of lumped parameter method

$$SR = I / C_{total}$$

$$C_{total} = C_{wire} + C_{cap} = 130 \text{ pF} + 470 \text{ pF} = 600 \text{ pF} \quad \text{regardless of resistance}$$

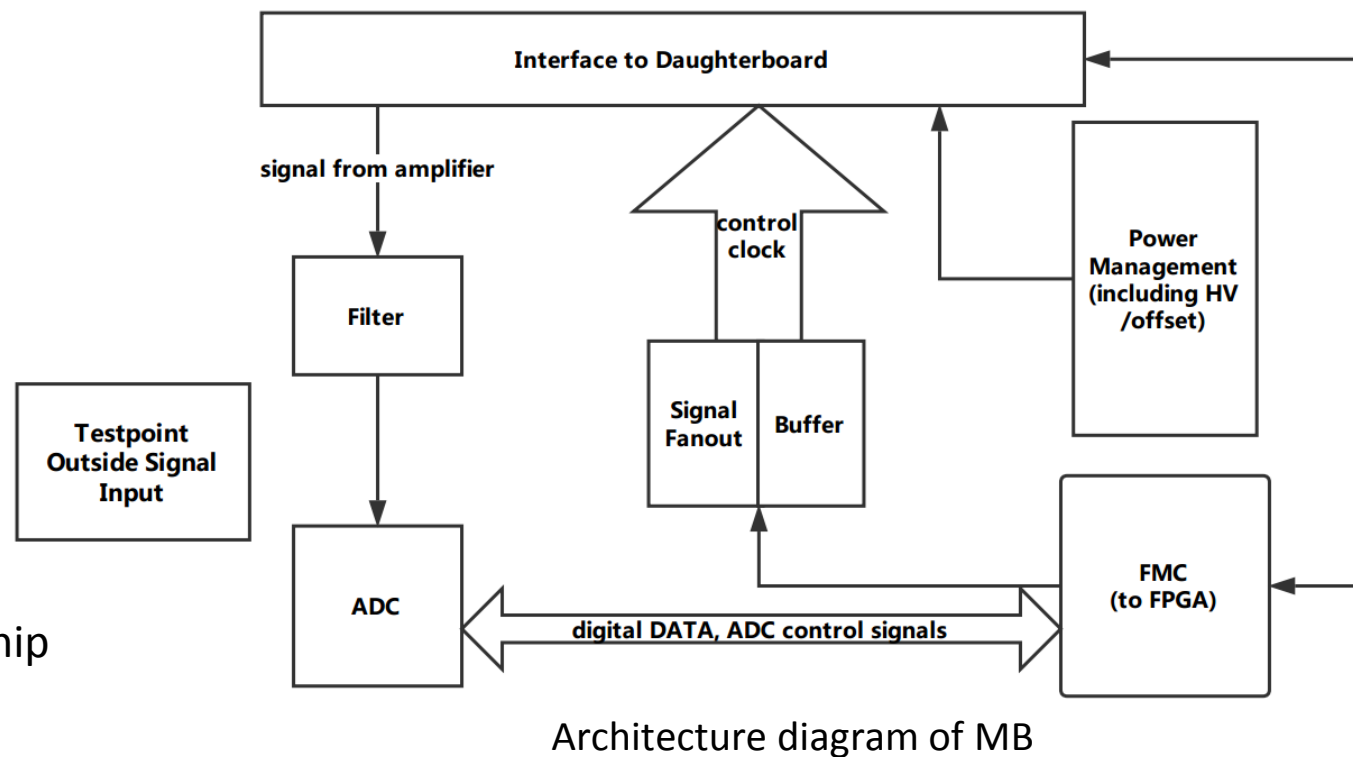
$$I = 6 \text{ mA}$$

Design of Mother Board



Mother Board

- Enough interface for different sectors of the chip
- High frequency filtering
- 16 channels ADC:
 - 16 bit ADC
 - 1.25-5V adjustable dynamic range
 - 5 Msps
 - Adjustable reference voltage and digital level



Estimate of noise



The reference voltage of ADC $V_{ref} = 4.096V$,
 $1 \text{ LSB} = V_{ref}/2^{N-1}$

$N=16$,

ADC $1\text{LSB} \sim 0.125 \text{ mV}$

So, output signal of detector which 1 LSB responds to is
 $0.125 \text{ mV}/8 = 15.6 \text{ uV}$,

Estimated detector capacitance $C=5 \text{ fF}$,
in terms of $Q=CU$

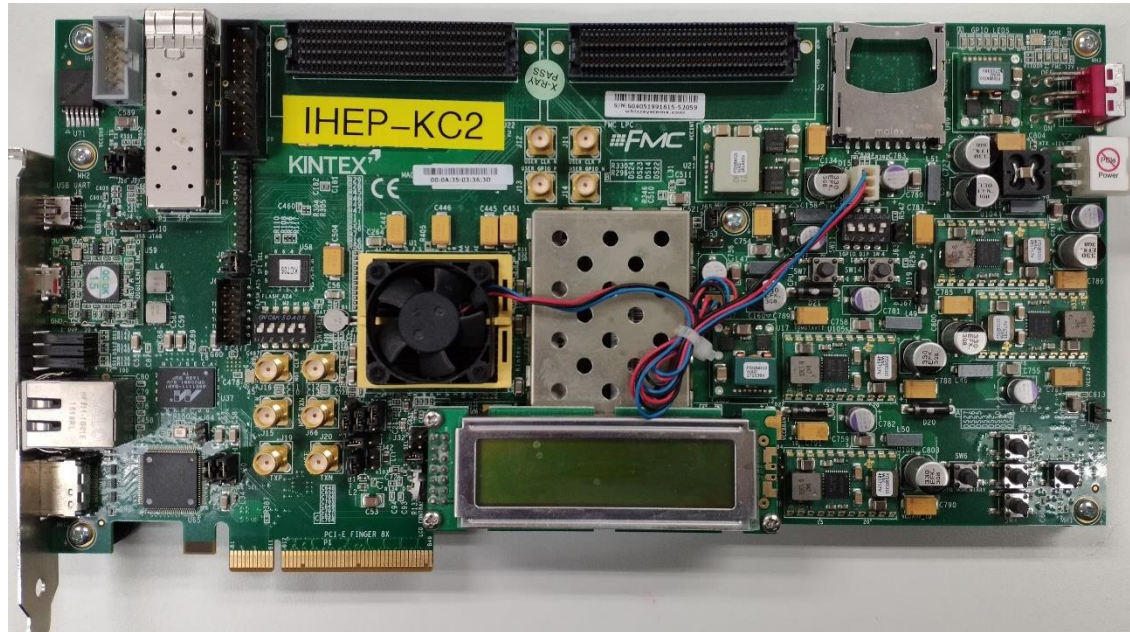
We can get the CVF (Charge convert to voltage factor) is about 31 uV/e
and $1\text{LSB} \sim 0.5 e^-$

ADC ENOB is 13bit , we can give a rough estimate:

The noise is

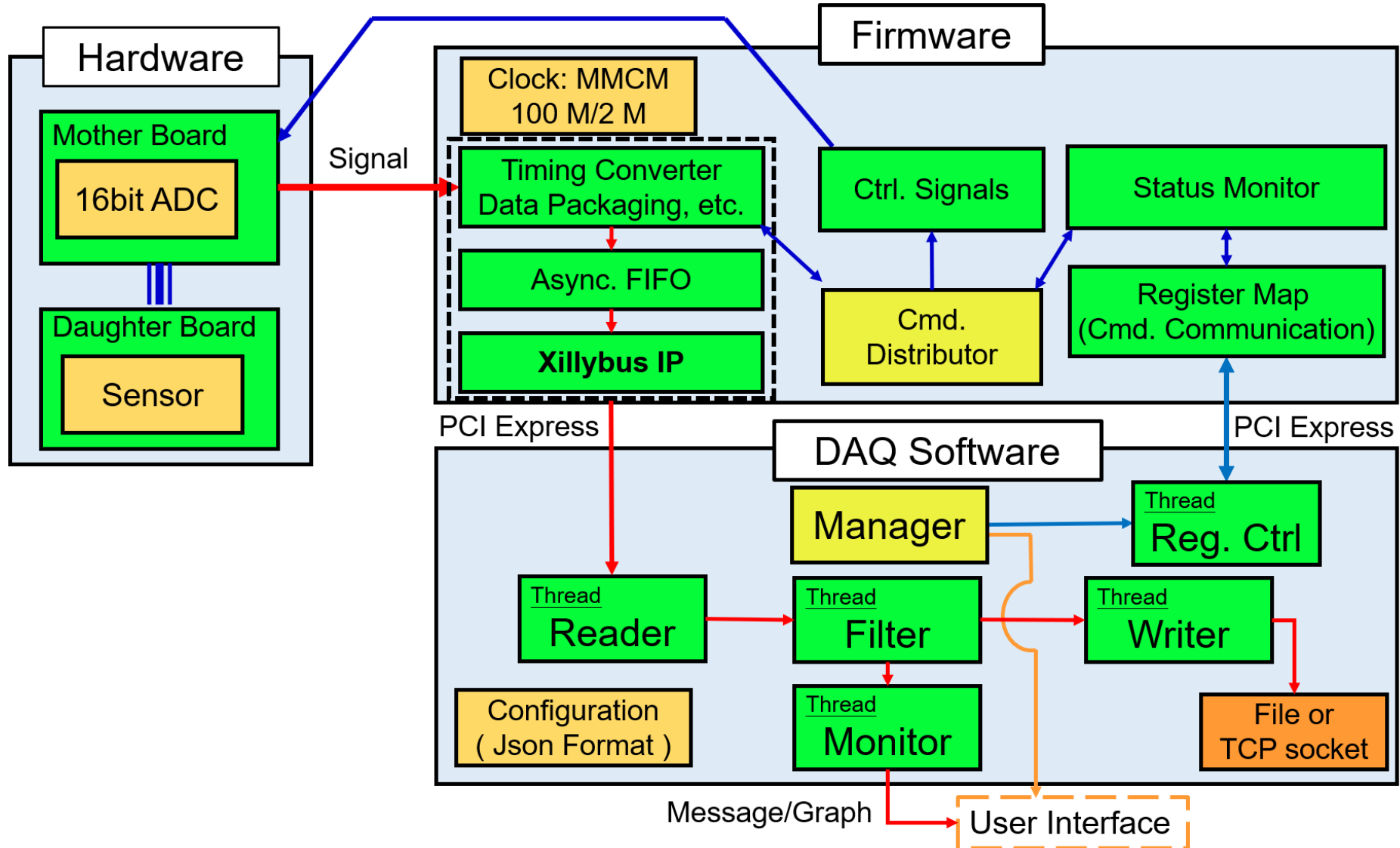
$$0.5 \times 2^3 = 4 e^-.$$

Xilinx KC705 evaluation board



- Commercial Xilinx KC705 evaluation board with good performance and mature technology meets the requirements and shorten design cycle.
- Data transmission rate through PCIe reaches nearly 6Gbps

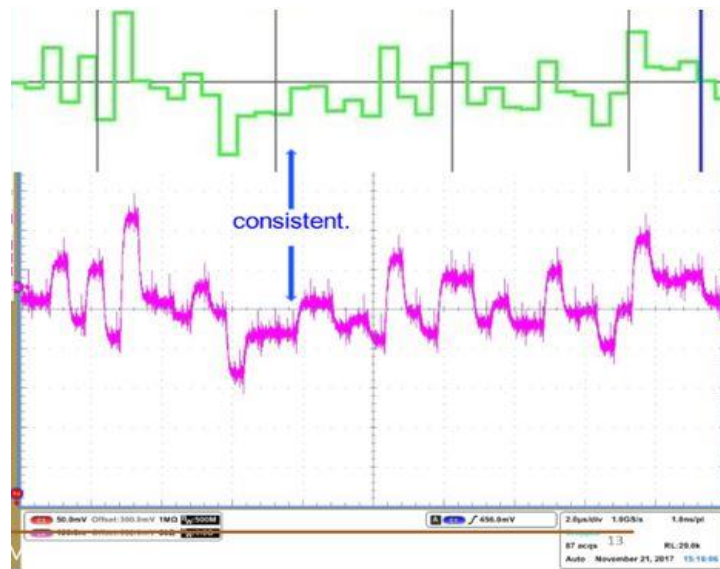
Firmware and software design



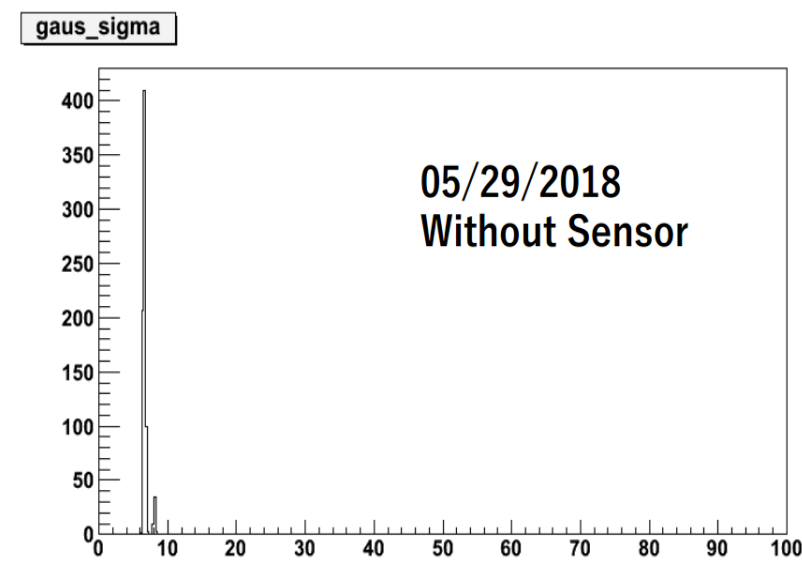
Test results



Radioactive source test

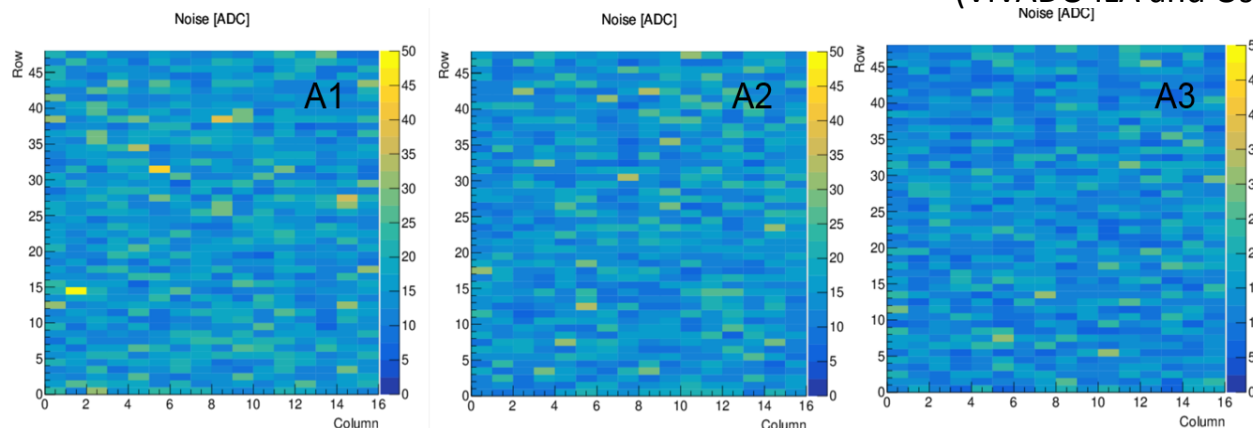


JadePix1 Output waveform comparison(after amplified)
(VIVADO ILA and Oscilloscope)



System noise distribution without chip

Sigma $\sim 170\mu\text{V} \sim 3.5e^-$



ENC $\sim 7.5e^-$

ENC $\sim 8e^-$

ENC $\sim 10e^-$

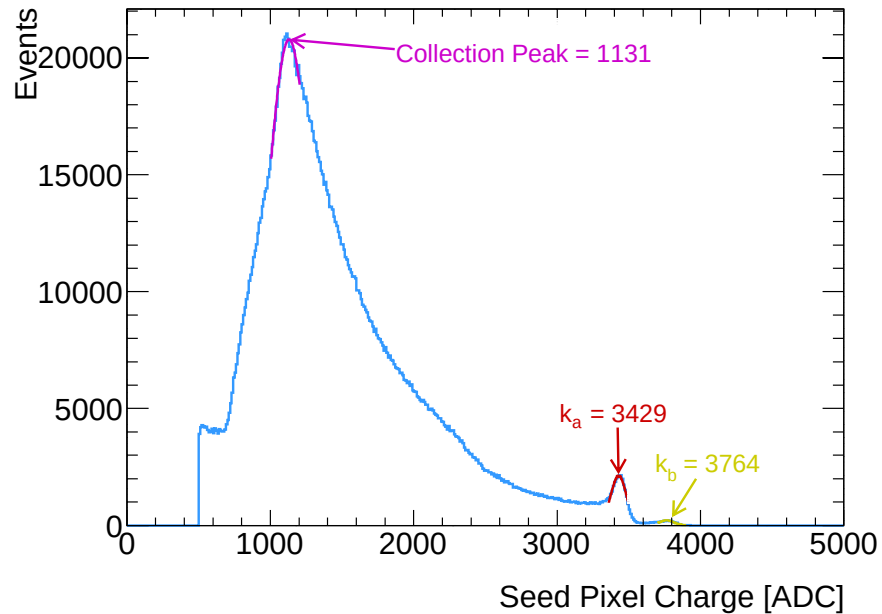
$$\sqrt{Noise_{total}^2 - Noise_{system}^2} = \sqrt{10^2 - 3.5^2} = 9.4e^-$$

The electronics noise of readout system has little effect on the sensor.



Measurement with ^{55}Fe

$k_\alpha k_\beta$ peaks are clear, we can calibrate the pixel gain and calculate the noise based on this

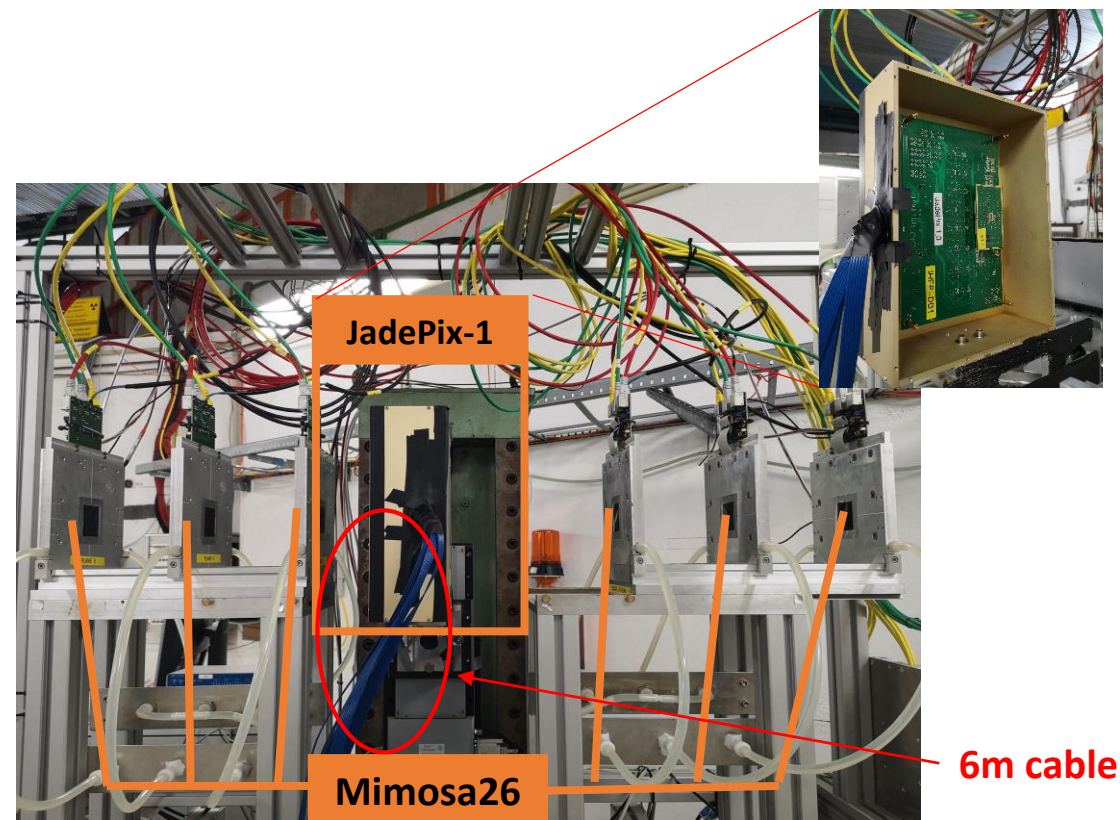
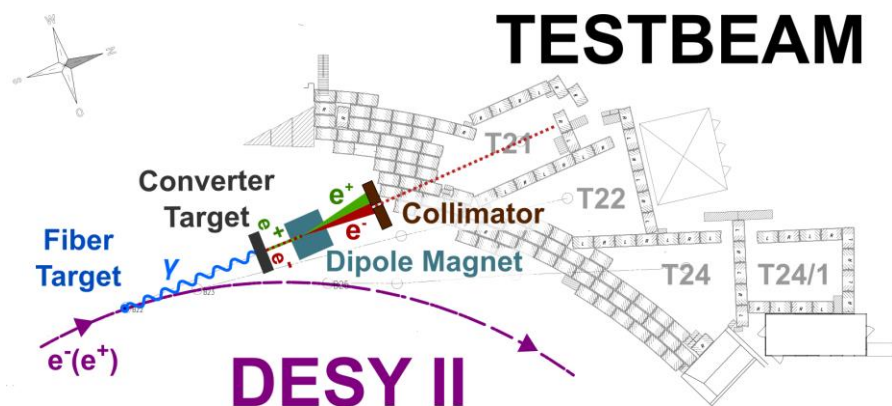


Sector	Collection peak [ADC]	k_α [ADC]	k_β [ADC]	Conversion gain [ADC/e]	CVF [$\mu\text{V}/e$]	CCE
A1	1131	3429 ± 54	3764 ± 50	2.091	31.9	32.97 %
A2	1035	3038 ± 39	3330 ± 46	1.852	28.3	34.06 %
A3	796	2198 ± 32	2412 ± 36	1.340	20.5	36.19 %
A4	1054	3514 ± 51	3864 ± 52	2.143	32.7	30.01 %
A5	883	2760 ± 40	3039 ± 37	1.683	25.7	32.00 %
A6	584	1689 ± 27	1853 ± 30	1.030	15.7	34.59 %
A7	970	3397 ± 55	3734 ± 54	2.071	31.6	28.57 %
A8	754	2458 ± 37	2705 ± 48	1.499	22.9	30.67 %
A9	553	1687 ± 28	1851 ± 32	1.029	15.7	32.81 %



Beam tests

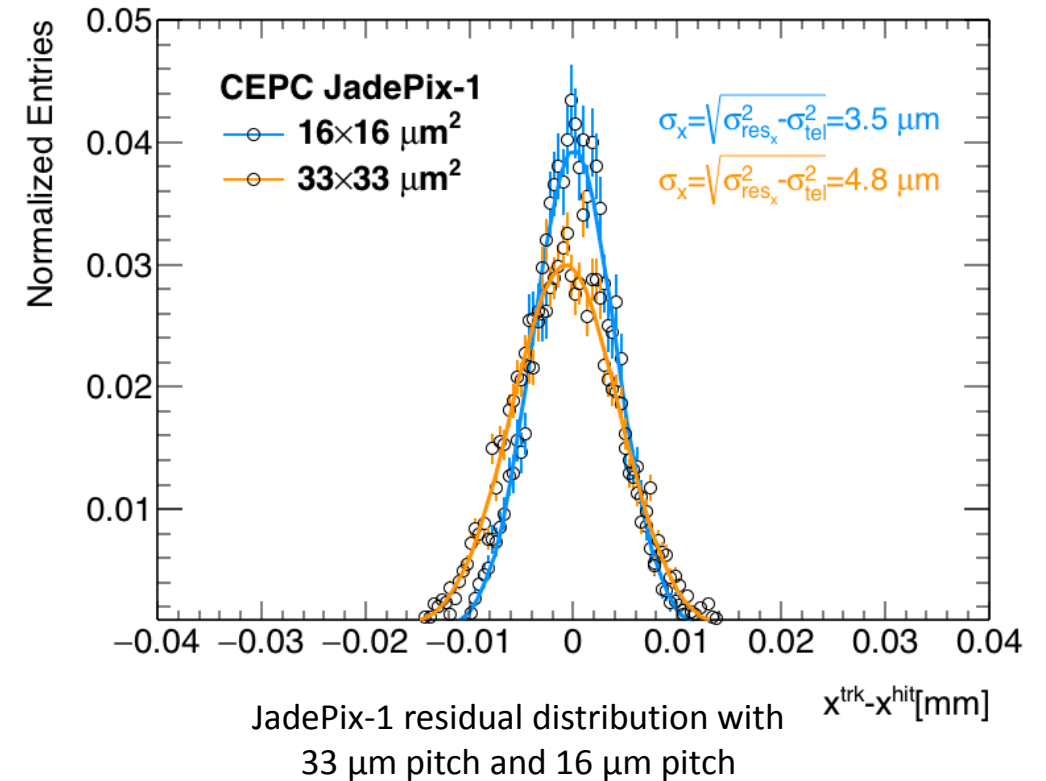
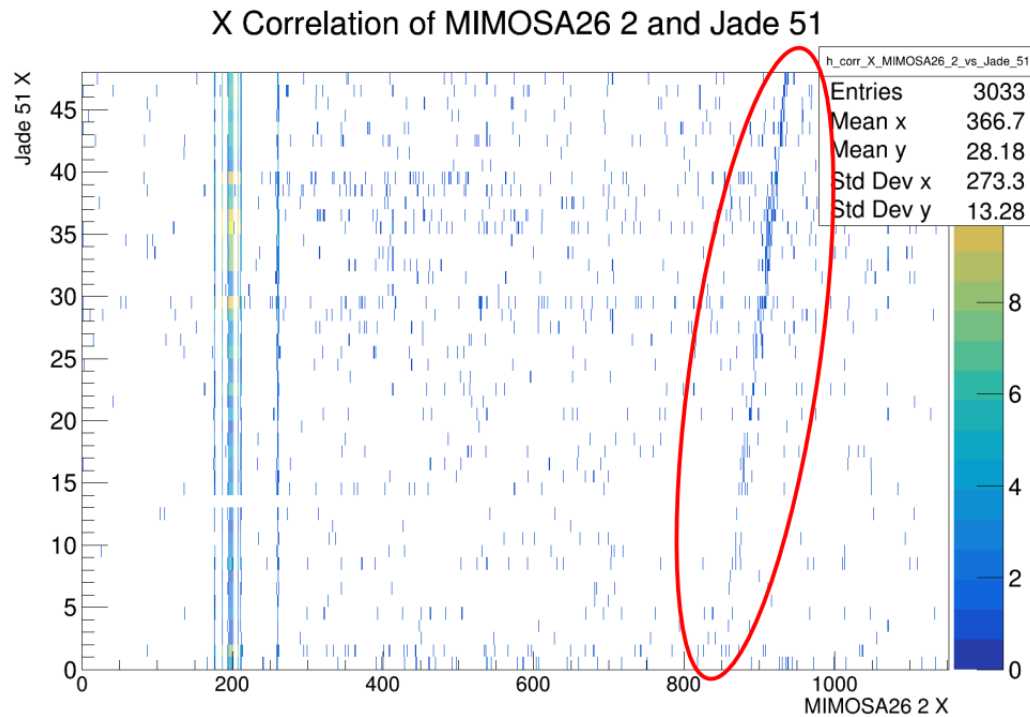
- To measure spatial resolution etc.
- 4.4GeV electron test beams @DESY
- EUDET telescope
 - reference plane (Mimosa26) with 2-3 μm resolution



Beam tests



Preliminary results show that spatial resolutions **better than $5\text{ }\mu\text{m}$ and $3.5\text{ }\mu\text{m}$** can be achieved for pixel sizes of $33\times 33\text{ }\mu\text{m}^2$ and $16\times 16\text{ }\mu\text{m}^2$, respectively.



Conclusion



- Have developed a readout system for CMOS pixel sensor prototype characterization
- Continue to evaluate JadePix-1 performance, e.g. radiation hardness
- System to be extended to support other sensors

Thank you for your attention!