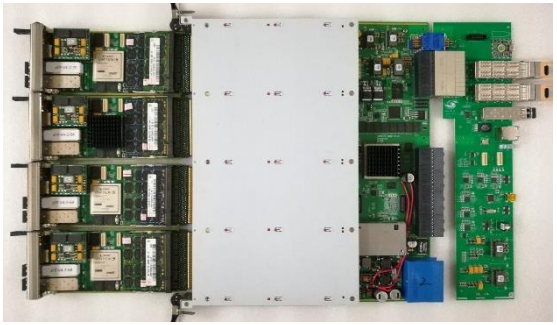
Hardware development for TDAQ



Jingzhou ZHAO[1], Zhen-An LIU[1], Wenxuan GONG[1], Pengcheng CAO[1], Wolfgang Kuehn[2]

1. Trigger Lab, Institute of High Energy Physics, Chinese Academy of Sciences
2. II. Physikalisches Institut, Justus-Liebig-Universität Gießen

CEPC2018, IHEP,Beijing

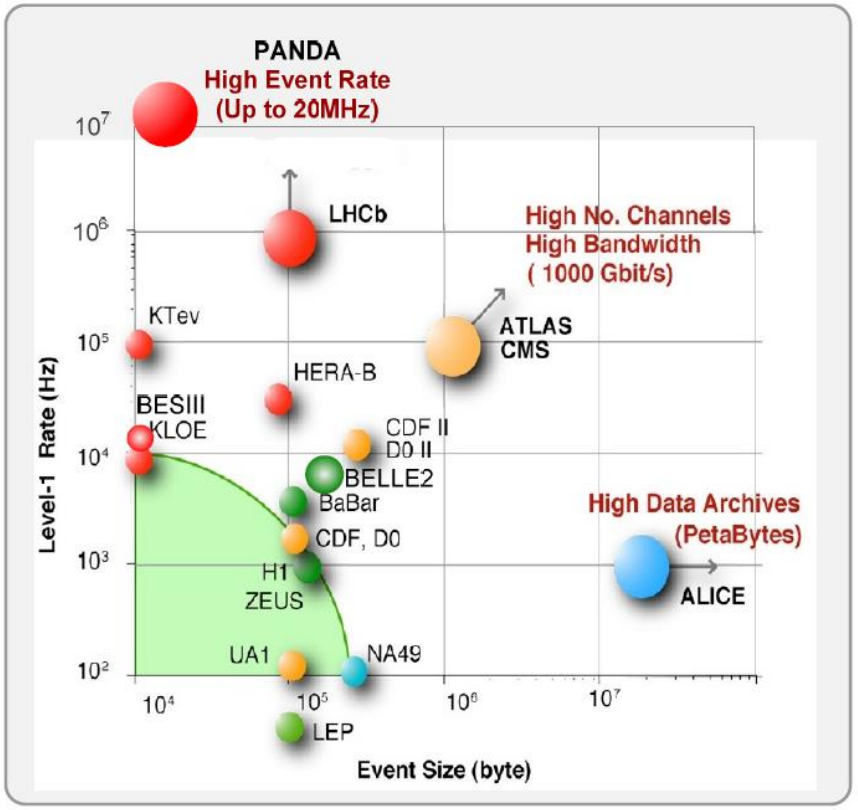
Outline

- Requirements to TDAQ system
- xTCA for Physics
- CN_V3 for Belle II PXD DAQ
- CN_V4 for PANDA DAQ
- CPPF for CMS trigger system
- summary

Requirements to TDAQ system

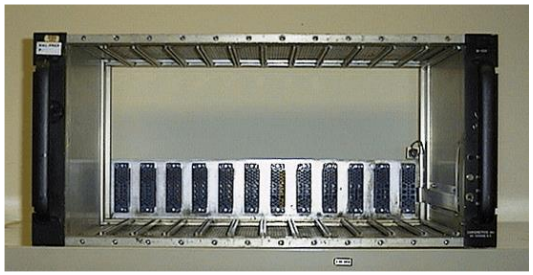
- Future Physical experiment accelerator and Spectrometer
  - High luminosity
    - CEPC(90-350GeV,
    - CEPC($10^{34}cm^{-2}s^{-1}$~$10^{35}cm^{-2}s^{-1}$)
  - High data event rate
    - CEPC(40MHz)

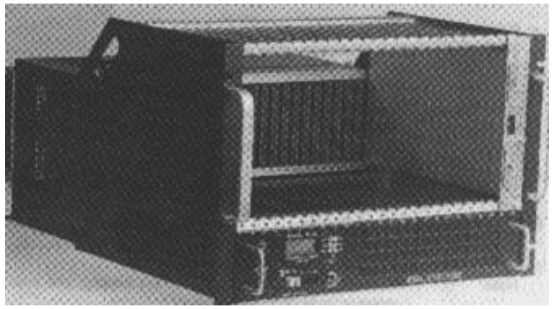
- Requirements to TDAQ system
  - High speed data transmission;
  - High performance data processing;
  - Mass data buffering

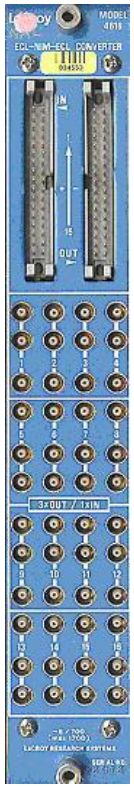


Standards for Nuclear Instrumentation

- 1960's
  - NIM: American Standard Beurea and NIM Module Committee
- • 70-80's CAMAC, FASTBUS, widely used
  - Nuclear Spectrum Measurement, Particle Physics, Medical Physics, Accelerator Instrument, Accelerator Control, Aerospace, Industrial control.
- ***• 90's VME from Industry***
- ***• 2000 CPCI***
- ***• Still in use, BUT limited by bandwith.***







xTCA for Physics

ATCA ->PIGMG3.8

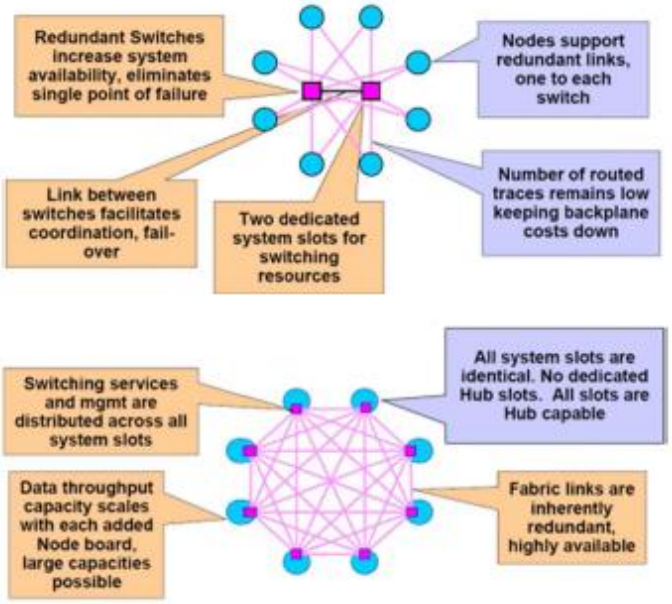
- – Advantages
  - • High speed IO and 10Gbps-25Gbps interconnections
  - • HA ~99.999%
  - • IP management
- – Add control signal

•MicroTCA (MTCA) ->MTCA 4.0

- – Advantages of ATCA
- – Half height, compact system
- – add rear transition board and control

• AdvancedMC（AMC）

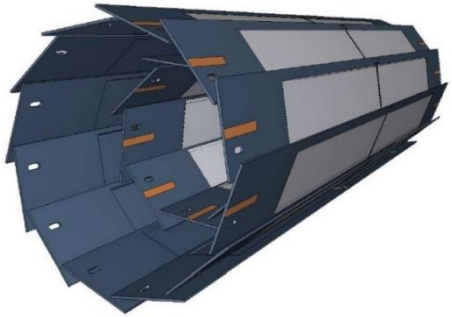
- – Modular design

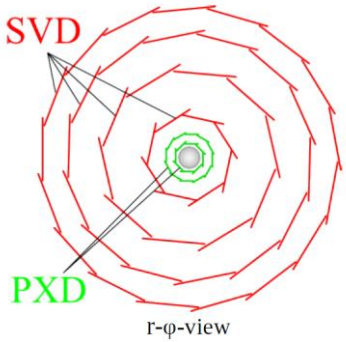


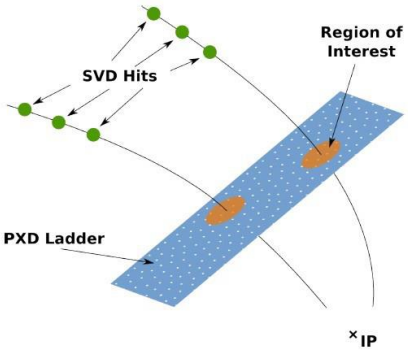
xTCA is the Next Trigger/DAQ standard

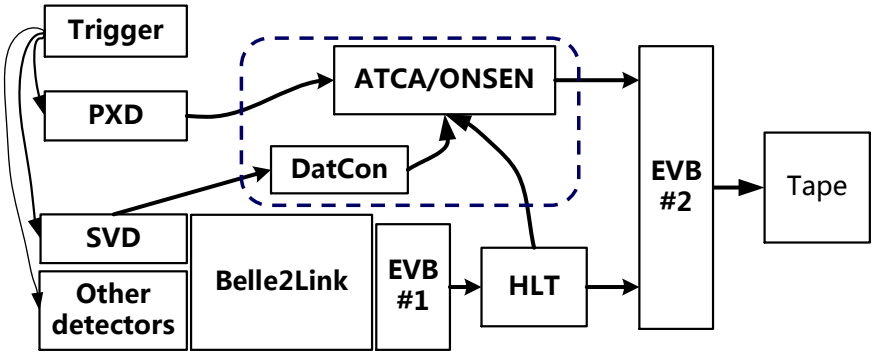
Compute Node for Belle II PXD DAQ

- PXD detector is a new detector in the upgrade of Belle II.
- Huge data output: ~200Gb/s.
- **PXD reduction**
  - Help with SVD track
    - 1/10
  - Tracking back
  - ROI searching
  - Data extraction
- **Difficulties**
  - Computing capability
  - Algorithms
  - 5s data buffer
- Data sharing between Processing node







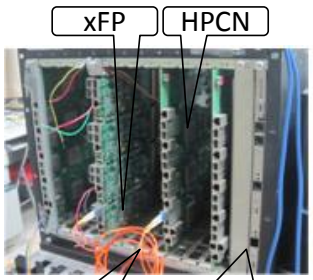


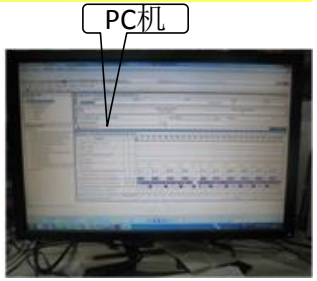
Compute Node for Belle II PXD DAQ

- High Performance FPGA is used for data processing,
- RocketIOs are used for high speed data transmission between data processing node,
- DDR is used for mass data buffering,
- ATCA/xTCA architecture is used for PXD DAQ,
- Intelligent platform management control system is used for system stable.

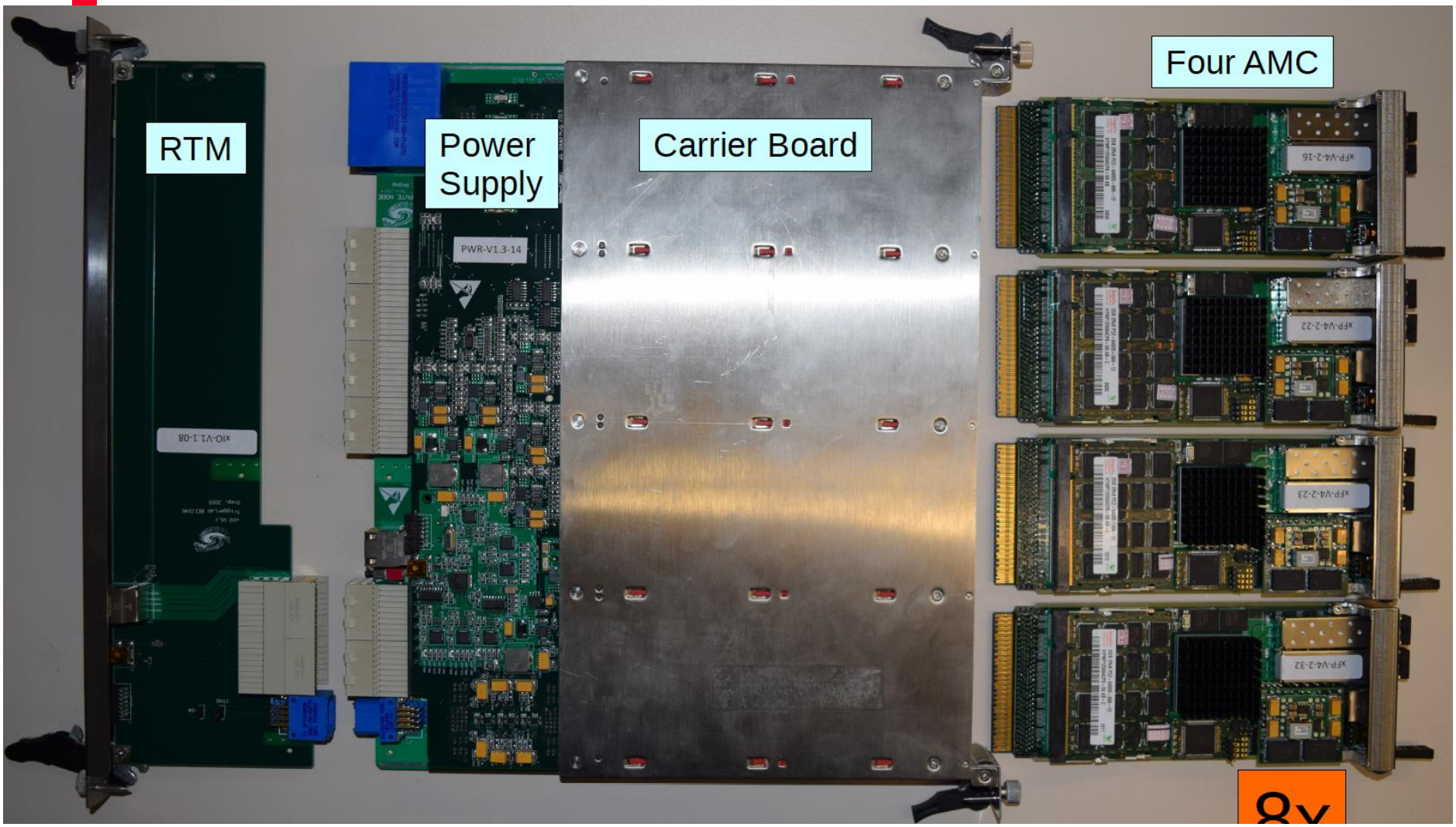
Key parts of PXD-DAQ

- ONSEN/PXD-DAQ
  - Firmware(Giessen Uni)
  - Hardware(IHEP Beijing)
    - 1 ATCA Shelf
    - 2 shelf managers
    - 1 Power Supply
    - 9 Compute Node(CN)
      - 1 ATCA Carrier(PICMG3.8)
      - 1 RTM
      - 1 Power Board
      - 4 xFP/AMC cards
      - 1 IPMC+ 4 MMCs



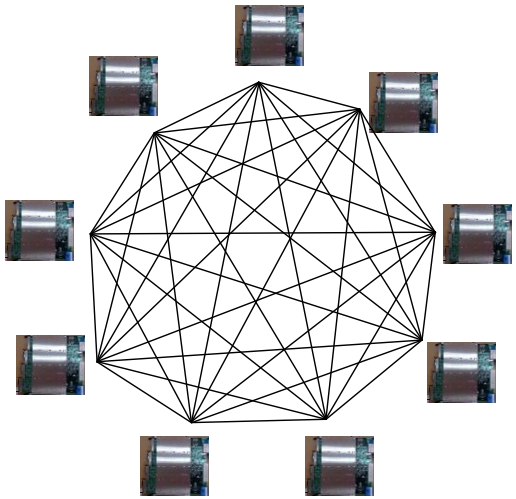


Full Compute Node for PXD DAQ

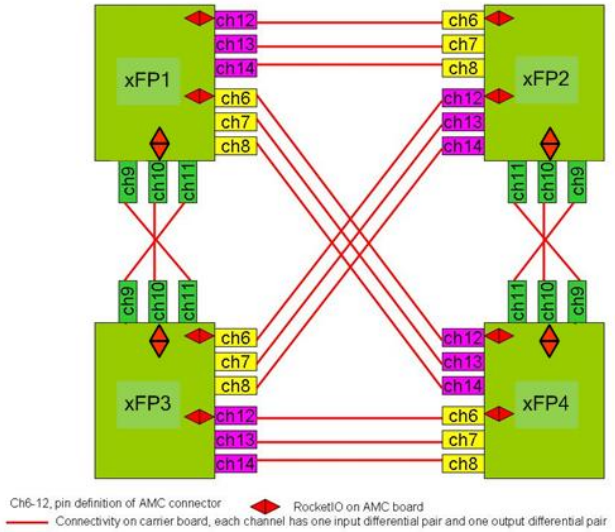


Full Mesh for PXD DAQ

- Full mesh backplane for CN data sharing with each node.
- Full mesh on board connection for AMC cards.
- Point to Point via one MGT channel,
- Line rate up to 3.125Gbps.



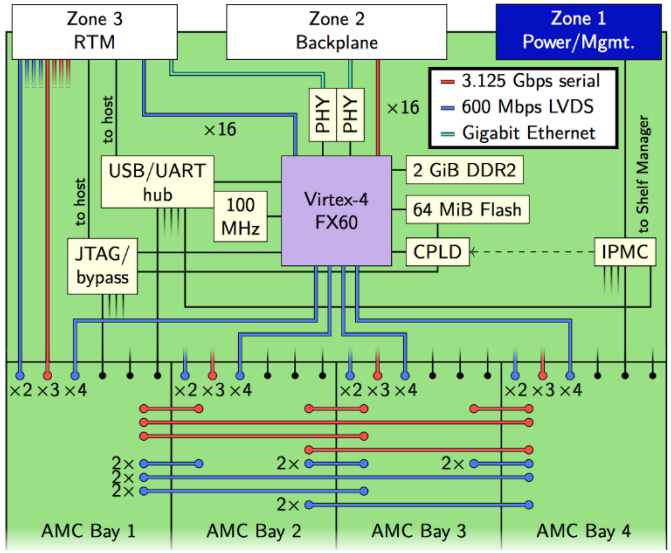
Full mesh backplane connection



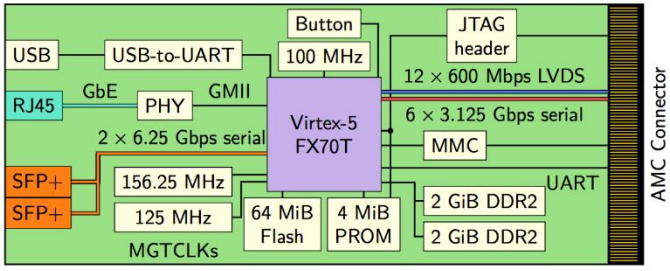
Full mesh on board connection for AMC

CNCB(CN Carrier Board)

- Function of CN Carrier Board V3.3
  - Virtex-4 FX60 with PowerPC405,
  - Embeded linux system for slow control,
  - 16 RocketIO channel connect to backplane,
  - 2GB DDR2,
  - 2 Ethernet ports,
  - IPMC



- Function of AMC
  - Virtex-5 FX70T with PowerPC440,
  - Embeded linux system for data management,
  - 2 SFP+ port, 6.25Gbps/ch
  - 4GB DDR2,
  - 1 Ethernet ports,
  - UART port,
  - MMC

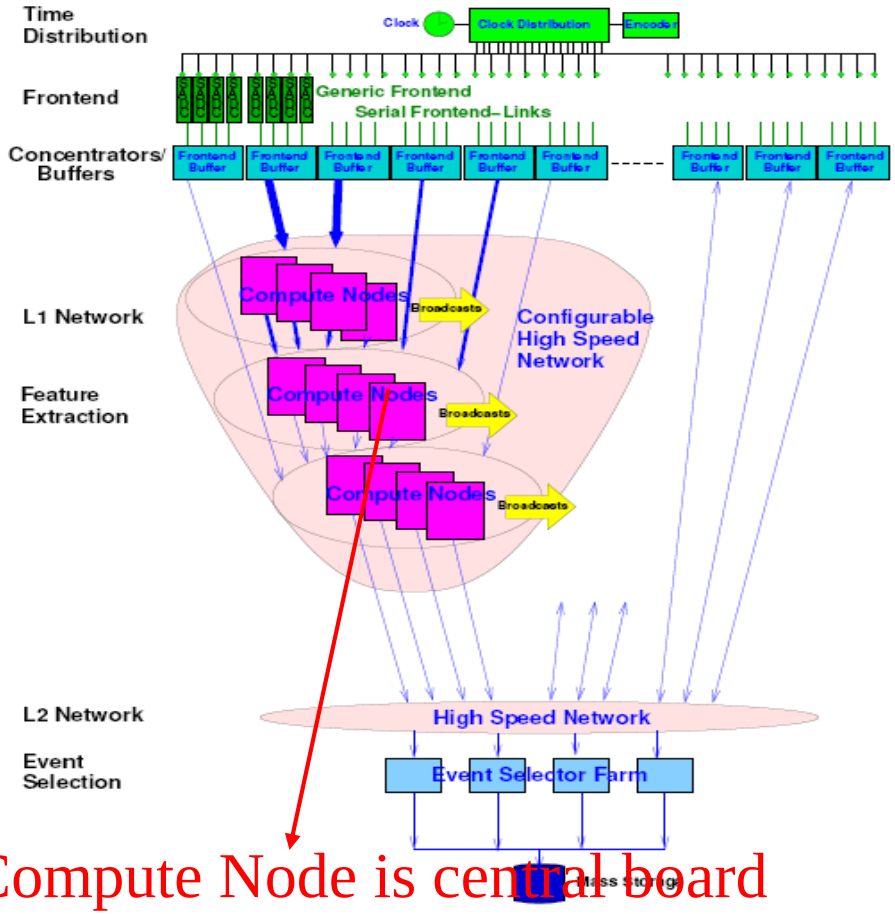


PANDA DAQ

Trigger-less streaming DAQ with event filtering

- High event Rate: up to 20MHz,
- Each event: 1.5Kbyte-4.5Kbyte
- Global time distribution for time stamping,
- L1 Network,
  - Extract particle information like energy, position, momentum and so on;
- L2 Network,
  - Make a preliminary reconstruction for physics events;
- Event selection will be done based on the research topics of PANDA experiment.

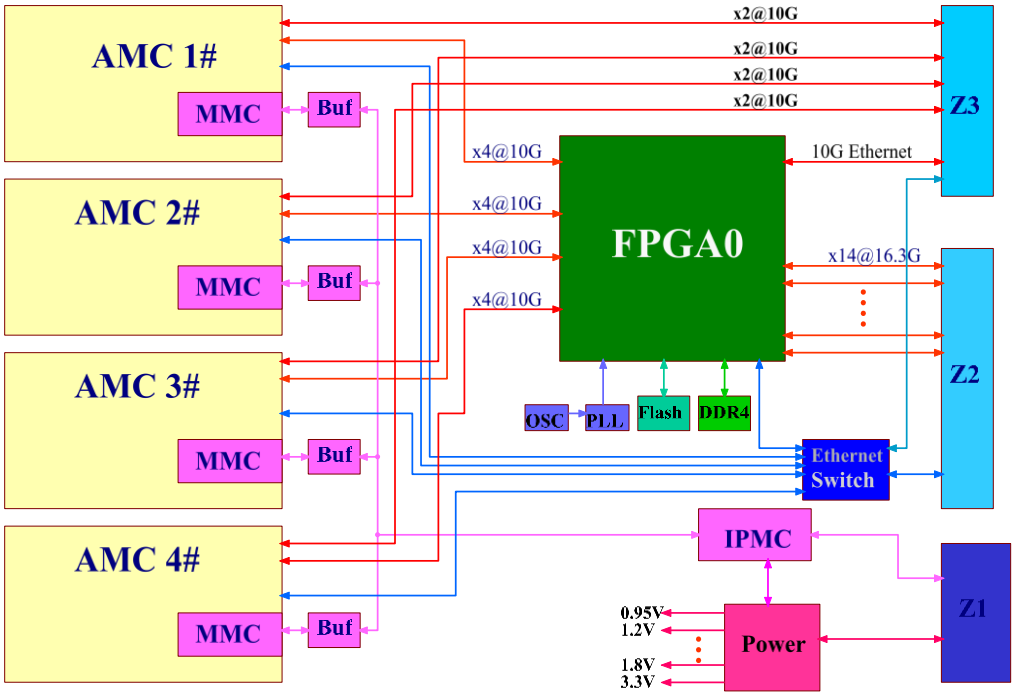
Please reference Wolfgang Kuehn's report



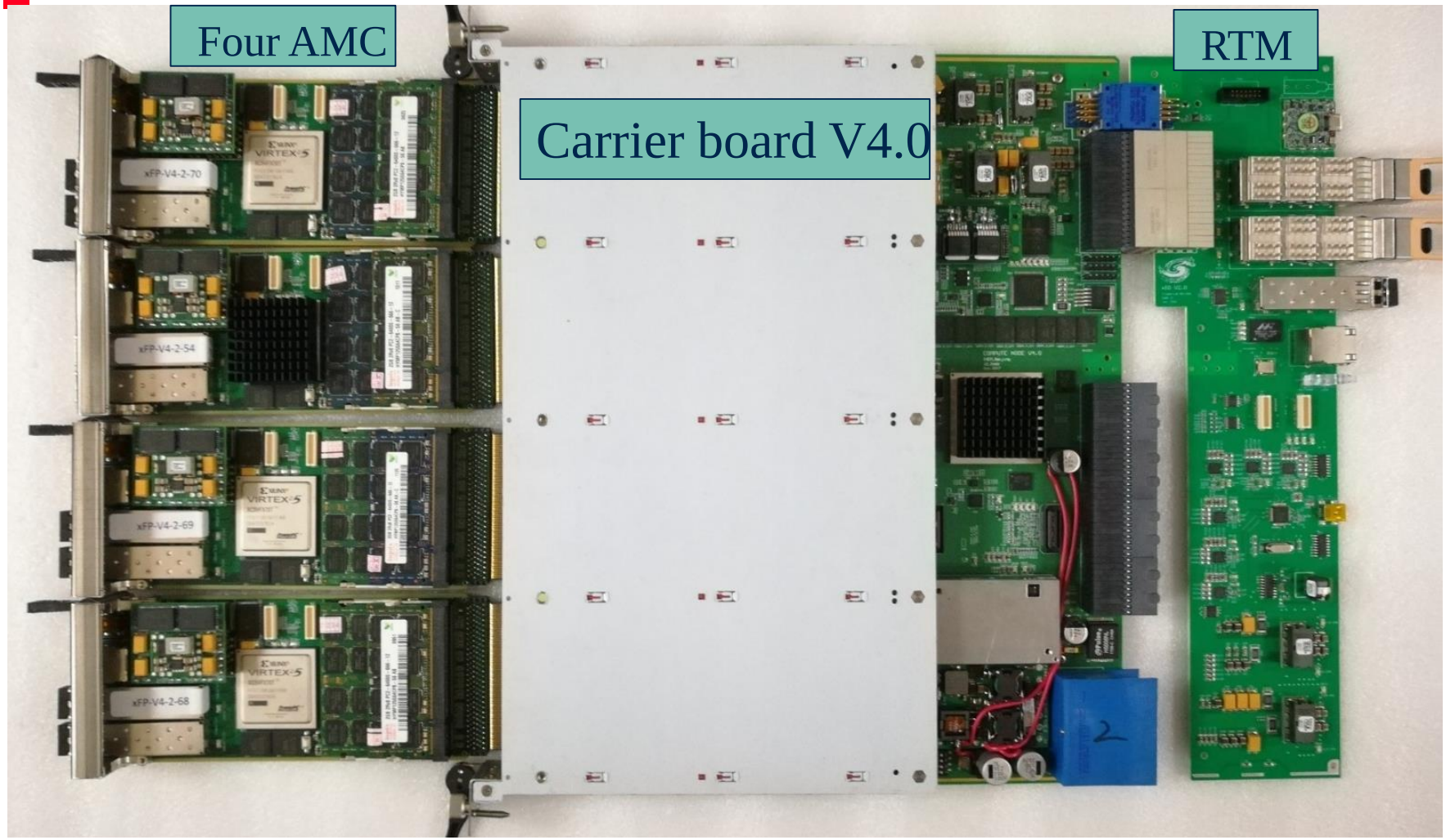
Compute Node is central board for PANDA DAQ.

Compute Node for PANDA

- **FPGA:** Ultrascale Kintex xcku060
- **RAM:** 16 GB DDR4 (8 chips)
- **MGTs:** 16.3 Gbps
  - 4 links to each AMC card;
  - 12 links to ATCA backplane;
  - 1 link to RTM (10G Ethernet);
- **GbE switch:**
  - 4 AMCs,
  - 1 switch FPGA,
  - 1 uplink to ATCA Base Interface
  - 1 RTM RJ45
- 10 Gigabit Ethernet to RTM(SPF+)
- **Configuration:** automatic from NOR Flash (master BPI)
- **Programmable MGT clock**
- CPLD as **JTAG hub**
- IPMC/MMC

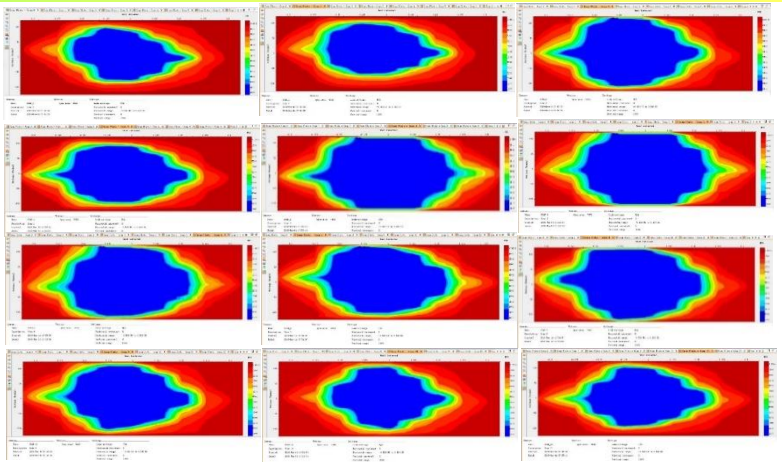


First Version of CNV4.0

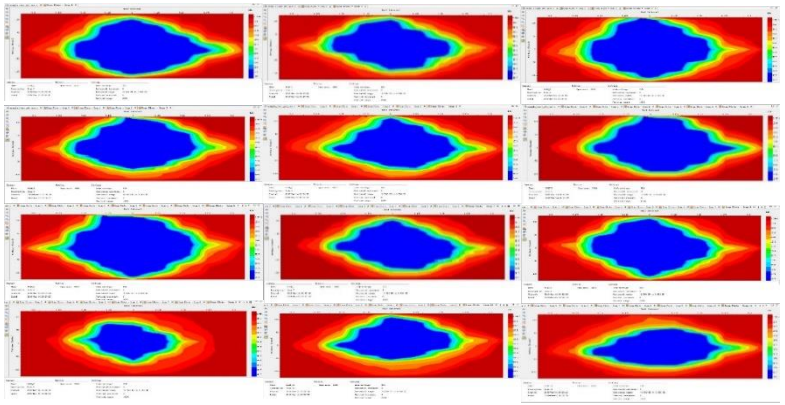


CN Backplane MGT channel test

- Crate:
  - Two ATCA Slots,
  - 12 Backplane channel point-to-point, connection between two slots,
  - 25Gbps/ch for Backplane connector.
- 24 hours, No error on 12.5Gbps.
- Error rate <1E-15.



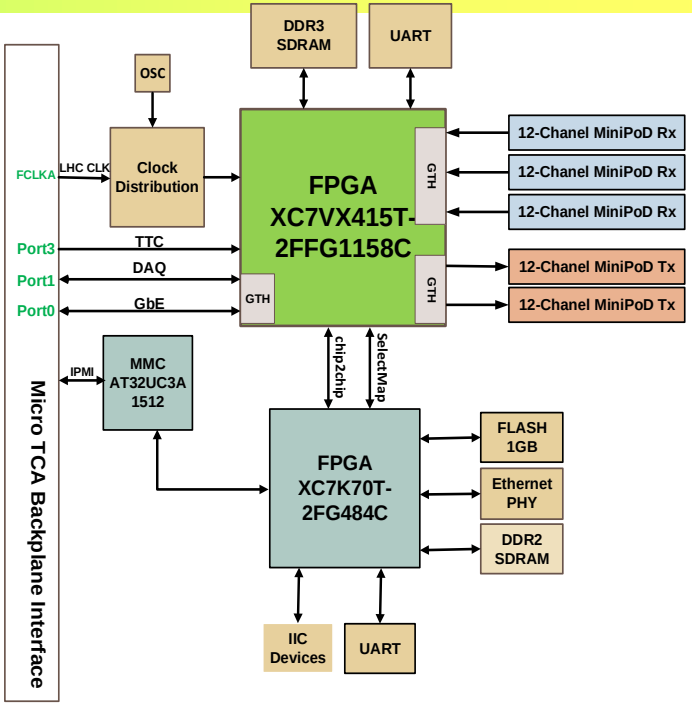
Backplane MGT 10G 12channel

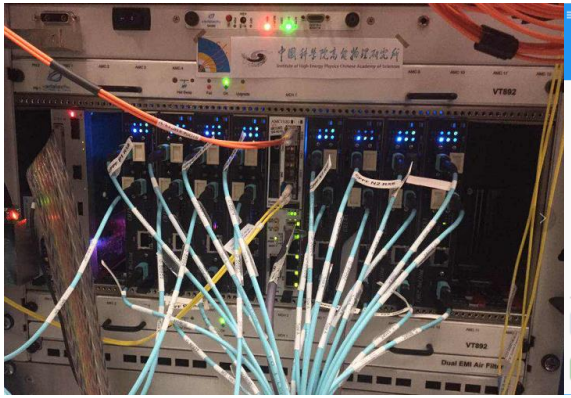


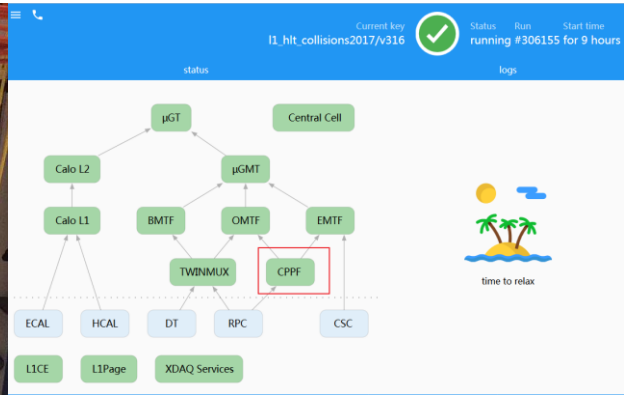
Backplane MGT 12.5G 12channel

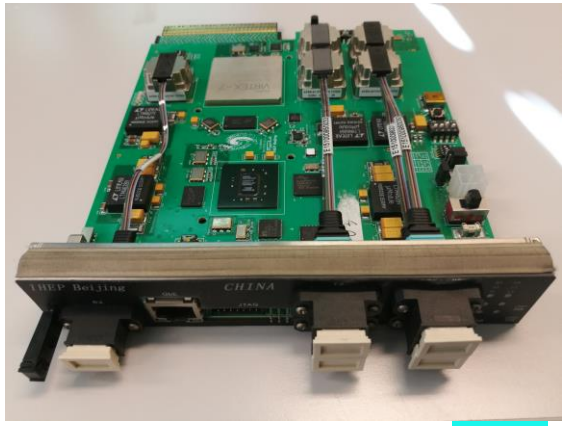
CPPF for CMS trigger system

- Based on MicroTCA protocol
- Two Xilinx FPGA chips for board controlling and functionalities implement
- 36 optical links input,
- 24 optical links output,
- Support 10Gbps/ch
- CPPF system was successfully integrated in CMS trigger system in May of 2017.









Summary

- xTCA is the Next Trigger/DAQ standard for physical experiment.
- CN V3 is designed and successful used for Belle II PXD DAQ.
- CN V4 is designed successfully for PANDA DAQ.
- New Compute Node will be designed for CEPC TDAQ according to requirements.

Backup

Belle II PXD data rate

average occupancy	1%	
maximum occupancy	3%	(A. Moll: inner ≈ 1%, outer ≈ 0.5%)
average cluster size	2	(A. Moll: ≈ 2.281)
pixel per half ladder	$0.192 \cdot 10^6$ pixel	250 · 768 Pixel
number of half ladder	40	
pixel full PXD	$7.68 \cdot 10^6$ pixel	$40 \cdot 0.192 \cdot 10^6$ Pixel
average fired pixel rate (half ladder)	$43.6 \cdot 10^6$ Hz	$0.192 \cdot 10^6$ pixel · 22.7 kHz · 1%
maximum fired pixel rate (half ladder)	$131 \cdot 10^6$ Hz	$0.192 \cdot 10^6$ pixel · 22.7 kHz · 3%
average fired pixel rate (PXD)	$1.74 \cdot 10^9$ Hz	$40 \cdot 43.6 \cdot 10^6$ Hz
maximum fired pixel rate (PXD)	$5.23 \cdot 10^9$ Hz	$40 \cdot 131 \cdot 10^6$ Hz
average data rate (half ladder)	174 MB/s	4 byte · $43.6 \cdot 10^6$ Hz
maximum data rate (half ladder)	523 MB/s	4 byte · $131 \cdot 10^6$ Hz
average data rate (PXD)	6.97 GB/s	4 byte · $1.74 \cdot 10^9$ Hz
maximum data rate (PXD)	20.9 GB/s	4 byte · $5.23 \cdot 10^9$ Hz
reduction rate by HLT	3	
reduction rate by ROI selection	10	
average output rate (half ladder)	5.81 MB/s	$\frac{1}{3} \cdot \frac{1}{10} \cdot 174$ MB/s
maximum output rate (half ladder)	17.4 MB/s	$\frac{1}{3} \cdot \frac{1}{10} \cdot 523$ MB/s
average output rate (PXD)	232 MB/s	$\frac{1}{3} \cdot \frac{1}{10} \cdot 6.97$ GB/s
maximum output rate (PXD)	697 MB/s	$\frac{1}{3} \cdot \frac{1}{10} \cdot 20.9$ GB/s