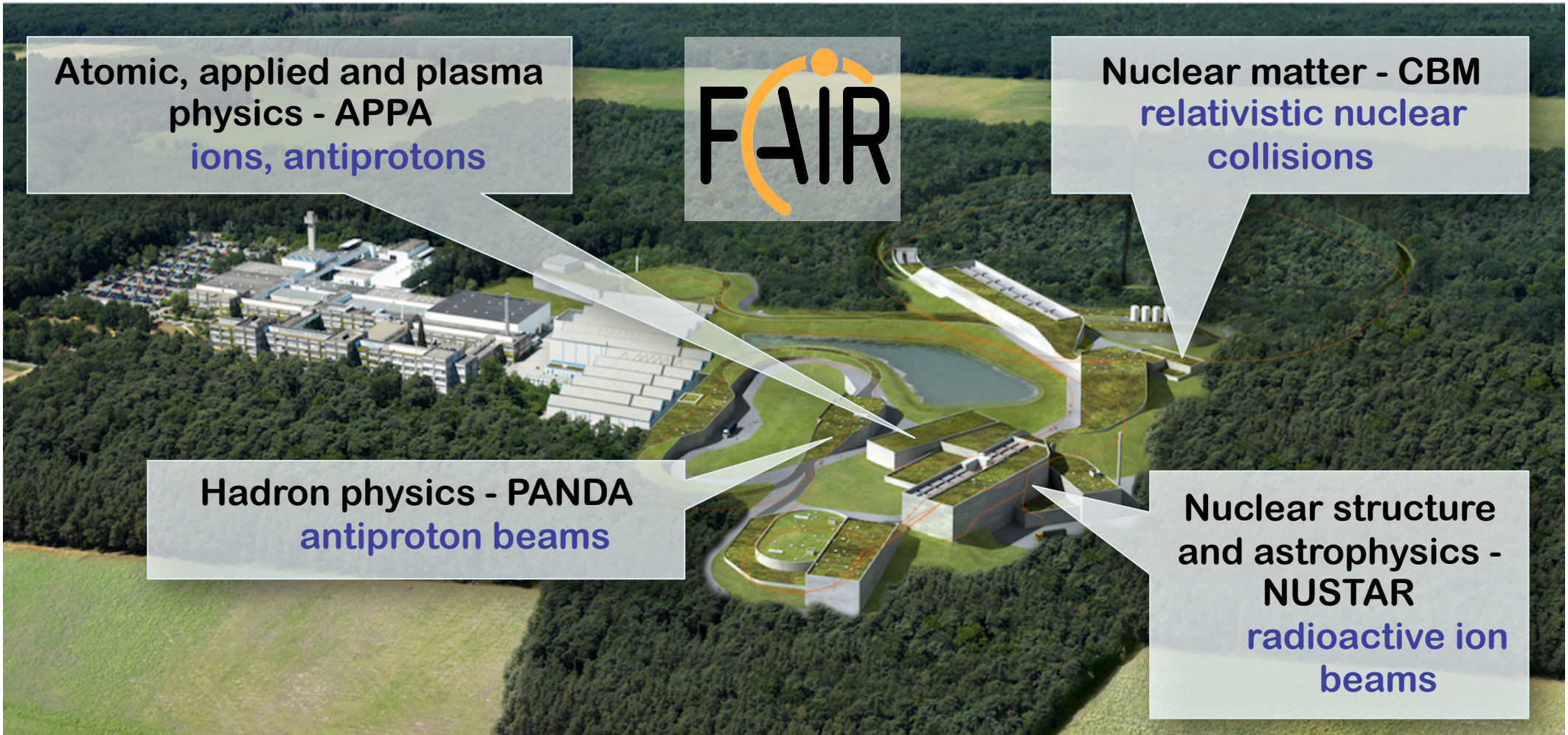
Data Acquisition for the PANDA Experiment at FAIR

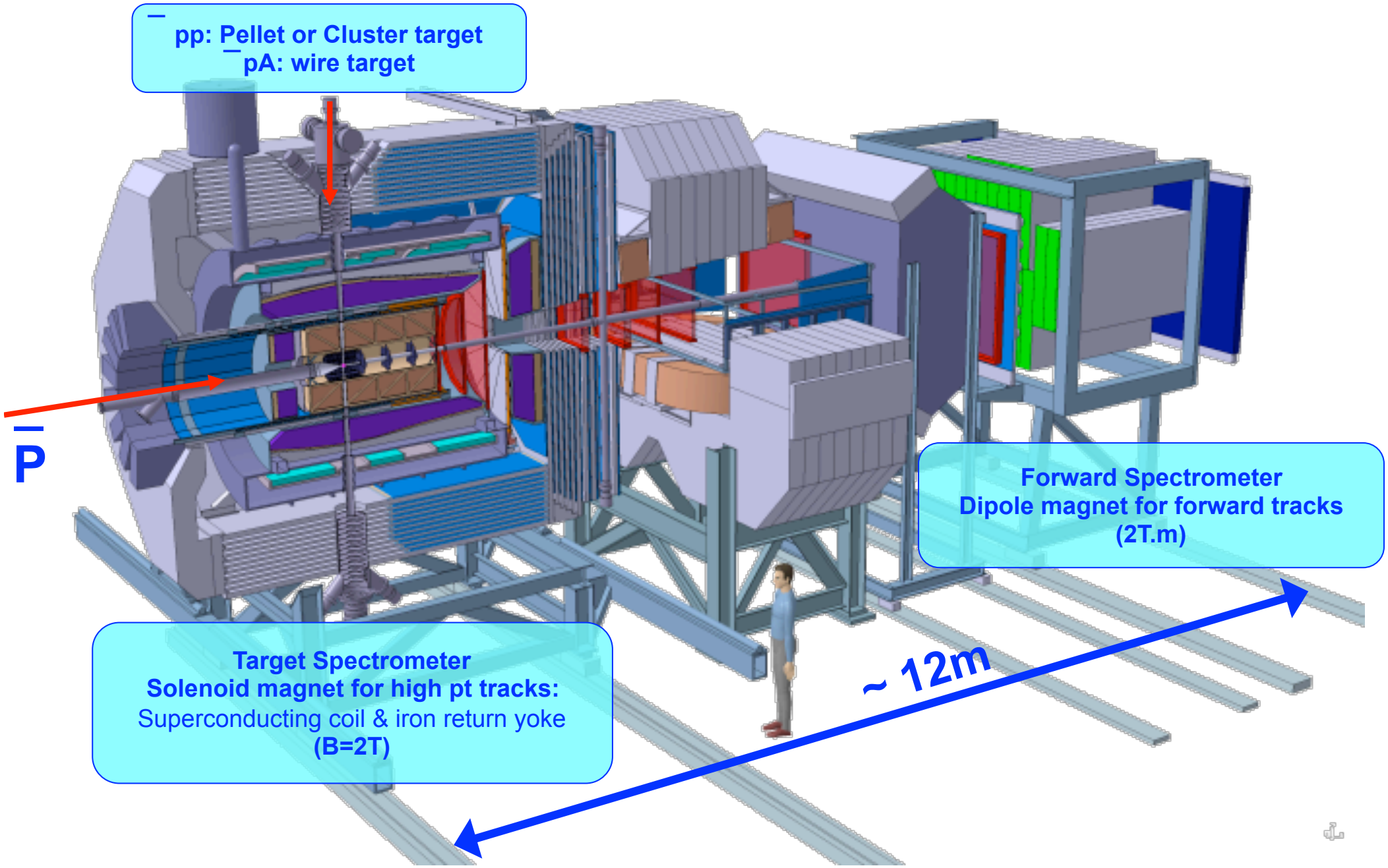
- What is FAIR ?
- What is PANDA ?
- What are the challenges for DAQ / Trigger ?
- Concept
- Conclusion

FAIR: Facility for Antiproton and Ion Research
Darmstadt / Germany

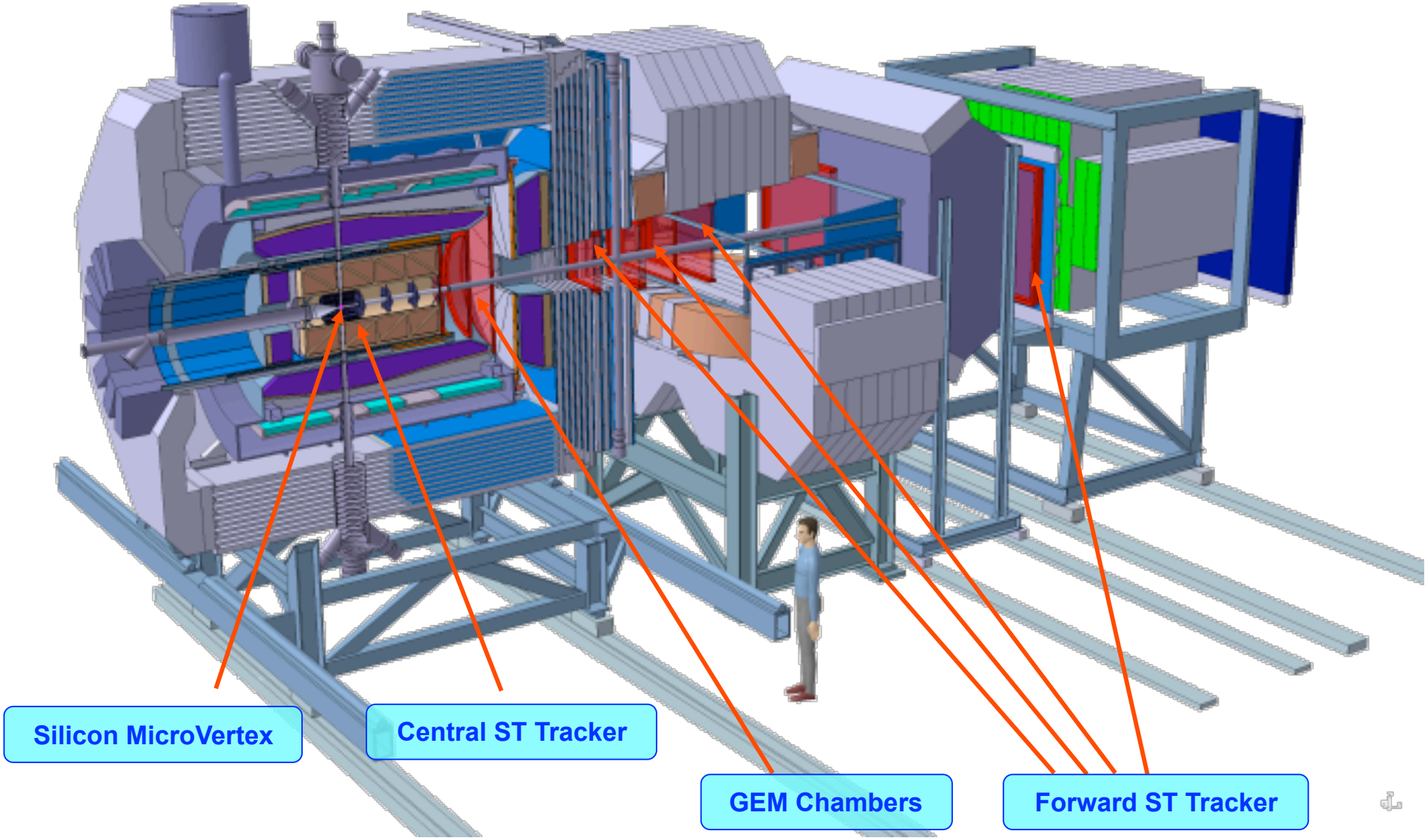
FAIR is the largest research infrastructure on the 2008 ESFRI Road Map (European Strategy Forum for Research Infrastructures)



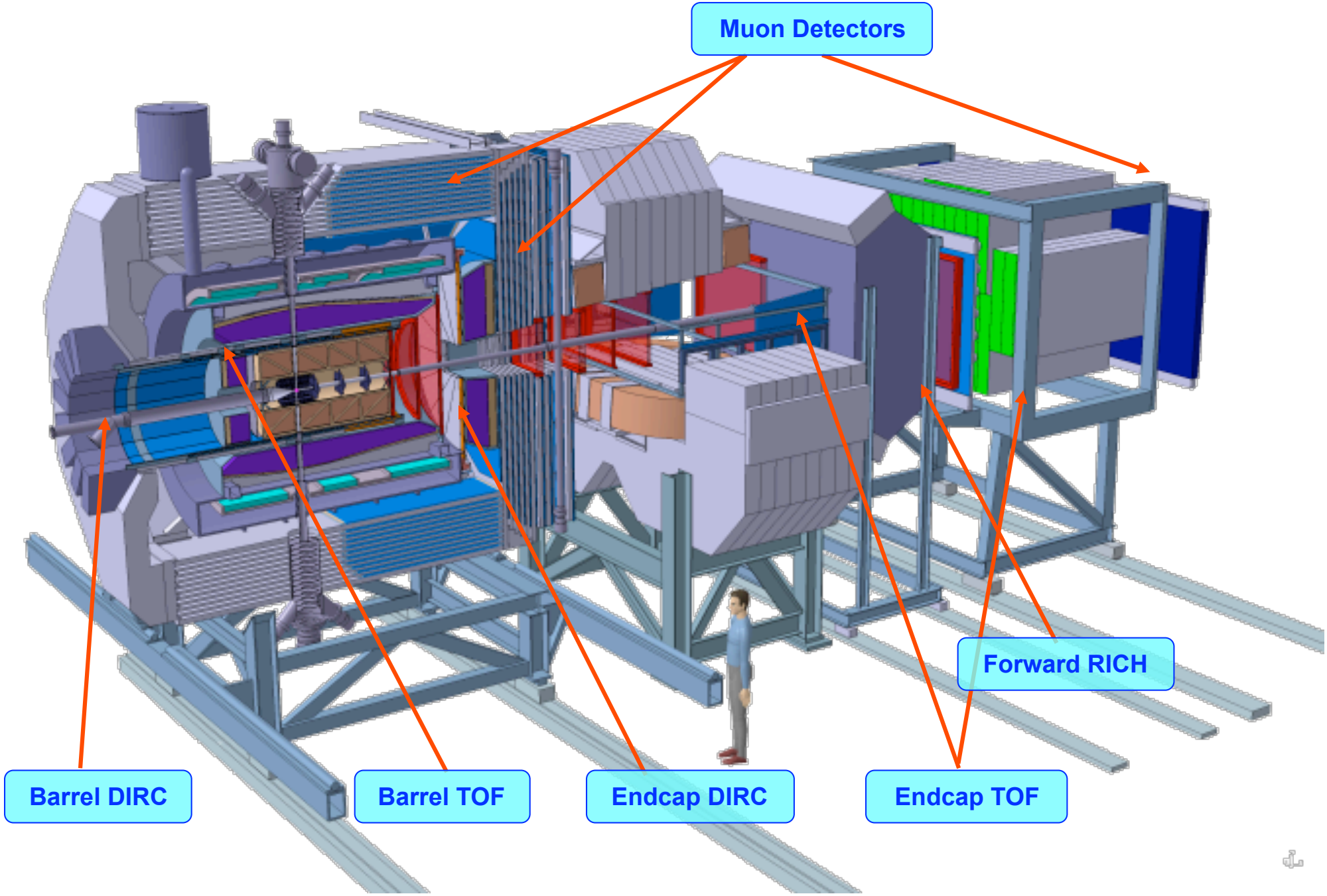
The PANDA detector



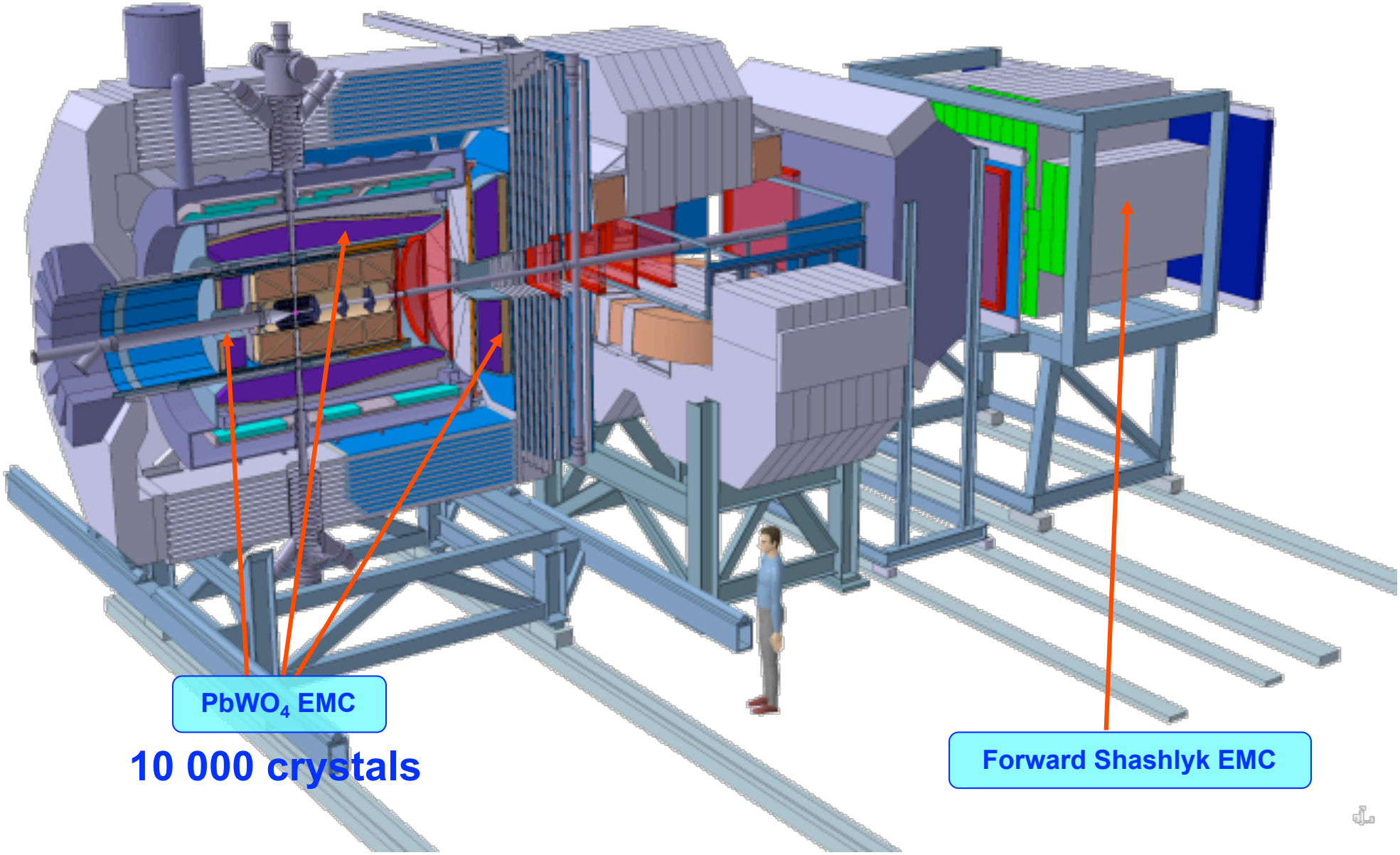
PANDA tracking systems



PANDA Particle Identification Detectors

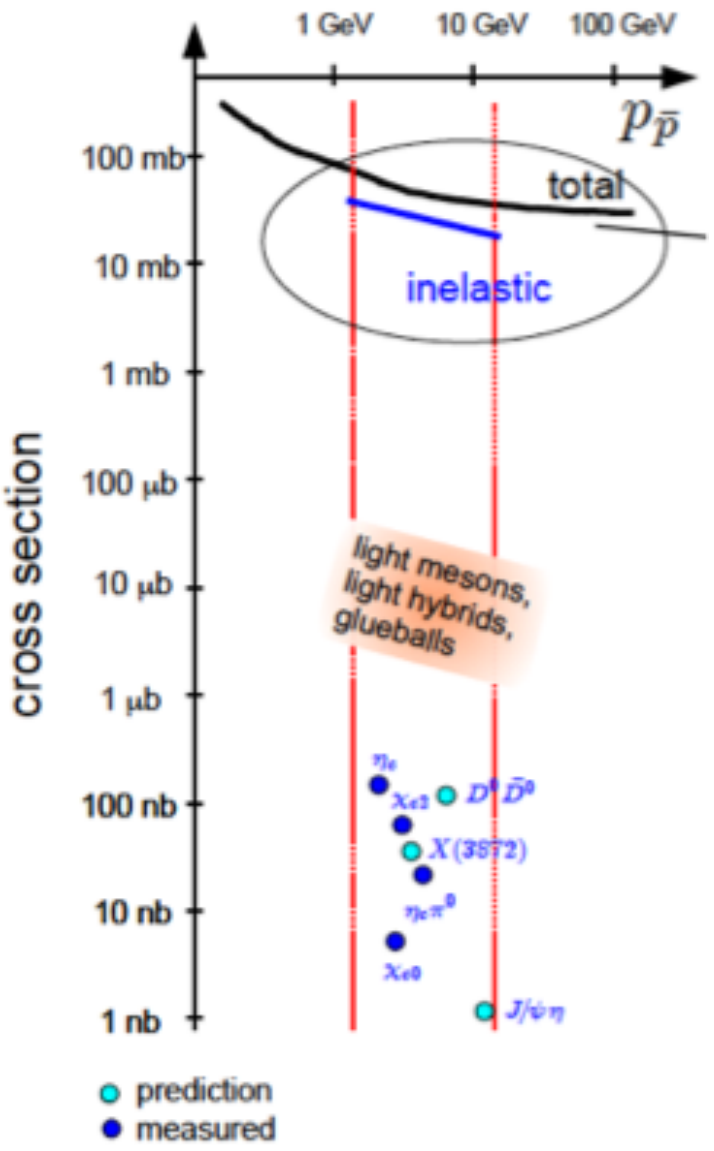


PANDA Electromagnetic Calorimeters



Physics, Data Acquisition and Event Filtering

- Problem: finding the needle in the haystack
- total inelastic cross section
  - 50 mb
- Interesting physics
  - most channels < 100 nb
- 2x10^7 interactions /s
- Data rate after FEE reduction: 200 GBytes/s
  - 17 PBytes/day
- Goal for online event filtering:
  - reduce "background" by factor of 1000

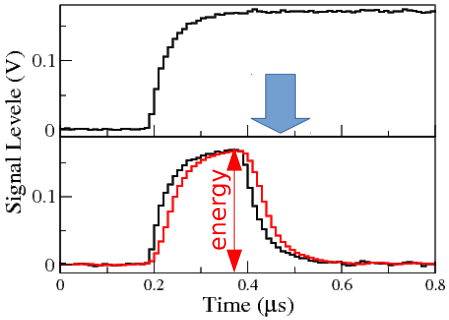


PANDA DAQ Approach

- Freely streaming data :"Trigger - less"
  - No hardware triggers
    - However, there will be event filtering, we cannot record everything !!
- Autonomous FEE, sampling ADCs with local feature extraction
- Time-stamping (SODAnet)
  - Data fragments can be correlated for event building
- Caveat: the high-rate capability implies overlapping events !!!
  - average time between two events can be smaller than typical detector time scales
  - This "pile-up" has to be treated and disentangled
  - Real-time event selection in this environment is very challenging and requires a lot of studies

Readout Approach for PANDA

The PANDA readout consist of:



- **Intelligent self-triggered front-end**:
  autonomous hit detection and data pre-processing (e.g. based on
  Sampling **A**nalogue to **D**igital **C**onverter)

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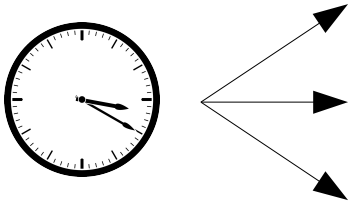
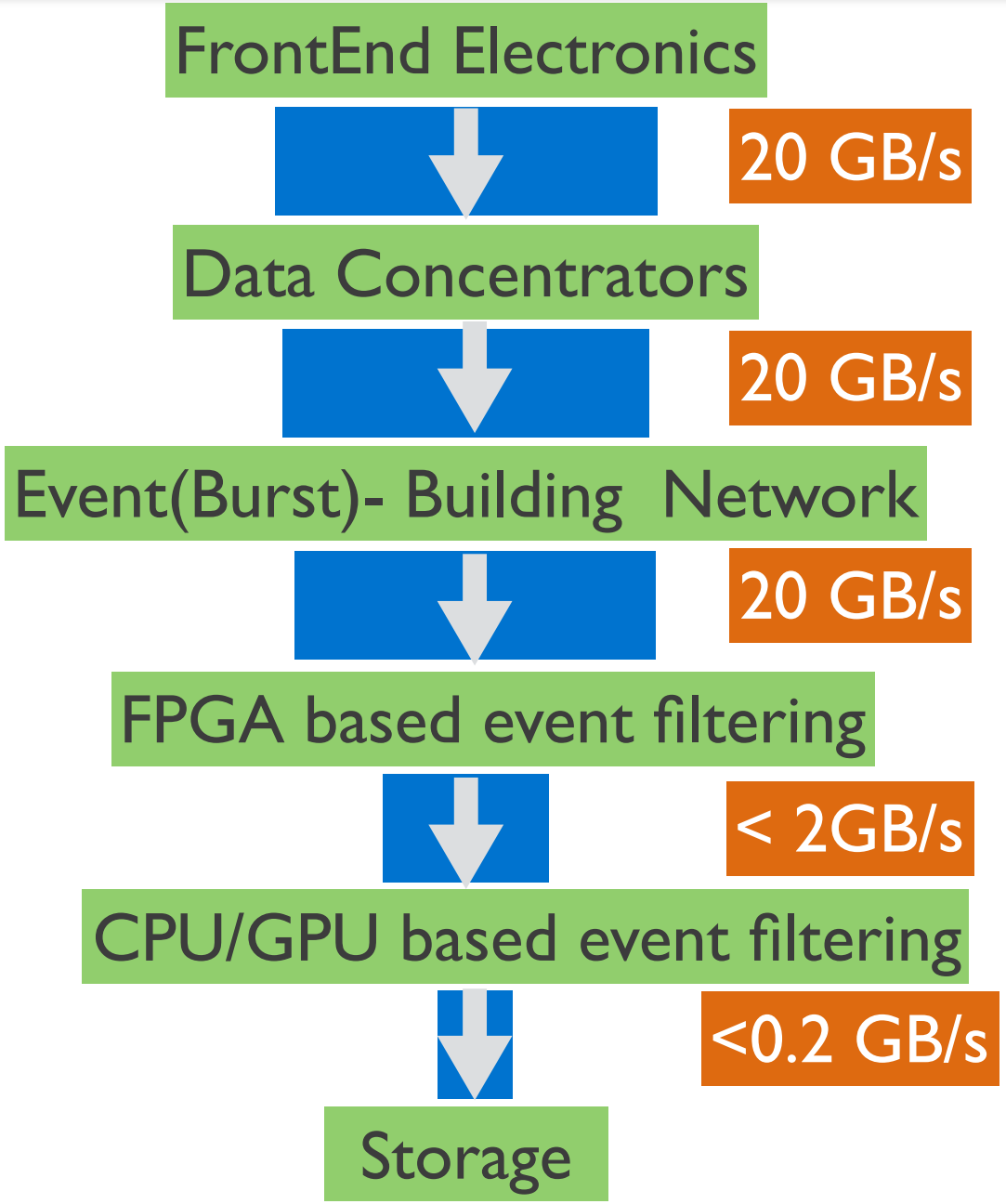
- **a very precise time distribution system (SODANET)**:
  single clock-source for PANDA (event correlation)



- **time-sorting and processing data in real-time**:
  processing in FPGA (**F**ield-**P**rogrammable **G**ate **A**rray)

DAQ Architecture

- Assumptions for Phase I
  - up to 10^6 events/s - 20 GB/s
  - separate runs for physics with "large" vs. "small" cross sections
  - negligible overlap between events (needs to be checked by simulations)
  - Final reduction factor for small cross section physics: 100
  - Reduction by FPGA layer: 10
    - Based on available resources at FAIR computing center
  - Large cross section physics requires reduced luminosity due to storage limitations



Conclusion: Key elements of PANDA DAQ&Event Filter

- **Flexibility:**
  - No hardware trigger
    - Advantage for CEPC: Be ready for the unknown
- **Event filtering** (rejection of "background" events) **based on physics content** of fully reconstructed events
  - much more sophisticated than "simple" hardware trigger
- **Cost-saving layered approach**
  - FEE/Data concentrators
  - FPGA based intermediate layer with large local buffer space (16 GB/FPGA)
    - Hardware: **see talk by Jingzhou Zhao**
    - can afford very large latency for decisions based on complex algorithms
    - Examples: FPGA based tracking algorithm for STT, cluster analysis for EMC
  - Final reconstruction and filtering on CPU/GPU farm
    - only 0.1 % of events need to be stored