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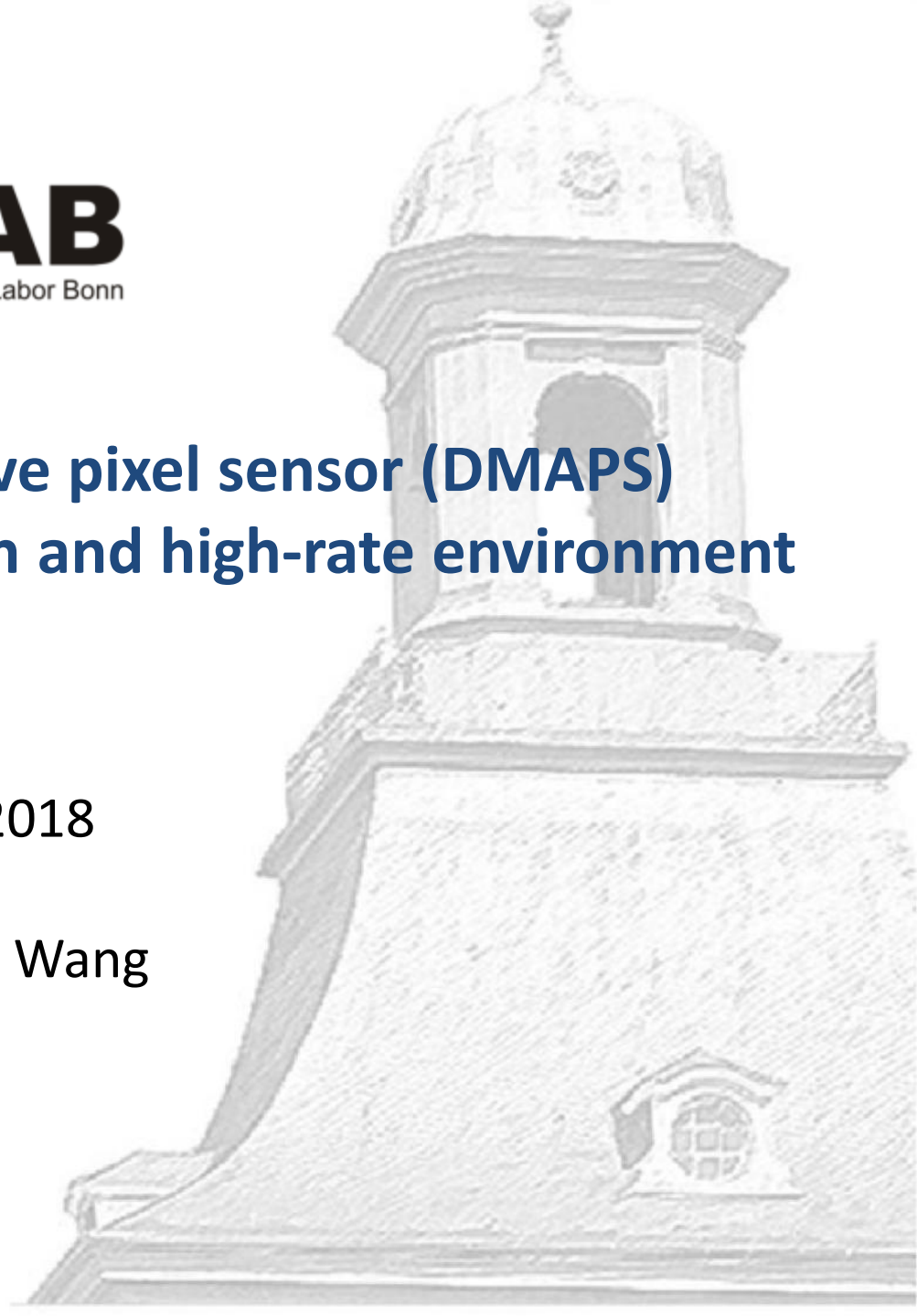
SI LAB
Silizium Labor Bonn

Depleted monolithic active pixel sensor (DMAPS) – R&D towards high-radiation and high-rate environment

CEPC 2018

Tianyang Wang



CMOS pixels (in commercial processes) for HEP

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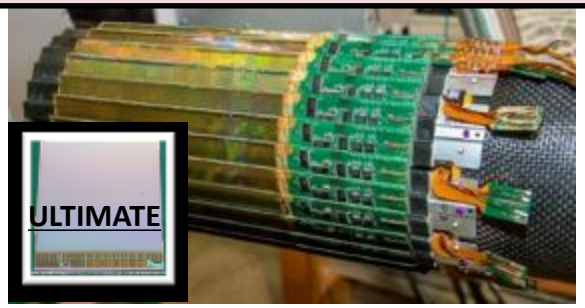
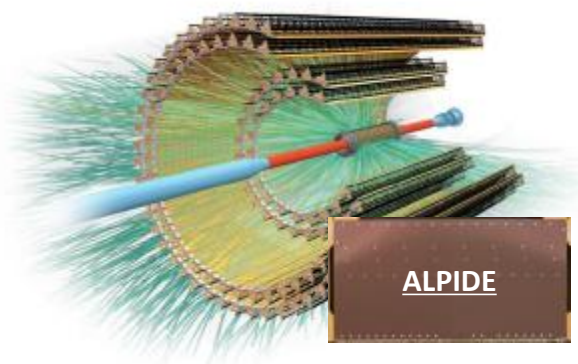
First MAPS-based vertex detector





MIMOSA28 (ULTIMATE) for STAR

Design led by IPHC Strasbourg

Twin-well 0.35 µm CMOS

Rolling shutter => ~200 µs int. time

~ 0.16 m^2 => 356 M pixels

ALPIDE for ALICE

Design led by CERN

Quadruple-well 0.18 µm CMOS

Sparse r.o. matrix => 10 µs int. time

~ 10 m^2 => 12 G pixels

Still many to come

Mu3e, CBM-MVD, sPHENIX, …

Future e^+-e^- colliders ?

HL-LHC (p-p) ?

2011 → **2016** → **Beyond 2018**

- R&D motivated by the need of **highly granular** sensors with very **low material budget**
  - Especially attractive and already successful for heavy-ion experiments
  - Proposed also for future e^+-e^- collider experiments
- Progressively evolve towards **higher radiation tolerance** and **faster readout**
  - Exploit advances in commercial CMOS technologies + dedicated designs => **HL-LHC (p-p) ?**

Depleted MAPS for ATLAS @ HL-LHC

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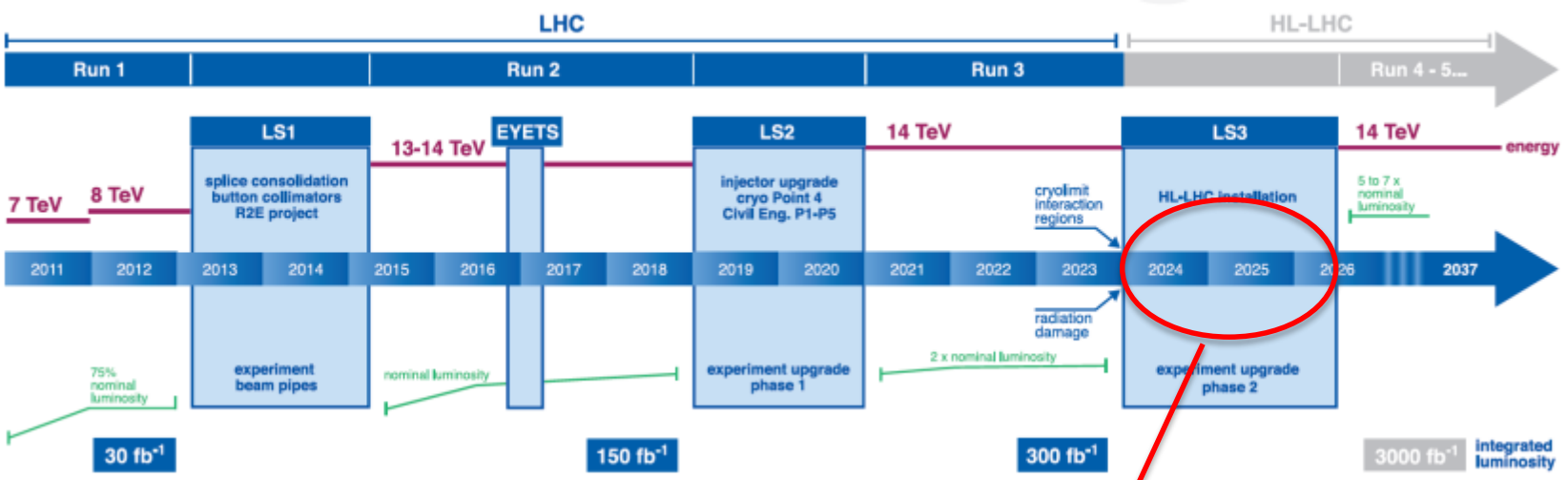
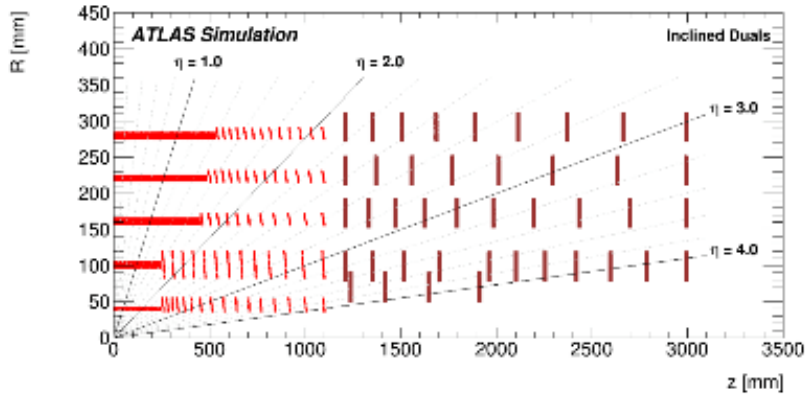
- **Strong R&D momentum** in the ATLAS community to achieve radiation hard MAPS through **depletion** towards ATLAS @ HL-LHC





Depleted MAPS for ATLAS @ HL-LHC

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- DMAPS has already been considered for the outermost pixel layer of ATLAS ITk
  - low cost and easy module assembly
  - require significantly enhanced rad. tolerance & speed w.r.t. the well established MAPS

	STAR	ALICE-LHC	ILC	ATLAS-HL-LHC	
				Outer	Inner
Fluence [n_{eq}/cm^2]	10^{12}	1.7×10^{13}	10^{12}	10^{15}	$2x10^{16}$
TID [Mrad]	0.2	< 3	0.4	80	> 1000
Required timing	~ 200 µs	20 µs	O(1 µs)	25 ns	25 ns
Hit Rate [kHz/mm^2]	4	10	250	1000	10 000

- **Non-ionizing radiation (displacement damage)**
  => fast collection by drift
- **Time resolution**
  => fast collection by drift
  => fast analog FE for small time walk
  => time stamping

} depletion

- **High hit rate**
  => short pulse duration (< 1 µs)
  => high readout bandwidth
  => massive on-chip mem.
  (long trig. Latency > 10 µs)

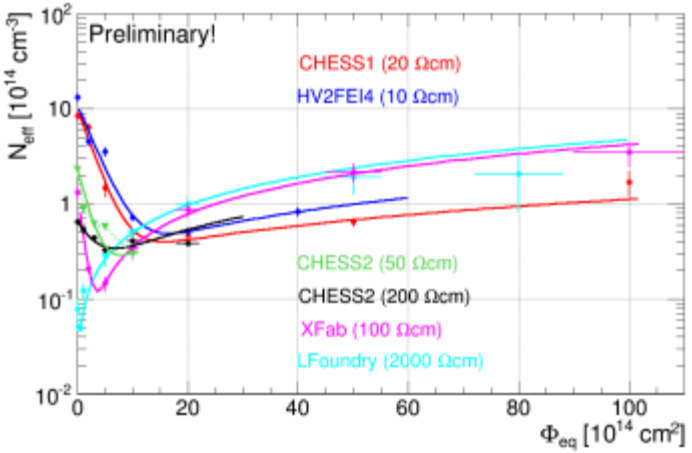
What are needed to realize DMAPS

1. **HV add-ons** to apply > 50 V bias I. Peric, DOI: 10.1016/j.nima.2007.07.115

2. **HR substrate** wafers (or epi) $d \sim \sqrt{\rho \cdot V}$
   - 100 Ω·cm – kΩ·cm
   - convergence of N_{eff} after high fluence (> 10^{15} n_{eq})
     => acceptor removal + deep acceptor introduction

3. **Multiple nested wells**
   - high voltage **shielding**
   - **full CMOS** in pixel

4. **Backside processing**
   - **thin** sensor (100 - 200 µm) with **backside bias**

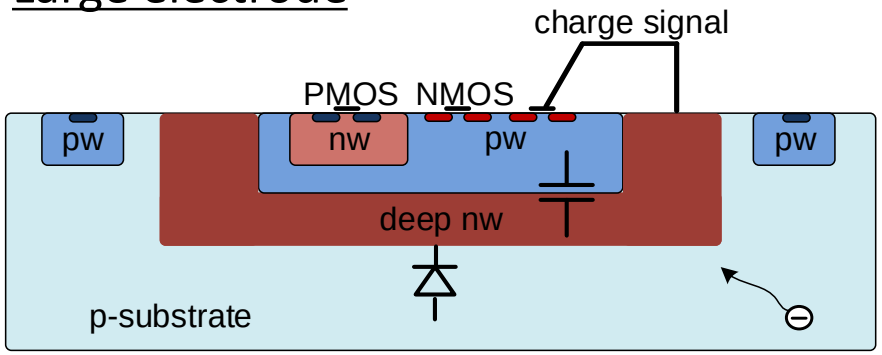


I. Mandić, et al., 29th RD50 workshop

- Design mostly implemented in “medium” feature size processes 130 nm -350nm
  => AMS 350 nm, **AMS/TSI 180nm**, **LFoundry 150 nm**, GlobalFoundry 130 nm, ESPROS 150 nm, **TowerJazz 180 nm**, IBM T3 130 nm, STM 180 nm, ON Semi 180 nm, SOI XFAB 180 nm

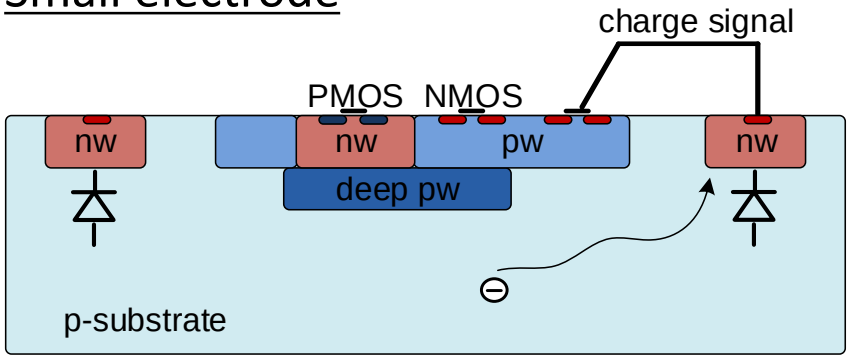
Sensor design approaches

Large electrode



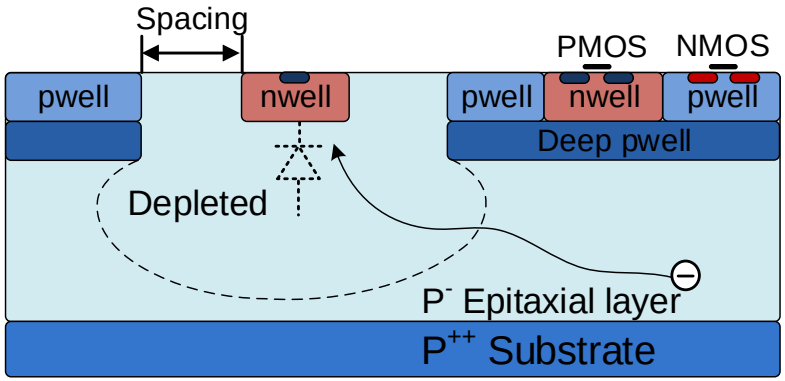
- Electronics **inside** charge coll. well
- Large charge collection electrode
  => resemble standard n-in-p sensor
  => no/little low field region
  => on average short(er) drift path
  } **radhard**
- Full CMOS with iso. between nw/dnw
- **Large** sensor **capacitance** (pw & dnw !)
  => noise & speed (power) penalty
  => dedicated design to mitigate x-talk

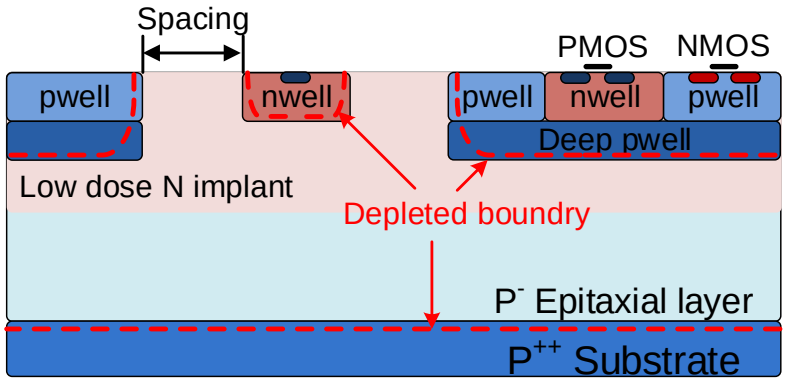
Small electrode



- Electronics **outside** charge coll. well
- Very **small** sensor **capacitance** (~ 5 fF)
  => lower power budget for analog FE
- Full CMOS with deep pwell
- Less prone to cross talk
- On average **long(er)** travelling path and potentially low field region
  => **process modification** for rad. hardness

Process modification – TowerJazz 180 nm CMOS





Standard process

- **High res.** P-type epi. (> 1 kΩ·cm)
  => typ. thickness **25 µm**
- Quadruple-well
  => deep pwell shields nwell => **full CMOS**
- **Reverse bias** typ. -6 V
  => enhanced, but not yet full depletion

Modified process

- Additional planar low dose **N implant**
  => improve depletion under deep pwell
  => **fully depleted** sensing volume possible
- Maintain small capacitance feature
- No significant circuit/layout changes

W. Snoeys et al. DOI: 10.1016/j.nima.2017.07.046

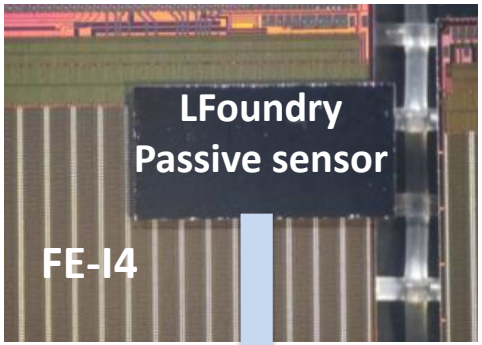
Sensor irradiation performance

- Good radiation hardness of large electrode sensor proven in various prototypes

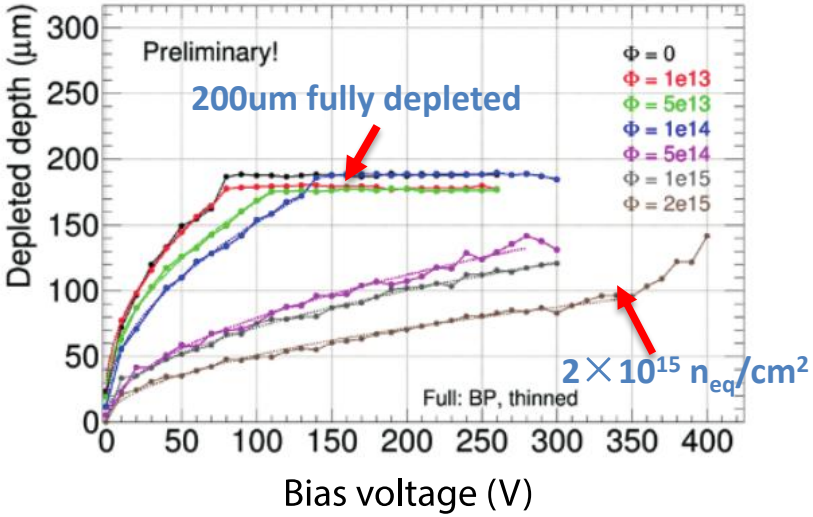
LFoundry 150 nm CMOS
P-substrate > 2 kΩ·cm
Bias 100 - 400 V
7 metal layers

T. Hirono et al., DOI: 10.1016/j.nima.2016.01.088
P. Rymaszewski et al., DOI: 10.1088/1748-0221/11/02/C02045

Passive sensor

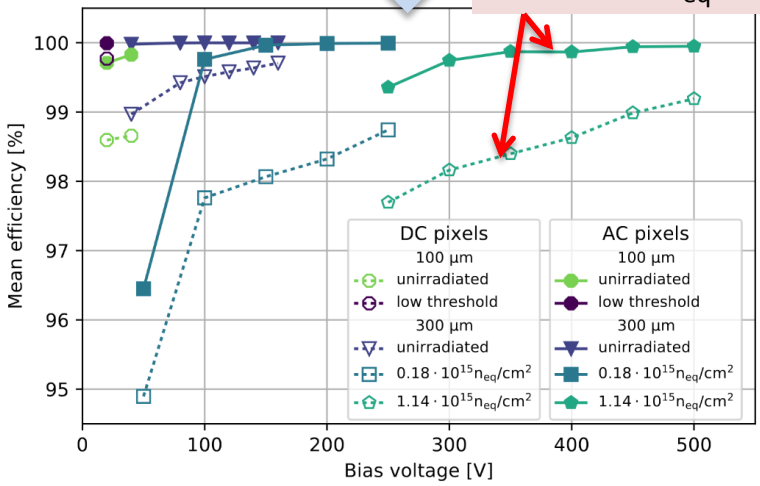


LFoundry test structure



I.Mandić, et al., DOI: 10.1016/j.nima.2018.06.062

$1.14 \cdot 10^{15}$ n_{eq}/cm^2



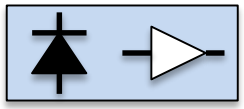
D.-L. Pohl, et al., DOI: 10.1088/1748-0221/12/06/P06020

Sensor irradiation performance

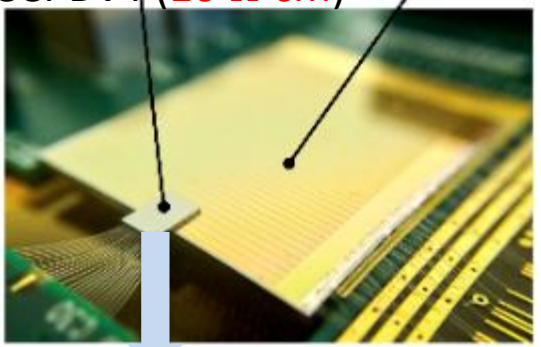
- Good radiation hardness of large electrode sensor proven in various prototypes

AMS 180 nm CMOS
P-substrate 0.01-2 kΩ·cm
Bias 60 - 100 V
6 metal layers

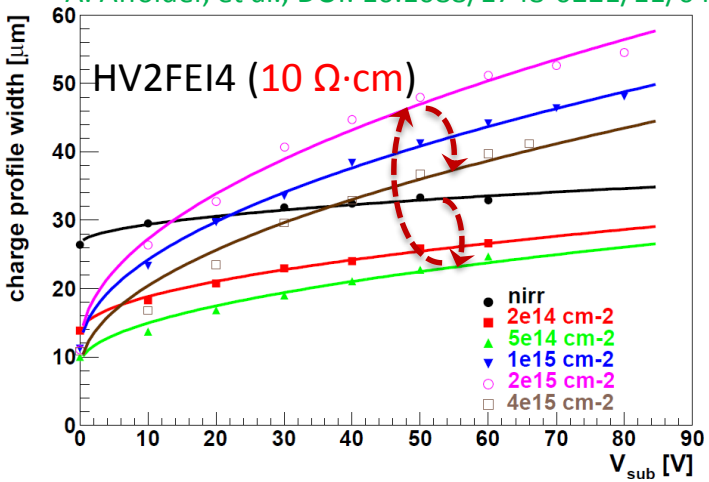
Active sensor/smart diode



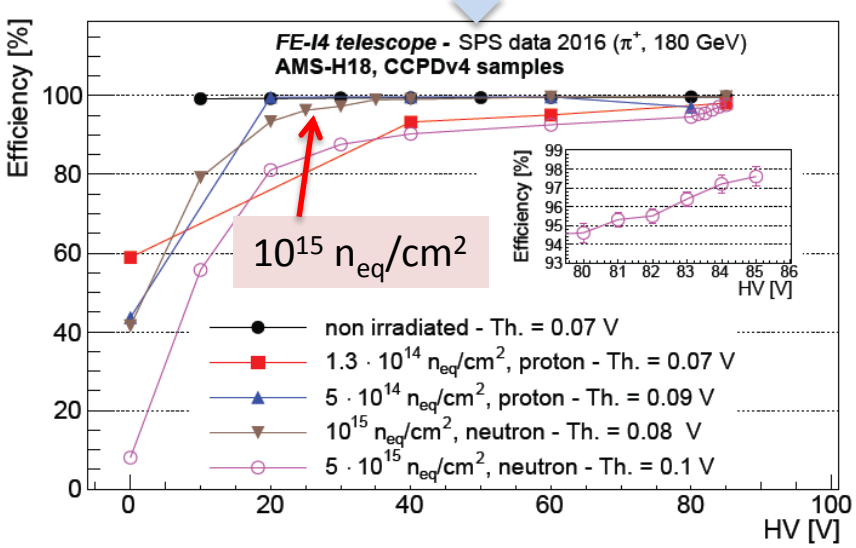
CCPDv4 (10 Ω·cm) FE-I4



A. Affolder, et al., DOI: 10.1088/1748-0221/11/04/P04007



Benefit from acceptor removal
=> However, "valley of tears" exits
=> Higher res. substrate should help



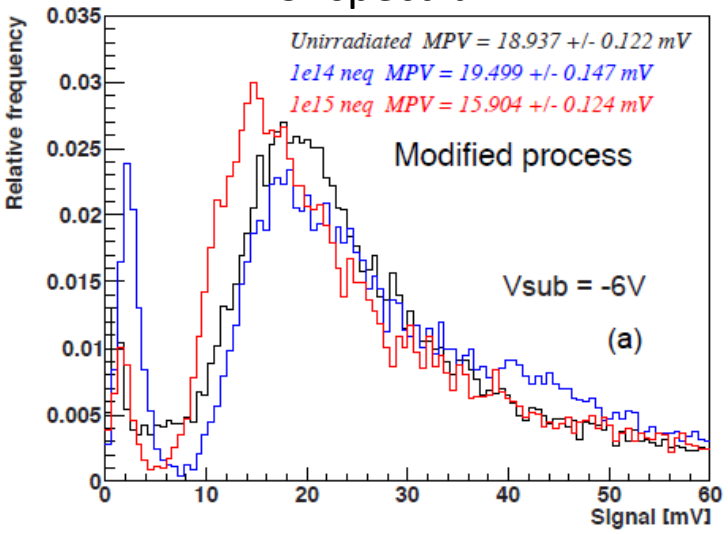
M. Benoit, et al., DOI: 10.1088/1748-0221/13/02/P02011

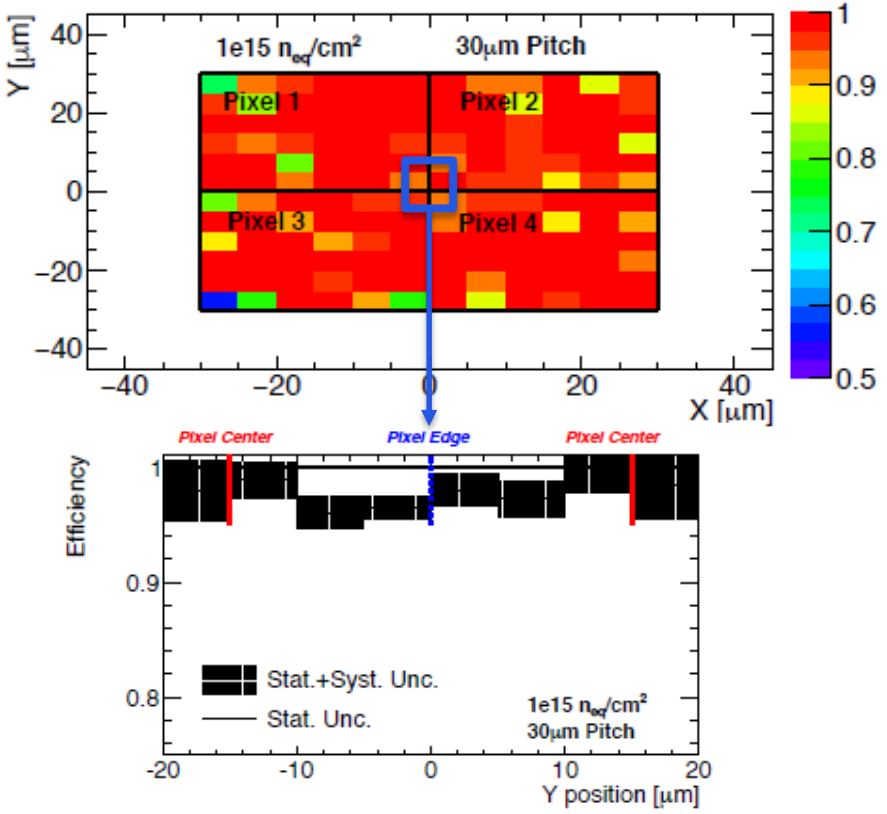
Sensor irradiation performance

- TowerJazz small electrode design in modified process showed promising results
  - > 97% efficiency after 10^{15} n_{eq}/cm^2 at low threshold (< 100 e^-) for 30 µm square pixel

TowerJazz 180 nm CMOS
P-epi. 25 µm (> 1kΩ·cm)
6 metal layers

^{90}Sr spectrum





H. Pernegger, et al., DOI: 10.1088/1748-0221/12/06/P06008

Demonstrator chips with large scale matrix

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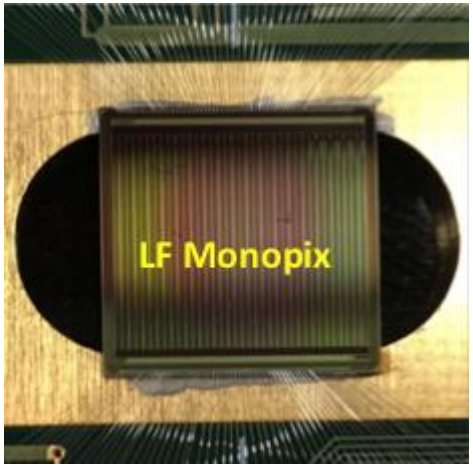
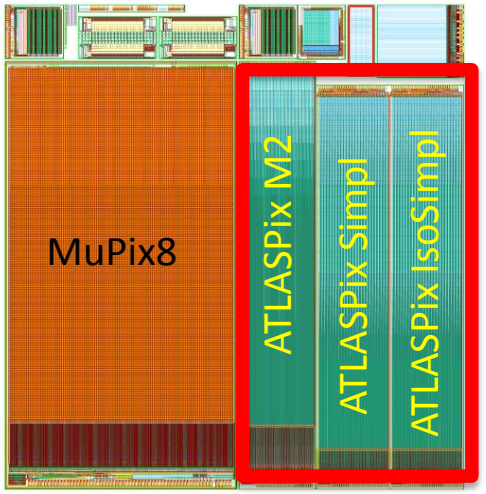
LFoundry 150 nm CMOS



Large electrode
Pixel size 50 µm × 250 µm
Pixel matrix 129 × 36
Thinned down to 100 µm

T. Wang, et al.,
DOI: 10.1088/1748-0221/12/01/C01039
P. Rymaszewski et al.,
DOI: http://doi.org/10.22323/1.313.0045
T. Hirono, et al.,
DOI: 10.1109/NSSMIC.2016.8069902
K. Moustakas et al.,
DOI: doi.org/10.1016/j.nima.2018.09.100

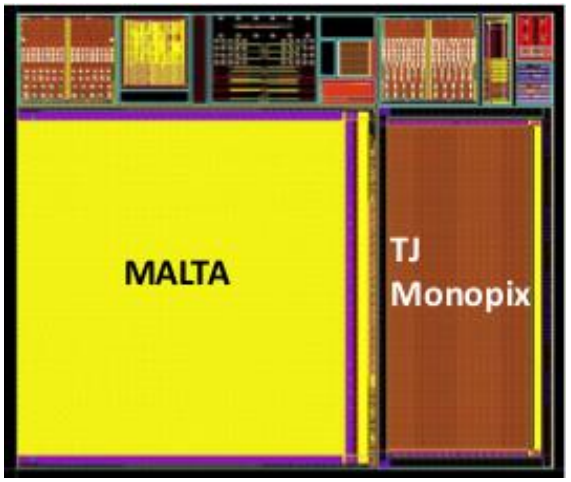
AMS 180 nm CMOS



Large electrode
10/80/200/1k Ω·cm sub.
Pixel size 40µm × 130µm
Pixel matrix 400 × 25
Thinned down to ~ 60 µm

I. Perić, et al.,
DOI: 10.1016/j.nima.2018.06.060
M. Kiehn, et al.,
DOI: 10.1016/j.nima.2018.07.061

TowerJazz 180 nm CMOS



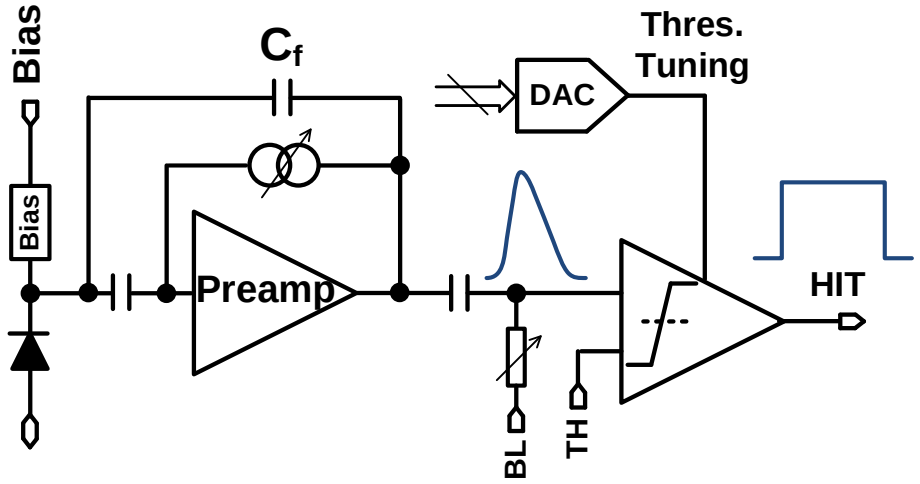
Small electrode
- MALTA: 36.4µm × 36.4µm
  512 × 512 pixels
- TJ-Monopix: 36µm × 40µm
  224 × 448 pixels

Standard/modified process
Thinned down to 100 µm

T. Wang, et al.,
DOI: 10.1088/1748-0221/13/03/C03039
I. Berdalovic, et. al,
DOI: 10.1088/1748-0221/13/01/C01023

Analog front-end – CSA vs. voltage amplifier

- The two sensor design approaches lead to different analog FE choices

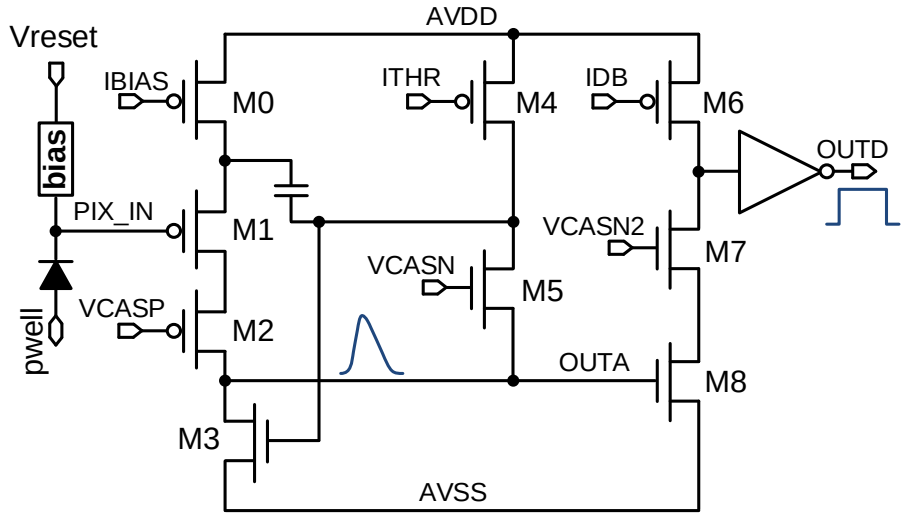


Charge Sensitive Amplifier

- Used for large electrode sensor
- Gain (ideally) independent of C_D
  => G ~ $1/C_f$ (Typ. C_f ~ fF)
- $\tau_{CSA} \propto \frac{C_D}{g_m \cdot C_f}$, $ENC_{thermal} \propto \frac{KT}{g_m}\frac{C_D^2}{\tau}$
  => need larger g_m (power) for large C_D
  => typ. power 5 – 20 µA
- In-pixel threshold trimming

Analog front-end – CSA vs. voltage amplifier

- The two sensor design approaches lead to different analog FE choices



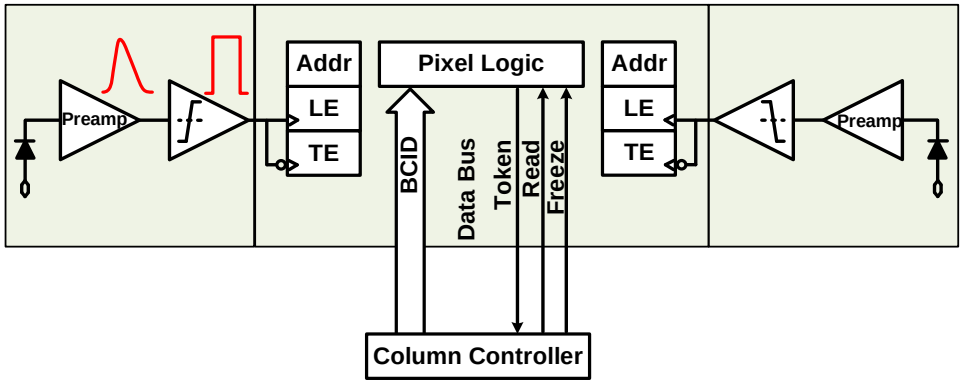
D. Kim et al., 10.1088/1748-0221/11/02/C02042

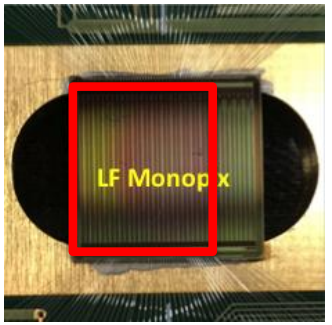
ALPIDE like amplifier

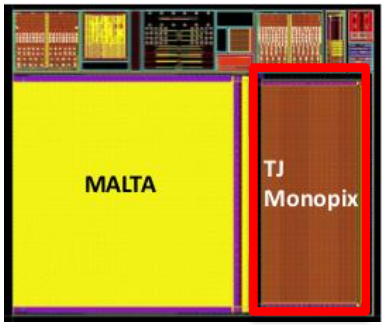
- Voltage amplifier
  => Profit from small sensor capacitance
  => large voltage excursion @ input node
- Very compact design
  => amplification + shaping in one stage
  => simple inverter as discriminator
  => no threshold trimming in ALPIDE
- Optimized power for required timing
  => ~ 500 nA for 25 ns peaking time

Readout architecture – DMAPS

DMAPS with synchronous matrix => time stamping in matrix







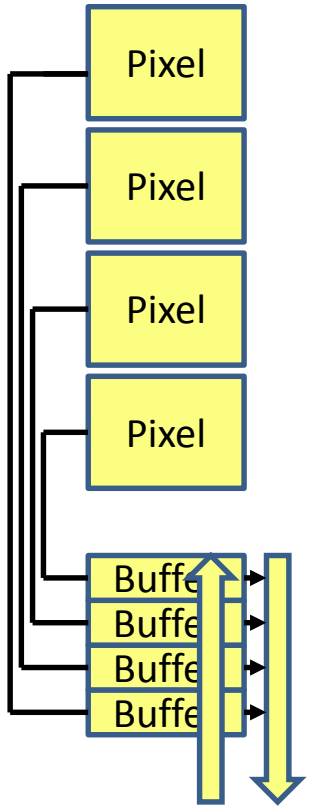
- Well established scheme in ATLAS – FE-I3 like
  => sufficient rate capability for ITk outer pixel layers
- Time reference distributed in the matrix
  => need small skew across the long column (~ 2cm for ITk)
- ToA & ToT recorded in pixel
- Hits read out following the token passing scheme on shared column bus
- In-pixel memories and digital r.o. logic
  => digital cross talk, pixel size, C_D (for large electrode design)

Readout architecture – DMAPS

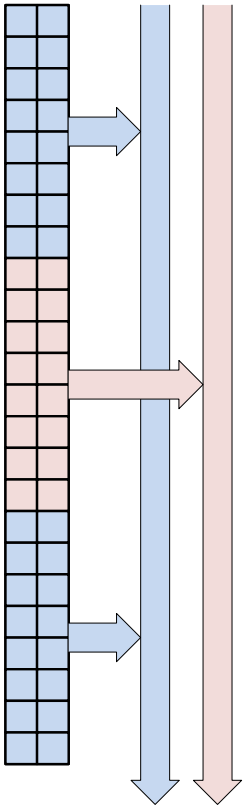
DMAPS with asynchronous matrix => time stamping at periphery

=> Hits transferred to periphery immediately => call for massive parallelism

One to one connection



Shared bus by pixel groups



Readout architecture – DMAPS

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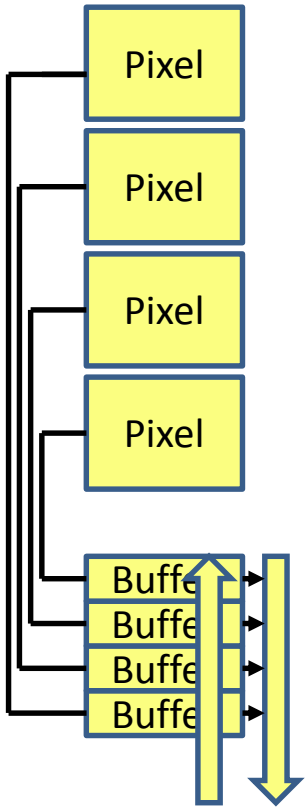
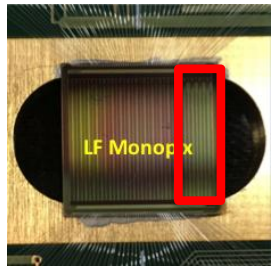
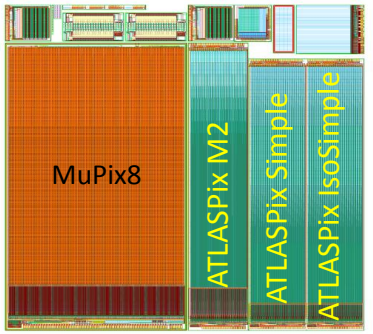
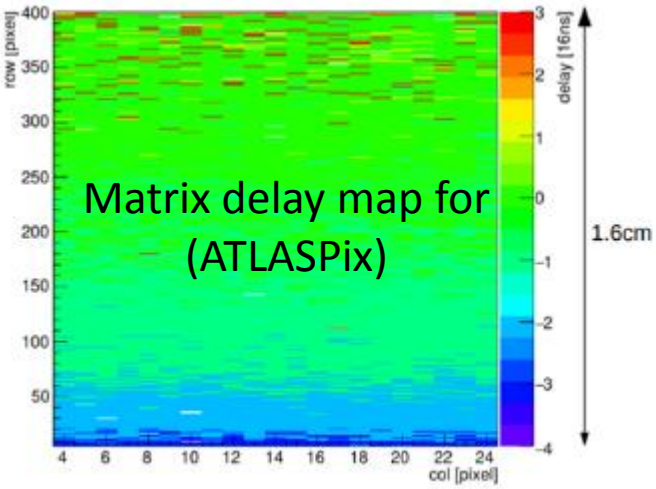
DMAPS with asynchronous matrix



- Analog only pixel (CSA + discri.)
  => good for cross talk to sensor, pixel size, capacitance
- All digital processing at periphery
- Complex column line routing
  => 400 lines in two metal layers for ATLASPix
- Position dependent hit transfer latency
  => need compensation/correction
- Larger periphery area







Readout architecture – DMAPS

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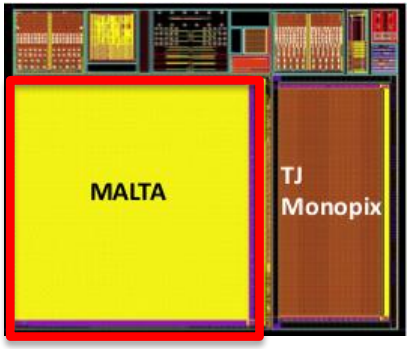
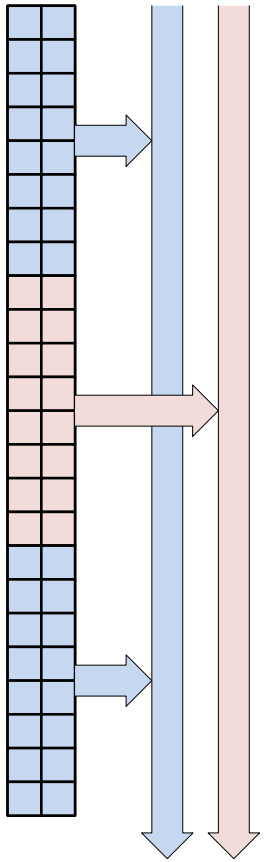
DMAPS with asynchronous matrix





- 2 independent buses serve alternating pixel groups
- High speed bus by transferring short pulses (~ 1ns)

  => pulse generated by the pixel logic in case of hit

  => reference pulse + parallel pulses indicating hit pixel address
- Special routing and buffering to balance load on the column bus to ensure the multi-bit data arrive simultaneously at periphery
- Max. pulse propagation delay along ~ 2 cm column ~ 7.5 ns
- Fast data synchronization (~ GHz) needed at periphery

  => not in the current MALTA, implemented recently in a test chip
- Careful study needed on data collision caused by simultaneous hits on pixel groups of the same color

Demonstrator chips with large scale matrix

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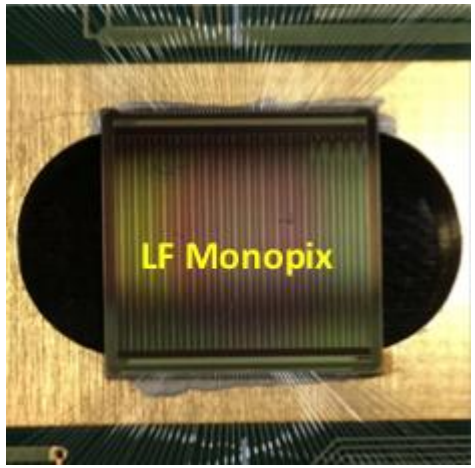
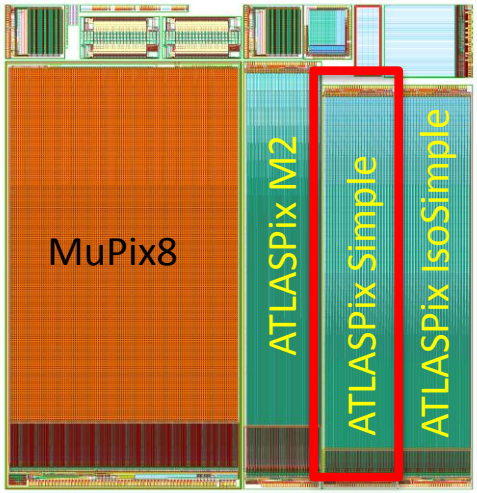
Test results

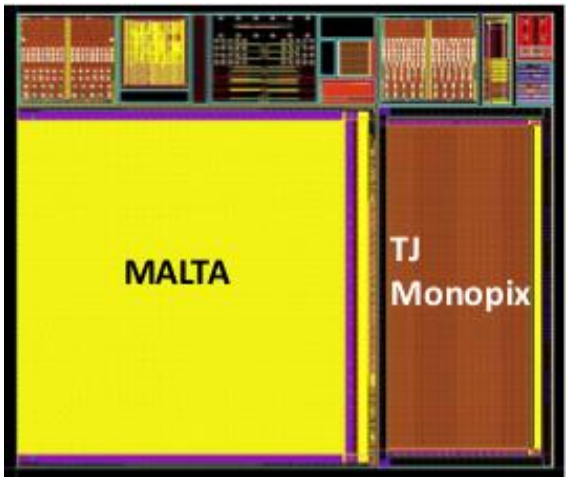
LF-Monopix



ATLASPix Simple



MALTA & TJ-Monopix



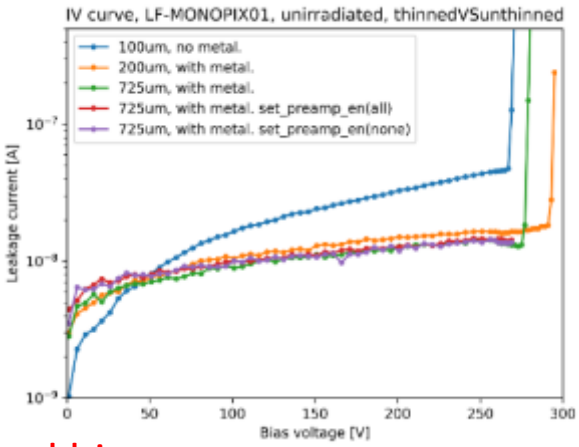
Large electrode design

Small electrode design

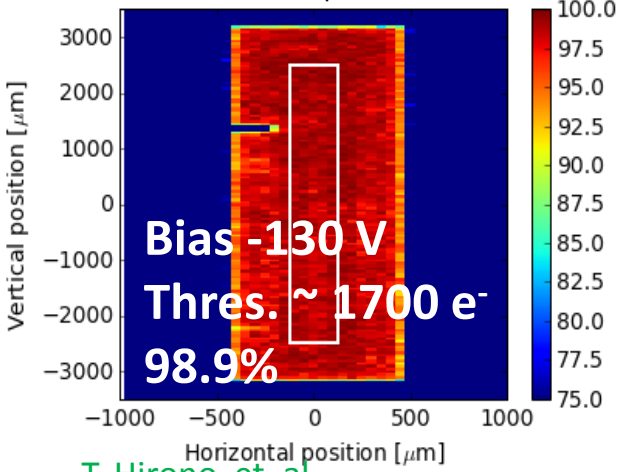
Results – LF-Monopix

- High BV ~ -280 V => large depletion + high field
- High and uniform efficiency even after irradiation
  - Achieved @ very low noise occupancy < 10^{-7}/25ns/pixel
- Promising timing, and can be improved by
  - Optimization of analog FE biasing
  - Enhanced charge collection in thinned sensor through HV backbias

I-V curve

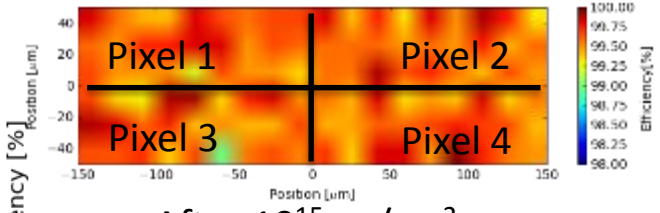


After $10^{15}n_{eq}/cm^2$ (neutron)

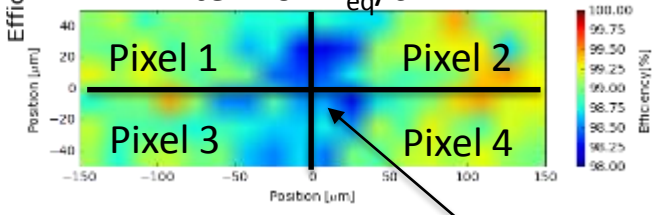


Uni-Bonn (Preliminary)

Before irrad.

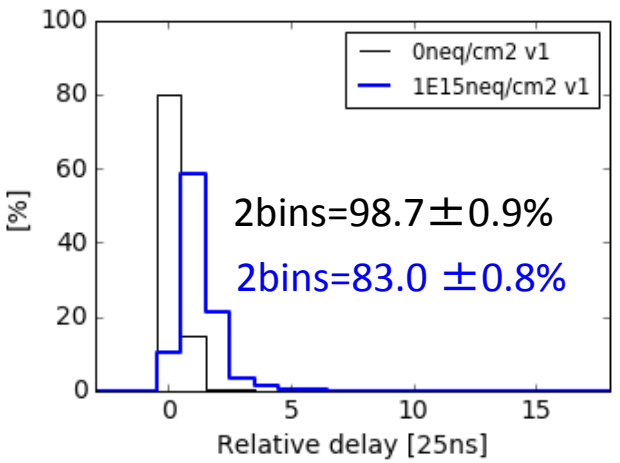


After $10^{15}n_{eq}/cm^2$



~ 98%

t_{hit} - t_{ref}



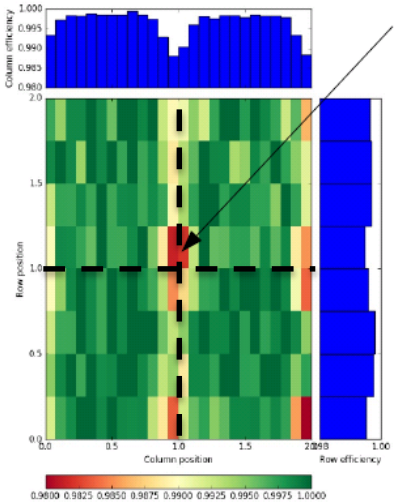
T. Hirono, et. al,
DOI: 10.1016/j.nima.2018.10.059

Results – ATLASPix Simple

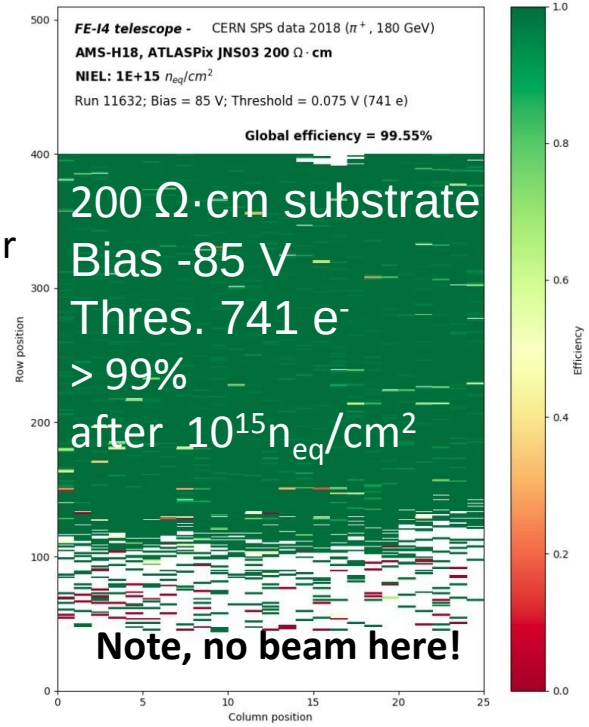
- High efficiency after $10^{15} n_{eq}/cm^2$ (neutron)
- Improved timing expected by correcting time walk based on ToT

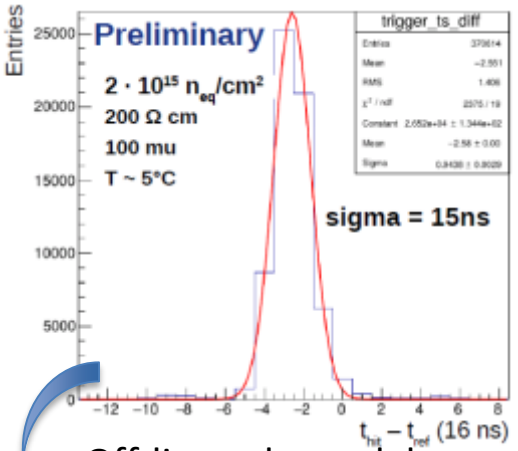
200 Ω·cm substrate
Bias -60 V
Before irradiation
Global efficiency > 99%

In-pixel

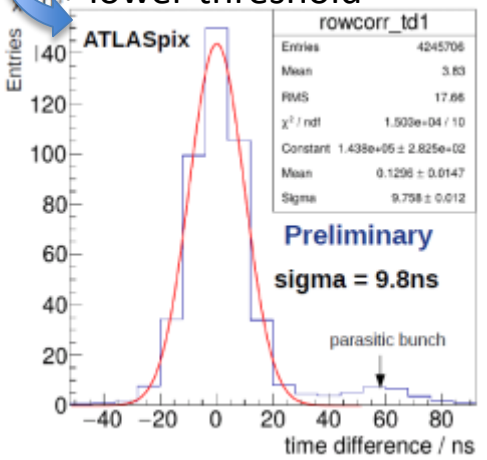


Pixel corner
98%





Off-line column delay correction
+ lower threshold

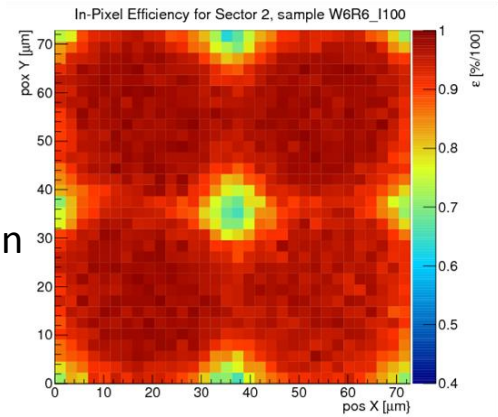


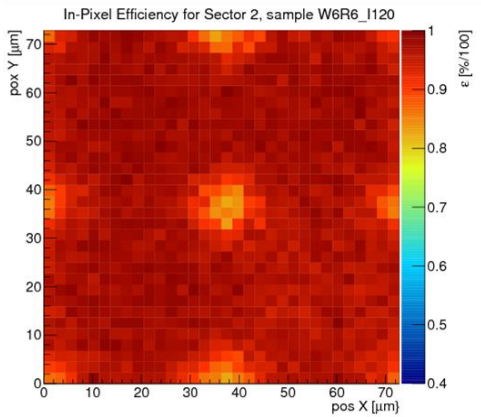
Measurement by Geneva-Heidelberg-KIT, Heidelberg
Source: VERTEX 2018

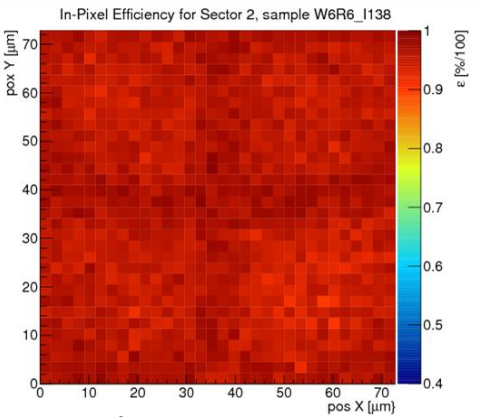
Results – MALTA & TJ-Monopix

- Low corner efficiency, especially after irradiation

MATLA
Before irradiation

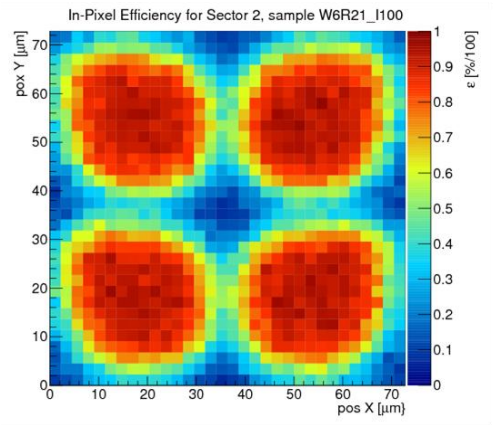


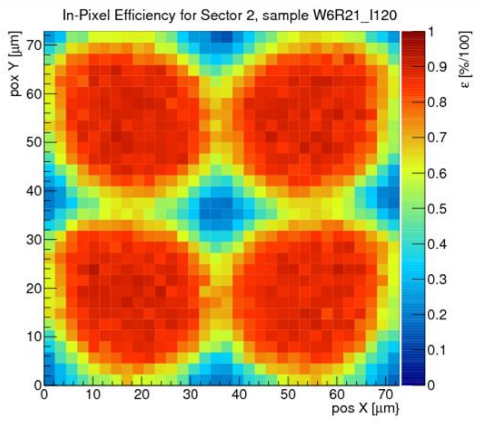




Decreasing threshold, from ~600 e^- to ~250(unirr)/350(irr) e^-

MATLA
Irradiated
5 x10^{14} n_{eq}/cm^2





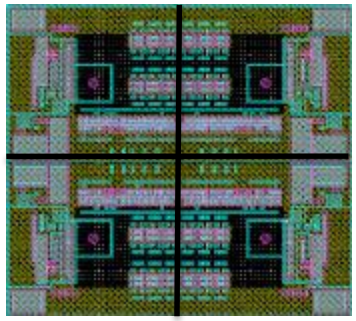
Couldn't reach lower threshold

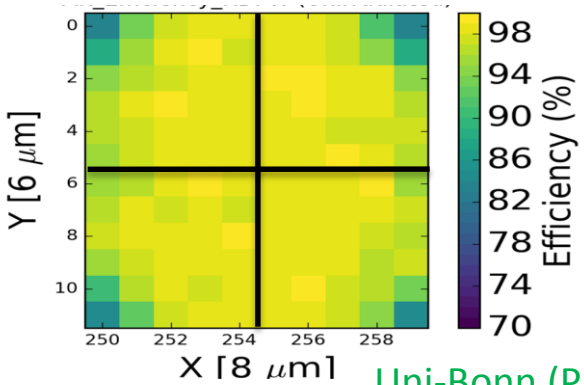
A. Sharma, et al., Vertex 2018

Results – MALTA & TJ-Monopix

- Lateral field configuration under deep pwell at pixel corner is critical

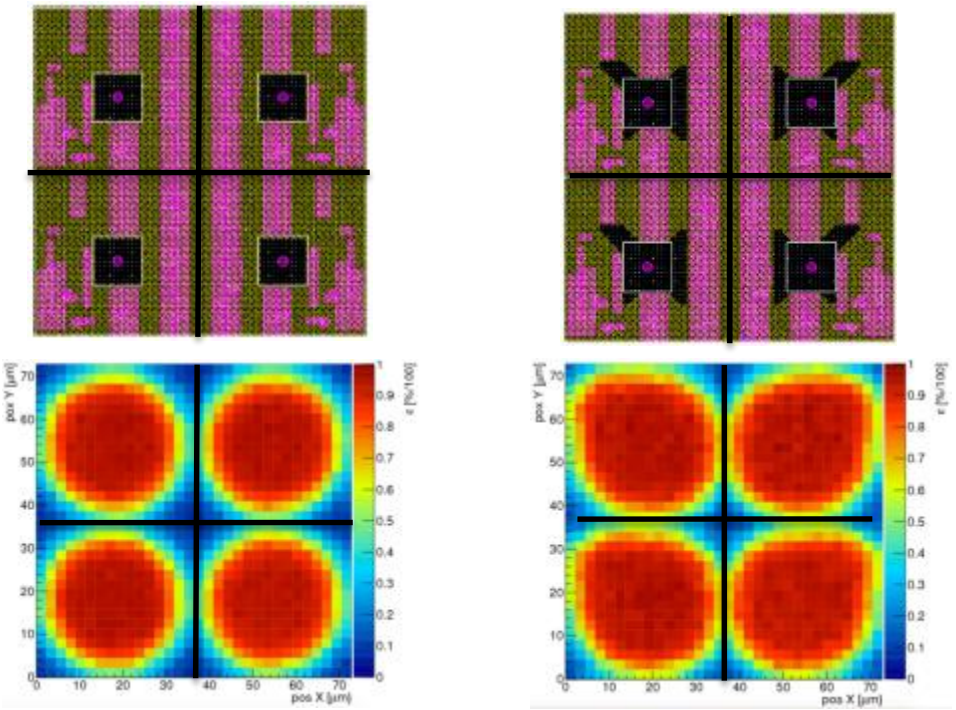
TJ-Monopix, before irradiation



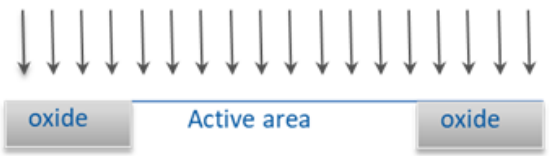


Uni-Bonn (Preliminary)

MALTA, **after irradiation**



A. Sharma, et al., VERTEX 2018



- TJ-Monopix: low efficiency corners coincide with large active area
- MALTA: efficiency depends on deep pwell configuration
- Modifications inspired and verified by TCAD (next slide)

Fixes to improve efficiency after irradiation

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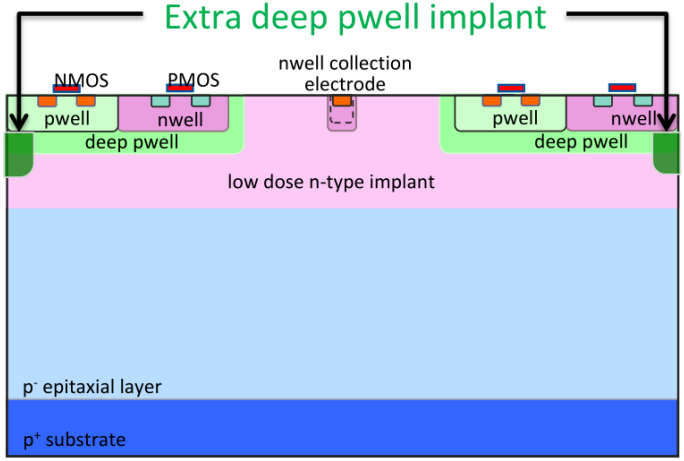
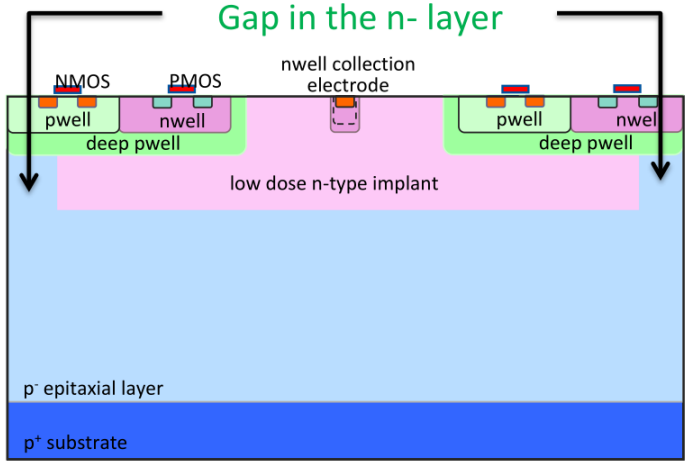
Extra deep pwell implant



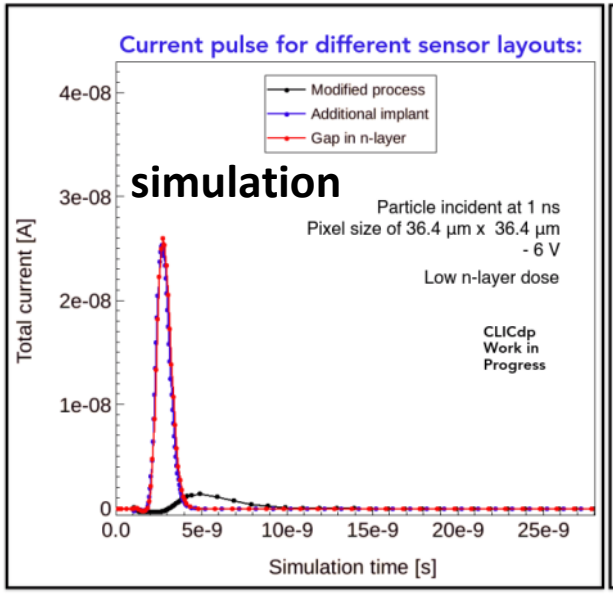
Gap in the n- layer

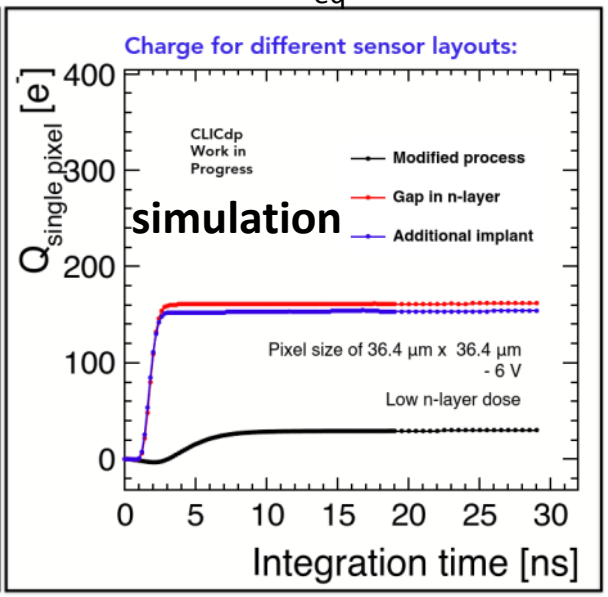


T. Kugathasan, et al., VERTEX 2018

Preliminary, M. Munker

TCAD simulation after irradiation ($10^{15} n_{eq}/cm^2$)





Reminder: simulation of worst case for particle impinging at pixel corner

- Simulation shows significantly improved charge collection time and less charge loss after irradiation with both proposed fixes
- New design with both fixes submitted in August 2018

Summary

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- Rapid progress on R&D of **D**MAPS for **high radiation** & **high rate** environment
  - *Aiming at the **outermost pixel layer** of ATLAS ITk @ HL-LHC => low cost, easy assembly*
  - ***Large demonstrator** chips exist in several technologies*
- Two sensor concepts pursued by the ATLAS ITk community
  - ***Large** electrode designs are intrinsically radiation hard*
    - High efficiency after 1 x $10^{15} n_{eq}/cm^2$
    - Promising timing, but not yet fully in time efficient (25 ns)
  - ***Small** electrode design offers low power and smaller pixels*
    - Low efficiency @ pixel corner after irradiation for the current iteration
    - Fixes implemented recently in MPW
- Still many work towards a ATLAS ready chip
  - *Faster timing for in-time efficiency > 95% after irradiation*
  - *Chip integration and verification*
  - *System level aspects: serial powering, data link, sensor bias, ...*
  - *The future is not only exciting, but also challenging…*

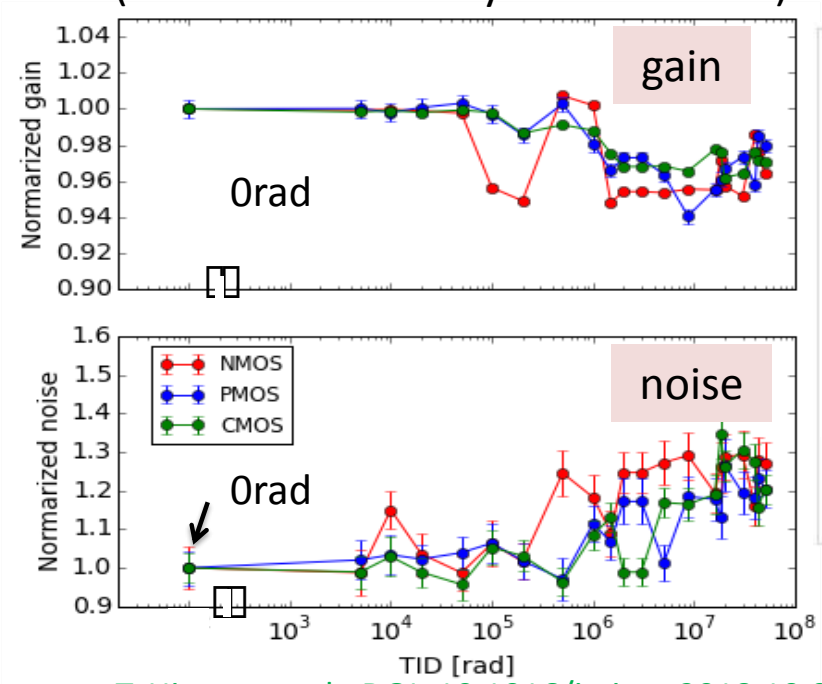
Thank you!

Back up

TID

- Deep sub-micro meter CMOS technology also offer good TID tolerance
  - Combined with radiation hard by design for sensitive blocks

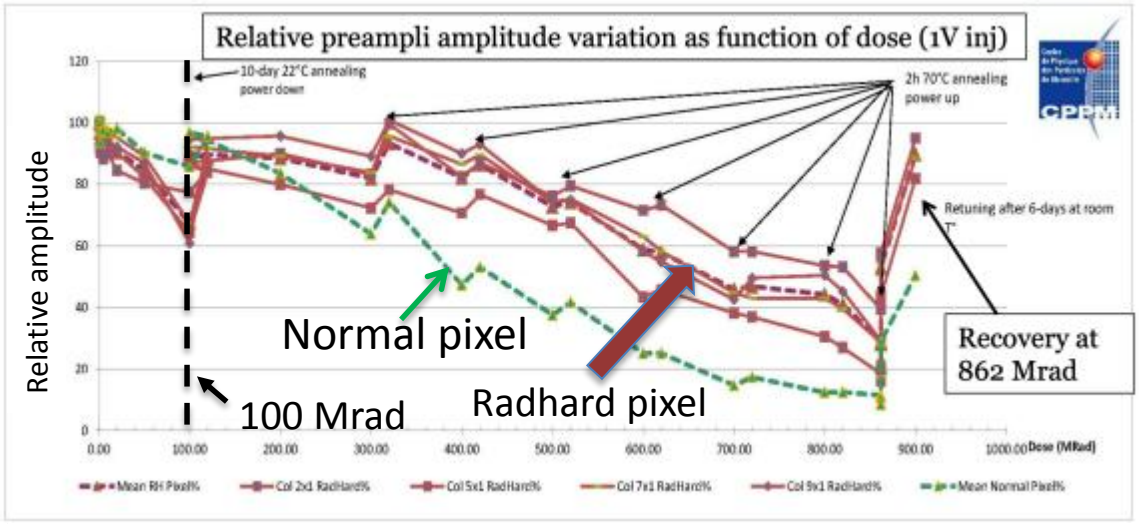
X-ray irradiation
(**LF-CPIX** – LFoundry **active sensor**)



T. Hirono, et al., DOI: 10.1016/j.nima.2018.10.059

- No significant performance loss after 50 Mrad

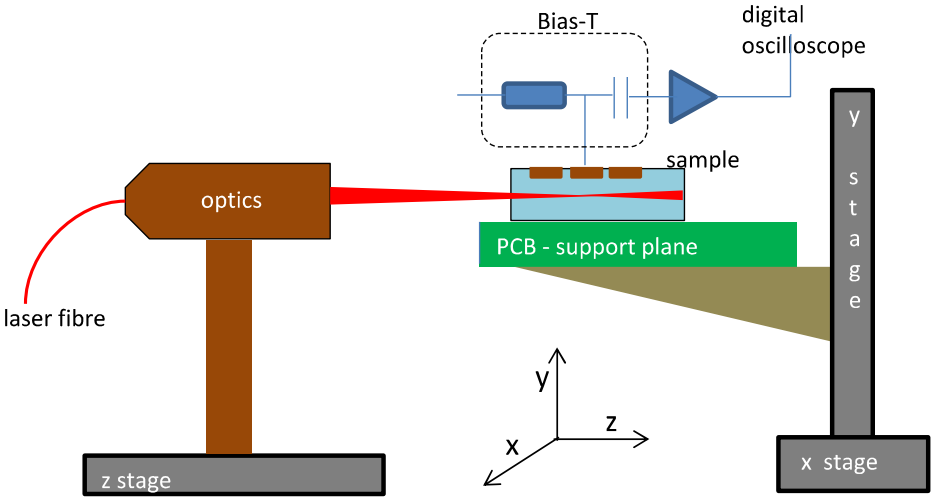
X-ray irradiation
(**HV2FEI4** – AMS **active sensor**)



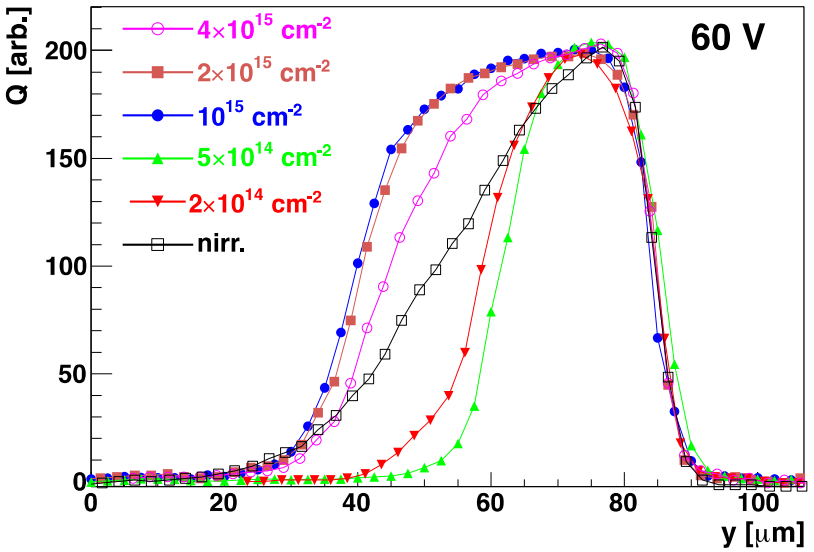
M. Barbero, et al., ATLAS HV-MAPS Workshop 2015

- Alive after over 800 Mrad
- Signal response improved by radiation hard design at high radiation level

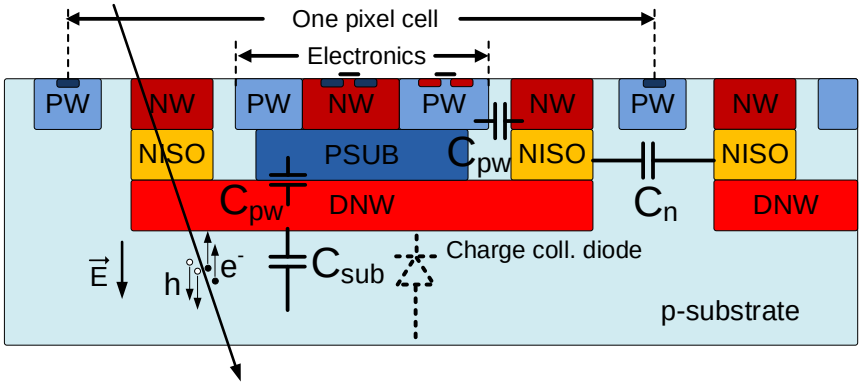
Edge TcT

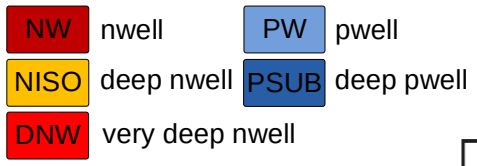


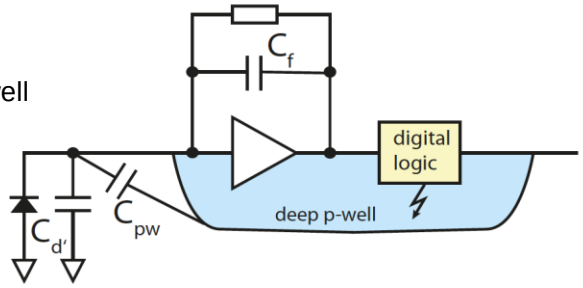
A. Affolder, et al., DOI: 10.1088/1748-0221/11/04/P04007



Design challenges for LF-Monopix







- Large detector capacitance $C_d = C_{sub} + C_n + C_{pw}$
  - ***C_{pw}*** *tends to be* ***dominant*** ***=>*** *depends on electronics area & DNW/PW junction width*
  - *Timing*

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$$

  - *Noise*

$$ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$$

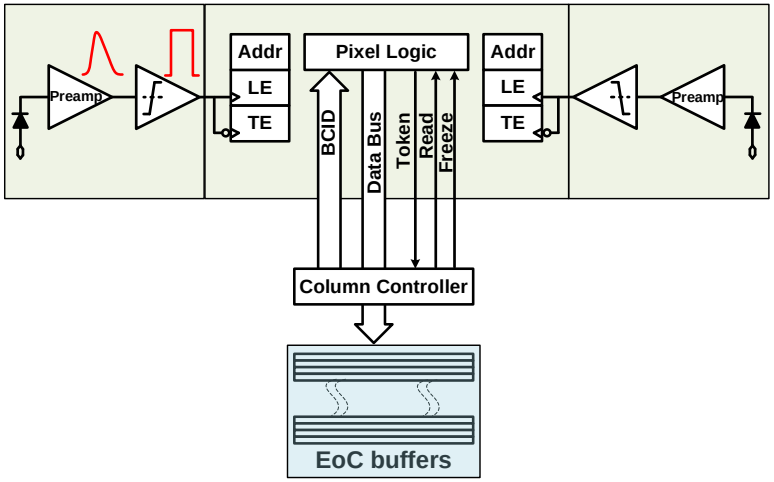
More ***power*** needed to compensate **=>** $g_m \propto I_d$

  - *Cross talk* **=>** *C_{pw} directly couples the substrate noise into the sensor*
    - *The minimum operation threshold may be affected*

Readout architecture – hybrid example

- For high hit rate capability, one would generally need
  - ❑ Small pixel
  - ❑ High logic (memory) density
  - ❑ Fast shaping
  - ❑ High data transmission bandwidth

FE-I3 (250 nm CMOS, 50 x 400 µm^2)

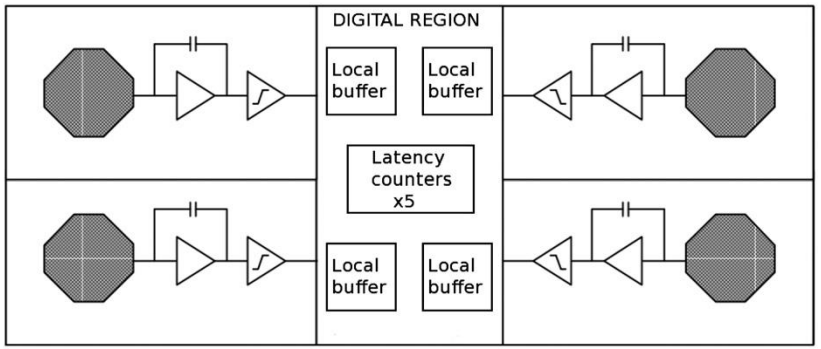


I. Perić, et al., DOI: 10.1016/j.nima.2006.05.032

- The so-called "column drain" readout
- Hit info. recorded in pixel
  => time of arrival (ToA), time over threshold (ToT)
- Hit data transferred over the column bus to EoC buffers following the token-passing scheme
  => double column organization
  => synchronous readout @ 20 MHz
- Hits stay at periphery until trigger latency
  => read out if triggered, discard if not
- Main bottleneck is column bus congestion

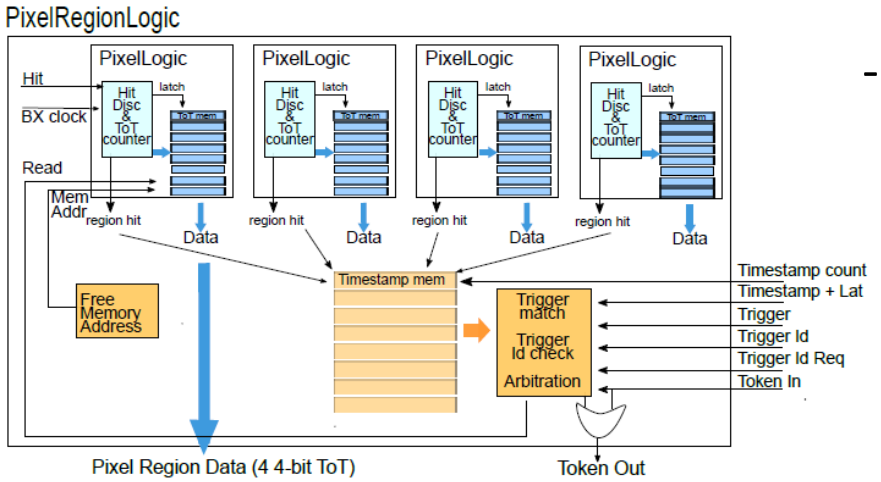
Readout architecture – hybrid example

FE-I4 (130 nm, 50 x 250µm^2)



M.Garcia-Sciveres, et al., DOI: 10.1016/j.nima.2010.04.101

RD53A (65 nm, 50 x 50µm^2)



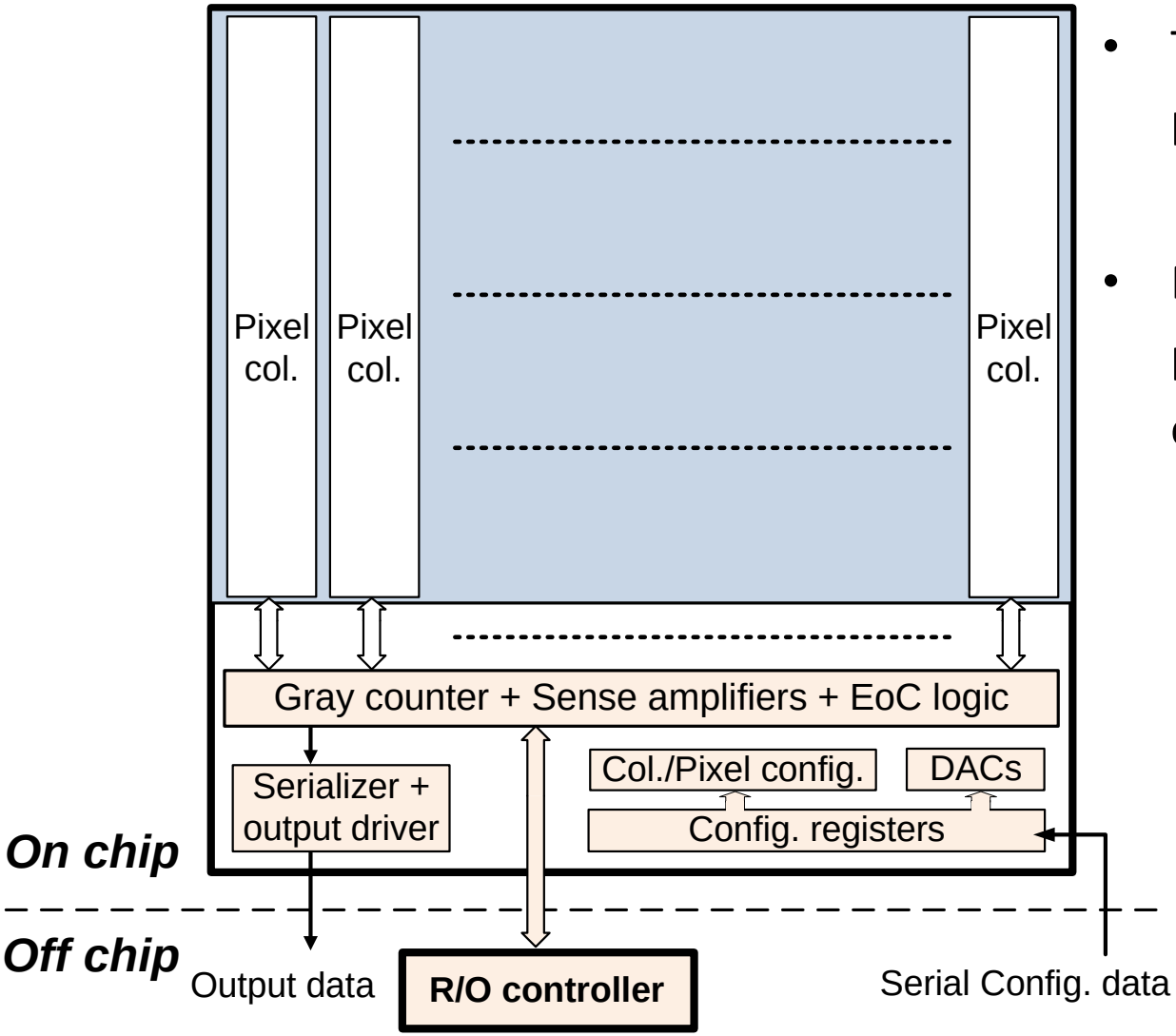
RD53 Collaboration, CERN-RD53-PUB-17-001

- Local hit storage within the matrix
  => use memory efficiently by grouping pixels into regions and exploiting the cluster feature of hits
- Hits stay in matrix until trigger latency
  => local trigger management
- Only transfer triggered hits to the periphery
  => relaxed column bus bandwidth requirement
- Higher logic density & smaller pixel achieved by exploiting deeper sub-micro tech. nodes

Note1: complex in-pixel logic is hard for DMAPS

Note2: logic density of hybrid always > monolithic

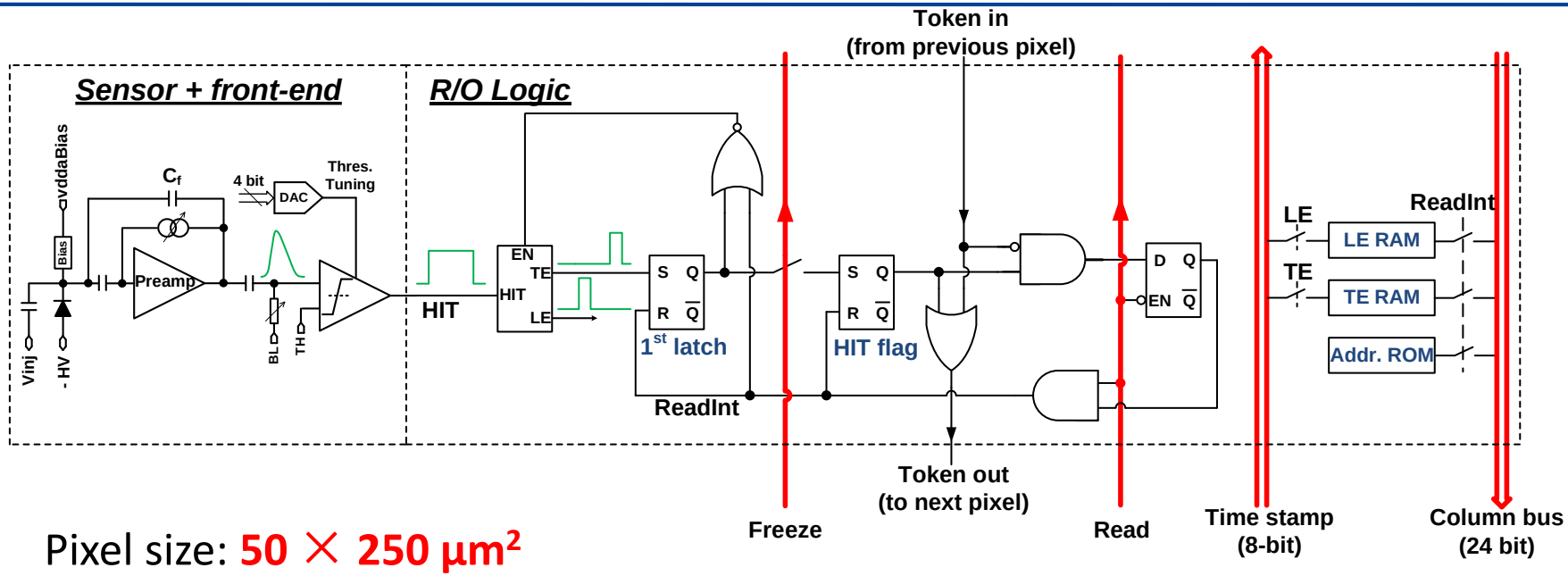
Chip design strategy – LF/TJ-Monopix



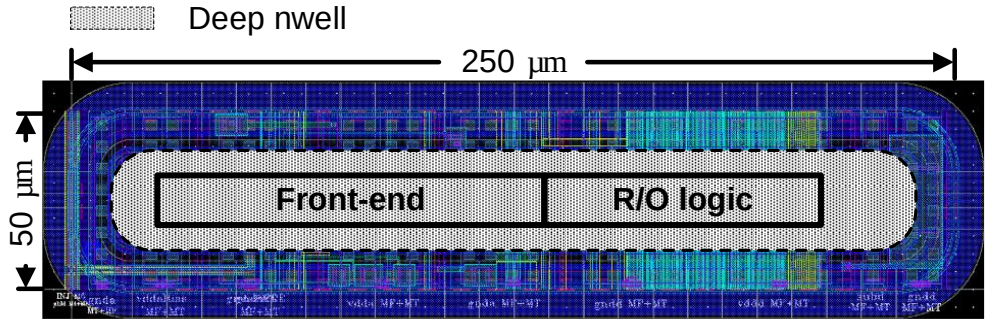
- The goal is to demonstrate a large pixel array with column drain r.o.
  - 1 - 2 cm^2 chip size
- For design simplicity, not all the peripheries expected for the final chip are included
  - *Off-chip r.o. controller by FPGA*
  - *No trigger memory on chip*

    => All hits r.o. sequentially via a serial link
  - *No high speed (Gbps) link, serial powering, etc.*

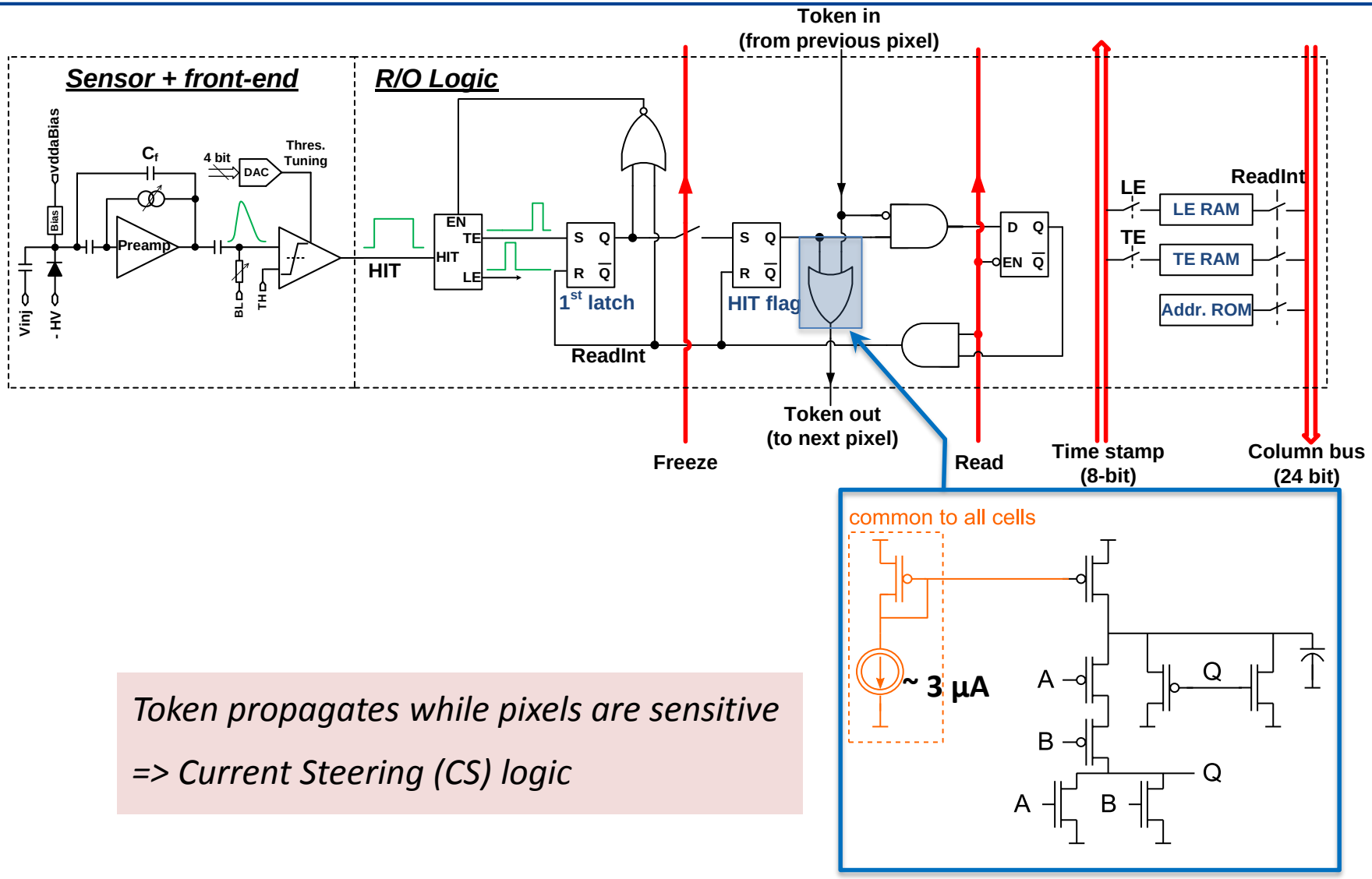
Pixel design: LF-Monopix



- Pixel size: **50 × 250 µm²**
- Fill factor **~ 55%**
- CSA + Discri. with **4-bit DAC**
  - *Optimized for **< 25 ns** time walk*
  - *Static current **~ 20 µA/pixel***
- **Full-custom** dig. Circuit
  - *Minimized area => reduce C_d*
  - *Special **low noise design**, e.g. current steering circuit*



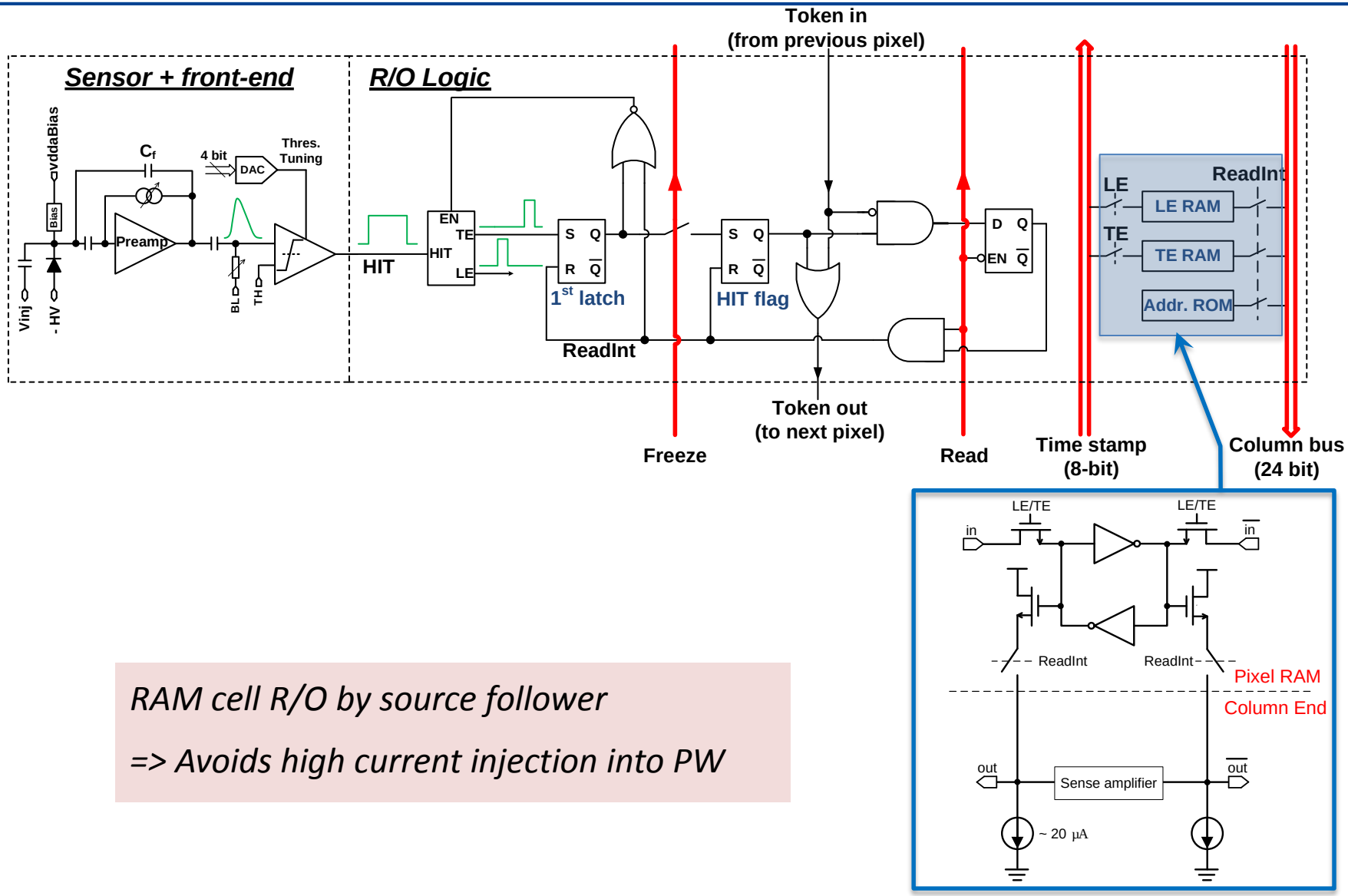
Pixel design: LF-Monopix



Token propagates while pixels are sensitive

=> Current Steering (CS) logic

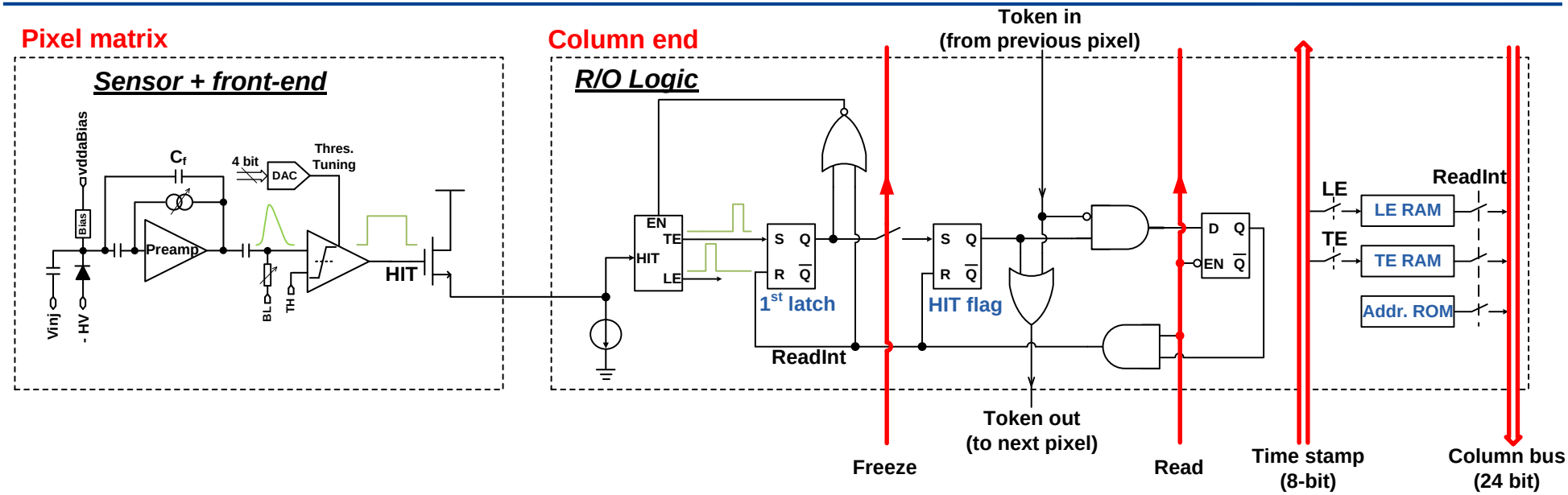
Pixel design: LF-Monopix



RAM cell R/O by source follower

=> Avoids high current injection into PW

Pixel design: LF-Monopix

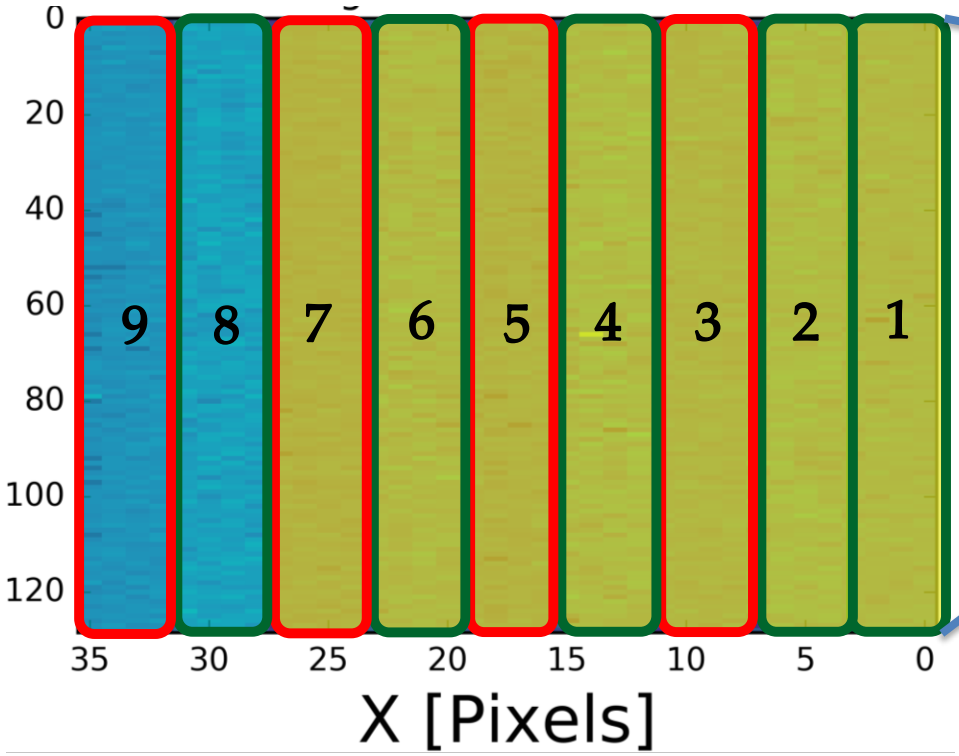


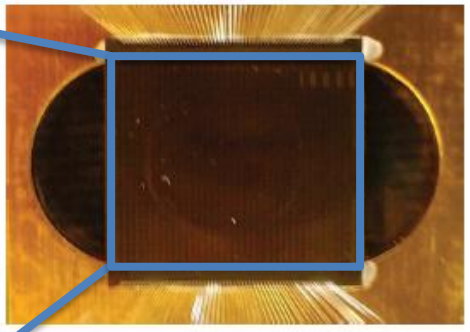
- We can move the in-pixel r.o. logic to the periphery
  - *Discriminator output r.o. by source follower*
  - *Less area needed for in-pixel electronic => less C_d*
  - *Almost no in-pixel digital transient*
  - *Almost no signal distributed in the column*

  } => *less* noise/cross talk

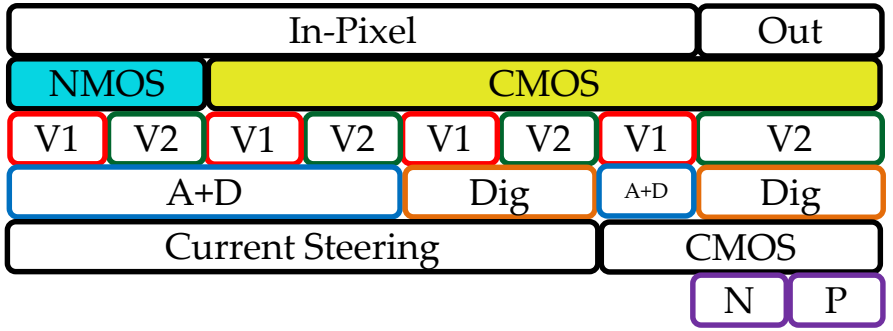
  - *One-to-one connection from pixel to R/O logic => Complex routing*

Matrix overview



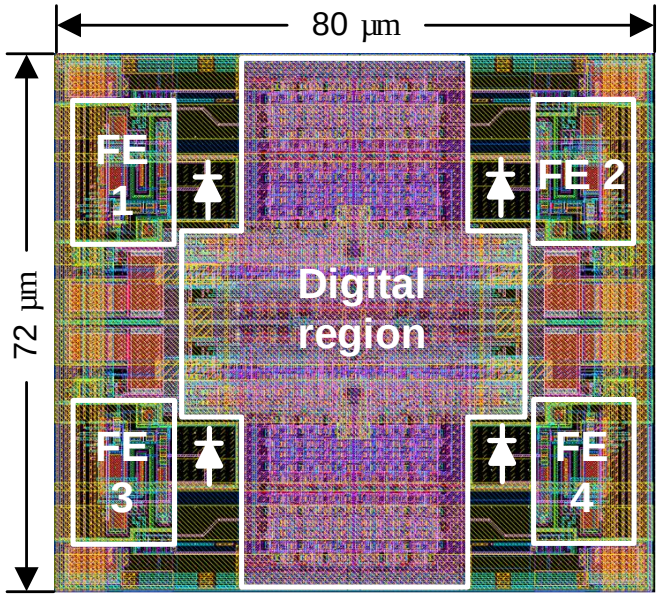


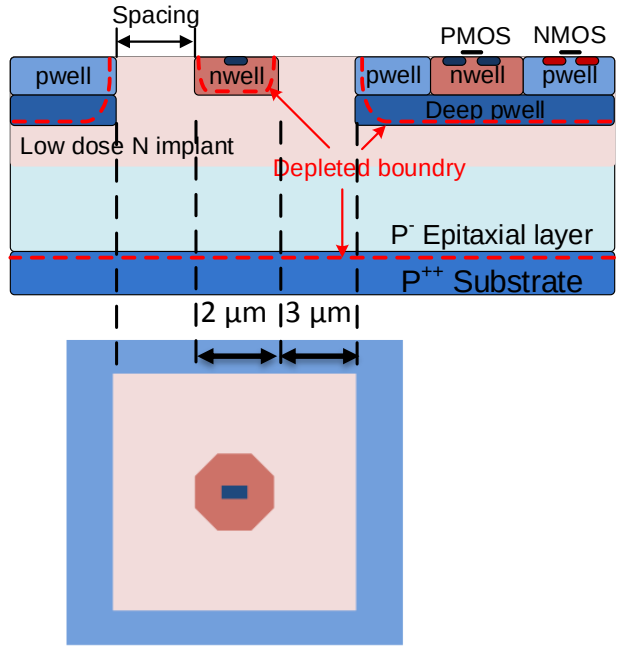
- Matrix size 129 × 36
- 9 pixel designs
  - Each has 4 columns
  - 1 - 2: binary pixel
  - 3 - 9: pixel with R/O logic



R/O logic
Amplifier (CSA)
Discriminator
Discri. power domain
Token
Source Follower

Pixel design: TJ-Monopix

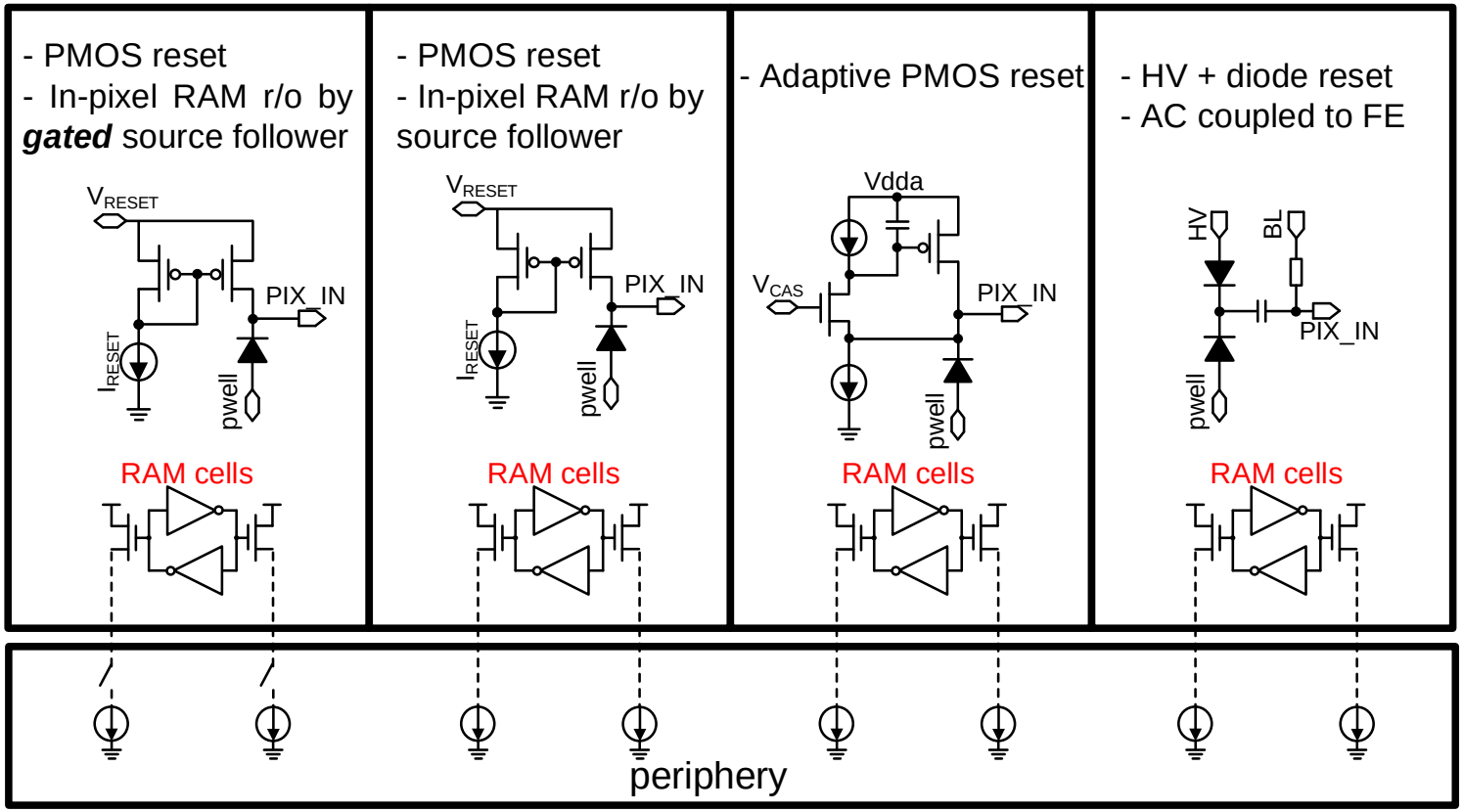




- Pixel size **36 × 40 µm²** => smaller than large fill factor design
- Small sensor footprint: **2 µm** diameter diode + **3 µm** spacing
- Separate digital & analog region
- **Full-custom** digital design
  - *Minimize area*

Pixel array: TJ-Monopix

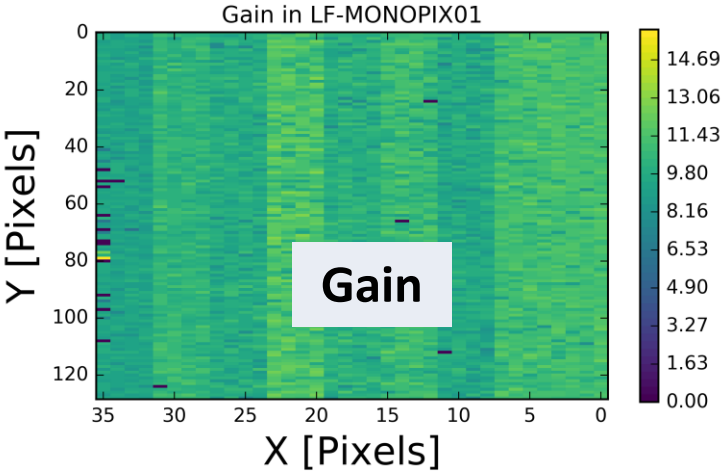
- Pixel array 224 × 448, composed of equally divided 4 sub arrays



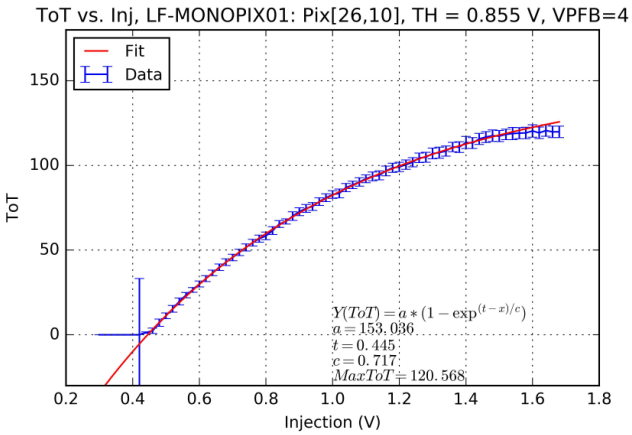
Laboratory results – LF-Monopix

- Breakdown @ **-280 V** => up to ~ 300 µm depletion
- ToT calibrated with sources: ^{241}Am, terbium
- Gain **10 -12 µV/e$^-$**
- Typical ENC ~ **200 e$^-$**
- Tunable threshold down to **1400 e$^-$**
  - dispersion ~ **100e$^-$**

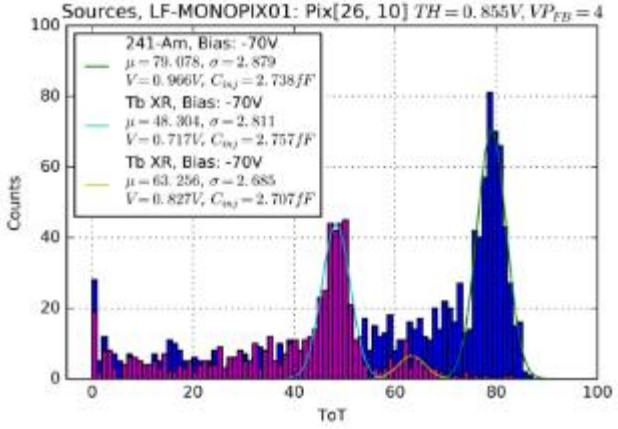
I. Caicedo, Bonn

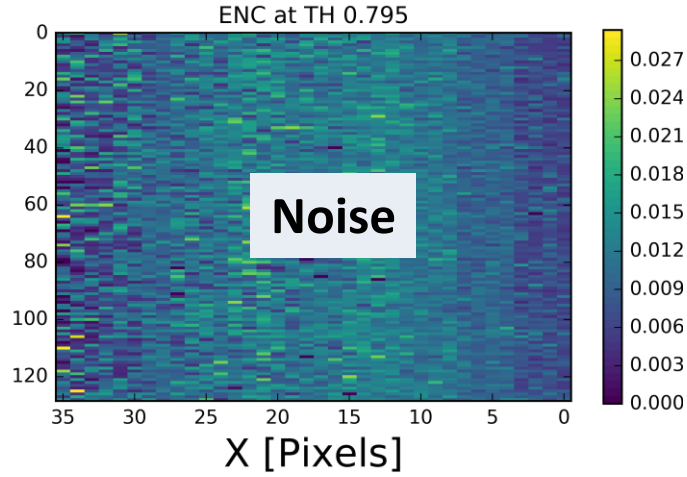


ToT vs. Injection

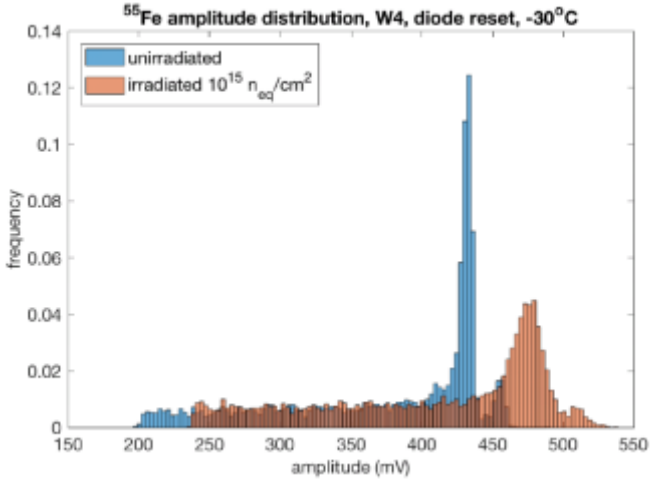


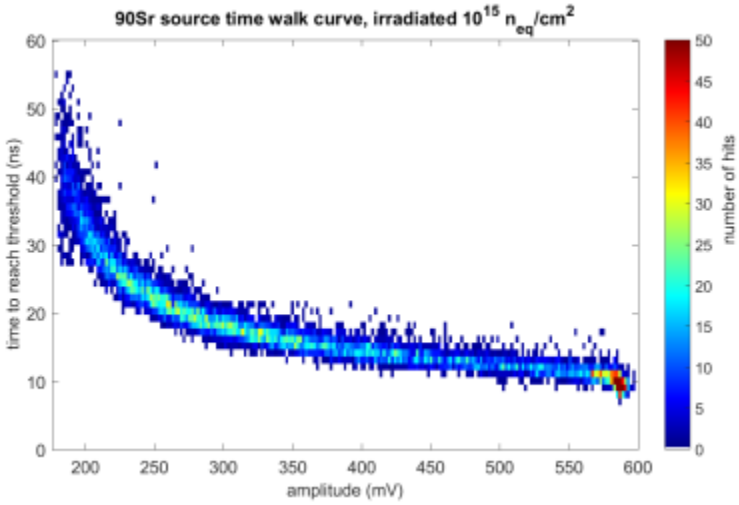
Response to sources

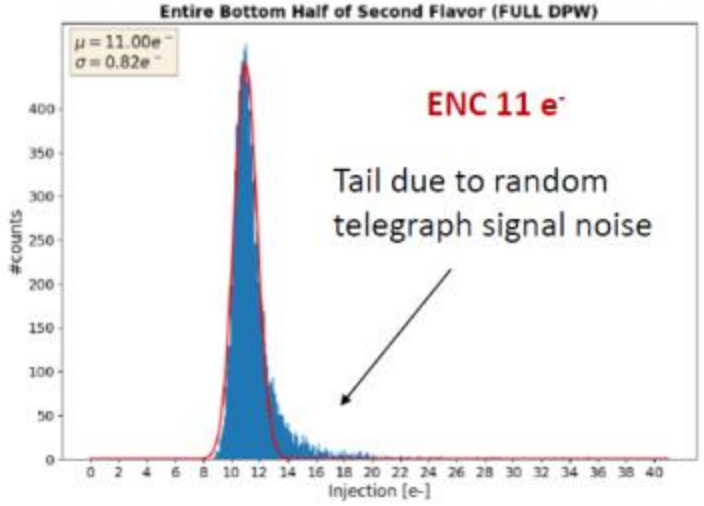


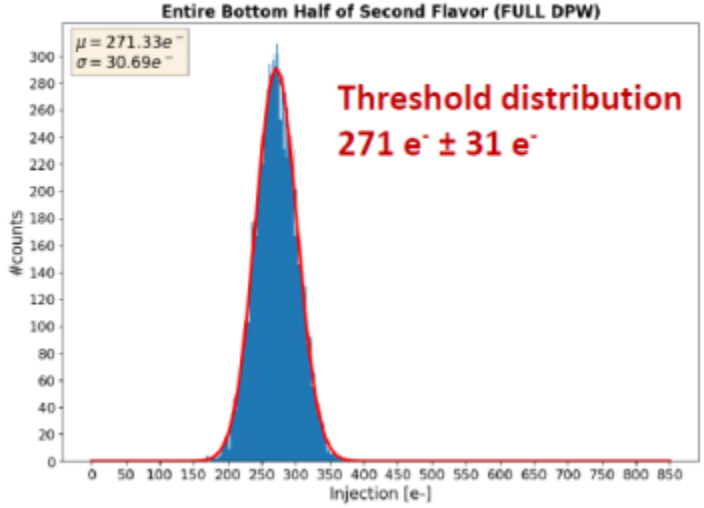


MALTA & TJ-Monopix – FE performance



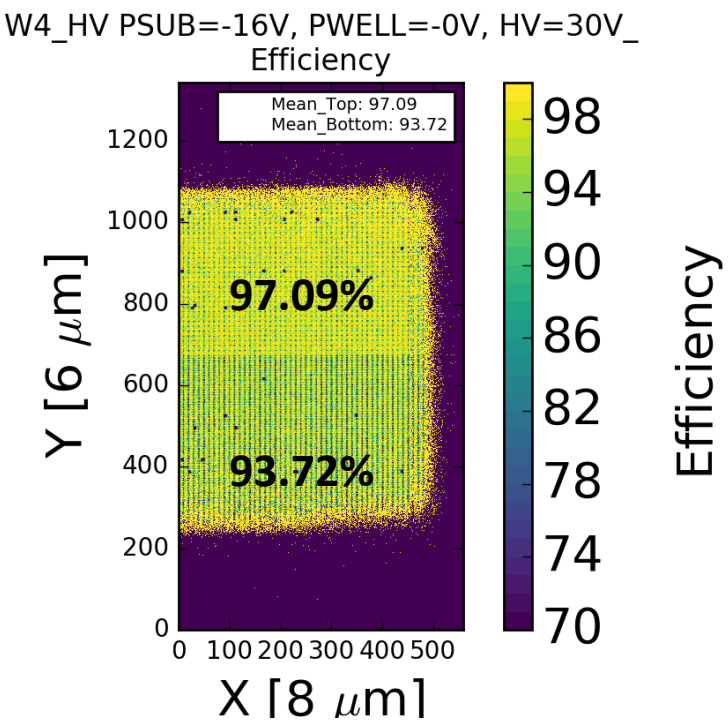




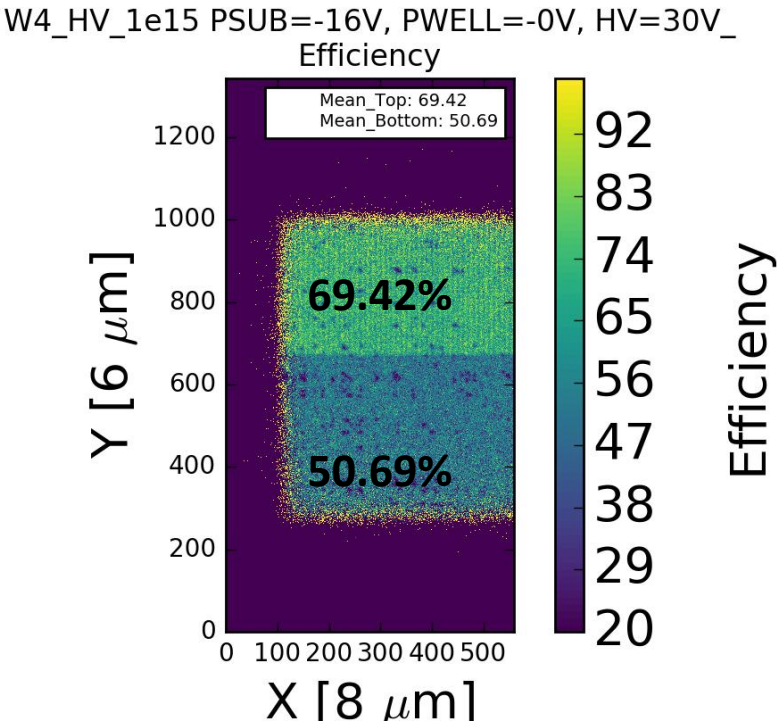


TJ-Monopix – efficiency

- Non-irradiated

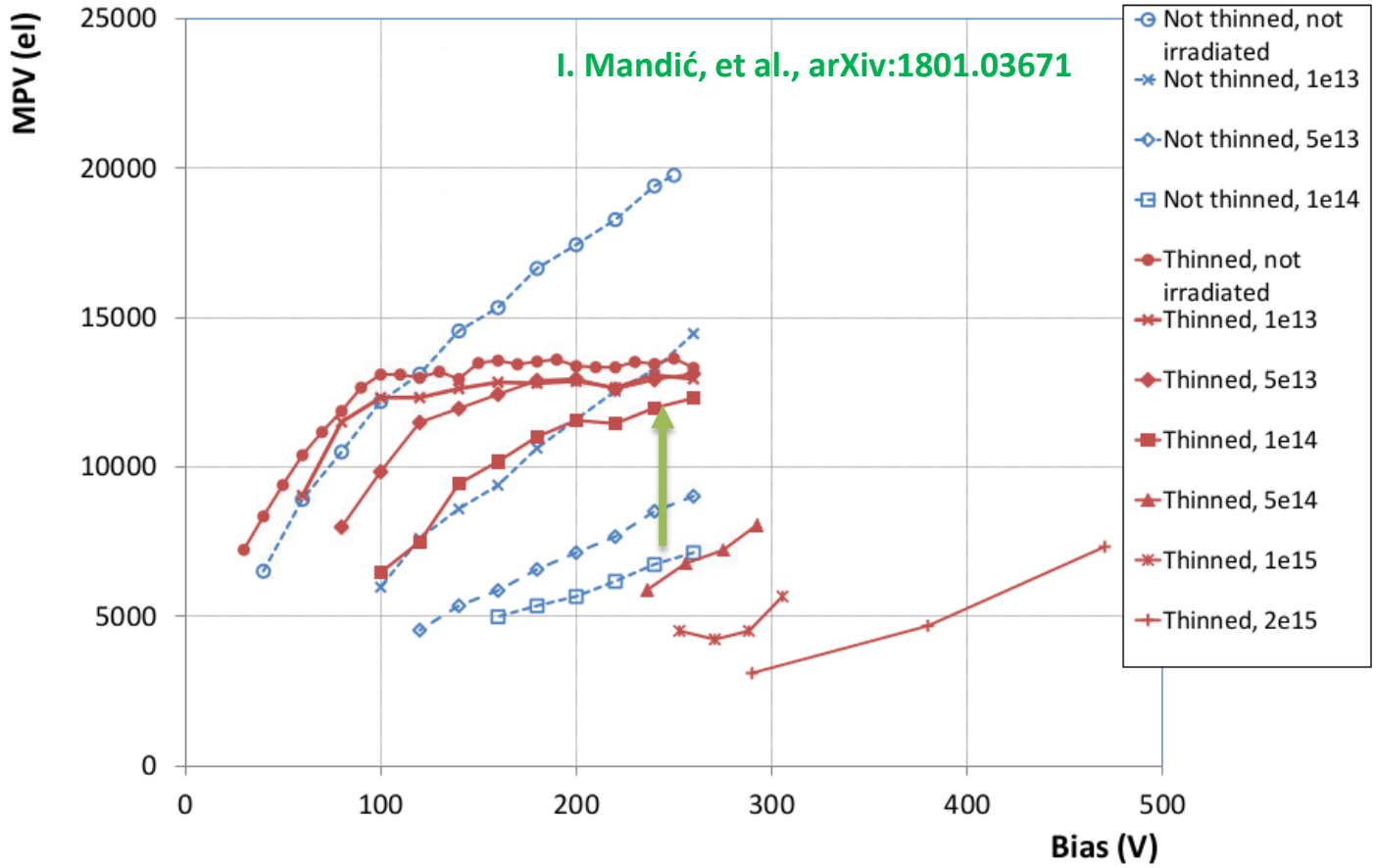


- $1 \times 10^{15} n_{eq}/cm^2$



- Lower efficiency for region with full deep P well
- Min. operational threshold increased after irradiation
  - ~ 350 e^- before irrad. & ~ 550 e^- after irrad.

Improvement after back-side processing



Rate capability of TJ-Monopix – the matrix

- It is assumed that in the final prototype
  - 2 double columns per r.o. unit **=>** 512 × 4 pixels
  - 20 MHz column bandwidth: **50 ns (2 BC)** per hit readout

    => a simple math: max. allowed hit rate = 1/column bandwidth = **0.5 hit/r.o.unit/BC**
- Inefficiency caused by trig. memory pileup not included here **=>** pure matrix performance
- Data loss increases steeply beyond **600 MHz/cm² => ~ 0.44 hits/r.o.unit/BC**