环形正负电子对撞机
Circular Electron Positron Collider

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Pixel design and prototype characterization in China

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On behalf of Vertex sub-detector group

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Outline

- Introduction
  - CEPC Silicon tracker
- Fine pixel
  - JadePix1/2, MIC4, CPV1/2
- Pixelated strip
  - SUPIX
- Summary

Note1: This talk covers only the pixel chips developed specifically for the CEPC, while other developments such as for X-ray applications are not included.

Note2: A fast timing pixel scheme to be presented by W. Wei in the TDAQ session

CEPC and Its Beam Timing

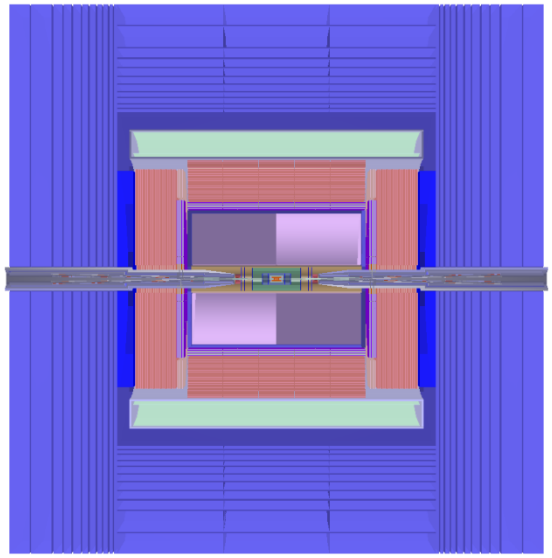
	Higgs	W	Z (3T)	Z (2T)
Center-of-mass energy (GeV)	240	160	91	
Number of IPs	2			
Luminosity/IP (10^{34} cm^{-2} s^{-1})	3	10	16	32
Number of years	7	1	2	
Total Integrated Luminosity (ab^{-1}) - 2 IP	5.6	2.6	8	16
Total number of particles	1×10^{6}	2×10^{7}	3×10^{11}	7×10^{11}
Bunch numbers (**Bunch spacing**)	242 (**680 ns**)	1524 (**210 ns**)	12000 (**25ns + 10% gap**)	

- Continuous colliding mode
  - Duty cycle ~ 50% @ Higgs, close to 100% @ W/Z
- General requirement on the detector development:
  - Precise measurement, Low power, Fast readout, Radiation-hard

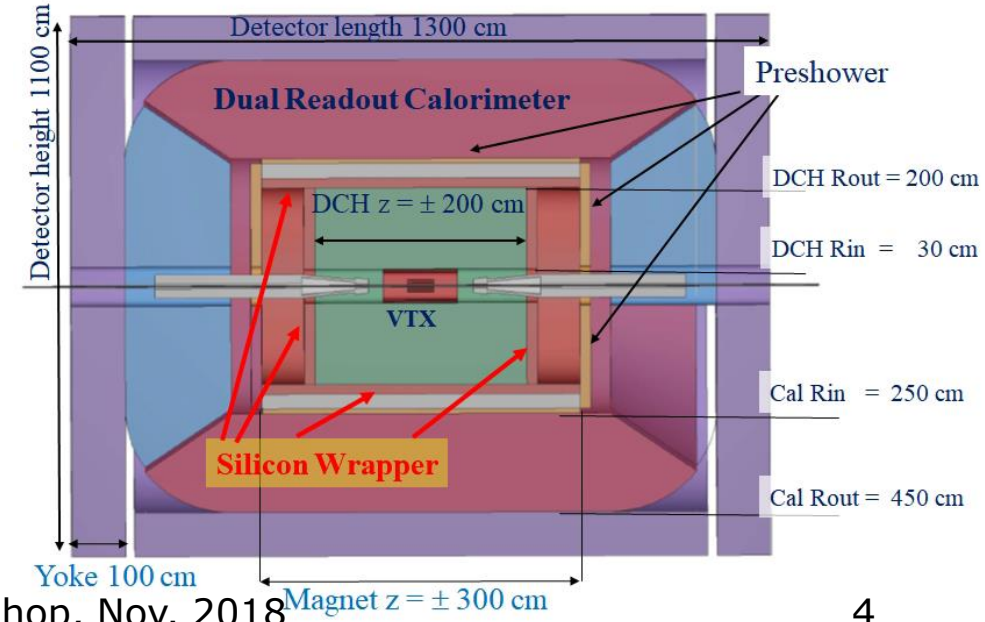
Two Detector Concepts

- Baseline detector concept
  - Silicon tracker + TPC

  or Full Silicon Tracker
  - High granular calorimetry system
  - 3 Tesla solenoid
  - Muon detector



- Alternative detector concept, IDEA
  - Silicon pixel + Drift Chamber
  - 2 Tesla solenoid
  - Dual readout calorimeter
  - Muon chamber

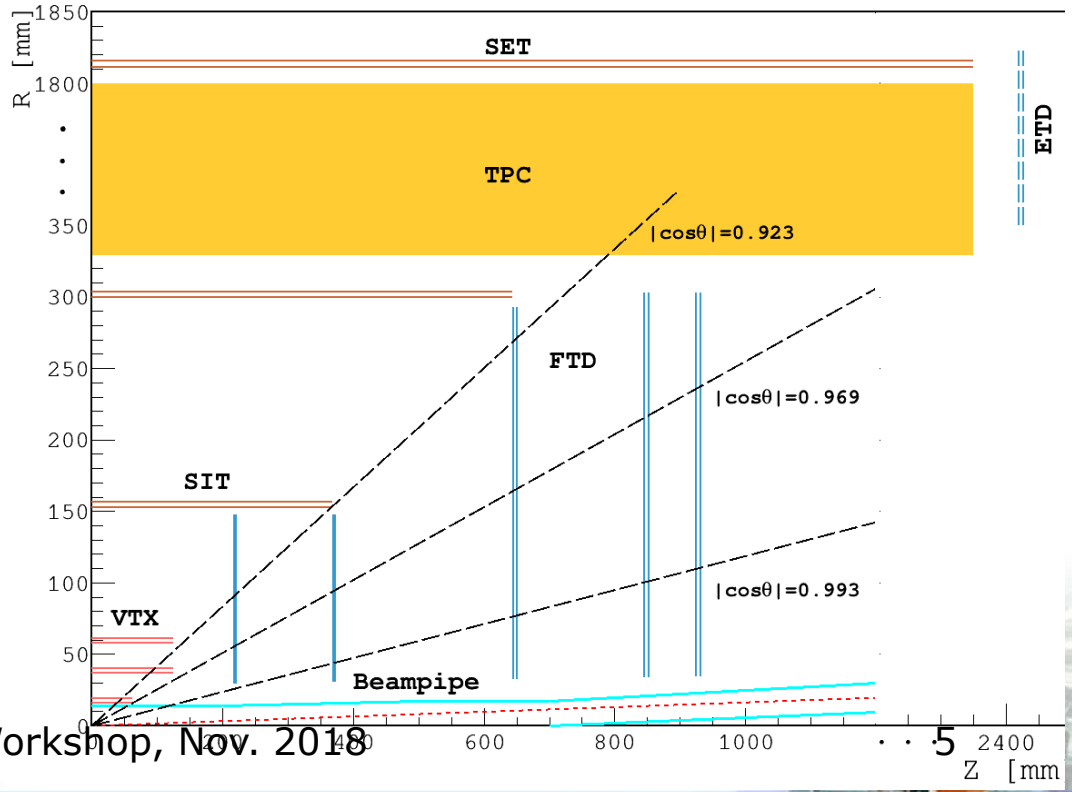


Baseline Silicon Tracker Layout

- Tracking part: Mainly microstrip
  - SIT, SET, ETD, and 3 outer disks of FTD, ETD: single-sided strips mounted back to back
  - 2 inner disks of FTD: pixel
- Vertex part: 3 double-sided pixel layers
  - Layer 1: best s.p. resolution
  - Layer 2: very fast readout

VTX parameters

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	$\sigma(\mu m)$
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4



Performance Requirements

B = 3T

- Momentum Resolution: $\sigma_{1/p_T} = 2\times10^{-5} \oplus 1\times10^{-3}/(p_T \sin\theta)$
- Impact Parameter Resolution: $\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$

- Vertex specifications:
  - σ_{SP} near the IP: ≤ 3 μm
  - Material budget: ≤ 0.15% X_0 / layer
  - First layer located at a radius: ~1.6 cm
  - Pixel occupancy: ≤ 1 %
- Tracking specifications:
  - σ_{SP} : ≤ 7 μm
  - Material budget: ≤ 0.65% X_0 / layer

Pixel Sensor Specifications

- To achieve single point resolution
  - Pixel size ~ 16 μm (Binary readout)
- To lower the material budget
  - Sensor thickness ~ 50 μm
  - Air cooling, heat load < 50 mW / cm^2
- To tackle beam-related background
  - Fast readout 1 ~ 100 μs / frame
  - 3.4Mrad / year & $6.2\times10^{12} n_{eq}$ / (cm^2·year)?

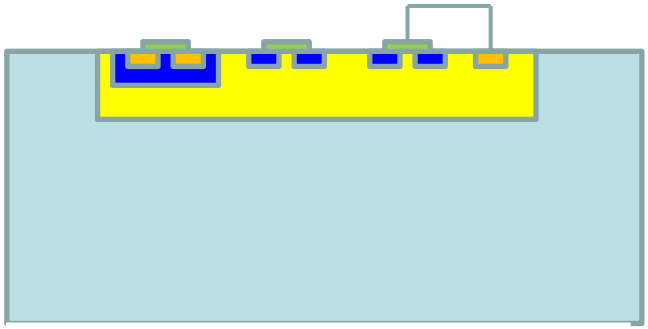
Physics driven requirements		**Running constraints**		**Sensor specifications**	
$\sigma_{s.p.}$	2.8 μm			Small pixel	16 μm
Material budget	0.15% X_0 / layer			Thinning	50 μm
		Air cooling		Low power	50 mW / cm^2
r of Inner most layer	16 mm	beam-related background		Fast readout	1 ~ 100 μs
		radiation damage		Radiation tolerance	*3.4 Mrad / year* *$6.2\times10^{12} n_{eq}$ / (cm^2 year)*

Key factors to low power design

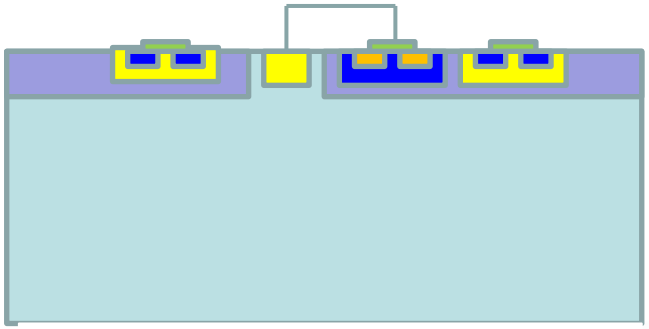
- Depleted sensing diode
  - Signal charge Q ↑ or cluster size ↓
  - Capacitance of the input node ↓
- Small fill factor
  - Capacitance of the input node ↓
- In pixel discriminator
  - Eliminate the large driving current of analog output

$$P \propto I \propto \left(\frac{S/N}{Q/C}\right)^{2\alpha}$$

α = 2 for strong inversion,
α = 1 for weak inversion



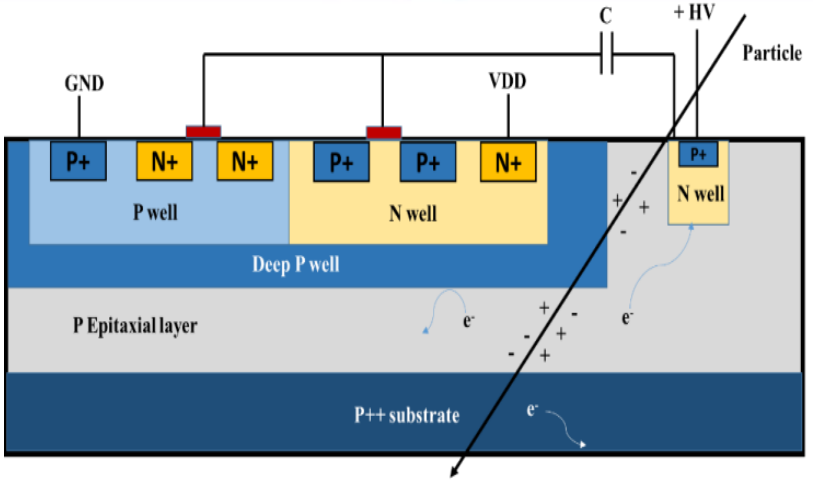
Large fill factor



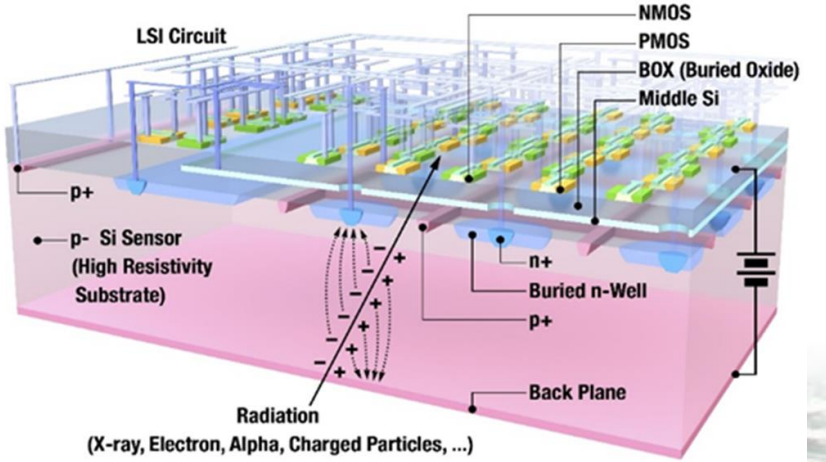
Small fill factor

Pixel technologies

- CMOS pixel sensor (CPS)
  - TowerJazz CIS 0.18 μm process
  - Quadruple well process
  - Thick (~20 μm) epitaxial layer
  - with high resistivity (≥1 kΩ•cm)



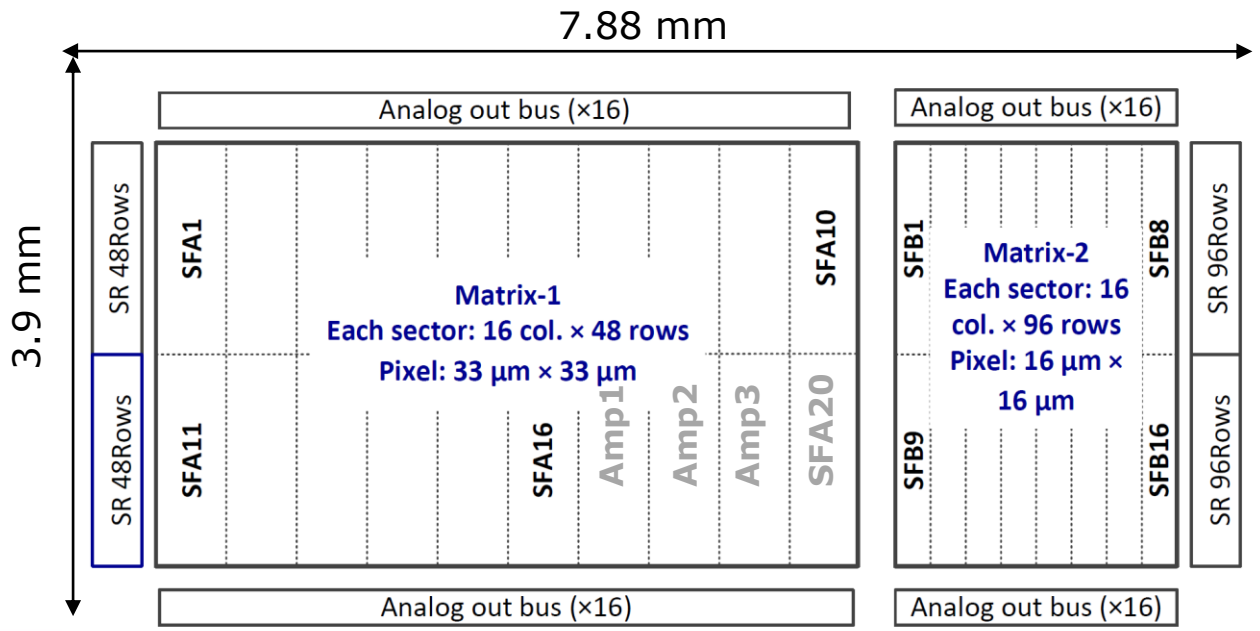
- SOI pixel sensor
  - LAPIS 0.2 μm SOI process
  - High resistive substrate (≥1 kΩ•cm)
  - Double SOI layers available
  - Thinning and backside process



CMOS Prototype: JadePix1

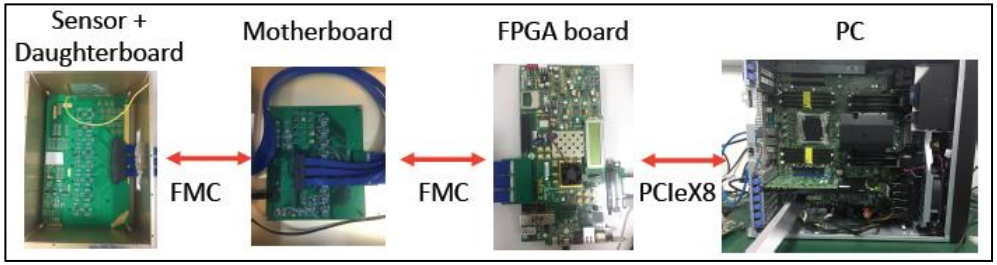
(Team in IHEP)

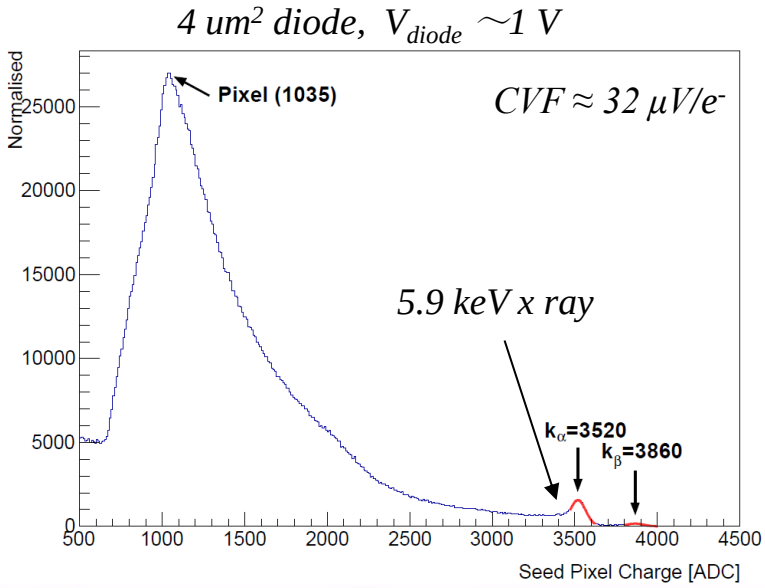
- Diode optimization and radiation hardness study
- Two independent matrices:
  - Matrix-1: 33 × 33 μm^2 pixels
  - Matrix-2: 16 × 16 μm^2 pixels.
- A variety of diode geometries
  - Matrix-1: 20 sectors, each sector includes 48 rows and 16 columns.
  - Matrix-2: 16 sectors, each 96 rows and 16 columns.
- Analog readout
  - Source follower or voltage amplifier
  - Multiplexed to 16 analog output ports

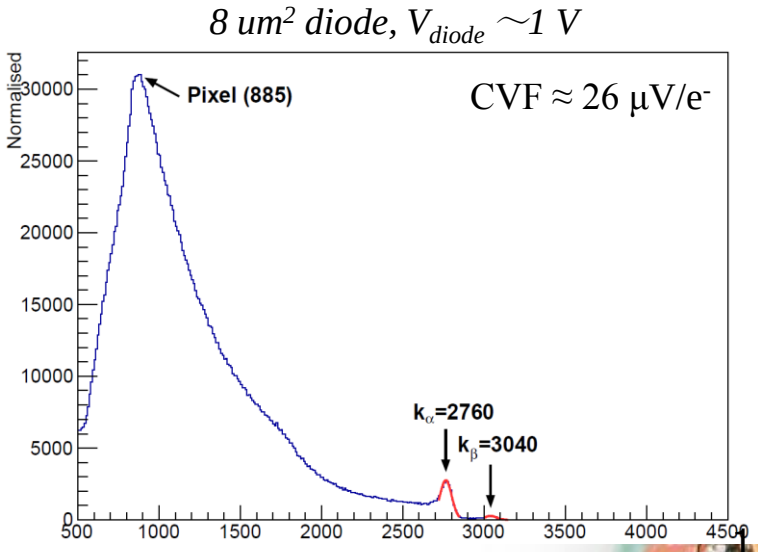


Measurement of Diode Capacitance

- JadePix1 readout system developed at IHEP
- ^{55}Fe calibration
  - K_α = 5.9 keV, K_β = 6.5 keV
  - Charge Voltage Factor (CVF)
- $C_{in} = C_d + C_{parasitic}$
  - C_{in} = 5 fF on 4 μm² diode
  - C_{in} = 6.15 fF on 8 μm² diode

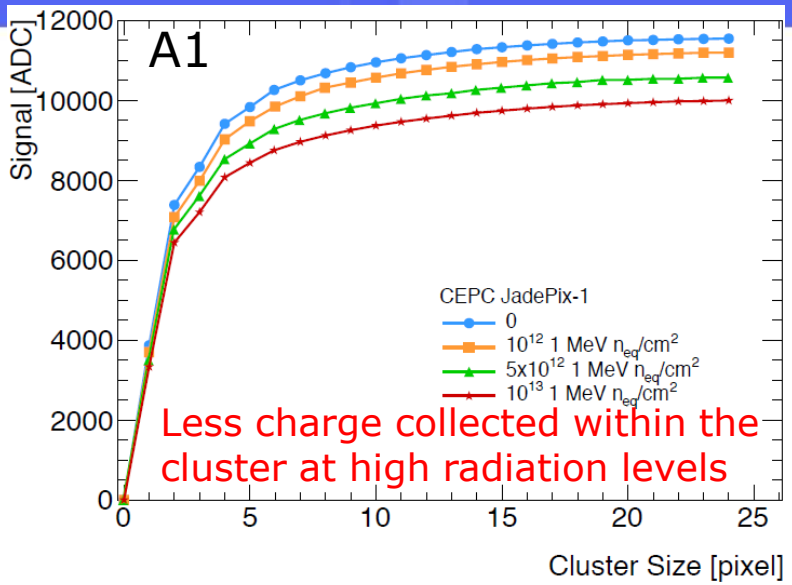


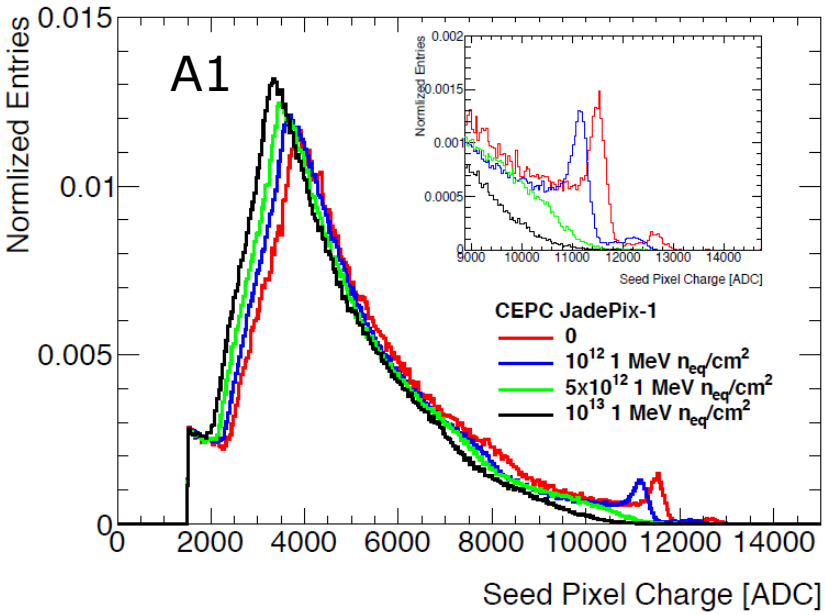


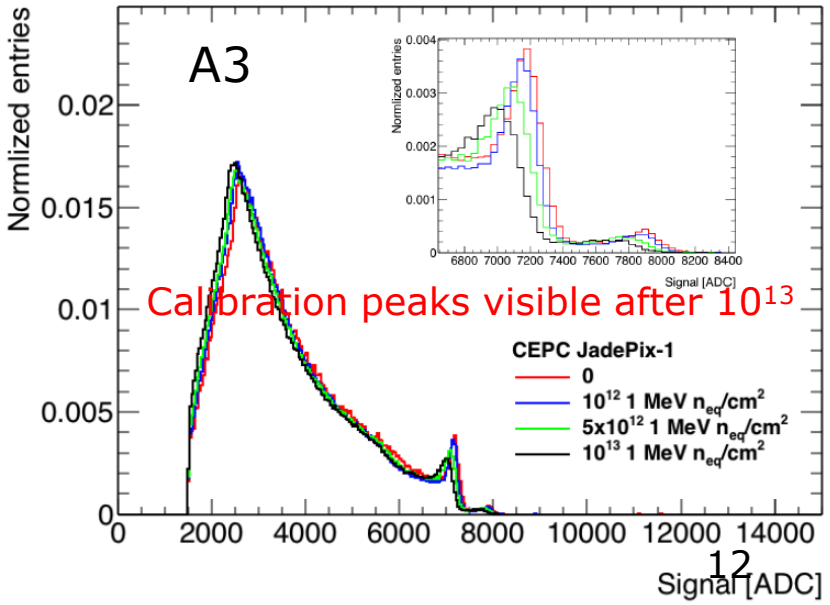


Performance after Irradiation

- JadePix-1 samples irradiated in neutron reactor to 10^{12}, 5×10^{12} and 10^{13} 1MeV n_{eq}/cm^2
- Larger diode (A3 >A1) more radiation hard as expected



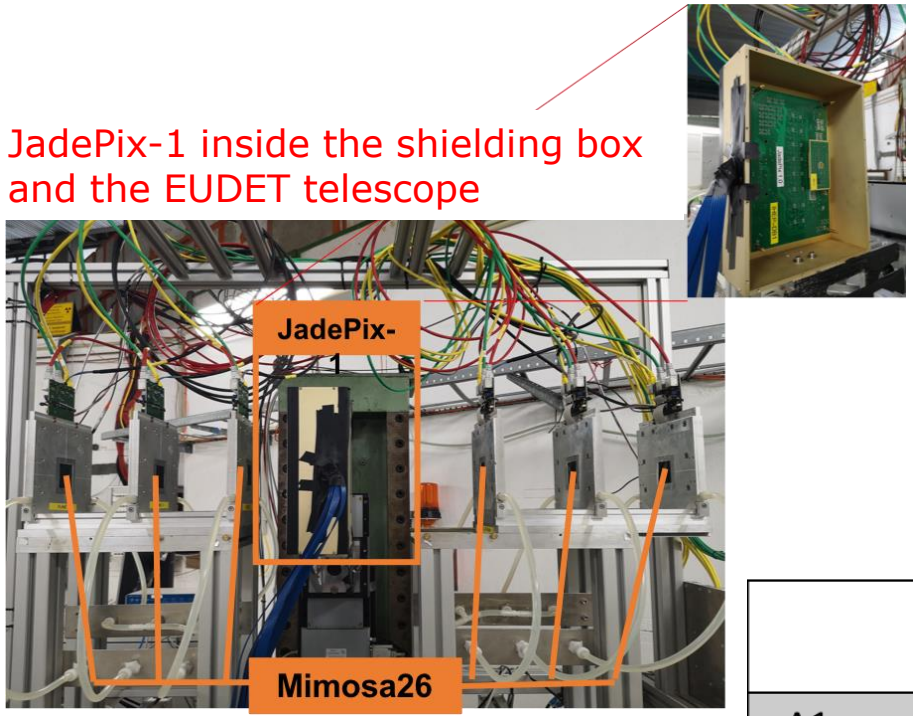




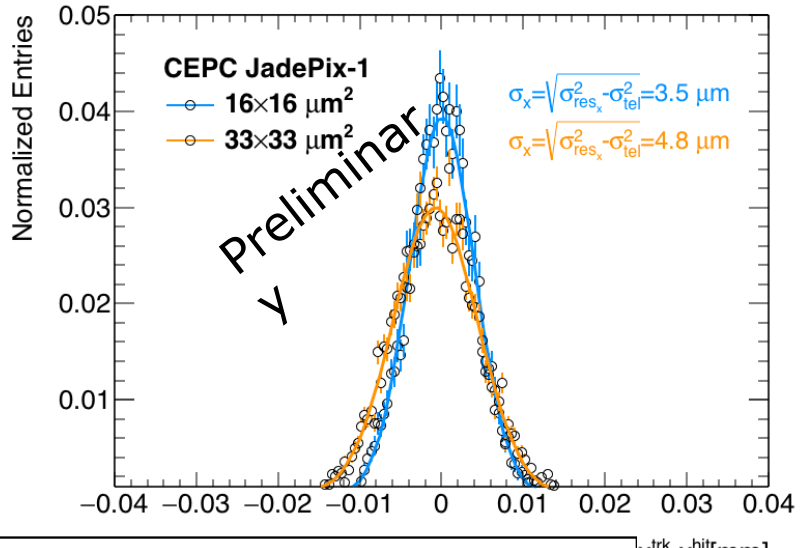
DESY Test Beam

- JadePix-1 position resolution characterized with the EUDET beam telescope and the electron beams at DESY;
- Offline event reconstruction with the EUTelescope software

JadePix-1 inside the shielding box and the EUDET telescope



Resolutions extracted from the residual distributions



	CVF [μV/e]	CCE (^{55}Fe)	S/N (Beam)
A1	33.4	94.39%	64
A2	29.0	95.23%	64
A3	20.8	97.09%	52

*Irradiation and beam test -> poster by L. Chen

Overview of JadePix2

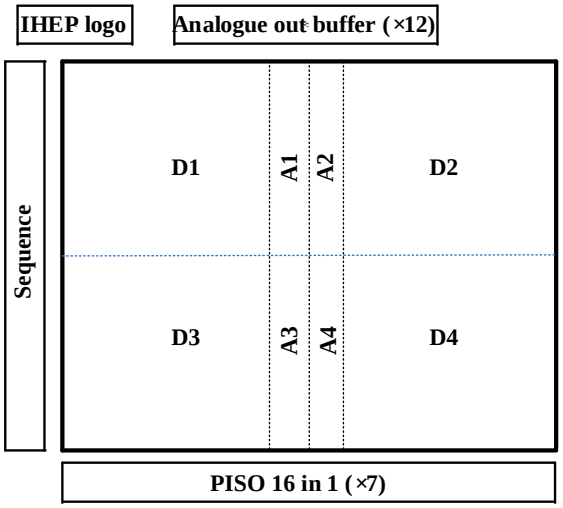
(Team in IHEP)

- Chip area: 3 × 3.3 mm^2;
- Matrix: 96 × 112 pixels with 8 sub-matrix
- Rolling shutter mode
- Every 16 columns of digital pixel share one

LVDS transmitter

  - 160 MHz clock
  - 16-to-1 serializer

- A few columns configured as analog readout
  - For calibration of sensing diode

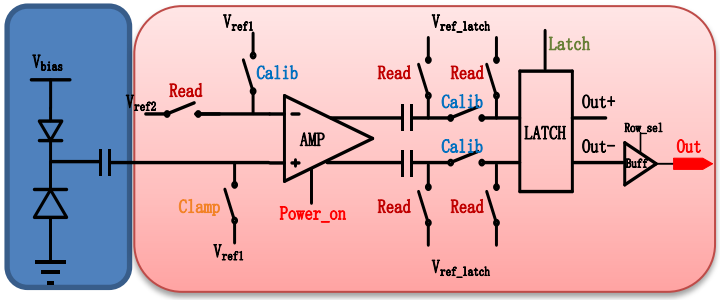


Floorplan of JadePix2

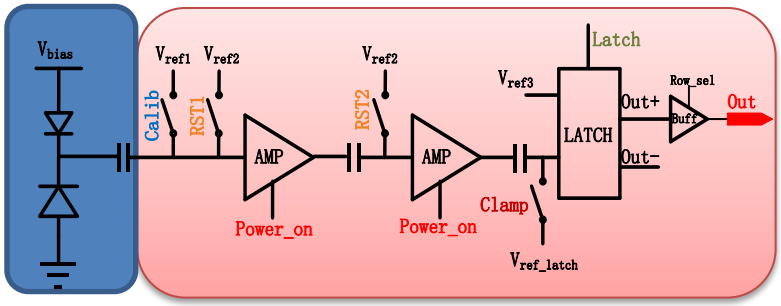
	D1	A1	A2	D2	D3	A3	A4	D4
Diode size	4 μm^2				8 μm^2			
Design Version	2: Single-end		1: Differential		2: Single-end		1: Differential	
Matrix size: ①48 row×44 col. ②48 row×4 col. ③48 row×60 col.	①	②		③	①	②		③

JadePix2: Voltage Discrimination in Pixel

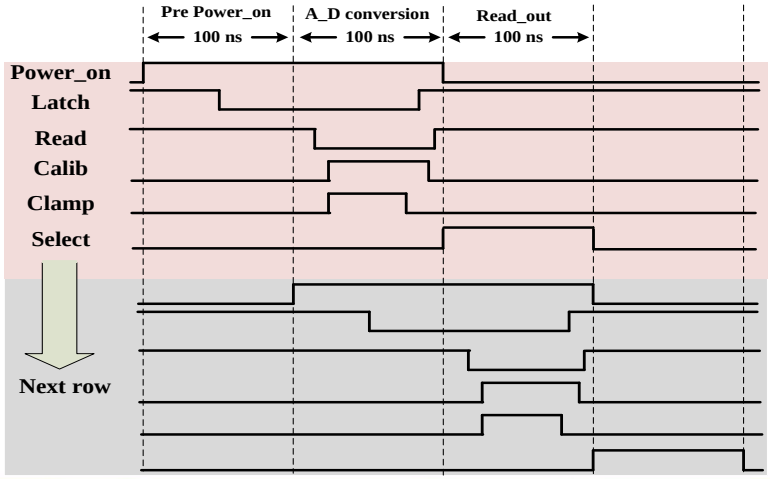
- Two versions of Front-end
  - Version 1: differential amplifier + dynamic latch
  - Version 2: cascaded amplifier (single-ended) + dynamic latch

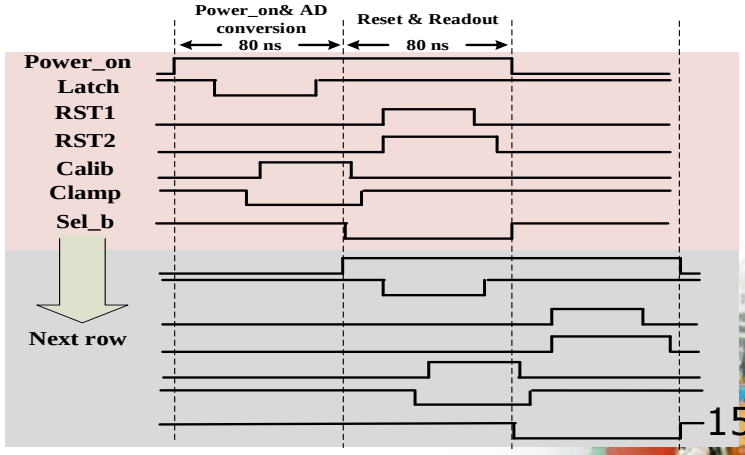


Version 1: differential amplifier + latch



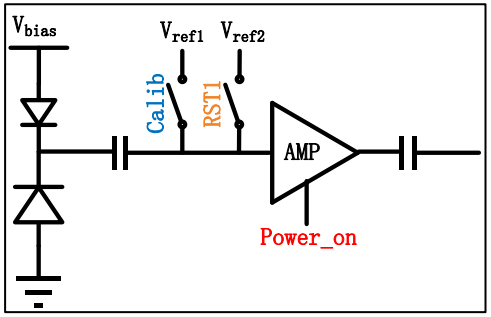
Version 2: two stage CS amplifiers + latch

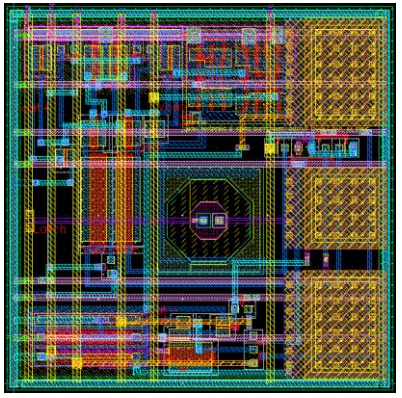




Design results of JadePix2

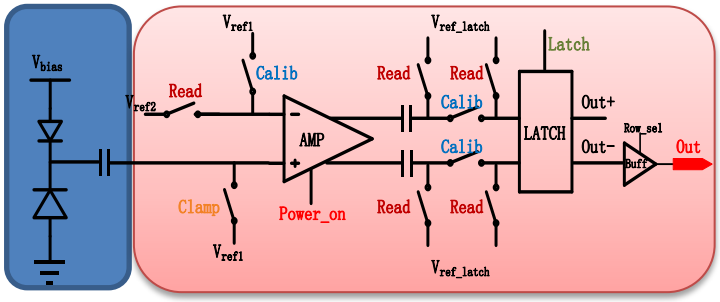
- Offset cancellation and high precision comparator
  - FPN (Fix Pattern Noise) ~ 20 e^-
  - TN (Temporal Noise) ~ 7 e^-
- Optimal sensing diode selected from JadePix1
  - Positively biased
  - AC coupled to the amplifier
- Rolling shutter mode
  - 100 ns / row (Version 1), 80 ns / row (Version 2)
  - 3.7 μA / pixel (Version 1), 6.5 μA / pixel (Version 2)
- Pixel size: 22 × 22 μm^2



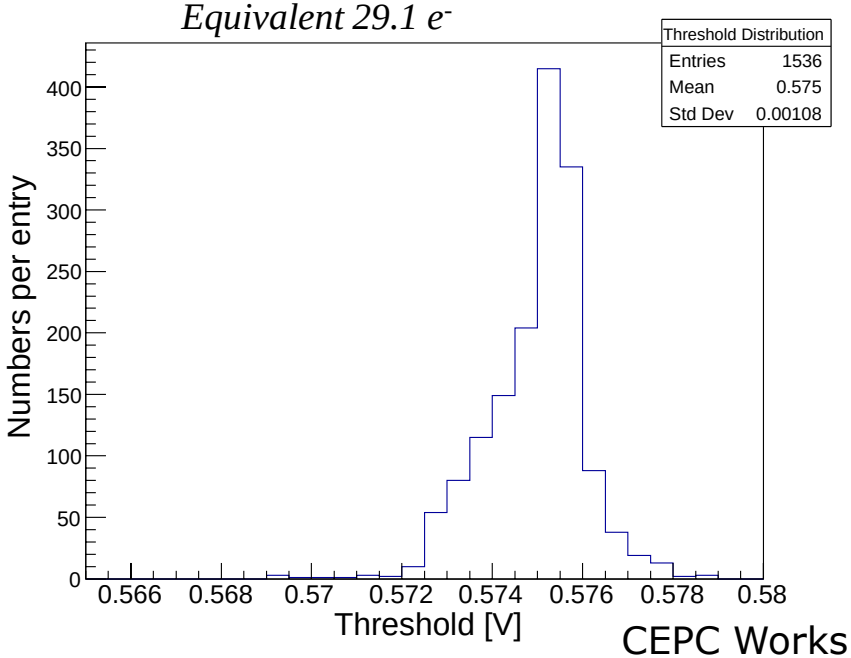


Noise Measurement on JadePix2

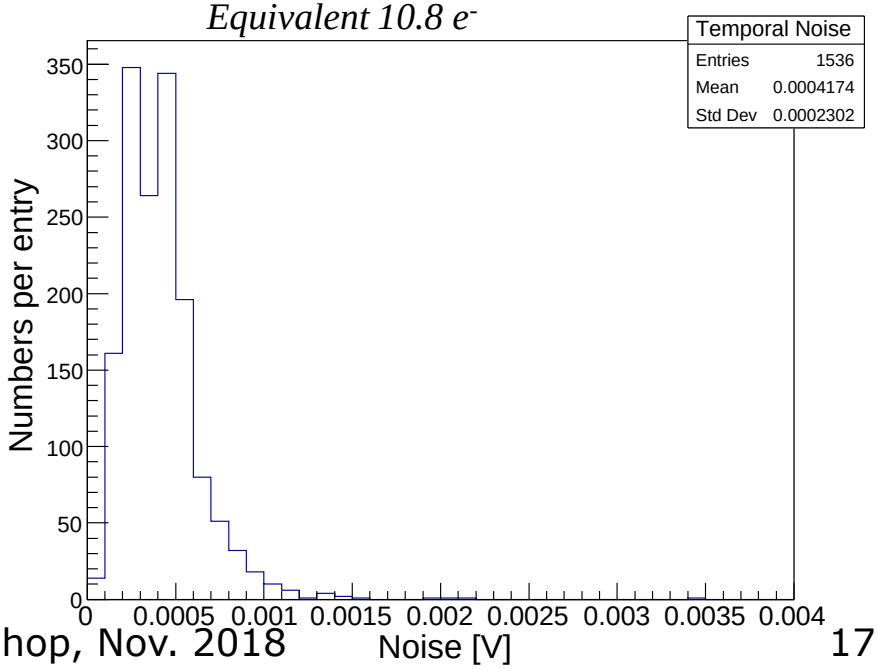
- S-curve measured on Version 1 pixels (differential)
  - Scan 'Vref2' while 'Clamp' closed
- ENC = 31 e^-
  - TN ~ 11 e^-
  - FPN ~ 29 e^-



FPN: 1.08mV @input node
Equivalent 29.1 e^-



TN: 0.4mV @input node
Equivalent 10.8 e^-

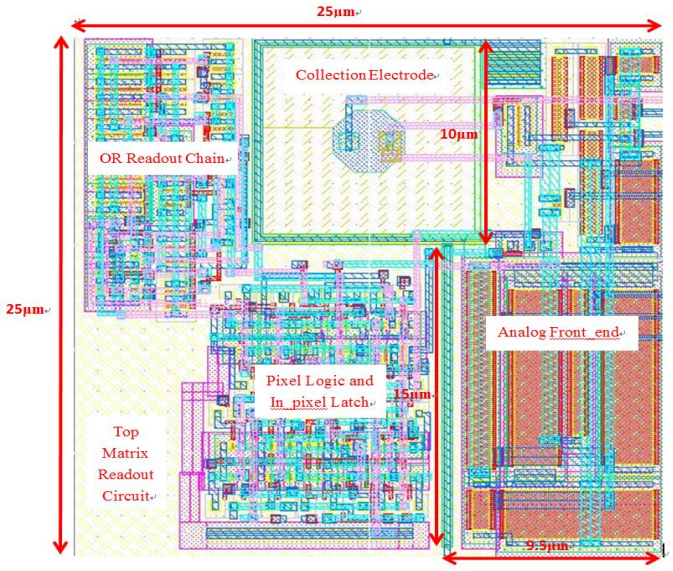


Overview of MIC4

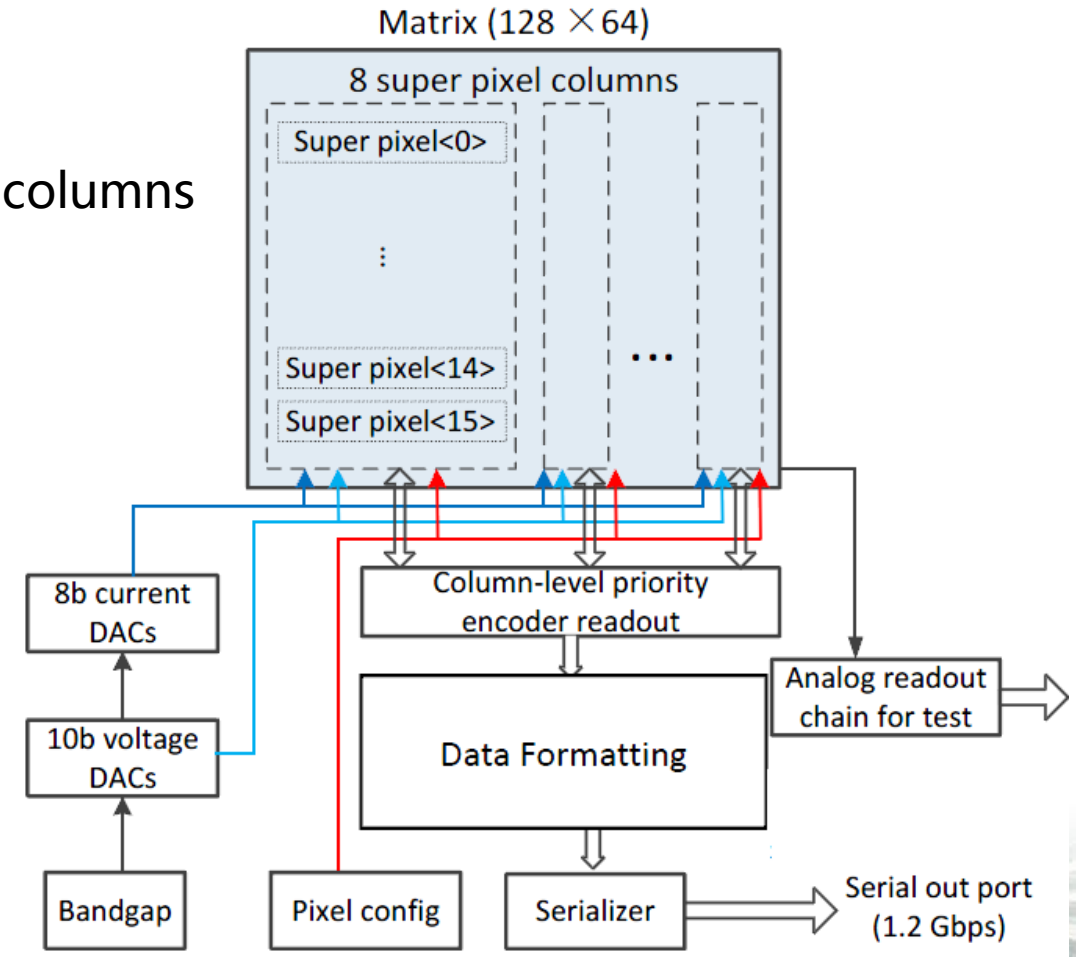
(Team in CCNU & IHEP)

- MIC4 (MAPS In CCNU 4)
- Pixel size: 25 um x 25 um
- Matrix: 128 rows x 64 columns
- Zero suppression embedded in columns
- High speed data link 1.2Gbps

Pixel Layout



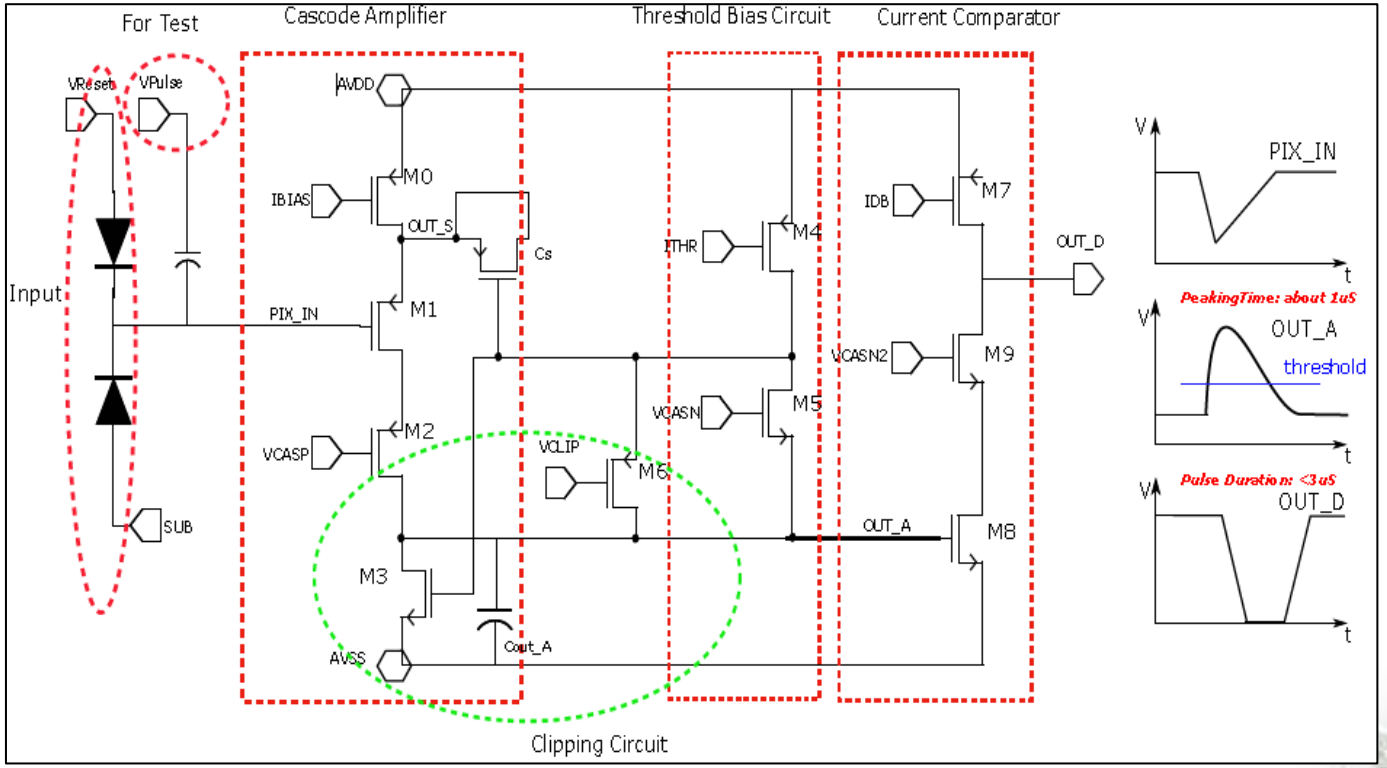
Block diagram of MIC4



MIC4: Pulse Height Discrimination in Pixel

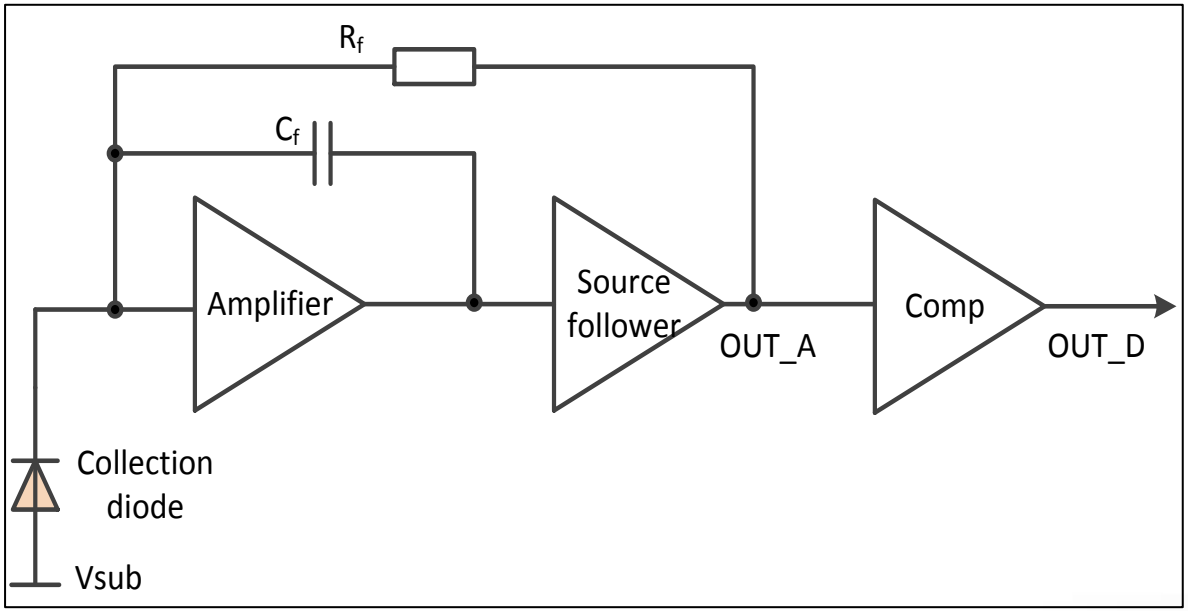
- Baseline front-end: the same structure as in ALPIDE*
  - Branch current 61 nA/pixel (increased by a factor of 3)
  - Peaking time< 1 μs, duration < 3 μs

*Reference:
G. A. Rinella, NIMA845

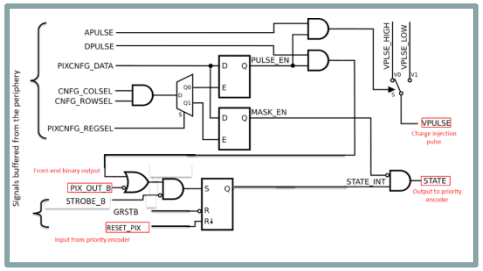


MIC4: Pulse Height Discrimination in Pixel

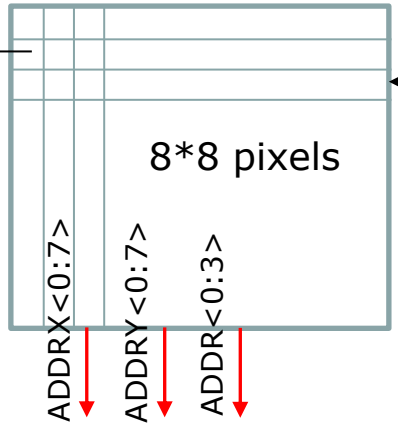
- Alternative front-end: Charge sensitive amplifier + current comparator
  - Feedback capacitance 0.2 fF
  - Peaking time < 550 ns @ Qin < 1.5 ke$^-$
  - Pulse duration < 8.3 μs @ Qin < 1.5 ke$^-$
  - 35 nW / pixel
  - ENC: 24 e$^-$



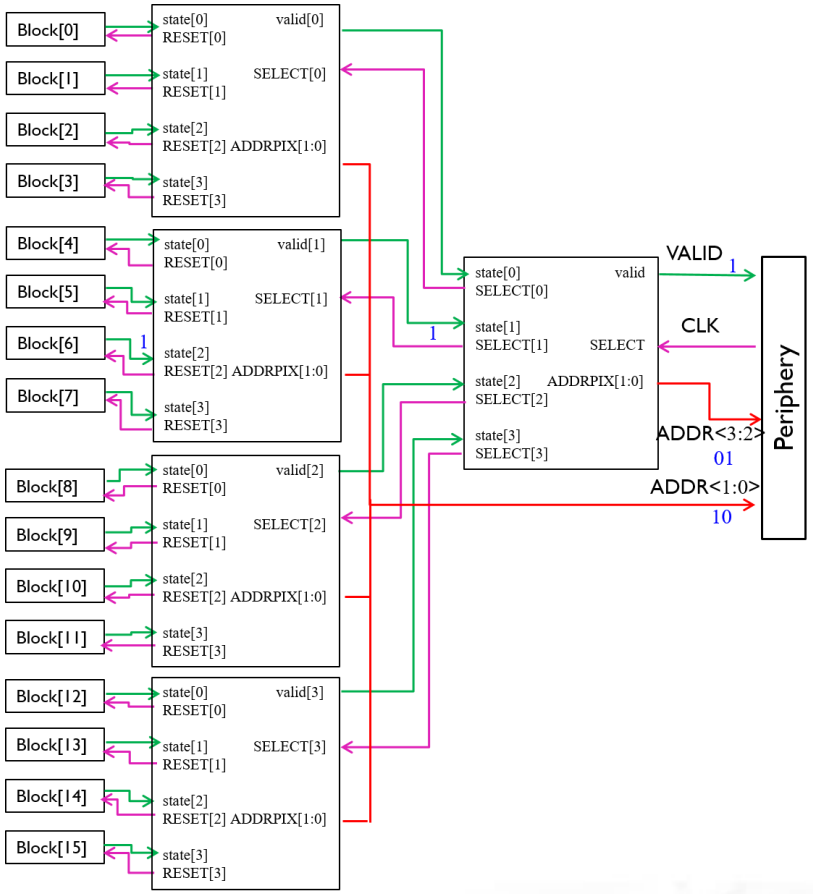
Readout Architecture



In-pixel digital logic



to the Periphery

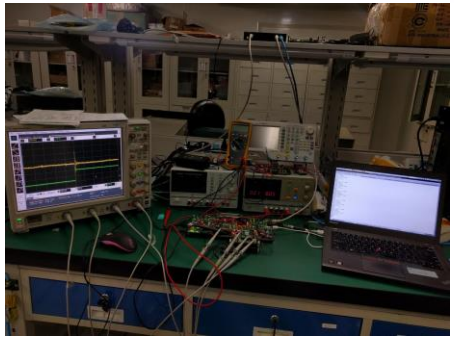


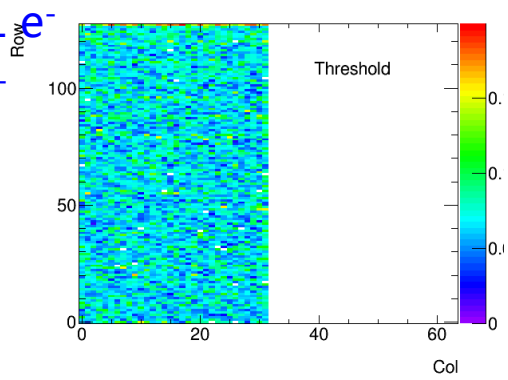
Fast readout architecture:

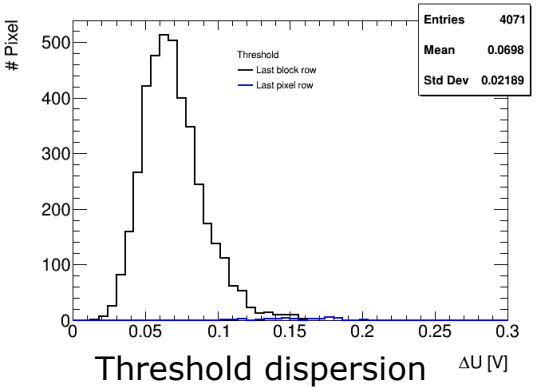
- Hit registered by the latch in each pixel;
- Row and column lines indicate the coordinates of the hit pixel within an 8*8 block;
  In sequence of a priority chain.
- AERD (Address-Encoder and Reset-Decoder) to select the blocks that contain hits.

Noise Measurement on MIC4

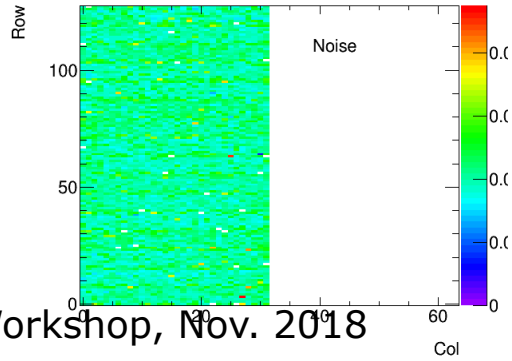
- A test system has been setup in CCNU
- S-curve measured on pixels with baseline front-end
  - Test pulse injection
- Threshold set to 69.8 mV, equivalent to 99 e^-
  - FPN = 21.9 mV, equivalent to 31 e^-
  - TN = 0.65 mV, equivalent to 6 e^-

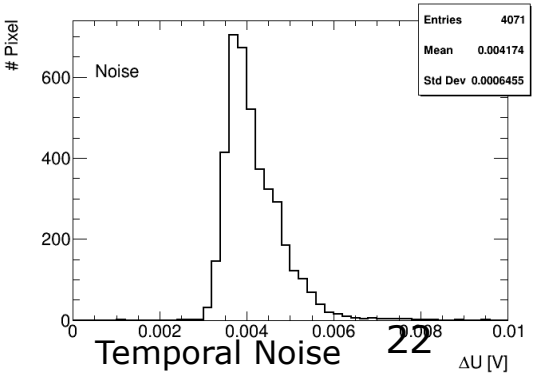






Threshold dispersion



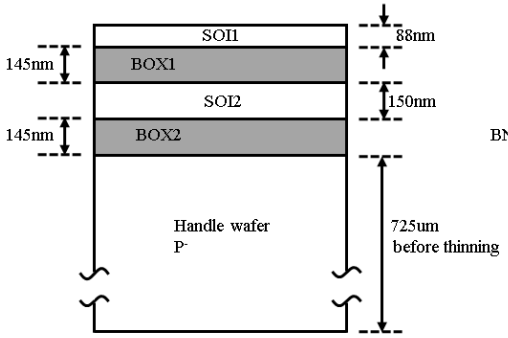


Temporal Noise

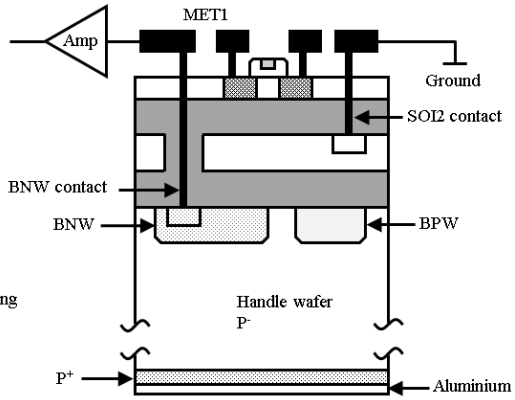
Development of SOI Pixel Sensor

(Team in IHEP)

- N-in-P sensor capable of full depletion
  - BNW and N^+ as collection electrode
  - BPW available as P-spray
- Isolation of transistors
  - Buried Oxide (insulation)
  - SOI2 (grounded for shielding)
- In-Pixel ampl. & disc:
  - Signal charge ~ 4000e (in 50 μm silicon)
  - Very small Cd
  - Voltage amplifier & comparator
  - Very compact pixel ~ 16 μm pitch



BOX: Buried Oxide
BNW: Buried N Well
BPW: Buried P Well

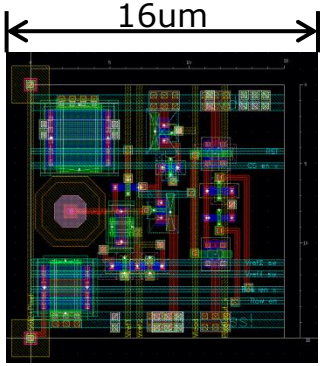


Pixel design in CPV1

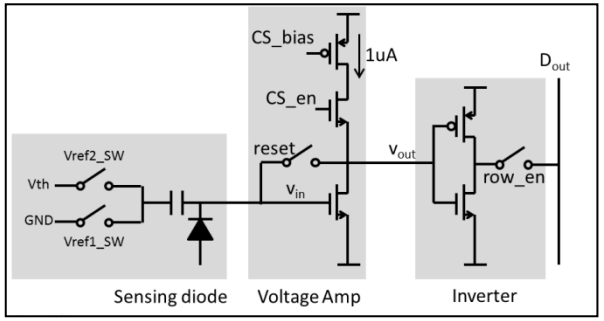
- CPV (Compact Pixel for Vertex)
- Sensing diode, 2 μm
  - Cd = 1 fF
- Voltage amplifier, DC Gain ~ 10
  - 1 μA, power on when row selected
- Offset cancellation reset
- Inverter as discriminator
- Charge injection at Vin
  - Setting threshold
- Minimize layout area
  - 16 × 16 μm^2

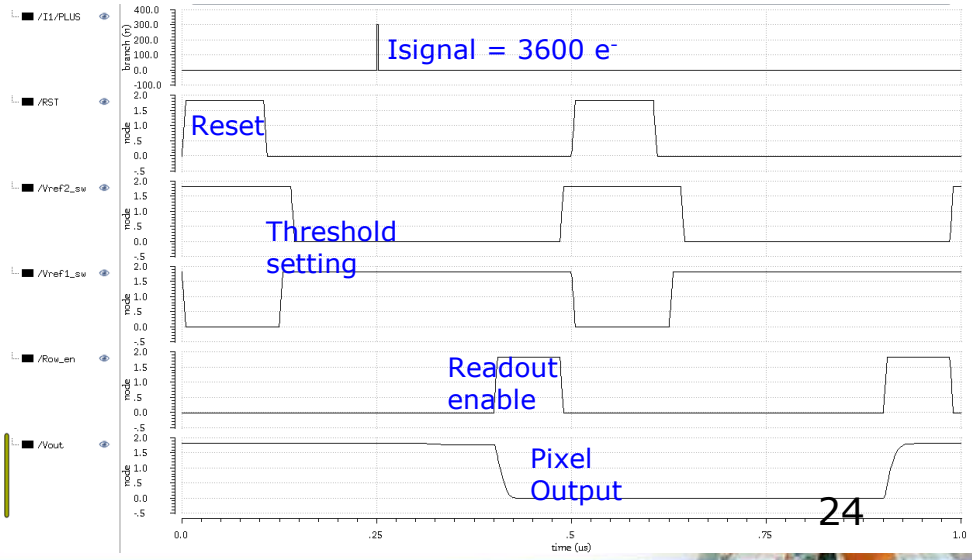
Simulated Cd @ Vbias = -20 V

Diode diameter (μm)	2	3	4
Cd (fF)	1	1.8	2.8



Pixel circuit in CPV1

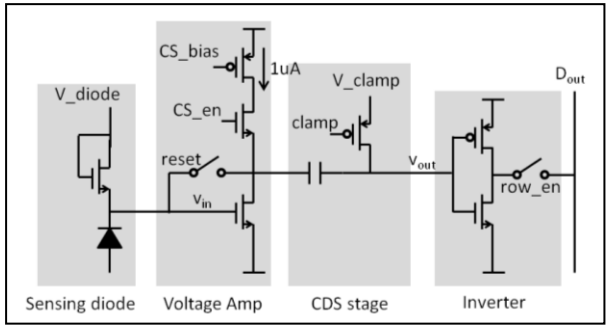


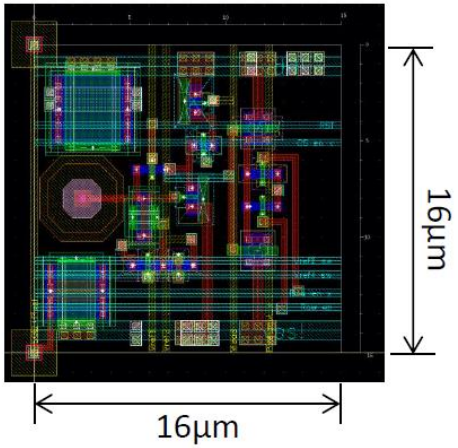


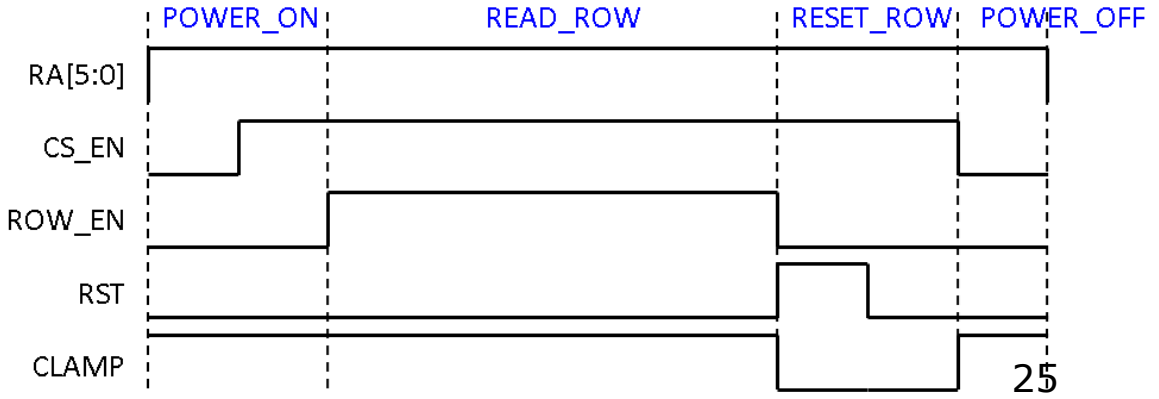
Pixel design in CPV2

- Pixel circuit adjusted on basis of CPV1
- Discharging transistor added to Vin
  - Diode-connected NMOS
  - V_diode = 0V
  - Discharging when Vin < 0V
- CDS stage inserted between apmp. and invt.
  - Improve RTC and FPN noise
  - Setting threshold by V_clamp

Pixel circuit in CPV2

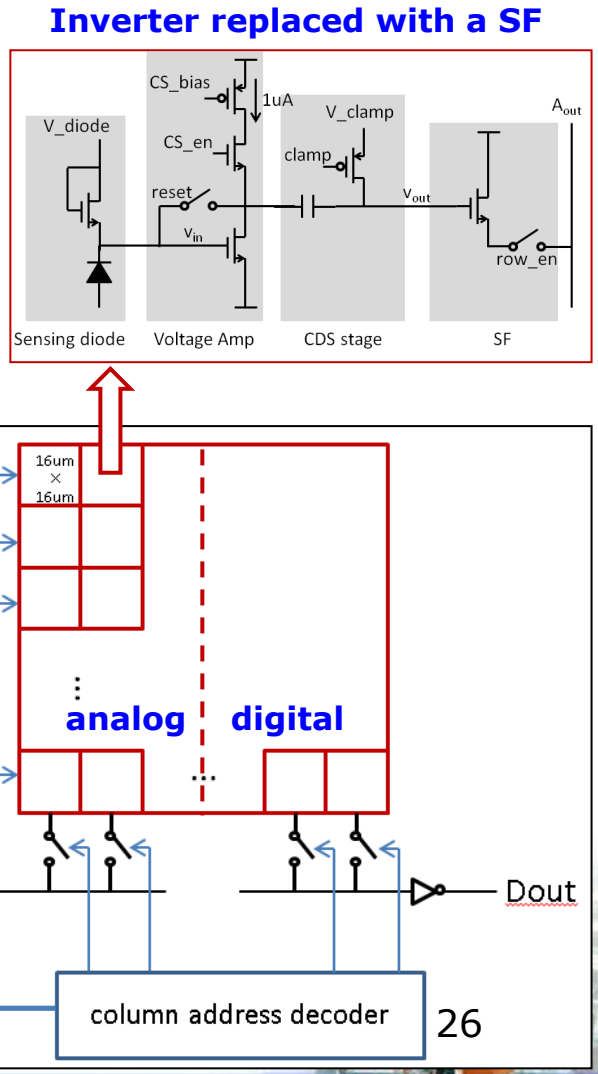






Chip architecture

- Rolling shutter mode
  - 100 ns / row
- 64 rows × 64 columns
  - Half matrix has SFs in place of inverters
- Address decoder to select column & row
  - Very flexible during test
- Same architecture for CPV1/2
  - I/O compatible
  - Readout using SEABAS* DAQ system



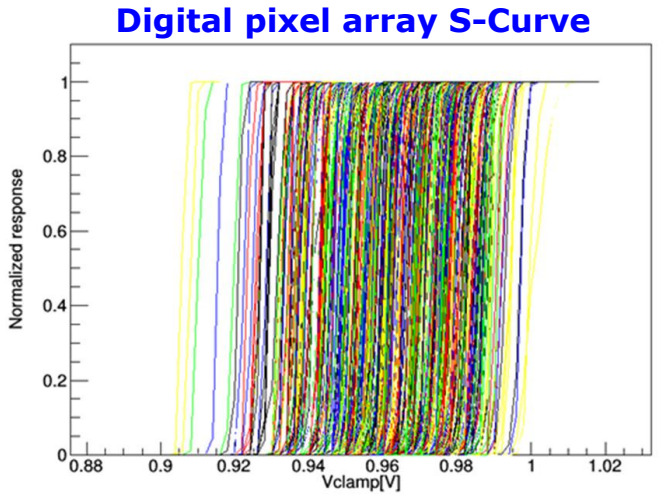
*SEABAS: SOI Evaluation Board with Si TCP/IP, by KEK

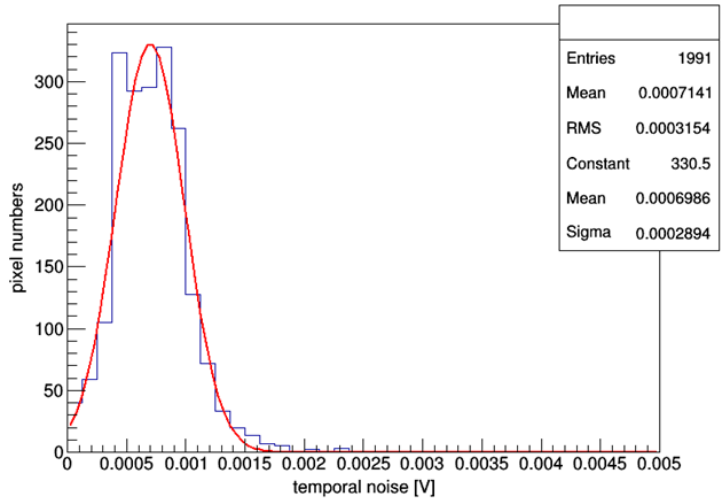
Prototype Characterization

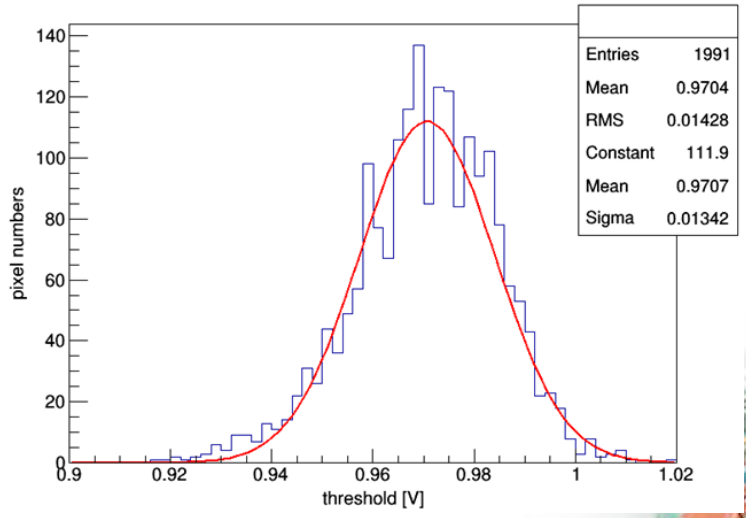
- CPV2 thinned down to 75 μm
  - Backside P^+ implantation after thinning
- Very low leakage current
  - ~ pA/pixel @ Vbias = -100 V
- Full depletion confirmed with ^{55}Fe and Infrared laser respectively
  - $V_{depletion}$ ~ -30 V
- Calibration with ^{55}Fe 5.9 keV X-ray
  - CVF = 123.3 μV/e- @ Vout
  - Can be improved by Cascode amplifier

Noise Measurement

- S-curve measured on the digital pixel array
  - TN ~ 6 e^-
  - FPN ~ 114 e^-



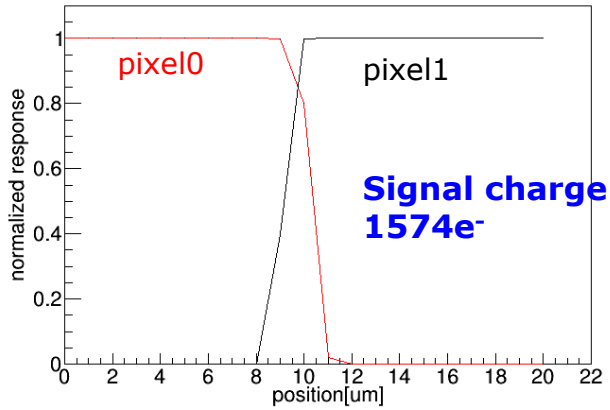


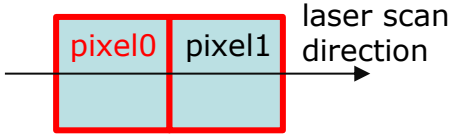


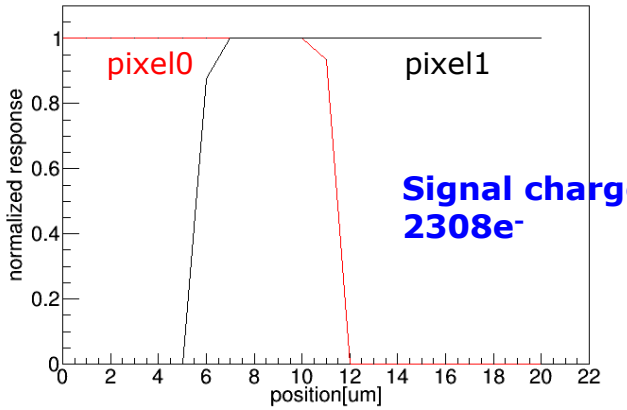
Laser position scan with different intensity

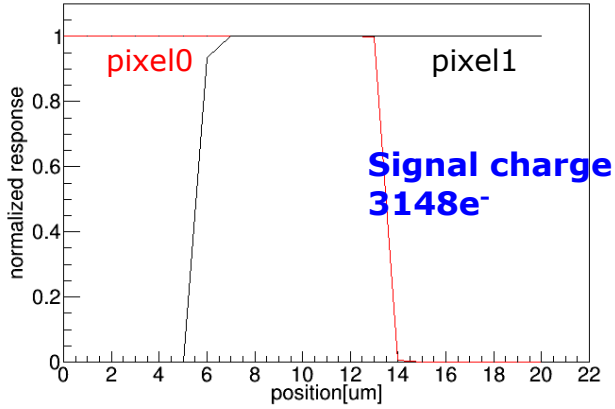
- Scan across two adjacent digital pixels
  - Threshold is fixed (minimum threshold without noise hit)
  - Step size of 1μm
  - Different beam intensity used

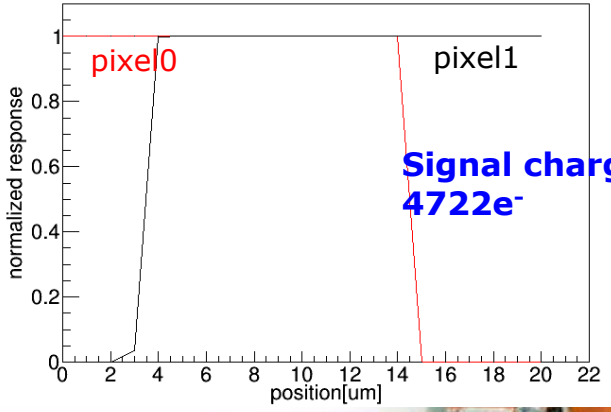
$$\text{Normalized response} = \frac{\text{Number of hits}}{\text{Number of pulses}}$$







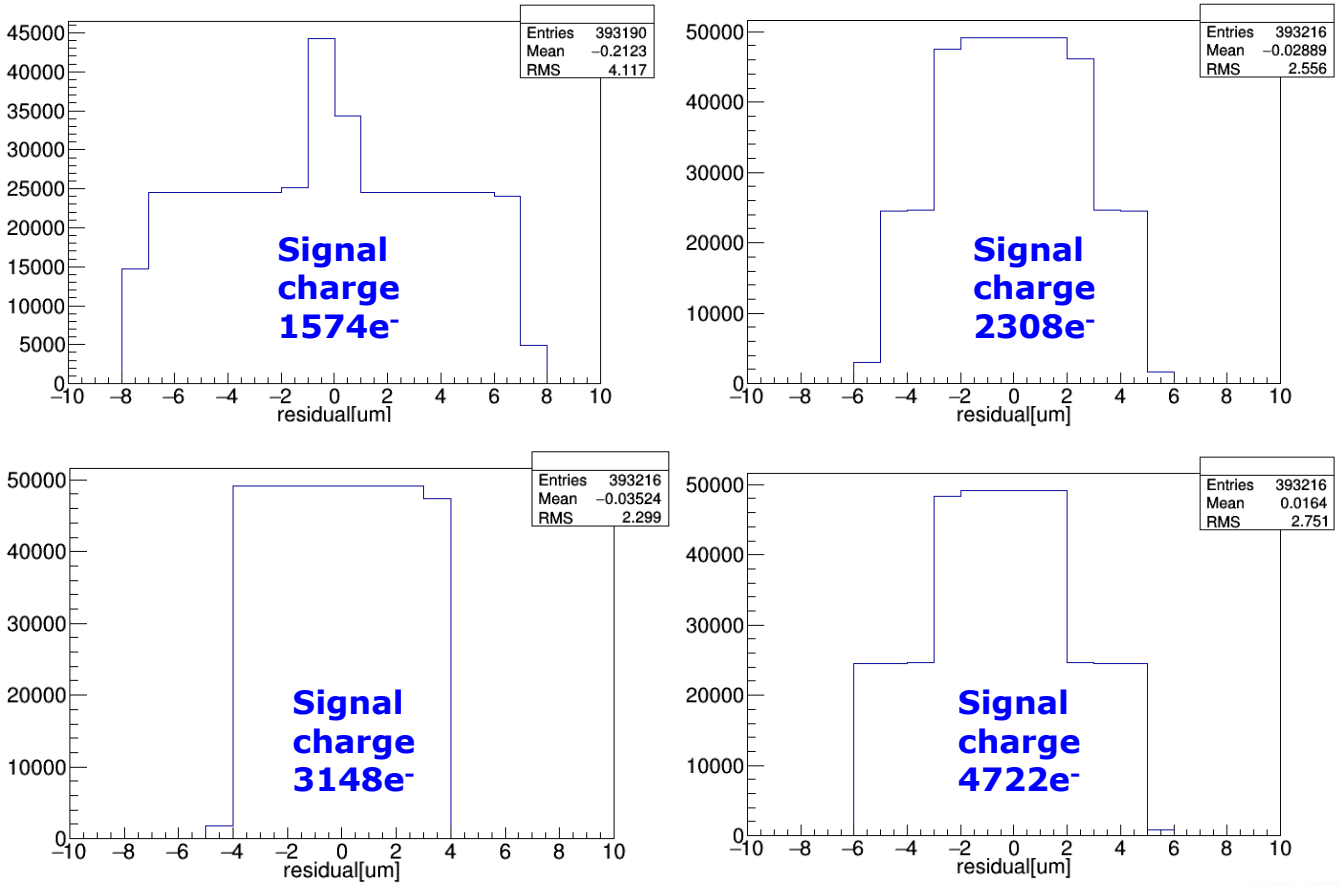




Residual distribution

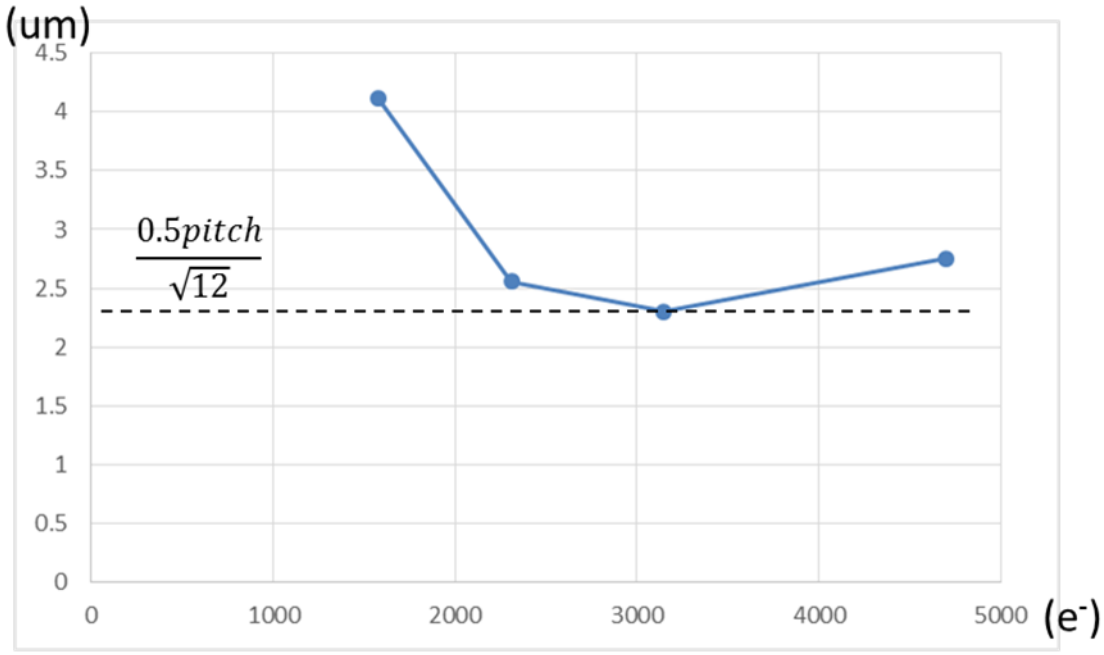
- RMS of residual distribution indicates its single point resolution

Residual distribution changes with beam intensity



Single Point Resolution

- Single point resolution versus signal charge
  - Obtained the best resolution of 2.3um around signal charge 3000 e^-
  - Low threshold is critical



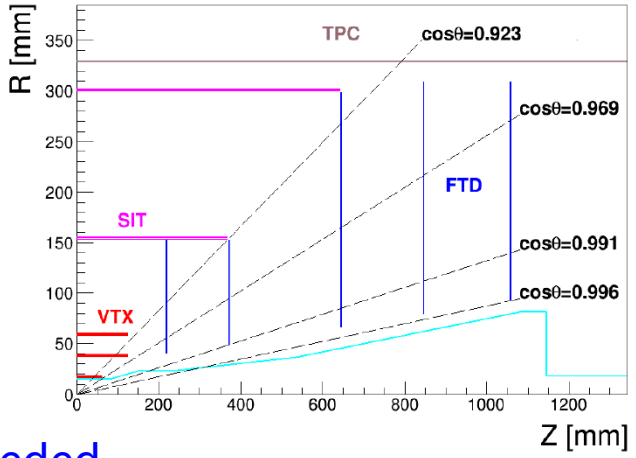
Comparison of digital pixel chips

	JadePix2	MIC4	CPV2
Process	CMOS	CMOS	SOI
Pixel size	22 × 22 μm^2	25 × 25 μm^2	16 × 16 μm^2
TN (e^-)	11	6	6
FPN (e^-)	29	31	114

Development of Pixelated Strip
(Team in Shandong University)

- As an alternative technology option for the SIT and FTD
- CMOS pixel sensor is of particular interest
  - High granularity
  - Low material budget
  - Large single chip via stitching
  - Possible cost reduction
- Readout channels increased significantly
  - Trade off between granularity and readout time needed
  - A case study conducted for the CDR writing

SIT and FTD in the silicon tracker

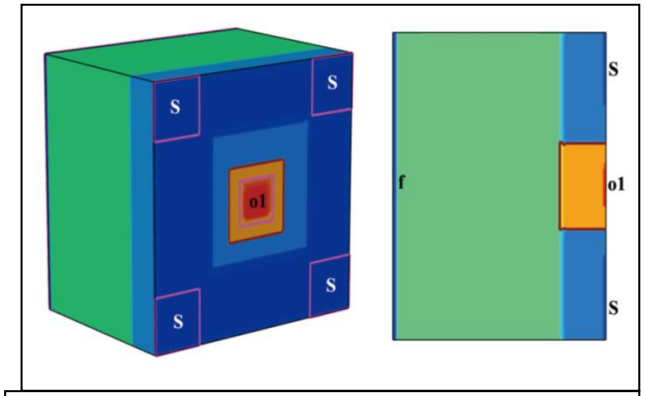


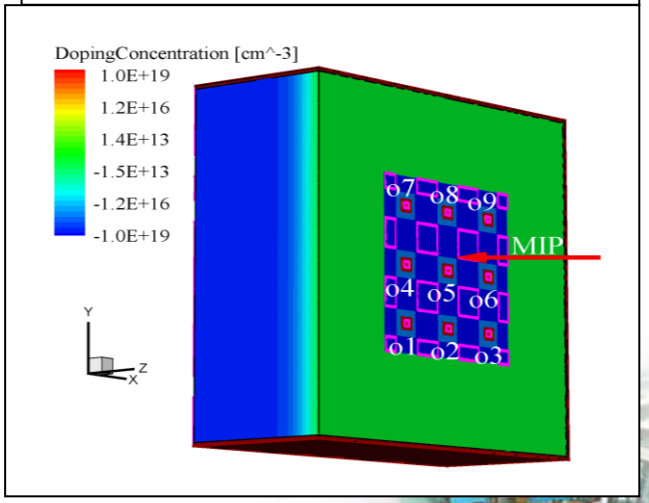
Operation mode	H (240)	W (160)	Z (91)
Track multiplicity (BX^{-1})	310	300	32
Bunching spacing (ns)	680	210	25
SIT-L1 occupancy (%)	0.19	0.58	0.52
FTD-D1 occupancy (%)	0.17	0.54	0.48

Estimated occupancies of the first layers in the SIT and FTD.
Pixel size of 50 × 350 μm^2, readout time of 10 μs assumed.

TCAD Simulation

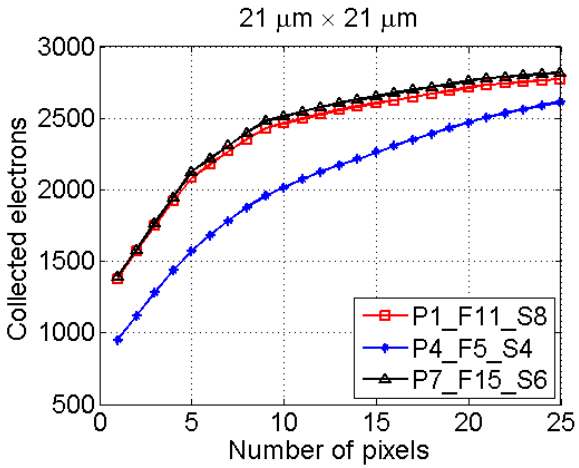
- To understand charge collection in **larger pixels** is essential for
  - Optimal pixel dimensions &
  - Diode geometries
- Structures in TCAD simulation
  - Pixel size: 21 × 21 μm², 21 × 42 μm², 21 × 84 μm²
  - A variety of diode geometries
  - 1 diode per pixel
  - The epitaxial layer: 18 μm & 1 kΩ·cm
  - Bias voltage: 1.8 V
  - Hit in the very center of pixel
  - 5×5 pixel cluster

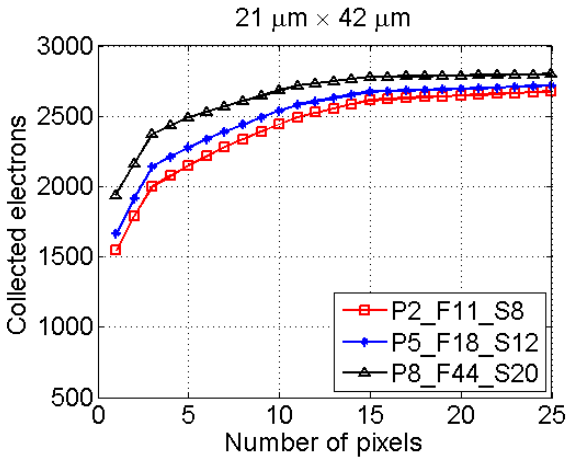


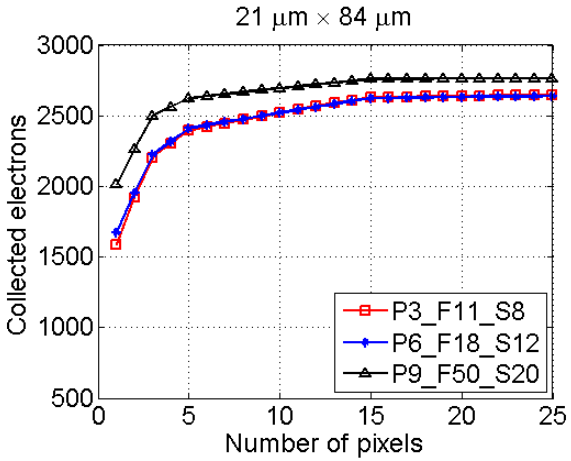


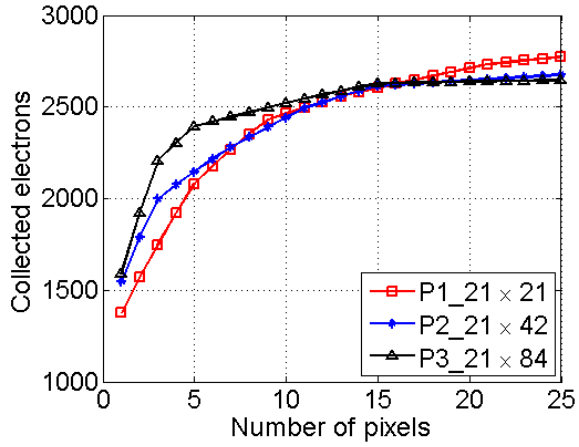
Simulation Results of Charge Collection

- Sum of charge collected by a cluster of 5 × 5 pixels
  - Lager pixels exhibit small cluster size







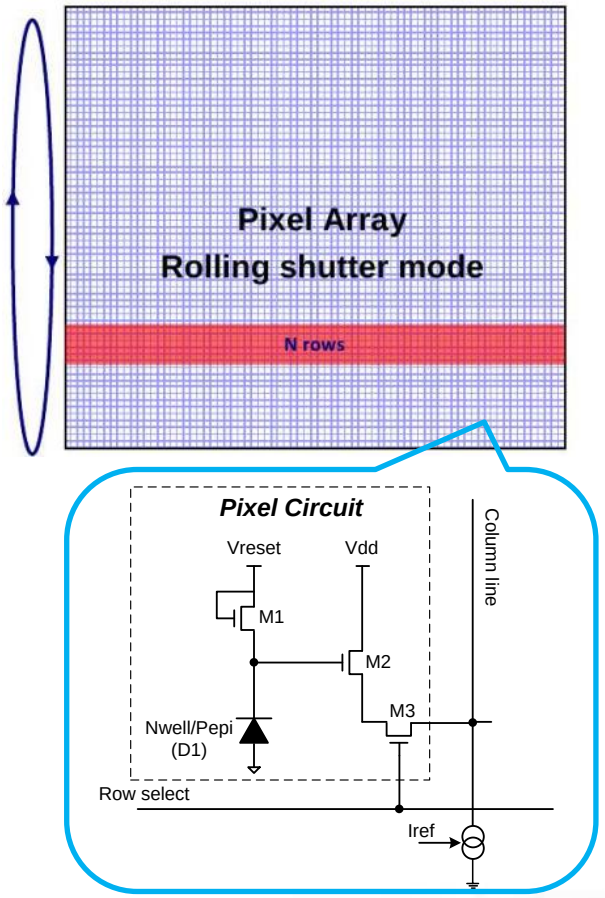


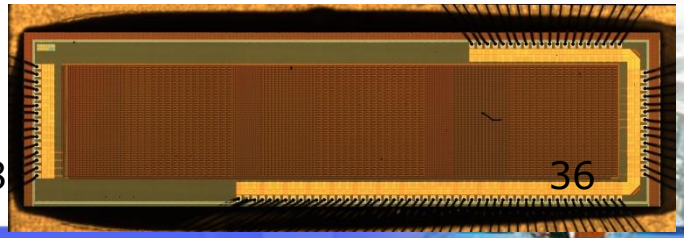
Pixel	P1	P2	P3	P4	P5	P6	P7	P8	P9
Pitch(x)(μm)	21	42	84	21	42	84	21	42	84
N(D)	1	1	1	1	1	1	1	1	1
F(D)(um^2)	11	11	11	5	18	18	15	44	50
S(D)(um^2)	8	8	8	4	12	12	6	20	20

N(D) = number of diodes in each pixel (1)
F(D) = footprint of diode (diode area + pwell opening):
5, 11, 15, 18, 44 & 50 μm^2
S(D) = surface of diode: 4, 6, 8, 12 & 20 μm^2

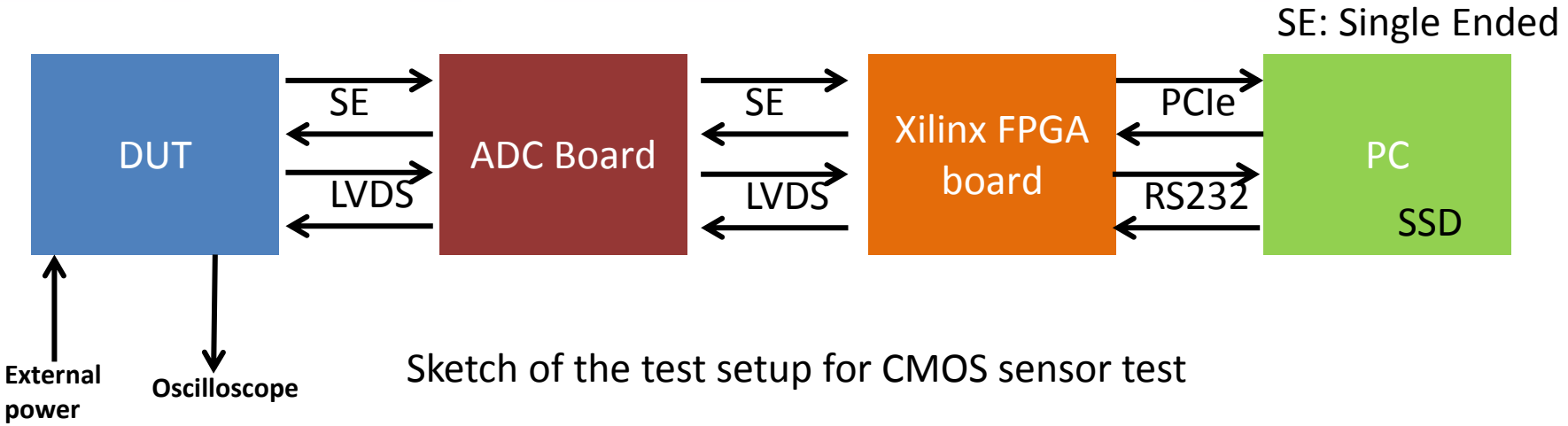
Prototype Chip using TowerJazz CIS 0.18 µm process

- SUPIX (Shandong University PIXel)
- Total sensitive area: 2 × 7.88 mm^2
  - 9 submatrices corresponding to the pixel structures in the TCAD simulation
  - Each submatrix: 16 × 64
- Analog readout
  - Source follower
  - Diode-connected transistor for reset
- Rolling shutter mode
  - 32 µs integration time at 2 MHz clock frequency
  - 16 parallel analog outputs
  - 50 µA current per column
- Gate-enclosed NMOS transistors
  - To improve radiation tolerance





Test setup

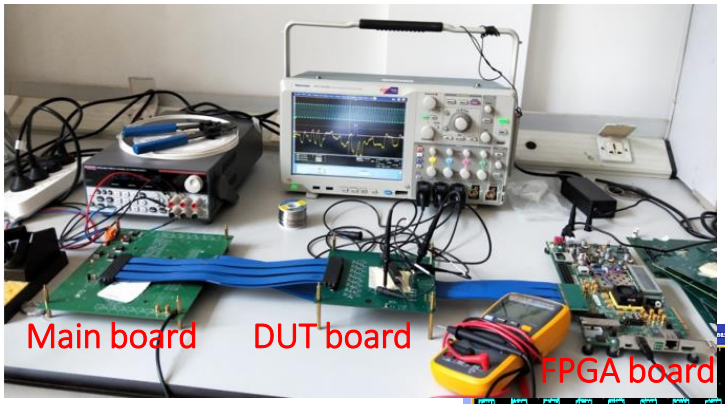


Sketch of the test setup for CMOS sensor test

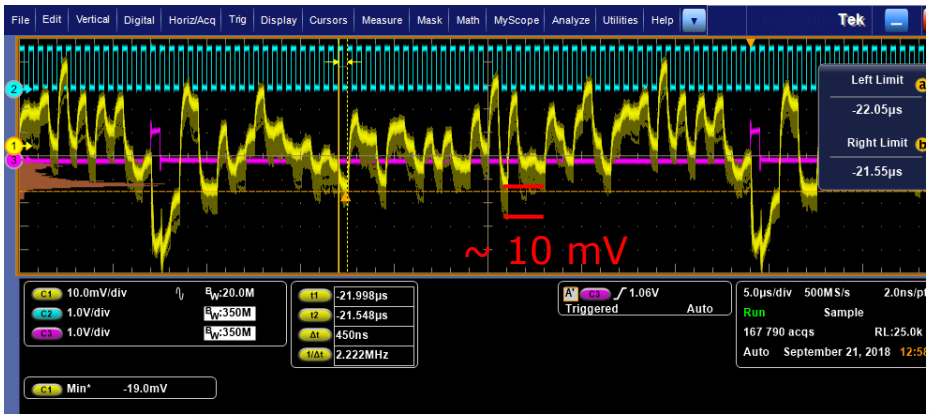
- The test setup consists of:
  - DUT board: customized for the chip
  - ADC board: provided by IHEP, the same as used for JadePix1 test
  - FPGA board: firmware and DAQ software in development
  - SSD high speed data storage → >1Gb/s.

Test in progress

- Output pedestal observed via oscilloscope
  - Variation of baseline measured: 10 mV peak to peak
  - ^{55}Fe source test ongoing



Persistence mode



Summary

- Pixel design of high spatial resolution, low power and fast readout is required for the CEPC silicon tracker.
- A variety of pixel chip designed specifically for CEPC as part of the R&D activities.
  - Optimization of sensing diode to improve Q/C
  - Low power low noise amplifier and discriminator in pixel
  - Fast readout architecture
- Sensing diode Q/C characterized
- Noise of different front-end characterized and compared
- Spatial resolution < 3 μm demonstrated on small pitch of 16 μm

Future Plan on R&D

- Laboratory and test-beam characterizations
- Coordination of design team for next submission
- Large area chip design
- Radiation hardness
- For time stamp @ Z-pole
  - Explore SOI 3D connection technology
  - Look for new process with smaller feature size

Acknowledgements

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- And the CAS Center for Excellence in Particle Physics (CCEPP)

Thank you for your attention!

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Team in CCNU:

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Below are backup slides

CEPC CDR Parameters

D. Wang

	Higgs	*W*	*Z（3T）*	*Z（2T）*
Number of IPs	2			
Beam energy (GeV)	120	80	45.5	
Circumference (km)	100			
Synchrotron radiation loss/turn (GeV)	1.73	0.34	0.036	
Crossing angle at IP (mrad)	16.5×2			
Piwinski angle	2.58	7.0	23.8	
Number of particles/bunch N_e (10^{10})	15.0	12.0	8.0	
Bunch number (bunch spacing)	242 (0.68μs)	1524 (0.21μs)	12000 (25ns+10%gap)	
Beam current (mA)	17.4	87.9	461.0	
Synchrotron radiation power /beam (MW)	30	30	16.5	
Bending radius (km)	10.7			
Momentum compact (10^{-5})	1.11			
β function at IP β_x^* / β_y^* (m)	0.36/0.0015	0.36/0.0015	0.2/0.0015	0.2/0.001
Emittance $\varepsilon_x/\varepsilon_y$ (nm)	1.21/0.0031	0.54/0.0016	0.18/0.004	0.18/0.0016
Beam size at IP σ_x/σ_y (μm)	20.9/0.068	13.9/0.049	6.0/0.078	6.0/0.04
Beam-beam parameters ξ_x/ξ_y	0.031/0.109	0.013/0.106	0.0041/0.056	0.0041/0.072
RF voltage V_{RF} (GV)	2.17	0.47	0.10	
RF frequency f_{RF} (MHz) (harmonic)	650 (216816)			
Natural bunch length σ_z (mm)	2.72	2.98	2.42	
Bunch length σ_z (mm)	3.26	5.9	8.5	
Betatron tune ν_x/ν_y	363.10 / 365.22			
Synchrotron tune ν_z	0.065	0.0395	0.028	
HOM power/cavity (2 cell) (kw)	0.54	0.75	1.94	
Natural energy spread (%)	0.1	0.066	0.038	
Energy acceptance requirement (%)	1.35	0.4	0.23	
Energy acceptance by RF (%)	2.06	1.47	1.7	
Photon number due to beamstrahlung	0.29	0.35	0.55	
Lifetime _simulation (min)	100			
Lifetime (hour)	0.67	1.4	4.0	2.1
F (hour glass)	0.89	0.94	0.99	
Luminosity/IP L (10^{34}cm^{-2}s^{-1})	2.93	10.1	16.6	32.1

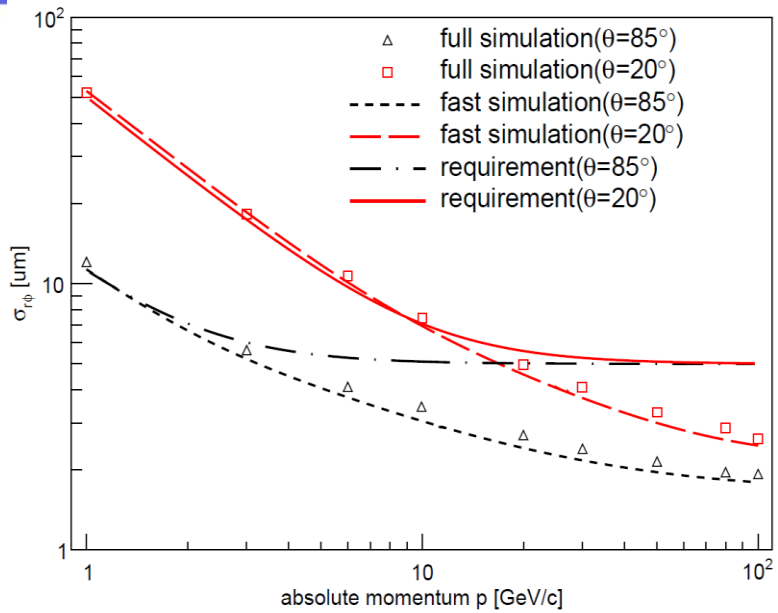
Occupancy at the first Vertex layer

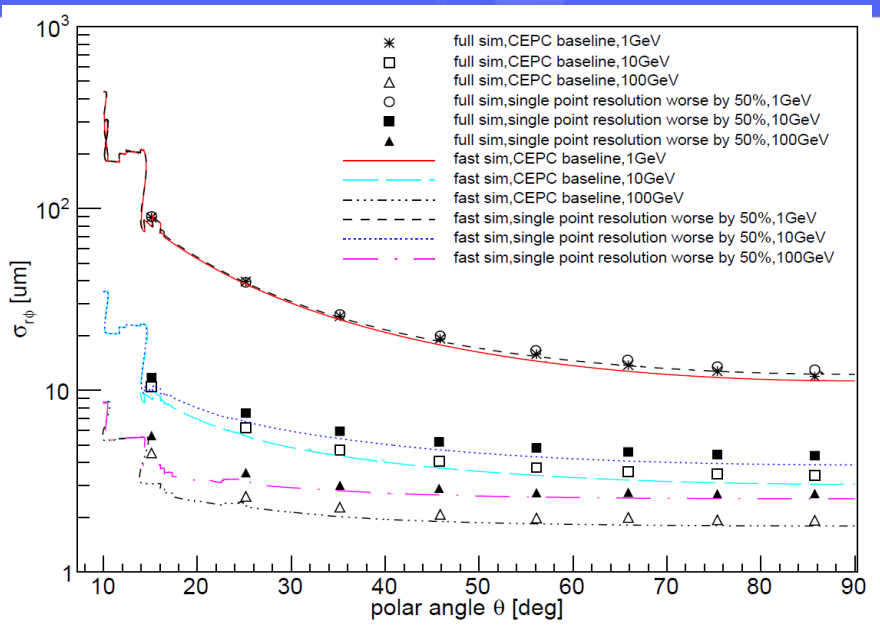
Operation mode	H (240)	W(160)	Z (91)
Hit density (hits $\cdot$ cm^{-2} $\cdot$ BX^{-1})	2.4	2.3	0.25
Bunching spacing (μs)	0.68	0.21	0.025
Occupancy (%)	0.08	0.25	0.23

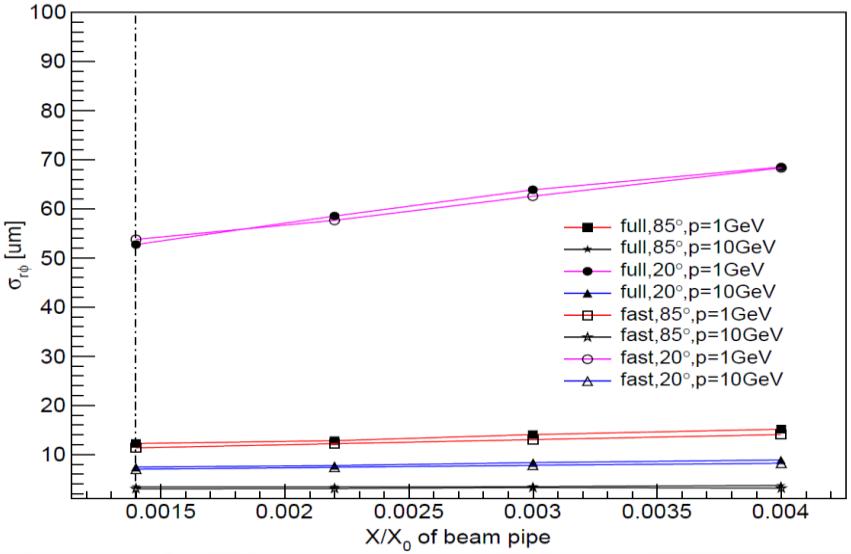
Table 4.2: Occupancies of the first vertex detector layer at different machine operation energies: 240 GeV for ZH production, 160 GeV near W-pair threshold and 91 GeV for Z-pole.

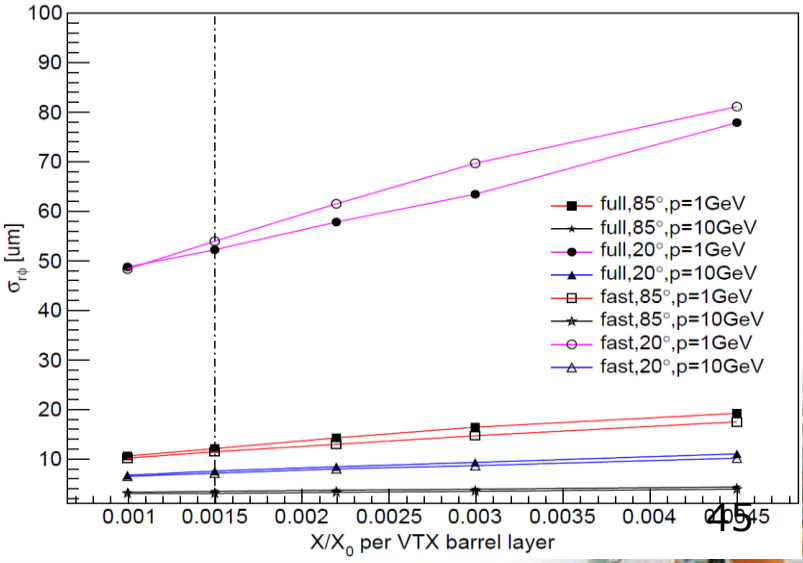
Here we assume 10 μs of readout time for the silicon pixel sensor and an average cluster size of 9 pixels per hit, where a pixel is taken to be 16×16 μm^2. The resulting maximal occupancy at each machine operation mode is below 1%.

Performance Studies – IP Resolution

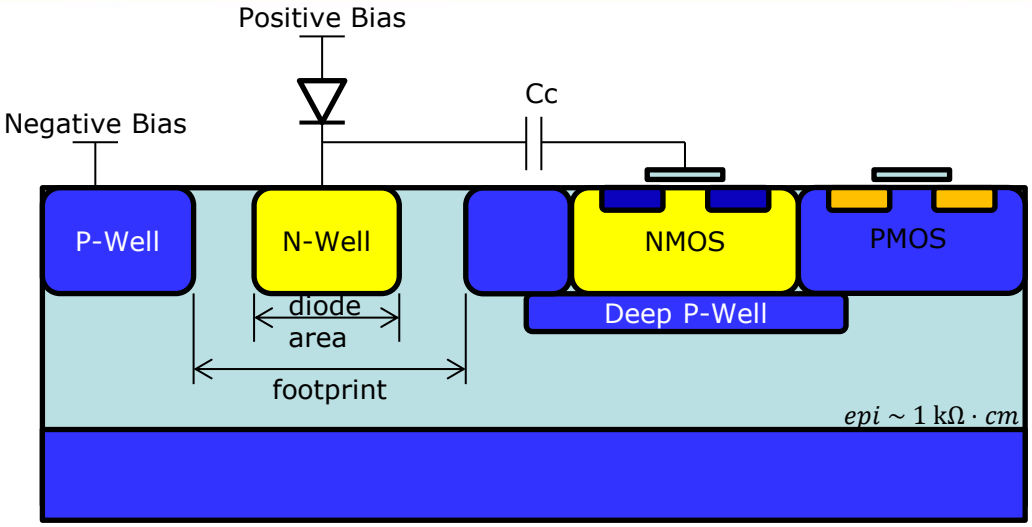








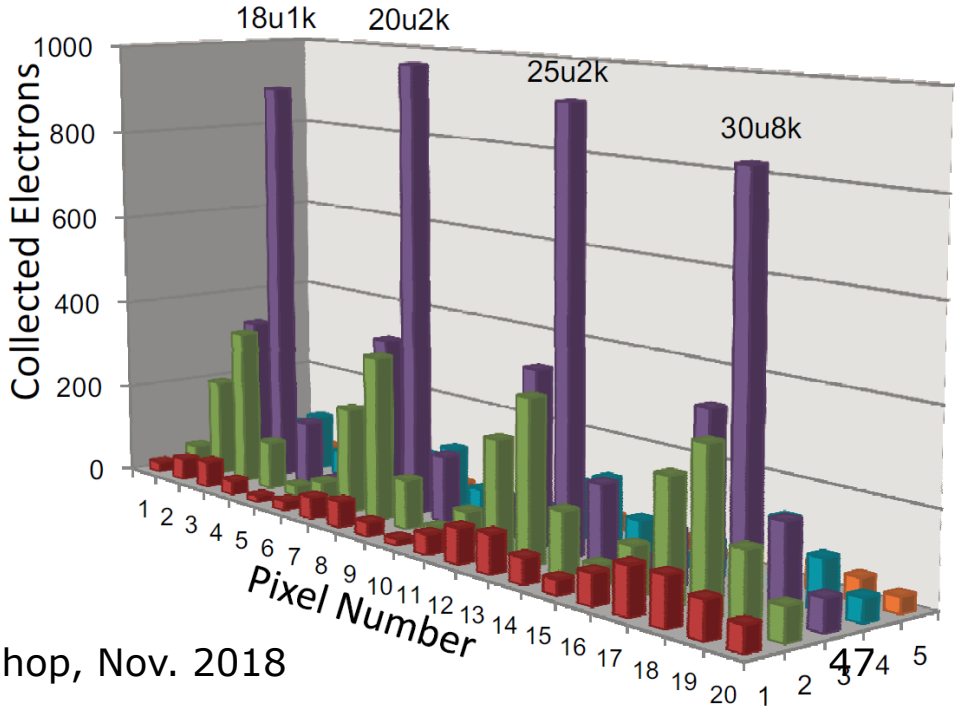
Reminder on CMOS Pixel Sensor



- Diode geometries compete for real estate with transistors
  - Diode area: charge collection electrode
  - Footprint: spacing between P/N-well is critical for low capacitance
- Methods to apply bias voltage
  - Positive bias: AC couple capacitor Cc
  - Negative bias: threshold shift of NMOS

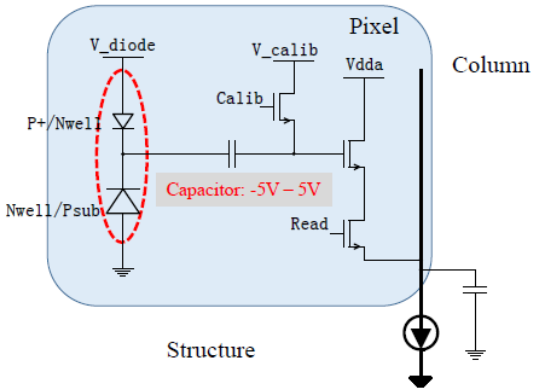
Charge Collection in HR epi. layer

- Pixel cluster with four different epitaxial layers (TCAD simulation)
  - 18 μm, 1 kΩ · cm
  - 20 μm, 2 kΩ · cm
  - 25 μm, 2 kΩ · cm
  - 30 μm, 8 kΩ · cm
- Seemingly optimal charge collection in 20 μm, 2 kΩ · cm
  - Maximum peak signal
  - Constrained cluster size

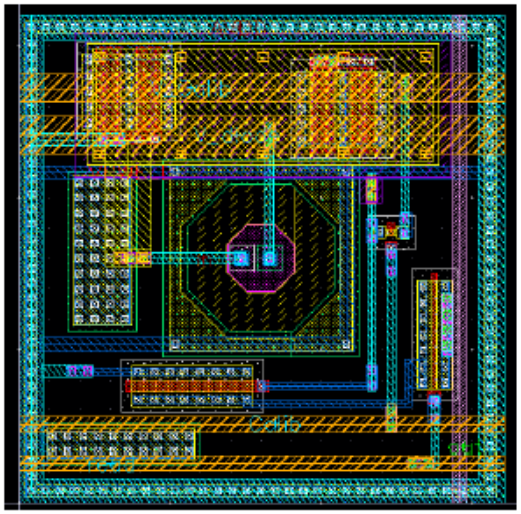


Positive Bias of Diode

- Bias voltage up to 10 V
  - To measure seed/cluster signal versus V_{bias}
  - To measure the cluster size
- Optimization of Cc, V_calib, SF and noise
- Layout
  - 16 × 16 μm²
  - Direct PAD for V_diode

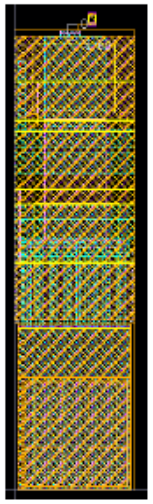


Structure



Pixel Layout

- *16 × 16 μm²;*
- *with transistors under MIM capacitor*



Direct PAD layout: for V_diode

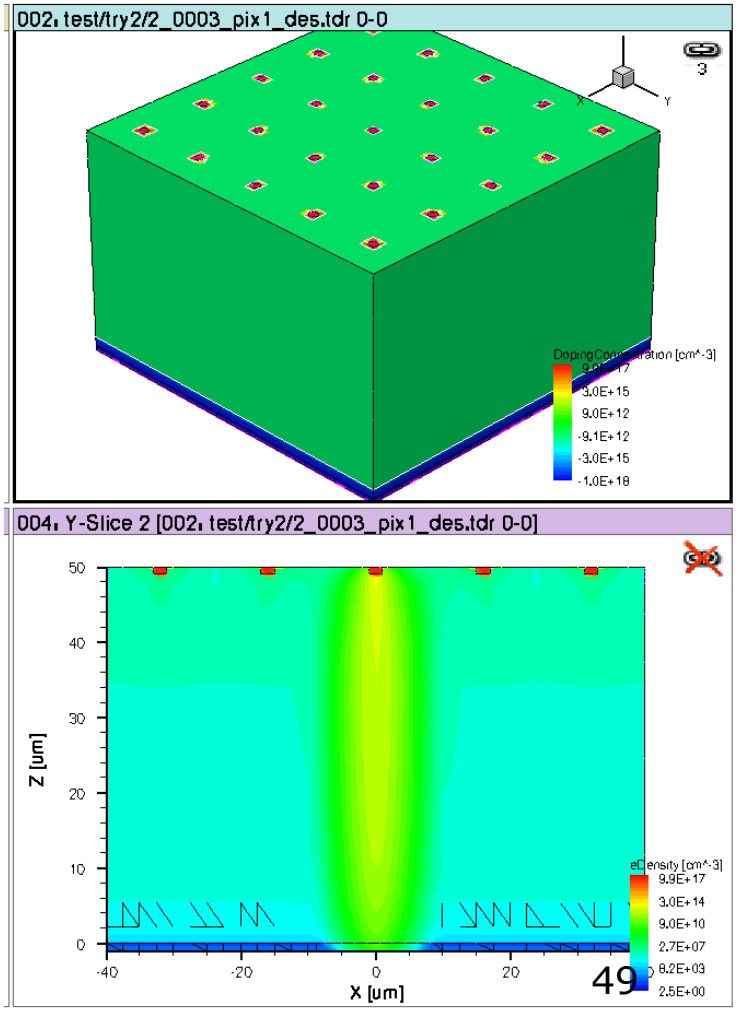
- *250 × 65 μm²*
- *Without ESD*
- *Both sizes & power lines match with other PADs provided by foundry*

Device simulation

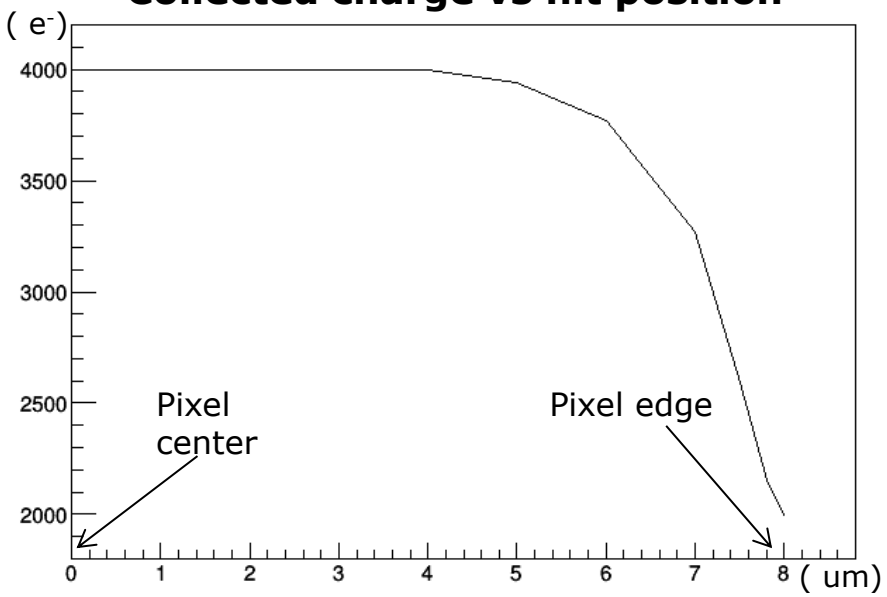
- Device configuration

How to achieve s.p. resolution < 3um?

  - 1 kΩ·cm DSOI wafer (P substrate)
  - N^+ electrode 2 μm in diameter
  - Pixel pitch 16 μm
  - Sensor thickness 50 μm
- Transport of charge carriers
  - Analyzed by TCAD tools



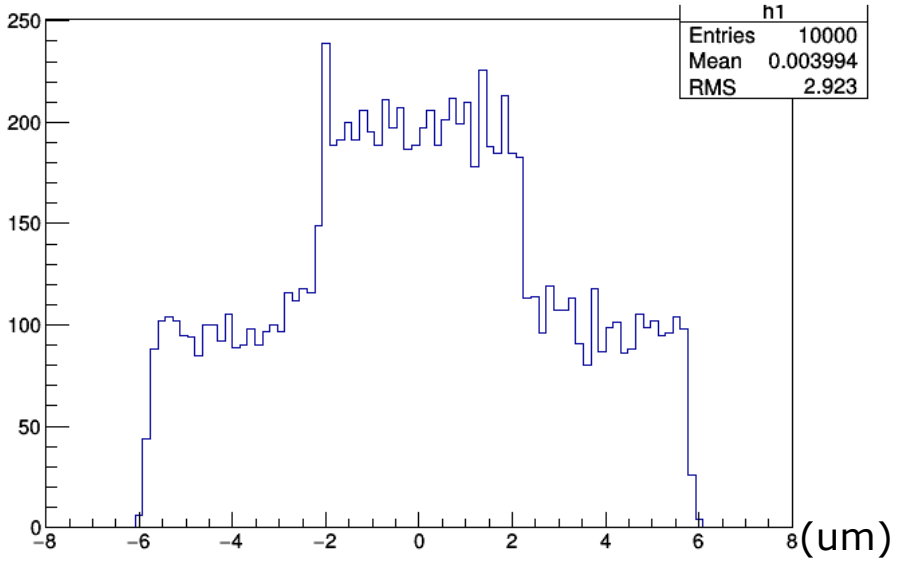
Collected charge vs hit position



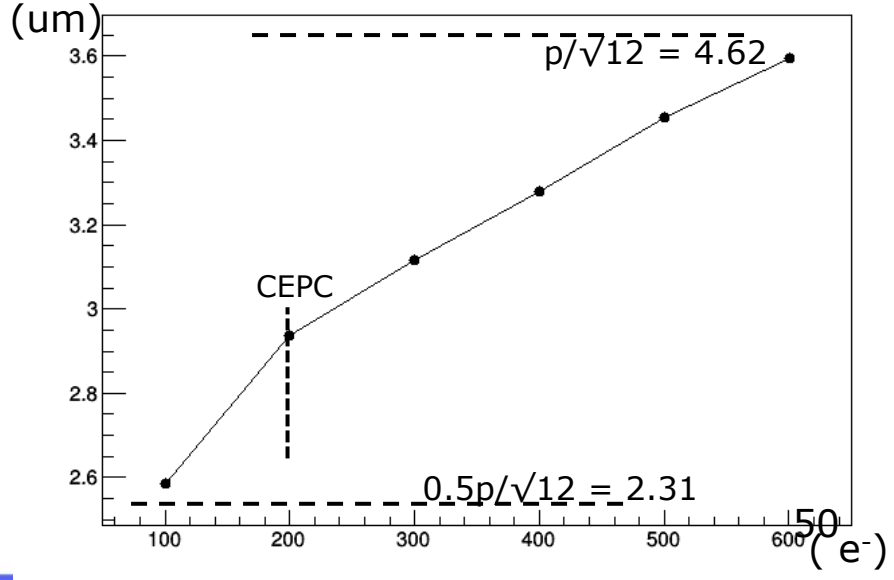
Device simulation

- Noise smearing and threshold discrimination applied numerically
  - ENC ~ 20e-
  - Threshold ~ 200e-
- Residual distribution changes with threshold
  - Low noise front-end is critical to exploit the charge sharing
  - Should note that only perpendicular tracks here
  - Detailed study → poster by Z. Wu

Residual distribution with threshold = 200 e-



Single point resolution vs threshold



Thinning process for CPV2

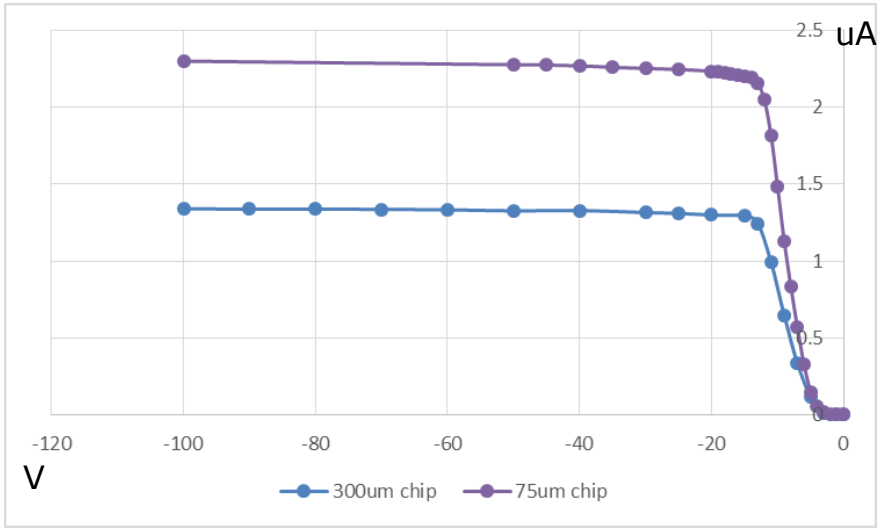
- Wafer thinning -> Chip dicing
  - SOIPIX collaboration
  - Thinning to 300 μm is regular
  - Thinning to 75 μm is available only on request
  - No aluminum on the backside of 75 μm chips
    - Enable backside illumination of infrared laser

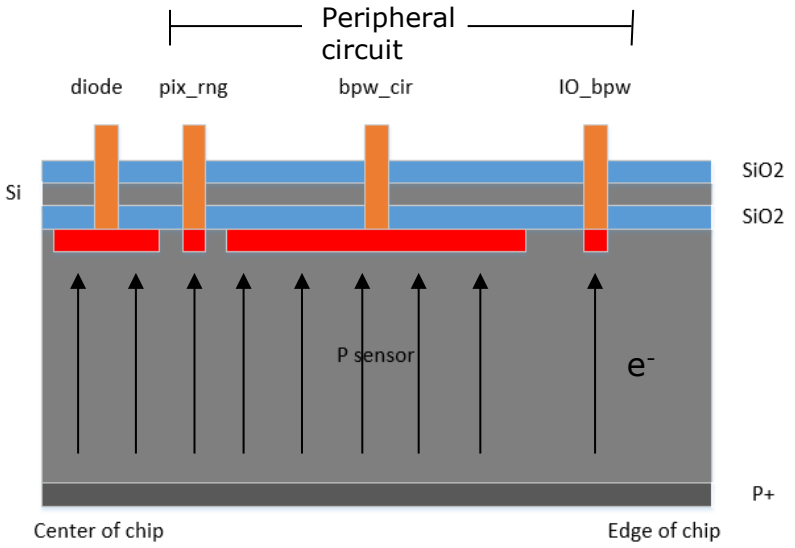
Thinning process flow

Initial wafer thickness 700μm
↓
Mechanical grinding 100μm
↓
Wet etching 75μm
↓
Implantation & Annealing 75μm
↓
Dicing 75μm

Leakage current

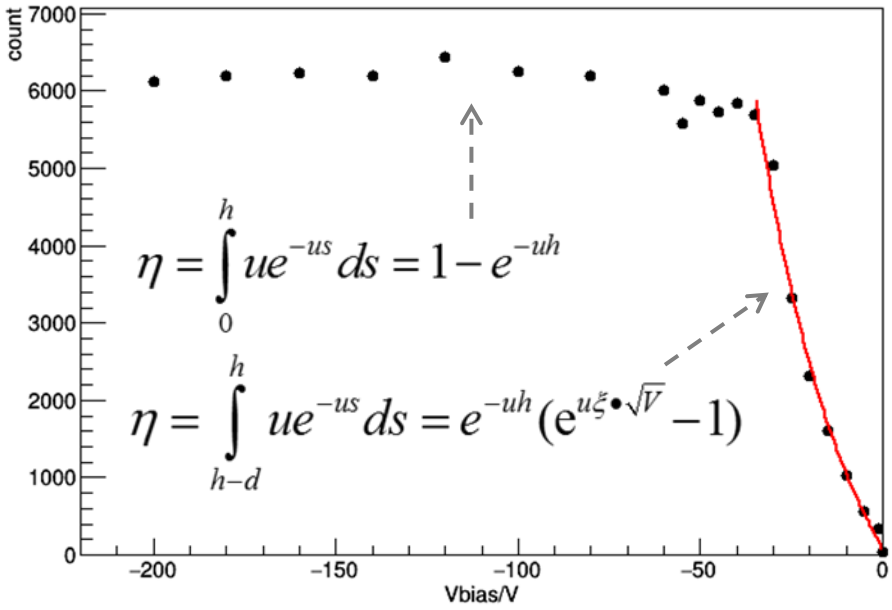
- I-V curve @ room temperature
  - Total Leakage current reaches the plateau when bias voltage is -15V
  - No breakdown up to 100 V
  - Diode current is very small both (~nA over the full matrix, 1mm^2)

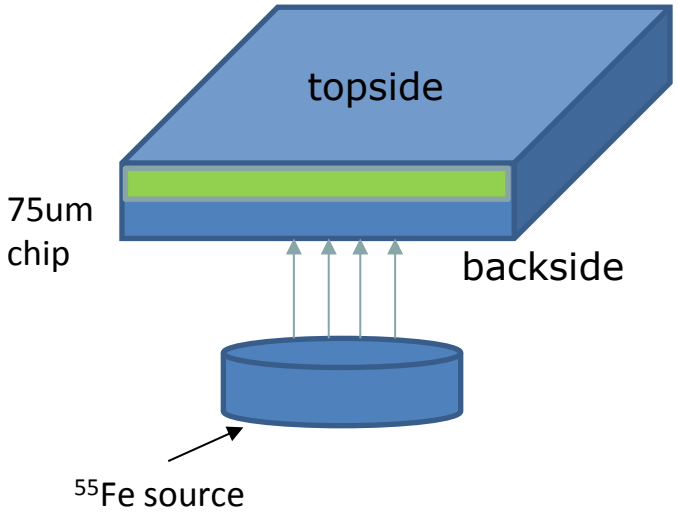




Depletion measurement

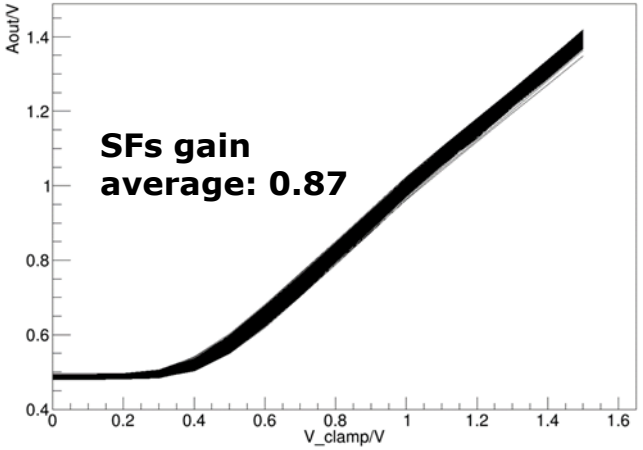
- ^{55}Fe signal Efficiency versus bias voltage
  - X-ray photons counted by analog pixel cluster
  - X-ray illuminates the sensor from backside
  - Depletion zone develops starting from the topside
  - Plateau reached @V_{bias} = -30V

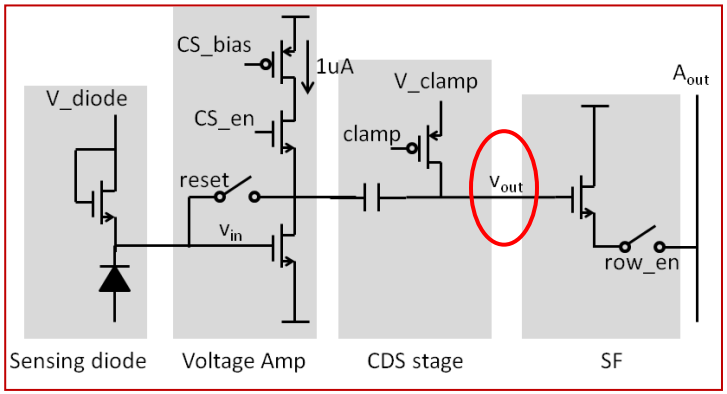


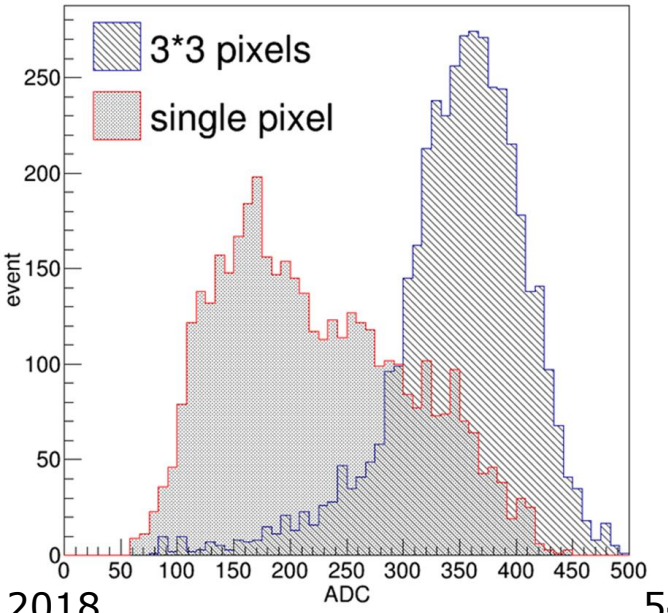


^{55}Fe source calibration

- Charge voltage factor (CVF)
  - Cluster peak at 360 (ADU)
  - SF gain measured 0.87
  - CVF = 123.3uV/e^- @ Vout
- Excessive C_{in}?
  - 14fF
  - Miller capacitance?

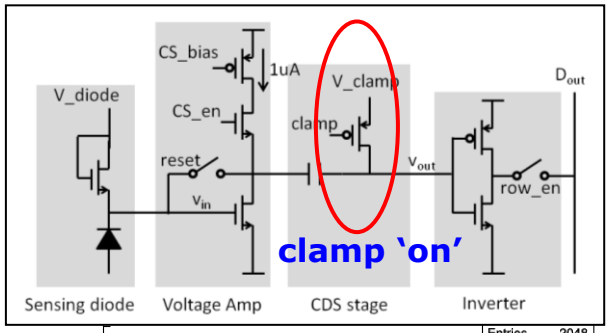


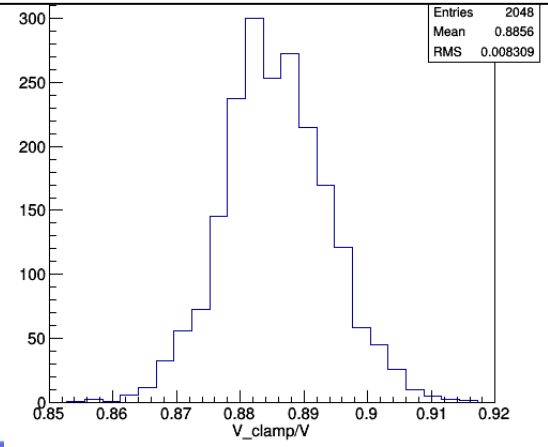




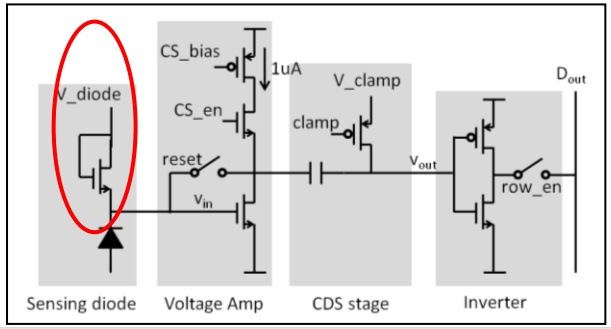
Investigation of threshold dispersion

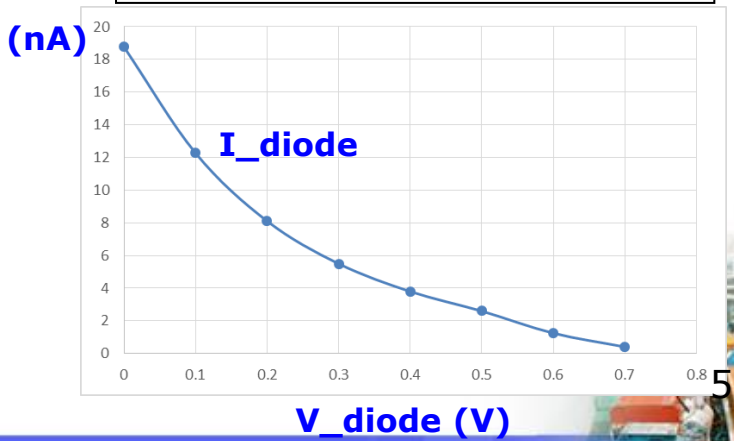
- Threshold dispersion 8.3 mV for inverter standalone
  - In contrast to 14 mV of complete pixels
  - Can be mitigated by improving CVF





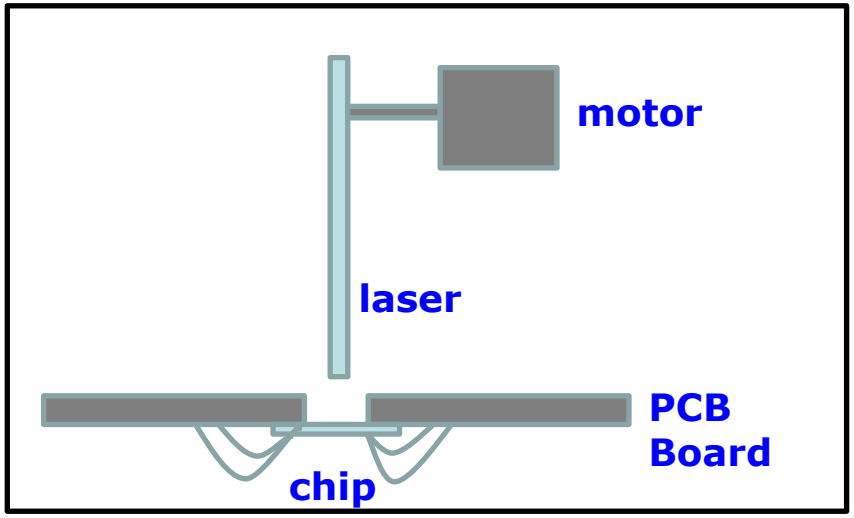
- Leakage of NMOS transistor
  - Low Vth &
  - Very short, W/L = 0.4u/0.2u
- Vin ~ 0.5V, V_diode = 0.35V
  - Minimize integration time

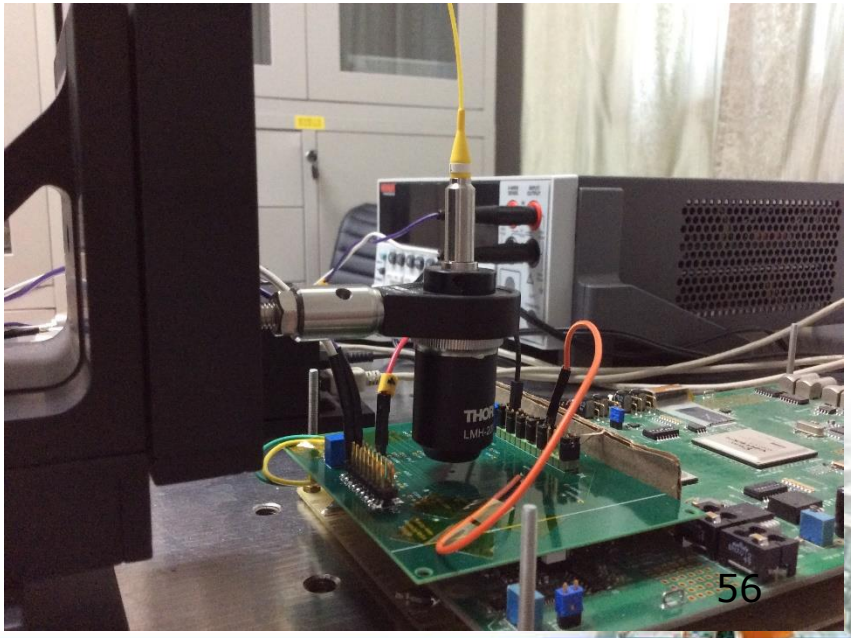




Laser test setup

- 1064nm laser beam
  - Focused beam waist ~ 3.4 μm
  - Adjustable energy ~ pJ/pulse
  - Short pulse duration ~ 100 ps
- 3-dimensional stepping motor
  - Minimum step size: 0.1 μm
  - Position resolution < 1 μm
- Backside illumination





Depletion reconfirmed by laser test

- Laser signal versus bias voltage
  - Inflection point @V_{bias} = -27V
  - Reconfirmed the result of ^{55}Fe source test
  - Choosing V_{bias} = -100V in the following laser scan test