Pixel design and prototype characterization in China

Yunpeng Lu

On behalf of Vertex sub-detector group

Nov. 13, 2018 / Beijing

CEPC Workshop, Nov. 2018
Outline

- Introduction
  - CEPC Silicon tracker
- Fine pixel
  - JadePix1/2, MIC4, CPV1/2
- Pixelated strip
  - SUPIX
- Summary

Note1: This talk covers only the pixel chips developed specifically for the CEPC, while other developments such as for X-ray applications are not included.

Note2: A fast timing pixel scheme to be presented by W. Wei in the TDAQ session

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## CEPC and Its Beam Timing

<table>
<thead>
<tr>
<th></th>
<th>Higgs</th>
<th>W</th>
<th>Z (3T)</th>
<th>Z (2T)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center-of-mass energy (GeV)</td>
<td>240</td>
<td>160</td>
<td>91</td>
<td></td>
</tr>
<tr>
<td>Number of IPs</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Luminosity/IP (10^{34} cm^{-2} s^{-1})</td>
<td>3</td>
<td>10</td>
<td>16</td>
<td>32</td>
</tr>
<tr>
<td>Number of years</td>
<td>7</td>
<td>1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Total Integrated Luminosity (ab^{-1}) - 2 IP</td>
<td>5.6</td>
<td>2.6</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>Total number of particles</td>
<td>1×10^6</td>
<td>2×10^7</td>
<td>3×10^{11}</td>
<td>7×10^{11}</td>
</tr>
<tr>
<td>Bunch numbers (Bunch spacing)</td>
<td>242 (680 ns)</td>
<td>1524 (210 ns)</td>
<td>12000 (25ns + 10% gap)</td>
<td></td>
</tr>
</tbody>
</table>

- **Continuous colliding mode**
  - Duty cycle ~ 50% @ Higgs, close to 100% @ W/Z
- **General requirement on the detector development:**
  - Precise measurement, Low power, Fast readout, Radiation-hard

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Two Detector Concepts

- **Baseline detector concept**
  - Silicon tracker + TPC
  - or Full Silicon Tracker
  - High granular calorimetry system
  - 3 Tesla solenoid
  - Muon detector

- **Alternative detector concept, IDEA**
  - Silicon pixel + Drift Chamber
  - 2 Tesla solenoid
  - Dual readout calorimeter
  - Muon chamber

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Baseline Silicon Tracker Layout

- Tracking part: Mainly microstrip
  - SIT, SET, ETD, and 3 outer disks of FTD, ETD: single-sided strips mounted back to back
  - 2 inner disks of FTD: pixel

- Vertex part: 3 double-sided pixel layers
  - Layer 1: best s.p. resolution
  - Layer 2: very fast readout

| VTX parameters | $R$ (mm) | $|z|$ (mm) | $|\cos \theta|$ | $\sigma$ (µm) |
|----------------|---------|-----------|----------------|-------------|
| Layer 1        | 16      | 62.5      | 0.97           | 2.8         |
| Layer 2        | 18      | 62.5      | 0.96           | 6           |
| Layer 3        | 37      | 125.0     | 0.96           | 4           |
| Layer 4        | 39      | 125.0     | 0.95           | 4           |
| Layer 5        | 58      | 125.0     | 0.91           | 4           |
| Layer 6        | 60      | 125.0     | 0.90           | 4           |
Performance Requirements

\( B = 3T \)

- Momentum Resolution: \( \sigma_{l/p_T} = 2 \times 10^{-5} \oplus 1 \times 10^{-3} / (p_T \sin \theta) \)
- Impact Parameter Resolution: \( \sigma_{r\phi} = 5 \mu m \oplus \frac{10}{p(GeV) \sin^{3/2} \theta} \mu m \)

- **Vertex specifications:**
  - \( \sigma_{SP} \) near the IP: \( \leq 3 \mu m \)
  - Material budget: \( \leq 0.15\% X_0 / \text{layer} \)
  - First layer located at a radius: \( \sim 1.6 \text{ cm} \)
  - Pixel occupancy: \( \leq 1 \% \)

- **Tracking specifications:**
  - \( \sigma_{SP} \): \( \leq 7 \mu m \)
  - Material budget: \( \leq 0.65\% X_0 / \text{layer} \)
# Pixel Sensor Specifications

- **To achieve single point resolution**
  - Pixel size ~ 16 μm (Binary readout)

- **To lower the material budget**
  - Sensor thickness ~ 50 μm
  - Air cooling, heat load < 50 mW / cm²

- **To tackle beam-related background**
  - Fast readout 1 ~ 100 μs / frame
  - 3.4Mrad / year & $6.2 \times 10^{12} n_{eq} / (cm^2 \cdot year)$?

<table>
<thead>
<tr>
<th>Physics driven requirements</th>
<th>Running constraints</th>
<th>Sensor specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma_{s.p.}$ 2.8 μm</td>
<td>Small pixel 16 μm</td>
<td></td>
</tr>
<tr>
<td>0.15% $X_0$ / layer</td>
<td>Thinning 50 μm</td>
<td></td>
</tr>
<tr>
<td>Material budget</td>
<td>Air cooling</td>
<td>Low power 50 mW / cm²</td>
</tr>
<tr>
<td>16 mm</td>
<td>beam-related background</td>
<td>Fast readout 1 ~ 100 μs</td>
</tr>
<tr>
<td>r of Inner most layer</td>
<td>radiation damage</td>
<td>Radiation tolerance</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.4 Mrad / year</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$6.2 \times 10^{12} n_{eq} / (cm^2 \cdot year)$</td>
<td></td>
</tr>
</tbody>
</table>

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Key factors to low power design

- Depleted sensing diode
  - Signal charge $Q \uparrow$ or cluster size $\downarrow$
  - Capacitance of the input node $\downarrow$

- Small fill factor
  - Capacitance of the input node $\downarrow$

- In pixel discriminator
  - Eliminate the large driving current of analog output

\[
P \propto I \propto \left( \frac{S/N}{Q/C} \right)^{2\alpha}
\]

$\alpha = 2$ for strong inversion, $\alpha = 1$ for weak inversion

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Pixel technologies

- **CMOS pixel sensor (CPS)**
  - TowerJazz CIS 0.18 μm process
  - Quadruple well process
  - Thick (~20 μm) epitaxial layer
  - with high resistivity (≥1 kΩ•cm)

- **SOI pixel sensor**
  - LAPIS 0.2 μm SOI process
  - High resistive substrate (≥1 kΩ•cm)
  - Double SOI layers available
  - Thinning and backside process
CMOS Prototype: JadePix1
(Team in IHEP)

- Diode optimization and radiation hardness study
- Two independent matrices:
  - Matrix-1: $33 \times 33 \, \mu m^2$ pixels
  - Matrix-2: $16 \times 16 \, \mu m^2$ pixels.
- A variety of diode geometries
  - Matrix-1: 20 sectors, each sector includes 48 rows and 16 columns.
  - Matrix-2: 16 sectors, each 96 rows and 16 columns.
- Analog readout
  - Source follower or voltage amplifier
  - Multiplexed to 16 analog output ports
Measurement of Diode Capacitance

- JadePix1 readout system developed at IHEP
- $^{55}\text{Fe}$ calibration
  - $K_\alpha = 5.9\ \text{keV},\ K_\beta = 6.5\ \text{keV}$
  - Charge Voltage Factor (CVF)
- $C_{\text{in}} = C_d + C_{\text{parasitic}}$
  - $C_{\text{in}} = 5\ \text{fF}$ on $4\ \mu\text{m}^2$ diode
  - $C_{\text{in}} = 6.15\ \text{fF}$ on $8\ \mu\text{m}^2$ diode

4 $\mu\text{m}^2$ diode, $V_{\text{diode}} \sim 1\ \text{V}$

8 $\mu\text{m}^2$ diode, $V_{\text{diode}} \sim 1\ \text{V}$
Performance after Irradiation

- JadePix-1 samples irradiated in neutron reactor to $10^{12}$, $5 \times 10^{12}$ and $10^{13}$ 1MeV $n_{eq}/cm^2$
- Larger diode (A3 > A1) more radiation hard as expected

Less charge collected within the cluster at high radiation levels

Calibration peaks visible after $10^{13}$
DESY Test Beam

- JadePix-1 position resolution characterized with the EUDET beam telescope and the electron beams at DESY;
- Offline event reconstruction with the EUTelescope software

*Irradiation and beam test -> poster by L. Chen*
Overview of JadePix2

(Team in IHEP)

- Chip area: $3 \times 3.3 \text{ mm}^2$;
- Matrix: $96 \times 112$ pixels with 8 sub-matrix
- Rolling shutter mode
- Every 16 columns of digital pixel share one LVDS transmitter
  - 160 MHz clock
  - 16-to-1 serializer
- A few columns configured as analog readout
  - For calibration of sensing diode

### Floorplan of JadePix2

<table>
<thead>
<tr>
<th>Sequence</th>
<th>Analogue out buffer ($\times 12$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>A1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Diode size</th>
<th>D1</th>
<th>A1</th>
<th>A2</th>
<th>D2</th>
<th>D3</th>
<th>A3</th>
<th>A4</th>
<th>D4</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 $\mu$m$^2$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8 $\mu$m$^2$</td>
<td></td>
<td></td>
<td></td>
<td>$\times 7$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Design Version</th>
<th>Matrix size:</th>
</tr>
</thead>
<tbody>
<tr>
<td>2: Single-end</td>
<td>$1: 48 \text{ row} \times 44 \text{ col.}$</td>
</tr>
<tr>
<td>1: Differential</td>
<td>$2: 48 \text{ row} \times 4 \text{ col.}$</td>
</tr>
<tr>
<td>2: Single-end</td>
<td>$1: 48 \text{ row} \times 60 \text{ col.}$</td>
</tr>
</tbody>
</table>

| 1 | 2 | 3 | 1 | 2 | 3 | 14 |
JadePix2: Voltage Discrimination in Pixel

- Two versions of Front-end
  - Version 1: differential amplifier + dynamic latch
  - Version 2: cascaded amplifier (single-ended) + dynamic latch
Design results of JadePix2

- Offset cancellation and high precision comparator
  - FPN (Fix Pattern Noise) $\sim 20 \text{ e}^{-}$
  - TN (Temporal Noise) $\sim 7 \text{ e}^{-}$
- Optimal sensing diode selected from JadePix1
  - Positively biased
  - AC coupled to the amplifier
- Rolling shutter mode
  - 100 ns / row (Version 1), 80 ns / row (Version 2)
  - 3.7 $\mu$A / pixel (Version 1), 6.5 $\mu$A / pixel (Version 2)
- Pixel size: $22 \times 22 \mu \text{m}^{2}$
Noise Measurement on JadePix2

- S-curve measured on Version 1 pixels (differential)
  - Scan ‘Vref2’ while ‘Clamp’ closed
- ENC = 31 e⁻
  - TN ~ 11 e⁻
  - FPN ~ 29 e⁻

![Diagram of LATCH Out+ Out- AMP Vref1 Vref1 Vref_latch Vref_latch Vref2 Read Read Read Read Read Calib Calib Calib Clamp Latch Vbias Power_on Buff Row_sel Out]

Threshold Distribution
- Entries: 1536
- Mean: 0.575
- Std Dev: 0.00108

FPN: 1.08mV @ input node
Equivalent 29.1 e⁻

Temporal Noise
- Entries: 1536
- Mean: 0.0004174
- Std Dev: 0.0002302

TN: 0.4mV @ input node
Equivalent 10.8 e⁻
Overview of MIC4

*Team in CCNU & IHEP*

- MIC4 (MAPS In CCNU 4)
- Pixel size: 25 um x 25 um
- Matrix: 128 rows x 64 columns
- Zero suppression embedded in columns
- High speed data link 1.2Gbps

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MIC4: Pulse Height Discrimination in Pixel

- Baseline front-end: the same structure as in ALPIDE*
  - Branch current 61 nA/pixel (increased by a factor of 3)
  - Peaking time < 1 $\mu$s, duration < 3 $\mu$s

*Reference: G. A. Rinella, NIMA845

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MIC4: Pulse Height Discrimination in Pixel

- Alternative front-end: Charge sensitive amplifier + current comparator
  - Feedback capacitance 0.2 fF
  - Peaking time < 550 ns @ Qin < 1.5 ke-
  - Pulse duration < 8.3 μs @ Qin < 1.5 ke-
  - 35 nW / pixel
  - ENC: 24 e-
Fast readout architecture:

- Hit registered by the latch in each pixel;
- Row and column lines indicate the coordinates of the hit pixel within an 8*8 block; In sequence of a priority chain.
- AERD (Address-Encoder and Reset-Decoder) to select the blocks that contain hits.
Noise Measurement on MIC4

- A test system has been setup in CCNU
- S-curve measured on pixels with baseline front-end
  - Test pulse injection
- Threshold set to 69.8 mV, equivalent to 99 e⁻
  - FPN = 21.9 mV, equivalent to 31 e⁻
  - TN = 0.65 mV, equivalent to 6 e⁻
Development of SOI Pixel Sensor

- N-in-P sensor capable of full depletion
  - BNW and N⁺ as collection electrode
  - BPW available as P-spray
- Isolation of transistors
  - Buried Oxide (insulation)
  - SOI2 (grounded for shielding)
- In-Pixel ampl. & disc:
  - Signal charge ~ 4000e (in 50 μm silicon)
  - Very small Cd
  - Voltage amplifier & comparator
  - Very compact pixel ~ 16 μm pitch
Pixel design in CPV1

- CPV (Compact Pixel for Vertex)
- Sensing diode, 2 µm
  - $Cd = 1 \text{ fF}$
- Voltage amplifier, DC Gain ~ 10
  - 1 µA, power on when row selected
- Offset cancellation reset
- Inverter as discriminator
- Charge injection at $Vin$
  - Setting threshold
- Minimize layout area
  - $16 \times 16 \mu m^2$

<table>
<thead>
<tr>
<th>Diode diameter ($\mu m$)</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Cd$ (fF)</td>
<td>1</td>
<td>1.8</td>
<td>2.8</td>
</tr>
</tbody>
</table>
Pixel design in CPV2

- Pixel circuit adjusted on basis of CPV1
- Discharging transistor added to Vin
  - Diode-connected NMOS
  - $V_{\text{diode}} = 0V$
  - Discharging when Vin < 0V
- CDS stage inserted between apmp. and invt.
  - Improve RTC and FPN noise
  - Setting threshold by $V_{\text{clamp}}$

![Pixel circuit in CPV2](image)
Chip architecture

- Rolling shutter mode
  - 100 ns / row
- 64 rows \times 64 columns
  - Half matrix has SFs in place of inverters
- Address decoder to select column & row
  - Very flexible during test
- Same architecture for CPV1/2
  - I/O compatible
  - Readout using SEABAS* DAQ system

*SEABAS: SOI Evaluation Board with Si TCP/IP, by KEK*
Prototype Characterization

- CPV2 thinned down to 75 µm
  - Backside P⁺ implantation after thinning
- Very low leakage current
  - ~ pA/pixel @ Vbias = -100 V
- Full depletion confirmed with $^{55}$Fe and Infrared laser respectively
  - $V_{\text{depletion}}$ ~ -30 V
- Calibration with $^{55}$Fe 5.9 keV X-ray
  - CVF = 123.3 µV/e⁻ @ Vout
  - Can be improved by Cascode amplifier
Noise Measurement

- S-curve measured on the digital pixel array
  - TN ~ 6 e⁻
  - FPN ~ 114 e⁻
Laser position scan with different intensity

- Scan across two adjacent digital pixels
- Threshold is fixed (minimum threshold without noise hit)
- Step size of 1µm
- Different beam intensity used

\[ \text{Normalized response} = \frac{\text{Number of hits}}{\text{Number of pulses}} \]
Residual distribution

- RMS of residual distribution indicates its single point resolution

Residual distribution changes with beam intensity

Signal charge: 1574e^-

Entries: 393190
Mean: -0.2123
RMS: 4.117

Signal charge: 2308e^-

Entries: 393216
Mean: -0.02989
RMS: 2.556

Signal charge: 3148e^-

Entries: 393216
Mean: 0.03524
RMS: 2.999

Signal charge: 4722e^-

Entries: 393216
Mean: 0.0164
RMS: 2.751
Single Point Resolution

- Single point resolution versus signal charge
  - Obtained the best resolution of 2.3μm around signal charge 3000 e⁻
  - Low threshold is critical

[Graph showing resolution versus signal charge]
# Comparison of digital pixel chips

<table>
<thead>
<tr>
<th></th>
<th>JadePix2</th>
<th>MIC4</th>
<th>CPV2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>CMOS</td>
<td>CMOS</td>
<td>SOI</td>
</tr>
<tr>
<td>Pixel size</td>
<td>$22 \times 22 , \mu m^2$</td>
<td>$25 \times 25 , \mu m^2$</td>
<td>$16 \times 16 , \mu m^2$</td>
</tr>
<tr>
<td>TN (e⁻)</td>
<td>11</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>FPN (e⁻)</td>
<td>29</td>
<td>31</td>
<td>114</td>
</tr>
</tbody>
</table>
As an alternative technology option for the SIT and FTD

CMOS pixel sensor is of particular interest
- High granularity
- Low material budget
- Large single chip via stitching
- Possible cost reduction

Readout channels increased significantly
- Trade off between granularity and readout time needed
- A case study conducted for the CDR writing

Estimated occupancies of the first layers in the SIT and FTD. Pixel size of $50 \times 350 \, \mu m^2$, readout time of 10 $\mu s$ assumed.
To understand charge collection in larger pixels is essential for

- Optimal pixel dimensions &
- Diode geometries

Structures in TCAD simulation

- Pixel size: 21 × 21 µm², 21 × 42 µm², 21 × 84 µm²
- A variety of diode geometries
- 1 diode per pixel
- The epitaxial layer: 18 µm & 1 kΩ·cm
- Bias voltage: 1.8 V
- Hit in the very center of pixel
- 5×5 pixel cluster
Simulation Results of Charge Collection

- Sum of charge collected by a cluster of 5 × 5 pixels
  - Larger pixels exhibit small cluster size

<table>
<thead>
<tr>
<th>Pixel</th>
<th>P1</th>
<th>P2</th>
<th>P3</th>
<th>P4</th>
<th>P5</th>
<th>P6</th>
<th>P7</th>
<th>P8</th>
<th>P9</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pitch(µm)</td>
<td>21</td>
<td>42</td>
<td>84</td>
<td>21</td>
<td>42</td>
<td>84</td>
<td>21</td>
<td>42</td>
<td>84</td>
</tr>
<tr>
<td>N(D)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>F(D)(µm²)</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>5</td>
<td>18</td>
<td>18</td>
<td>15</td>
<td>44</td>
<td>50</td>
</tr>
<tr>
<td>S(D)(µm²)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>4</td>
<td>12</td>
<td>12</td>
<td>6</td>
<td>20</td>
<td>20</td>
</tr>
</tbody>
</table>

N(D) = number of diodes in each pixel (1)
F(D) = footprint of diode (diode area + pwell opening):
5, 11, 15, 18, 44 & 50 µm²
S(D) = surface of diode: 4, 6, 8, 12 & 20 µm²
Prototype Chip using TowerJazz CIS 0.18 μm process

- SUPIX (Shandong University Pixel)
- Total sensitive area: 2 × 7.88 mm²
  - 9 submatrices corresponding to the pixel structures in the TCAD simulation
    - Each submatrix: 16 × 64
- Analog readout
  - Source follower
  - Diode-connected transistor for reset
- Rolling shutter mode
  - 32 μs integration time at 2 MHz clock frequency
  - 16 parallel analog outputs
  - 50 μA current per column
- Gate-enclosed NMOS transistors
  - To improve radiation tolerance

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The test setup consists of:

- DUT board: customized for the chip
- ADC board: provided by IHEP, the same as used for JadePix1 test
- FPGA board: firmware and DAQ software in development
- SSD high speed data storage \( \rightarrow >1\text{Gb/s} \).
Output pedestal observed via oscilloscope

- Variation of baseline measured: 10 mV peak to peak
- $^{55}$Fe source test ongoing

Persistence mode

Clock

Output pedestal

Frame out

~ 10 mV
Summary

- Pixel design of high spatial resolution, low power and fast readout is required for the CEPC silicon tracker.
- A variety of pixel chip designed specifically for CEPC as part of the R&D activities.
  - Optimization of sensing diode to improve Q/C
  - Low power low noise amplifier and discriminator in pixel
  - Fast readout architecture
- Sensing diode Q/C characterized
- Noise of different front-end characterized and compared
- Spatial resolution $< 3 \, \mu\text{m}$ demonstrated on small pitch of $16 \, \mu\text{m}$
Future Plan on R&D

- Laboratory and test-beam characterizations
- Coordination of design team for next submission
- Large area chip design
- Radiation hardness
- For time stamp @ Z-pole
  - Explore SOI 3D connection technology
  - Look for new process with smaller feature size
Thank you for your attention!

Team in IHEP:

Team in Shandong University:
J. Dong, L. Li, J. Liu, M. Wang, L. Zhang

Team in CCNU:
C. Gao, W. Ren, X. Sun, D. Wang, L. Xiao, P. Yang

Below are backup slides
<table>
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<td>Number of IPs</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Beam energy (GeV)</td>
<td>120</td>
<td>80</td>
<td>45.5</td>
<td></td>
</tr>
<tr>
<td>Circumference (km)</td>
<td></td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Synchrotron radiation loss/turn (GeV)</td>
<td>1.73</td>
<td>0.34</td>
<td>0.036</td>
<td></td>
</tr>
<tr>
<td>Crossing angle at IP (mrad)</td>
<td></td>
<td></td>
<td>$16.5 \times 2$</td>
<td></td>
</tr>
<tr>
<td>Piwinski angle</td>
<td>2.58</td>
<td>7.0</td>
<td>23.8</td>
<td></td>
</tr>
<tr>
<td>Number of particles/bunch $N_p$ $\left(10^{10}\right)$</td>
<td>15.0</td>
<td>12.0</td>
<td>8.0</td>
<td></td>
</tr>
<tr>
<td>Bunch number (bunch spacing)</td>
<td>242 ($0.68\mu$s)</td>
<td>1524 ($0.21\mu$s)</td>
<td>12000 (25ns+10%gap)</td>
<td></td>
</tr>
<tr>
<td>Beam current (mA)</td>
<td>17.4</td>
<td>87.9</td>
<td>461.0</td>
<td></td>
</tr>
<tr>
<td>Synchrotron radiation power/beam (MW)</td>
<td>30</td>
<td>30</td>
<td>16.5</td>
<td></td>
</tr>
<tr>
<td>Bending radius (km)</td>
<td></td>
<td></td>
<td>10.7</td>
<td></td>
</tr>
<tr>
<td>Momentum compact ($10^{-5}$)</td>
<td></td>
<td>1.11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\beta$ function at IP $\beta_1 \beta_2$ ($\mathrm{m}$)</td>
<td>0.36/0.0015</td>
<td>0.36/0.0015</td>
<td>0.2/0.0015</td>
<td>0.2/0.001</td>
</tr>
<tr>
<td>Emittance $\xi_1 / \xi_2$ ($\mu$m)</td>
<td>1.21/0.0031</td>
<td>0.54/0.0016</td>
<td>0.18/0.004</td>
<td>0.18/0.0016</td>
</tr>
<tr>
<td>Beam size at IP $\sigma_1 / \sigma_2$ ($\mu$m)</td>
<td>20.9/0.068</td>
<td>13.9/0.049</td>
<td>6.0/0.078</td>
<td>6.0/0.04</td>
</tr>
<tr>
<td>Beam-beam parameters $\xi_1 / \xi_2$</td>
<td>0.031/0.109</td>
<td>0.013/0.106</td>
<td>0.0041/0.056</td>
<td>0.0041/0.072</td>
</tr>
<tr>
<td>RF voltage $V_{RF}$ (GV)</td>
<td>2.17</td>
<td>0.47</td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>RF frequency $f_{RF}$ (MHz) (harmonic)</td>
<td></td>
<td>650 (2168)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Natural bunch length $\sigma$ ($\mu$m)</td>
<td>2.72</td>
<td>2.98</td>
<td>2.42</td>
<td></td>
</tr>
<tr>
<td>Bunch length $\sigma$ ($\mu$m)</td>
<td>3.26</td>
<td>5.9</td>
<td>8.5</td>
<td></td>
</tr>
<tr>
<td>Betatron tune $\nu_1 / \nu_2$</td>
<td></td>
<td></td>
<td>363.10 / 365.22</td>
<td></td>
</tr>
<tr>
<td>Synchrotron tune $\nu_s$</td>
<td>0.065</td>
<td>0.0395</td>
<td>0.028</td>
<td></td>
</tr>
<tr>
<td>HOM power/cavity (2 cell) (kw)</td>
<td>0.54</td>
<td>0.75</td>
<td>1.94</td>
<td></td>
</tr>
<tr>
<td>Natural energy spread (%)</td>
<td>0.1</td>
<td>0.066</td>
<td>0.038</td>
<td></td>
</tr>
<tr>
<td>Energy acceptance requirement (%)</td>
<td>1.35</td>
<td>0.4</td>
<td>0.23</td>
<td></td>
</tr>
<tr>
<td>Energy acceptance by RF (%)</td>
<td>2.06</td>
<td>1.47</td>
<td>1.7</td>
<td></td>
</tr>
<tr>
<td>Photon number due to beamstrahlung</td>
<td>0.29</td>
<td>0.35</td>
<td>0.55</td>
<td></td>
</tr>
<tr>
<td>Lifetime simulation (min)</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lifetime (hour)</td>
<td>0.67</td>
<td>1.4</td>
<td>4.0</td>
<td>2.1</td>
</tr>
<tr>
<td>$F$ (hour glass)</td>
<td>0.89</td>
<td>0.94</td>
<td>0.99</td>
<td>42</td>
</tr>
<tr>
<td>Luminosity/IP $L \left(10^{34} \text{cm}^{-2}\text{s}^{-1}\right)$</td>
<td>2.93</td>
<td>10.1</td>
<td>16.6</td>
<td>32.1</td>
</tr>
</tbody>
</table>
Occupancy at the first Vertex layer

Here we assume 10 μs of readout time for the silicon pixel sensor and an average cluster size of 9 pixels per hit, where a pixel is taken to be 16×16 μm². The resulting maximal occupancy at each machine operation mode is below 1%.
Diode geometries compete for real estate with transistors
- **Diode area**: charge collection electrode
- **Footprint**: spacing between P/N-well is critical for low capacitance

Methods to apply bias voltage
- **Positive bias**: AC couple capacitor $C_c$
- **Negative bias**: threshold shift of NMOS

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Charge Collection in HR epi. layer

- Pixel cluster with four different epitaxial layers (TCAD simulation)
  - 18 μm, 1 kΩ \cdot cm
  - 20 μm, 2 kΩ \cdot cm
  - 25 μm, 2 kΩ \cdot cm
  - 30 μm, 8 kΩ \cdot cm

- Seemingly optimal charge collection in 20 μm, 2 kΩ \cdot cm
  - Maximum peak signal
  - Constrained cluster size

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Positive Bias of Diode

- Bias voltage up to 10 V
  - To measure seed/cluster signal versus $V_{bias}$
  - To measure the cluster size
- Optimization of $C_c$, $V_{calib}$, SF and noise
- Layout
  - $16 \times 16 \, \mu m^2$
  - Direct PAD for $V_{diode}$

Pixel Layout
- $16 \times 16 \, \mu m^2$
- with transistors under MIM capacitor

Direct PAD layout for $V_{diode}$
- $250 \times 65 \, \mu m^2$
- Without ESD
- Both sizes & power lines match with other PADs provided by foundry
Device simulation

- **Device configuration**
  - 1 kΩ·cm DSOI wafer (P substrate)
  - N⁺ electrode 2 µm in diameter
  - Pixel pitch 16 µm
  - Sensor thickness 50 µm

- **Transport of charge carriers**
  - Analyzed by TCAD tools

**How to achieve s.p. resolution < 3µm?**

**Collected charge vs hit position**

![Graph showing collected charge vs hit position.](image)
Device simulation

- Noise smearing and threshold discrimination applied numerically
  - ENC ~ 20e-
  - Threshold ~ 200e-
- Residual distribution changes with threshold
  - Low noise front-end is critical to exploit the charge sharing
  - Should note that only perpendicular tracks here
  - Detailed study → poster by Z. Wu

Residual distribution with threshold = 200 e⁻

Single point resolution vs threshold

- \( p \sqrt{12} = 4.62 \)
- \( 0.5p/\sqrt{12} = 2.31 \)
Thinning process for CPV2

- Wafer thinning -> Chip dicing
  - SOIPIX collaboration
  - Thinning to 300 μm is regular
  - Thinning to 75 μm is available only on request
  - No aluminum on the backside of 75 μm chips
    - Enable backside illumination of infrared laser

**Thinning process flow**

1. Initial wafer thickness 700μm
2. Mechanical grinding 100μm
3. Wet etching 75μm
4. Implantation & Annealing 75μm
5. Dicing 75μm

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Leakage current

- I-V curve @ room temperature
  - Total Leakage current reaches the plateau when bias voltage is -15V
  - No breakdown up to 100 V
  - Diode current is very small both (~nA over the full matrix, 1mm$^2$)

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Depletion measurement

- $^{55}$Fe signal Efficiency versus bias voltage
  - X-ray photons counted by analog pixel cluster
  - X-ray illuminates the sensor from backside
  - Depletion zone develops starting from the topside
  - Plateau reached @ $V_{bias} = -30V$
55Fe source calibration

- Charge voltage factor (CVF)
  - Cluster peak at 360 (ADU)
  - SF gain measured 0.87
  - CVF = 123.3uV/e- @ Vout

- Excessive $C_{in}$?
  - 14fF
  - Miller capacitance?

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Investigation of threshold dispersion

- Threshold dispersion 8.3 mV for inverter standalone
  - In contrast to 14 mV of complete pixels
  - Can be mitigated by improving CVF

- Leakage of NMOS transistor
  - Low Vth &
  - Very short, W/L = 0.4u/0.2u
- Vin ~ 0.5V, V_diode = 0.35V
  - Minimize integration time
Laser test setup

- 1064nm laser beam
  - Focused beam waist ~ 3.4 µm
  - Adjustable energy ~ pJ/pulse
  - Short pulse duration ~ 100 ps

- 3-dimensional stepping motor
  - Minimum step size: 0.1 µm
  - Position resolution < 1 µm

- Backside illumination
Depletion reconfirmed by laser test

- Laser signal versus bias voltage
  - Inflection point @ $V_{bias} = -27V$
  - Reconfirmed the result of $^{55}$Fe source test
  - Choosing $V_{bias} = -100V$ in the following laser scan test

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