SOIPIX
Silicon-On-Insulator Pixel Detector Project

SOIPIX: Status & Perspectives

~ ILC vertex detector & 3D Integration ~

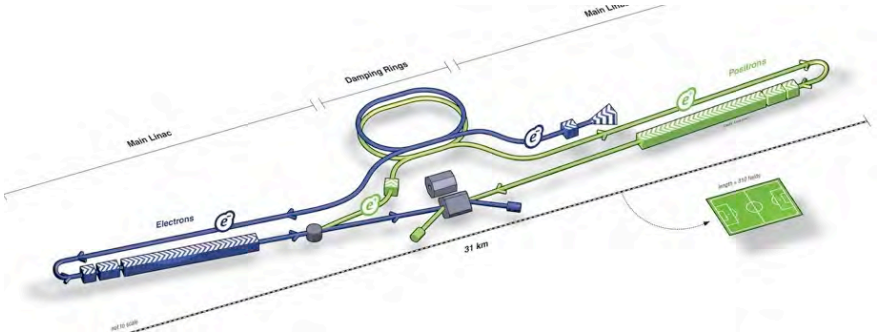
Nov. 13, 2018 @ international workshop on the high energy Circular Electron-Positron Collider (CEPC), IHEP, Beijing

Yasuo Arai

High Energy Accelerator Research Organization (KEK)

yasuo.arai@kek.jp, *http://rd.kek.jp/project/soi/*

Outline

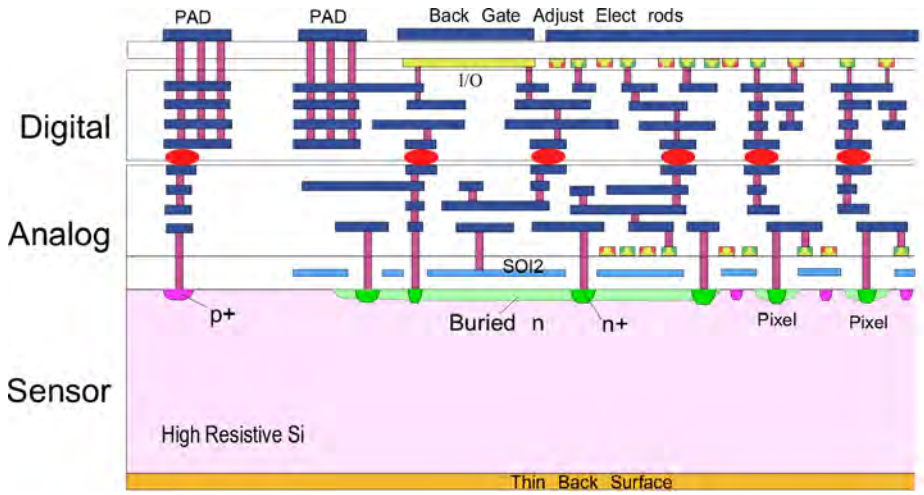


I. Introduction

II. SOI Pixel Detector

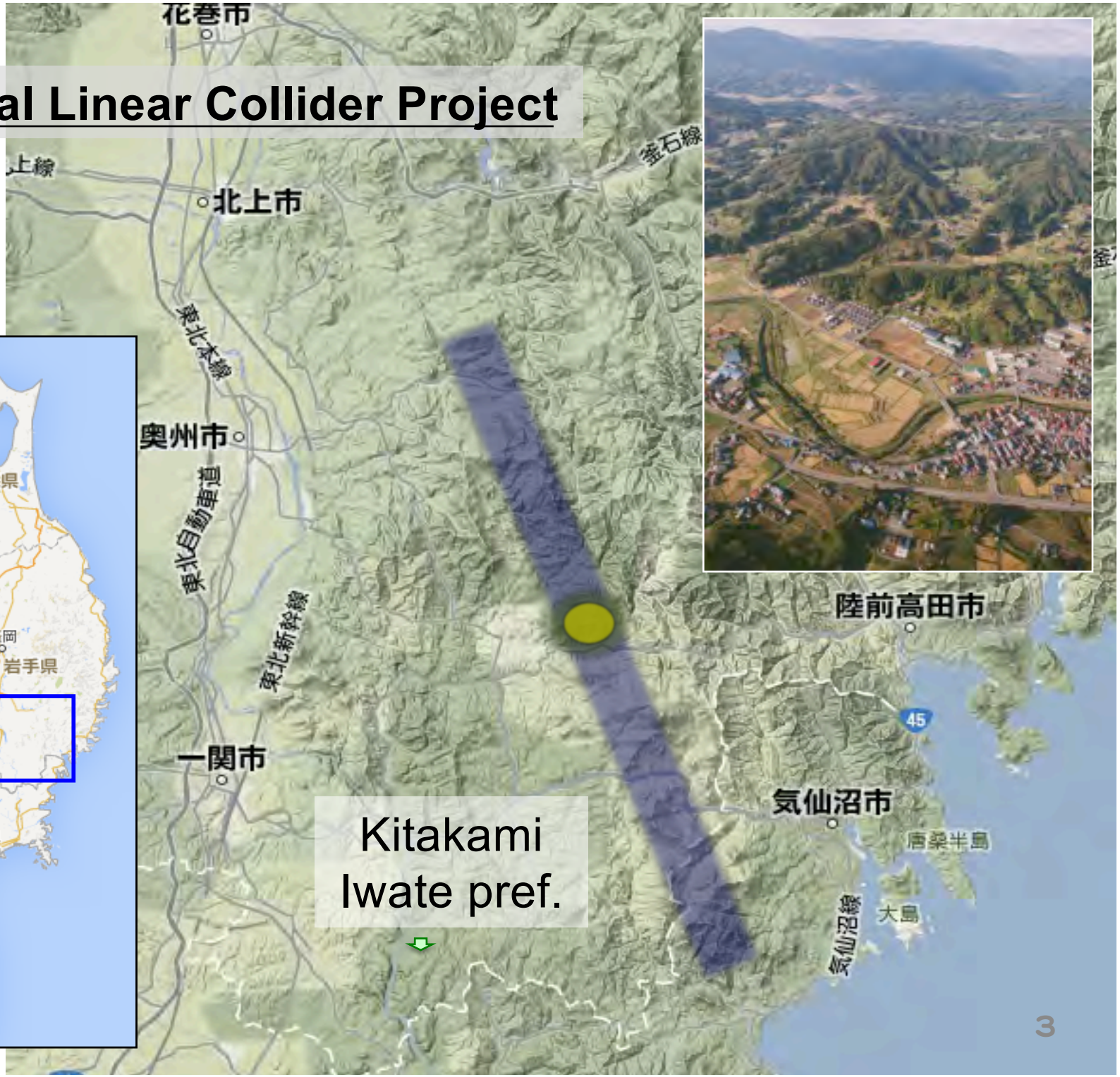
III. R&D for ILC Vertex Detector & 3D Integration

IV. Summary



(SOI: Silicon-On-Insulator)

International Linear Collider Project



Kitakami
Iwate pref.

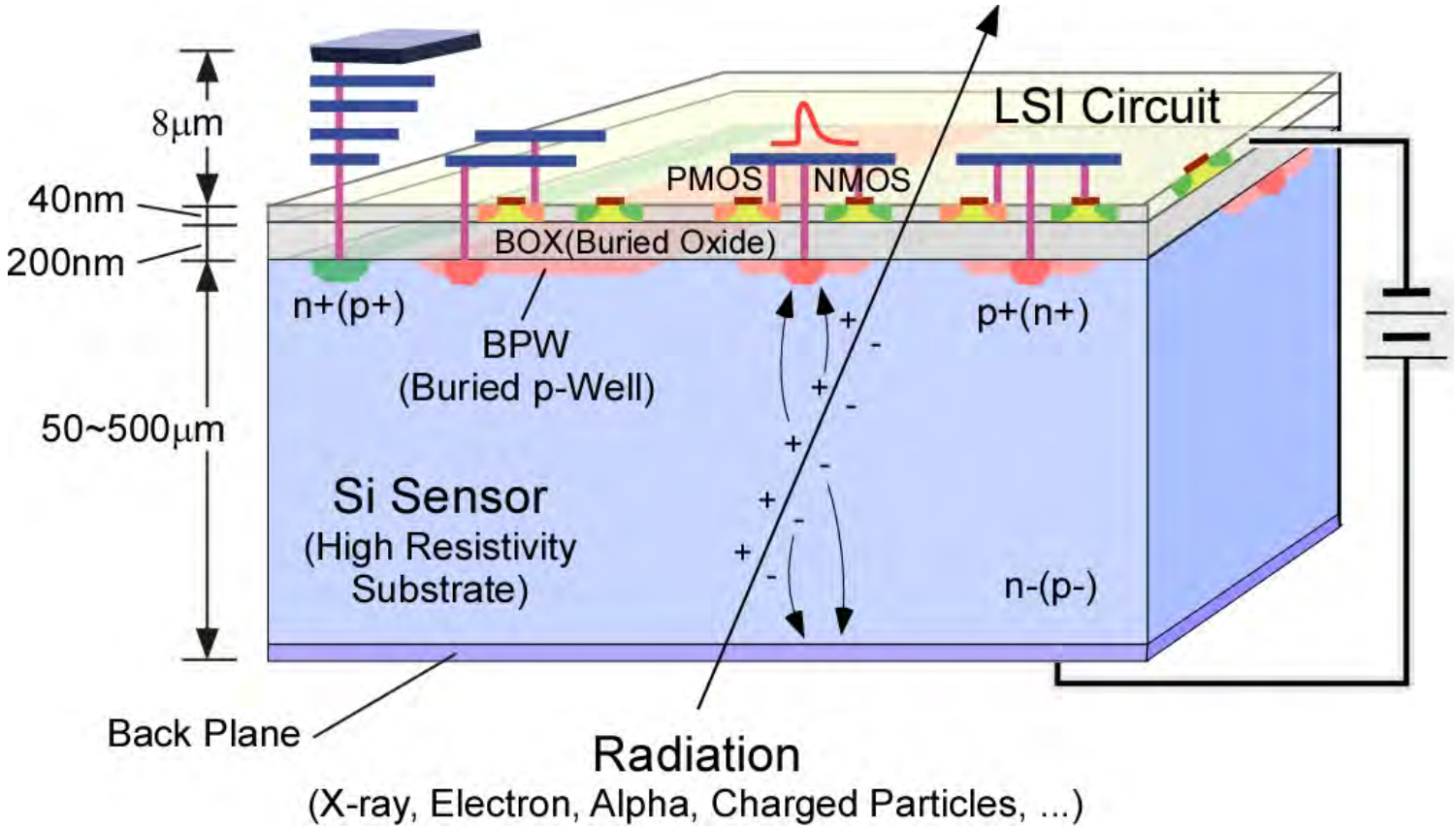
ILC Vertex detector

Requirements:

1) Single point resolution: better than 3 μm
   -> Pixel size: ~20 × 20 μm^2
2) Time resolution: single-crossing (554 ns interval) time resolution
3) Detector occupancy: < 2 %
4) Low material budget: $X \leq 0.1 - 0.2\ \%\ X_0$ / Layer
   → ~50 μm thick Si
   → low-power ASICs (~ 50 mW/cm^2) + gas-flow cooling
5) Radiation hardness:
   TID : < 1 kGy / year
   NIEL: < 10^{11} 1MeV n_{eq} / cm^2 / year

II. SOI Pixel Detector

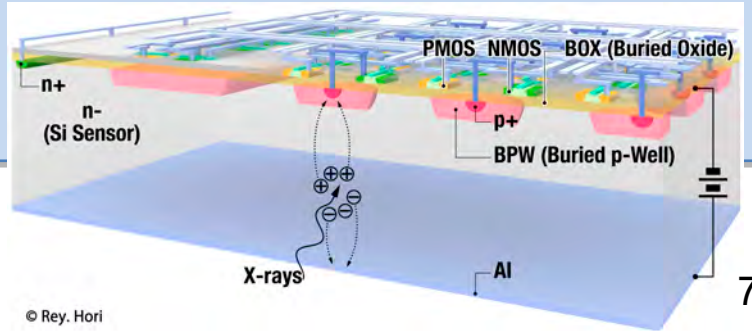
Silicon-On-Insulator Pixel Detector (SOIPIX)



Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.

Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding.
- Fabricated with semiconductor process only.
  → High reliability and Low Cost.
- High Resistive fully depleted sensor (50um~700um thick) with Low sense node capacitance. → Large S/N.
- On Pixel processing with CMOS circuits.
- No Latch up and very low Single Event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.



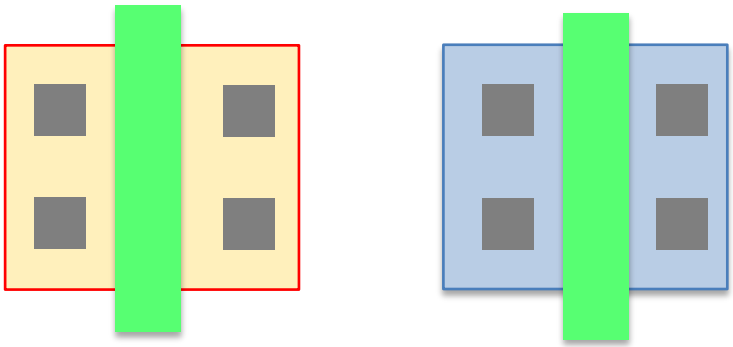
Lapis Semi. Co., Ltd 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer (single)	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

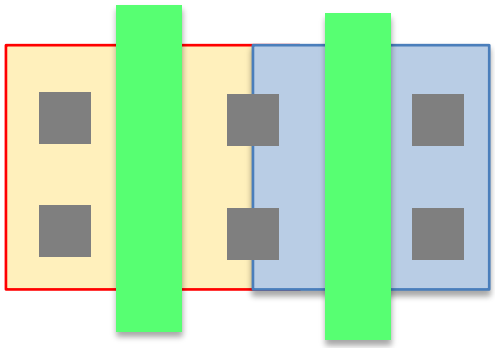
Layout Shrink（Active Merge)

SOI

PMOS NMOS

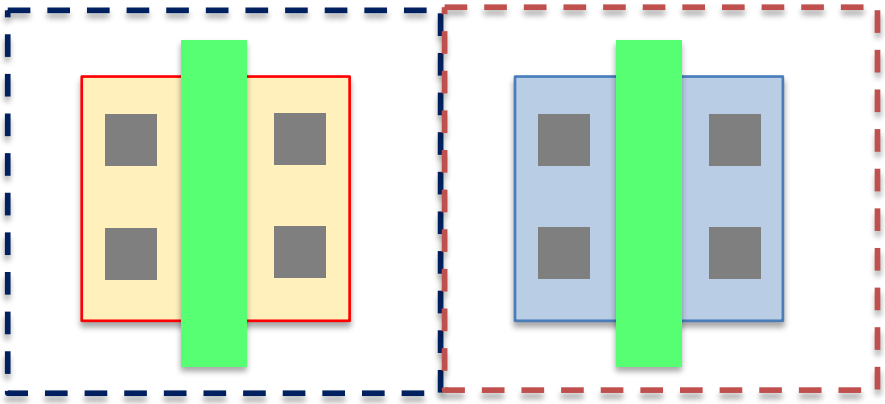


Share Contacts



Bulk CMOS

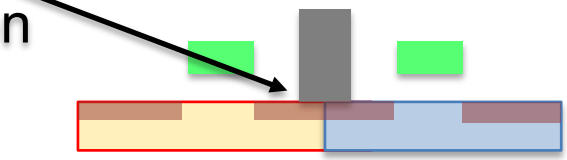
PMOS NMOS



N-Well P-Well

Much smaller layout is possible while keeping high analog operating voltage.

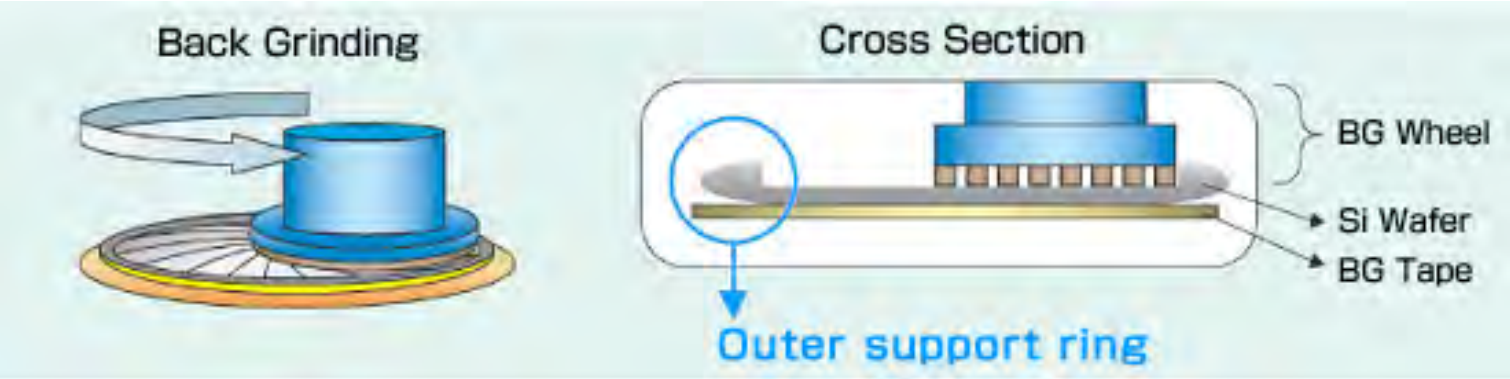
Salicide Connection



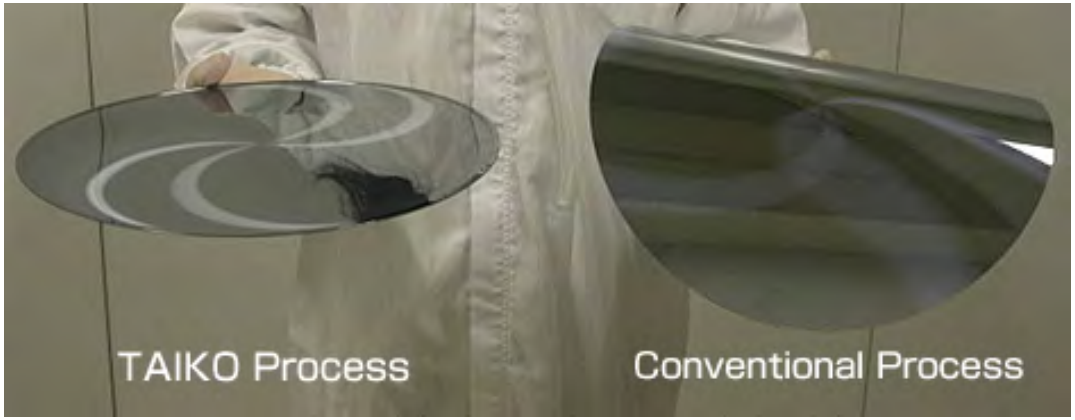
Wafer Thinning

TAIKO Process by DISCO Co.

DISCO
Kiru·Kezuru·Migaku Technologies

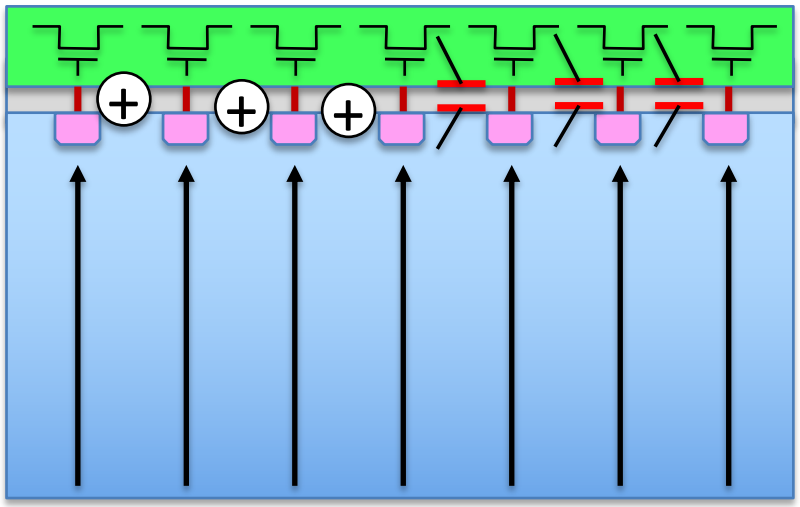


With outer support ring
- Lower wafer warpage
- Improve wafer strength
- Easy wafer handling
- Easy backside processing (ion implantation, annealing, Metalizing etc) after thinning



We have successfully thinned several SOI wafers to ~75 μm thick.

Issues in SOI Pixel

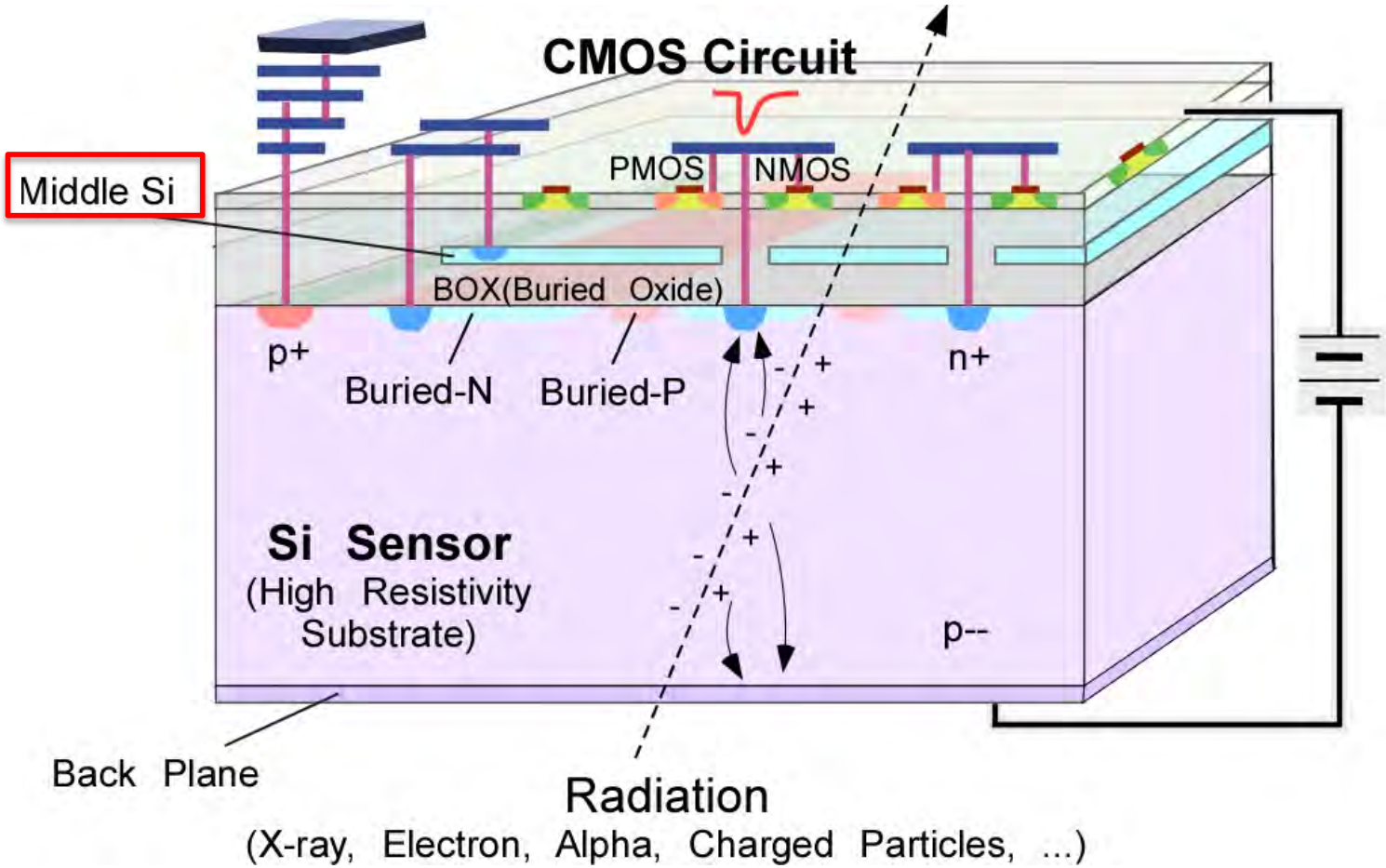


- Transistors does not work with high Detector Voltage. (Back-Gate Effect)
- Coupling between Circuit signal and sense node. (Signal Cross Talk)
- Oxide trapped hole induced by radiation will shift transistor threshold voltage. (Radiation Tolerance)

The use SOI technology for pixel detector is already discussed in 1990(*). Unfortunately, in 1990s, due to immature process technology, no good high-resistivity SOI wafer etc. , many SOI sensor R&D projects were stopped.

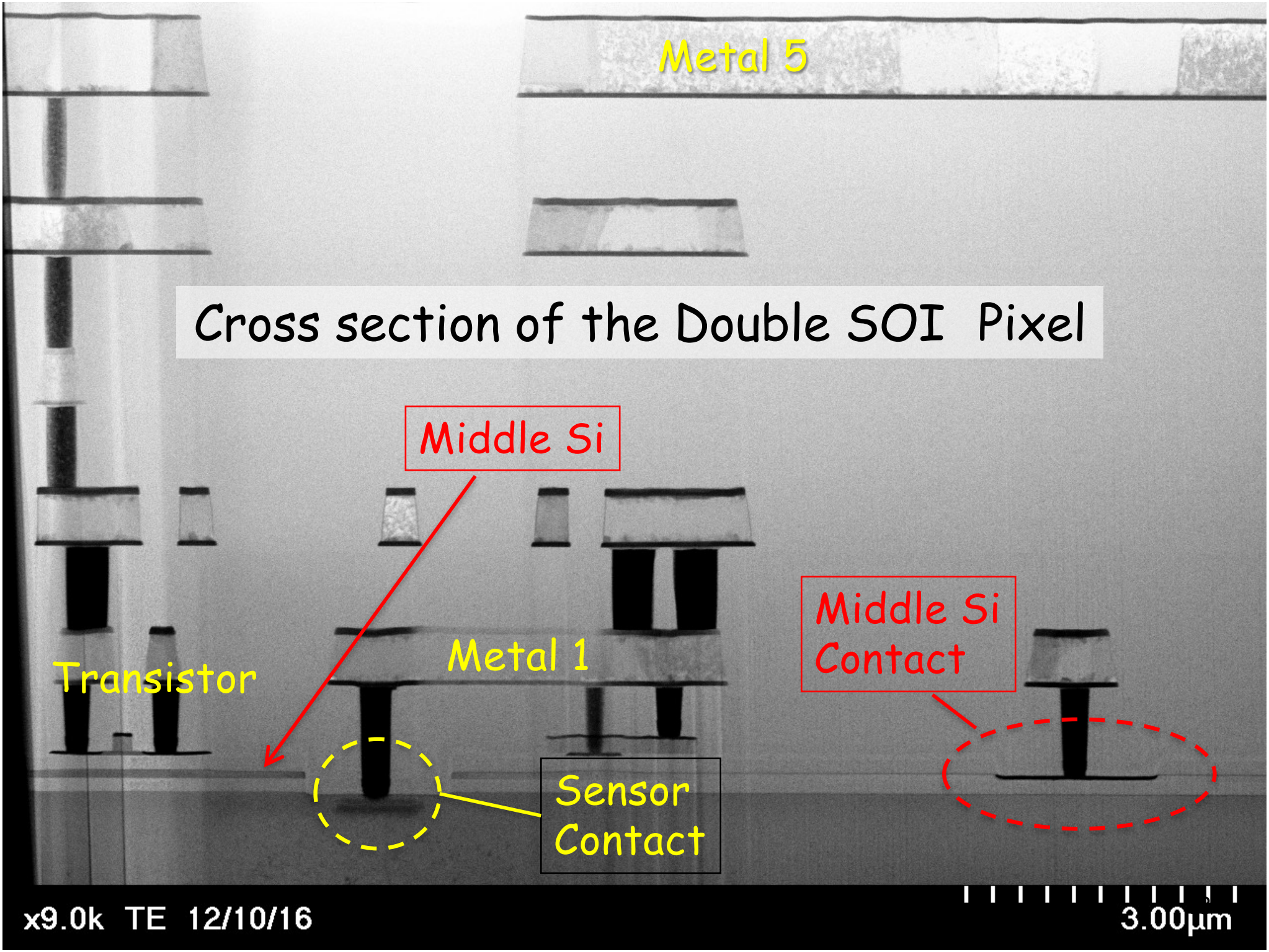
(*) Jean-Pierre Colinge, 'An overview of CMOS-SOI technology and its potential use in particle detection systems', NIM A305 (1991) 615-619.

Double-SOI PIX Detectors



Double SOI Detector

- Middle Si layer shields coupling between sensor and circuit.
- It also compensate E-field generated by radiation trapped hole.
- Good for Complex function and Counting-type sensor.
- Can be used in High radiation environment.

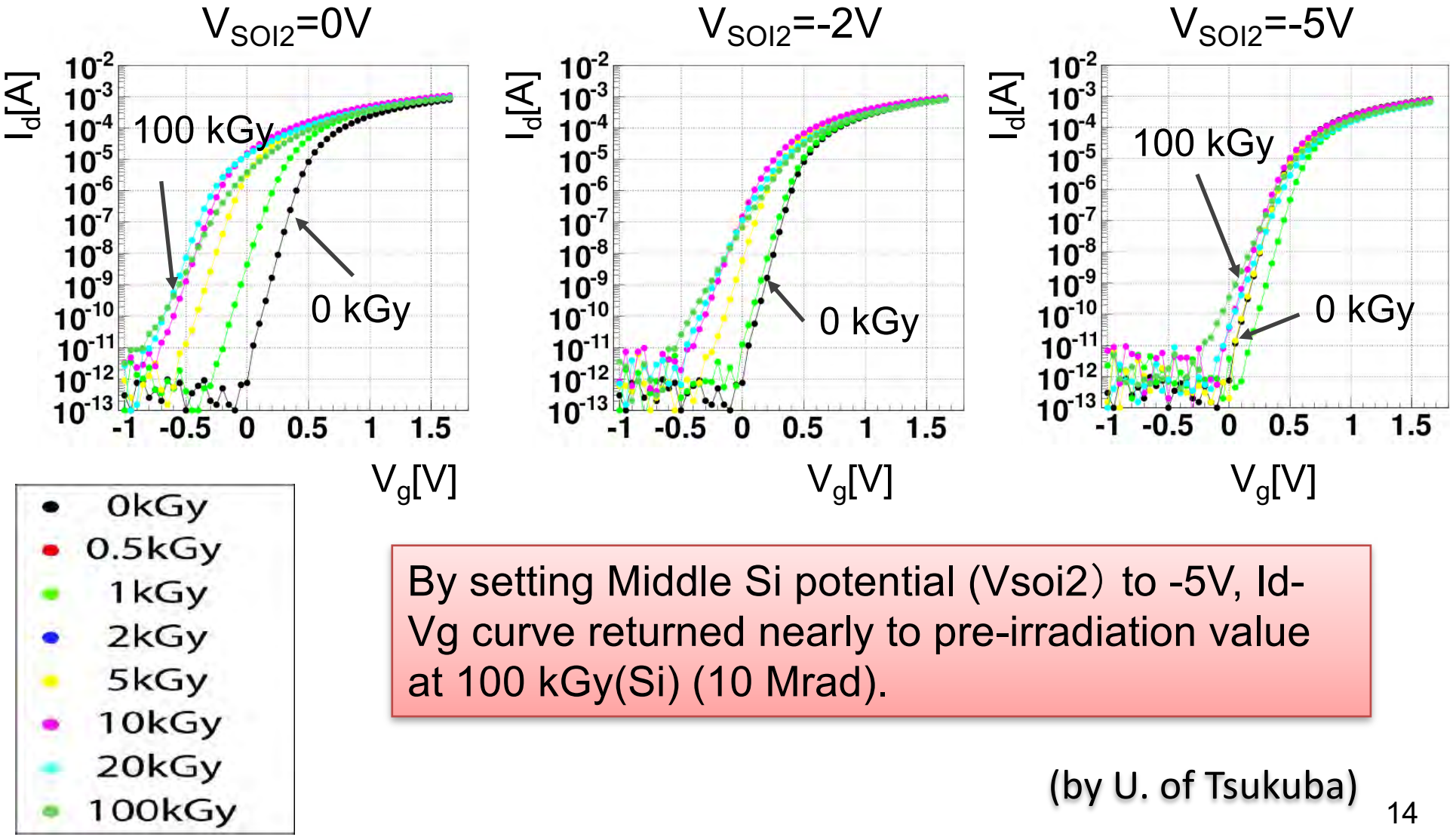

Metal 5
Cross section of the Double SOI Pixel
Middle Si
Transistor
Metal 1
Middle Si Contact
Sensor Contact
x9.0k TE 12/10/16
3.00µm

Gamma-ray Irradiation Test

(Id-Vg Characteristics v.s. SOI2 Potential)

I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

NMOS



By setting Middle Si potential (Vsoi2) to -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si) (10 Mrad).

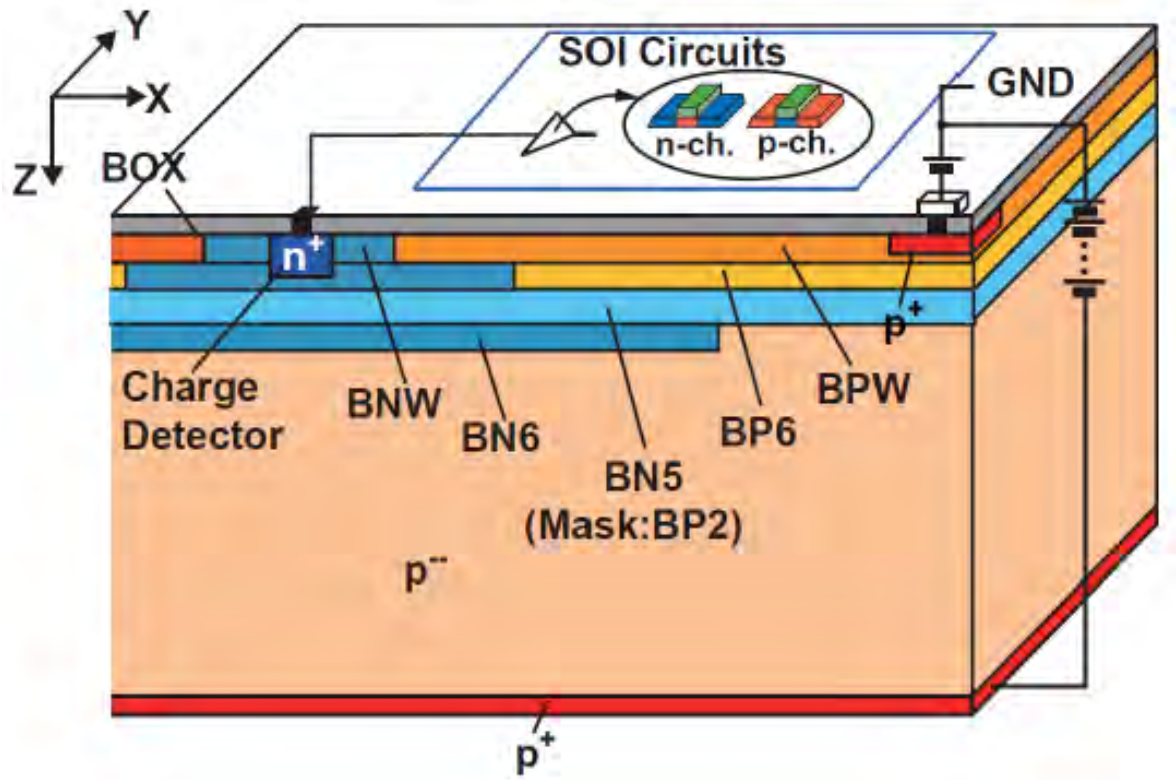
(by U. of Tsukuba)

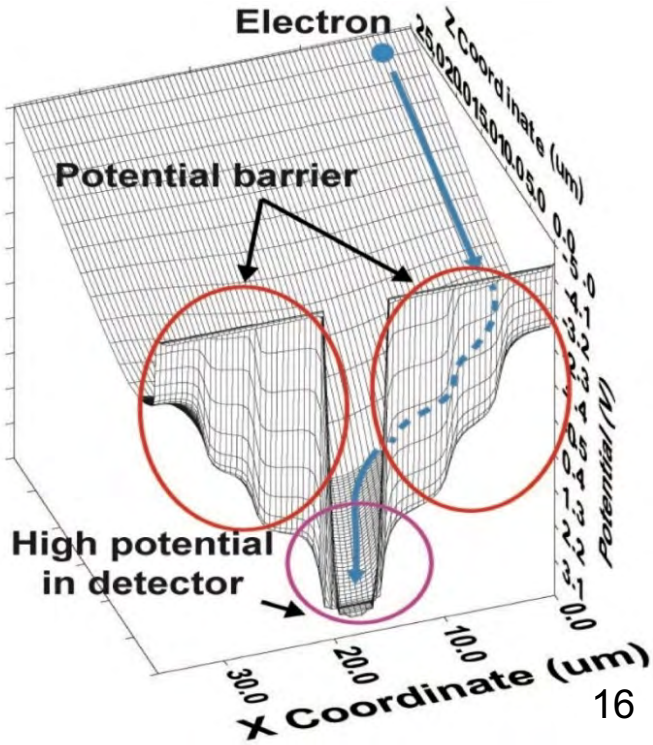
Present issue in the Double SOI Wafer

- Double SOI technology showed very good performance and solved major issues in the SOI Detector.
- Unfortunately, quality of the DSOI wafer is not so good at present stage since it is not commercial wafer and number of produced wafer is still very small.
- This causes process troubles (void, bending,,,) sometime. Furthermore, delivery time is very long especially when the wafer maker is very busy (now).
- Then, we also developed another sensor structure by introducing many buried well, called Pinned Depleted Diode (PDD) in parallel.

New Sensor Structure: Pinned Depleted Diode (SOIPIX-PDD)

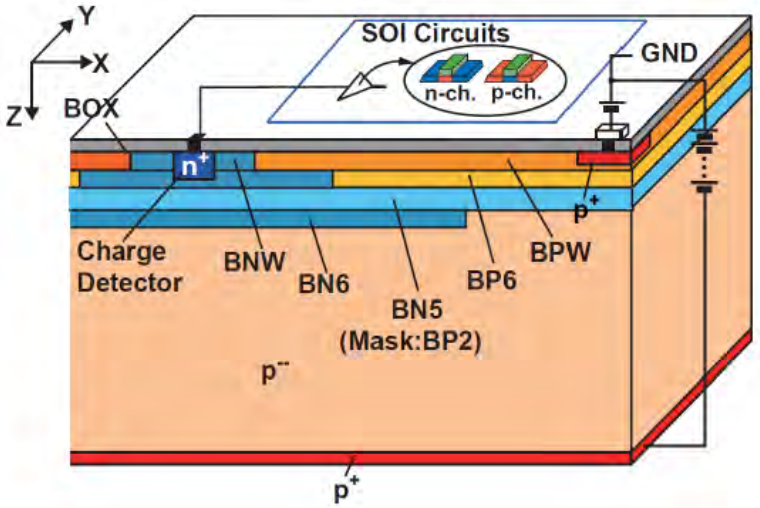
Si-SiO_2 interface is pinned.
Charge is collected in very small node.

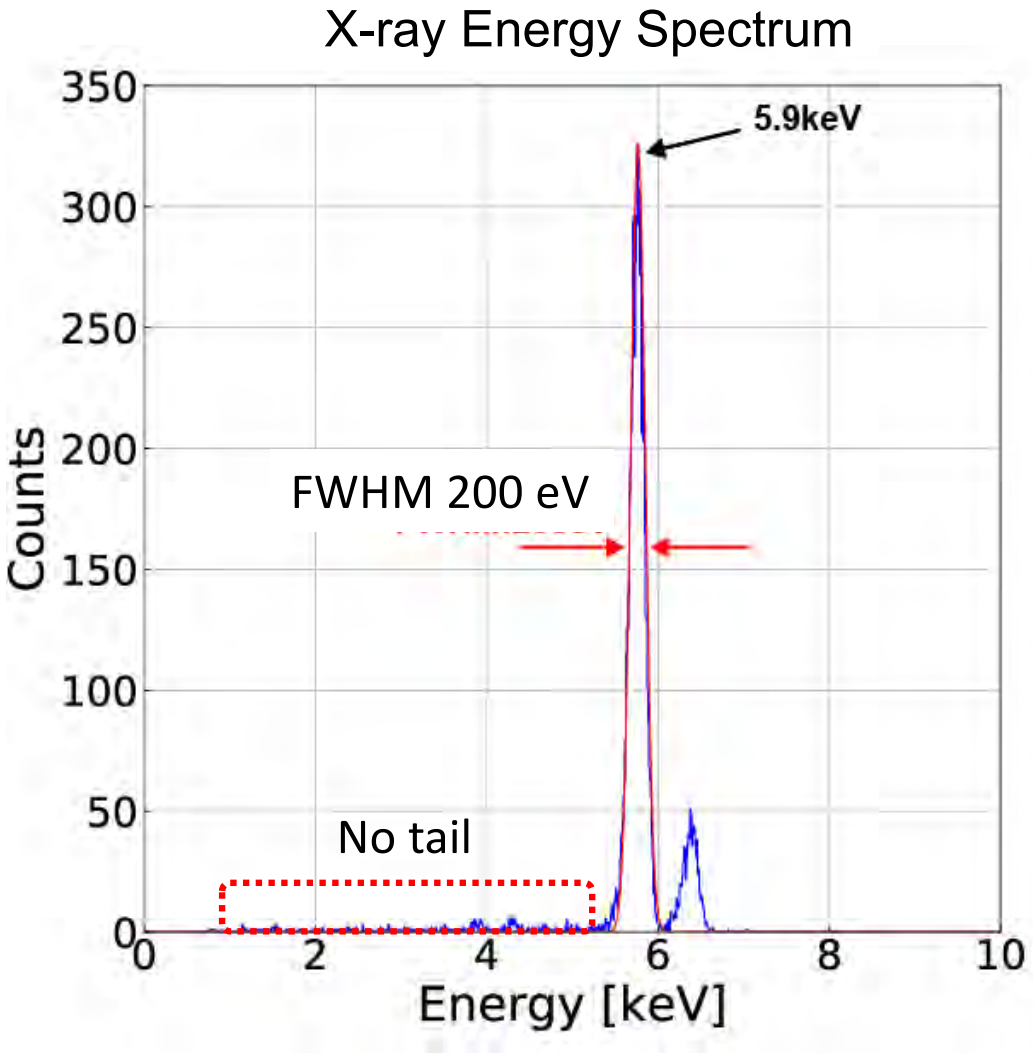




(Shizuoka U., Prof. Kawahito)

Pinned Depleted Diode (SOIPIX-PDD)

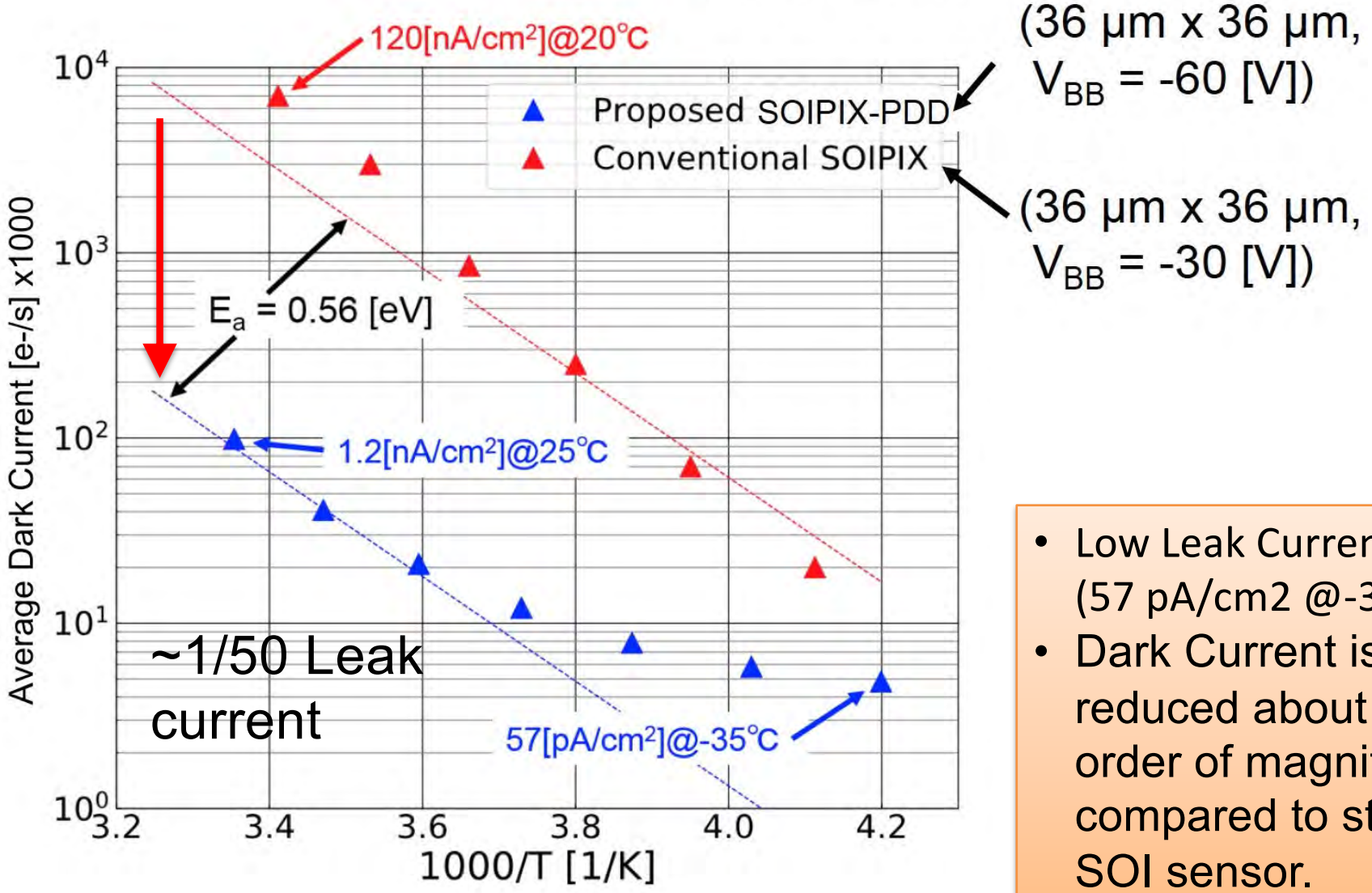




- High Gain (70 μV/e-)
- Good Energy Resolution (Noise = 11.0 e-)
- High Charge Collection Efficiency (No X-ray tail)

(Shizuoka U., Prof. Kawahito)

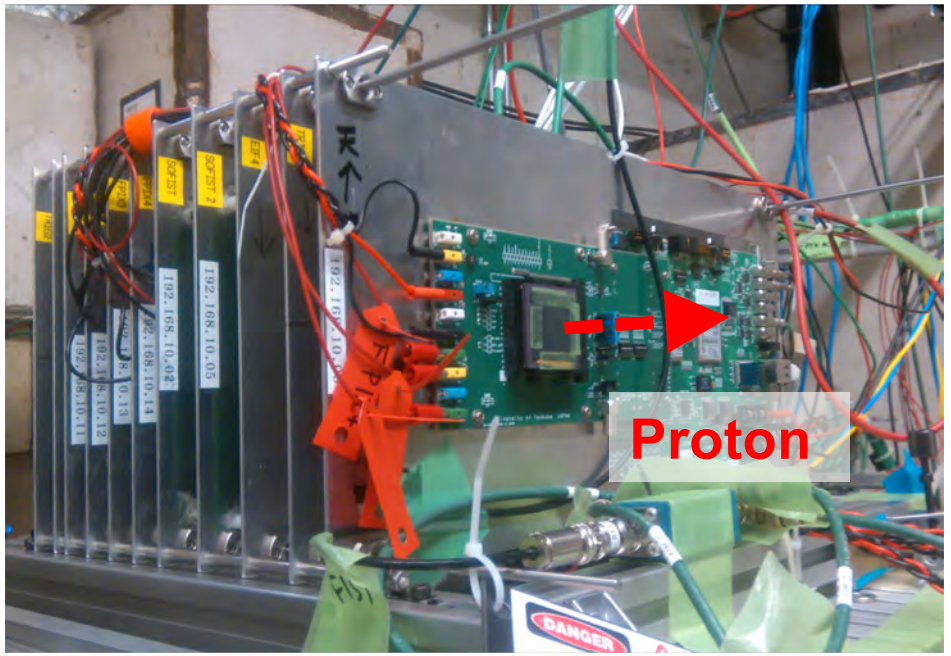
Dark Current

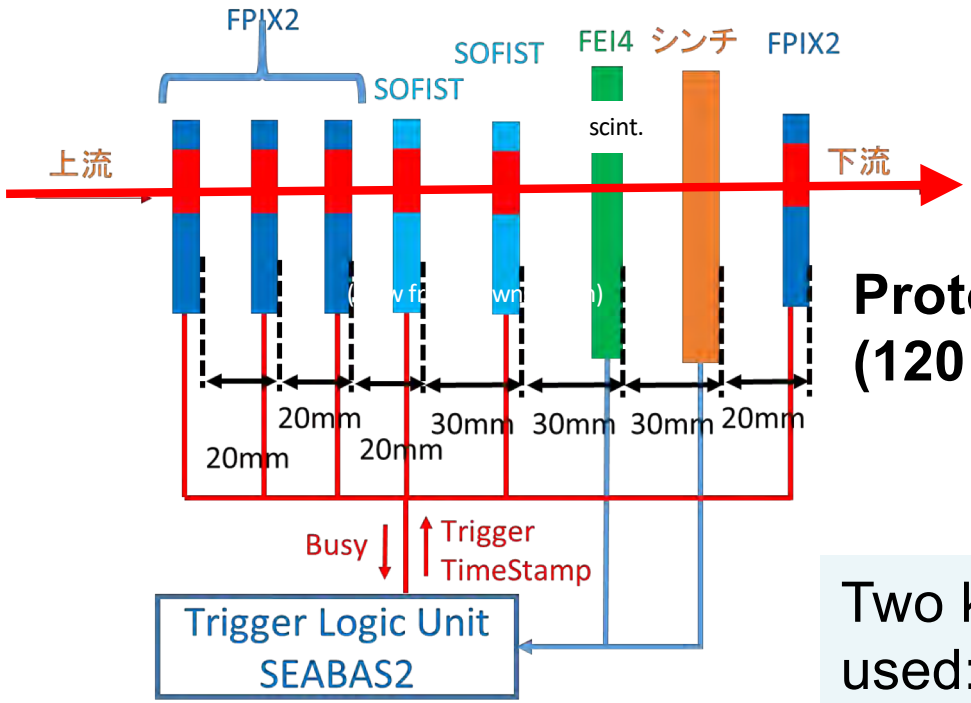


- Low Leak Current (57 pA/cm2 @-35˚C)
- Dark Current is reduced about 1.5 order of magnitude compared to standard SOI sensor.

III. R&D for ILC Vertex Detector & 3D Integration

Tracking Resolution: High-Energy Beam test @Fermi National Accelerator Lab.





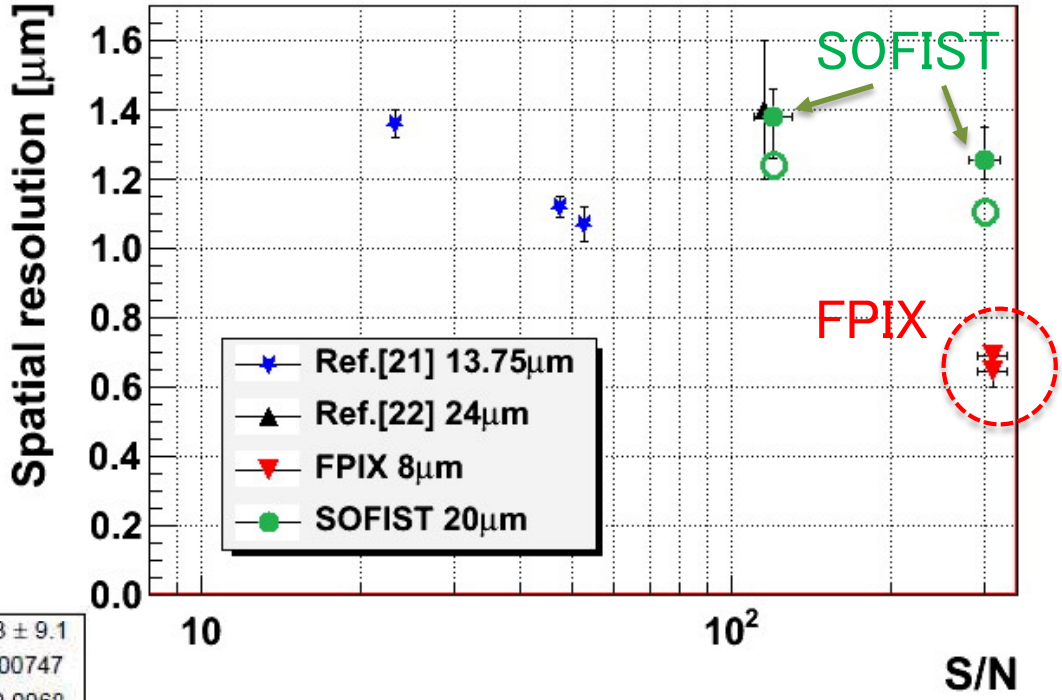
Proton Beam (120 GeV/c)

Two kinds of SOIPIX-DSOI detectors are used:

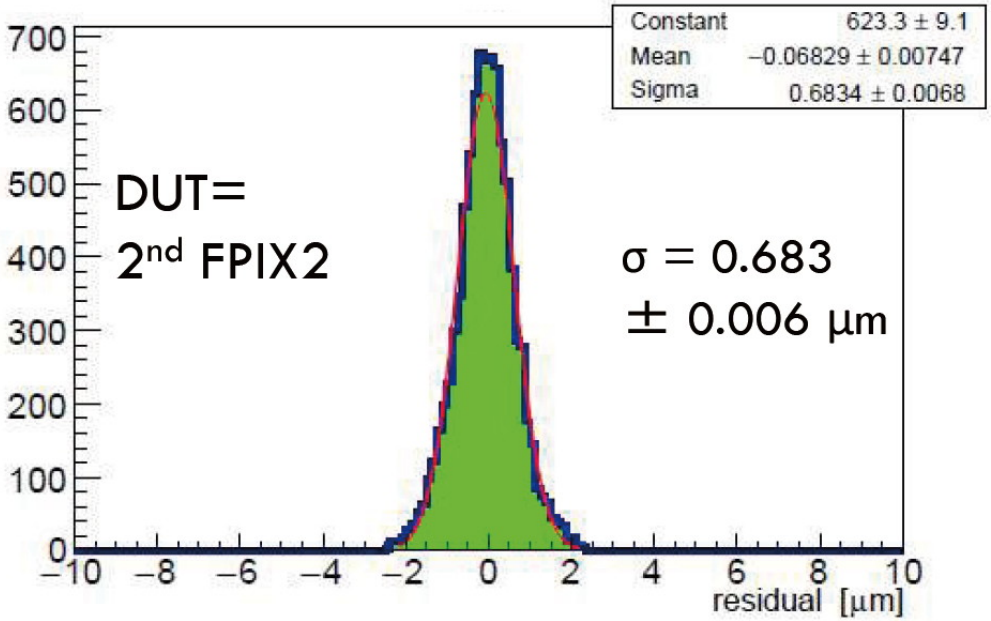
- **FPIX2** x 4: 8 μm square pixel detector
- **SOFIST**(v.1 & 2) x 2: 20 μm square pixel detector

Tracking Resolution

Less than 1 μm Position Resolution for high-energy charged particle is achieved first in the world !



FPIX2

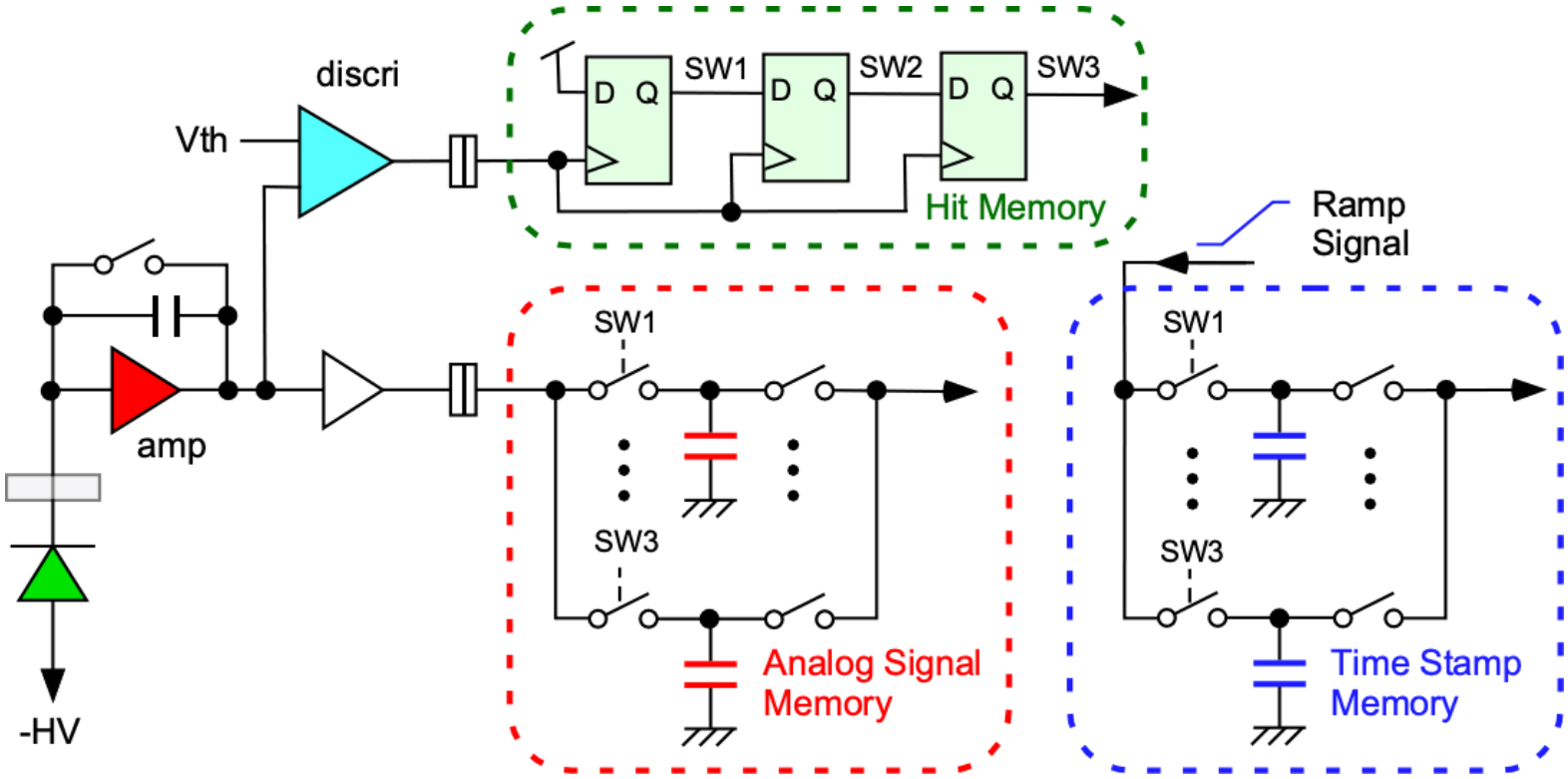


Detector	Pixel size	Resolution
ATLAS Pix	13.75 μm	1.1 μm
DEPFET	24 μm	1.4 μm
SOFIST	20 μm	**1.2 μm**
FPIX	8 μm	**0.65 μm**

(K. Hara et al., Development of Silicon-on-Insulator Pixel Detectors, Proceedings of Science, to be published)

ILC Vertex Detector R&D : SOFIST

(SOI sensor for Fine measurement of Space & Time)



- Gain: 32 mV/ke- (@Cf=5fF)
- Analog signal memories: 3 for signal or 3 for time
- Column-ADC: 8 bit
- Zero Suppression Logic

Position Resolution

SOFIST Ver. 1

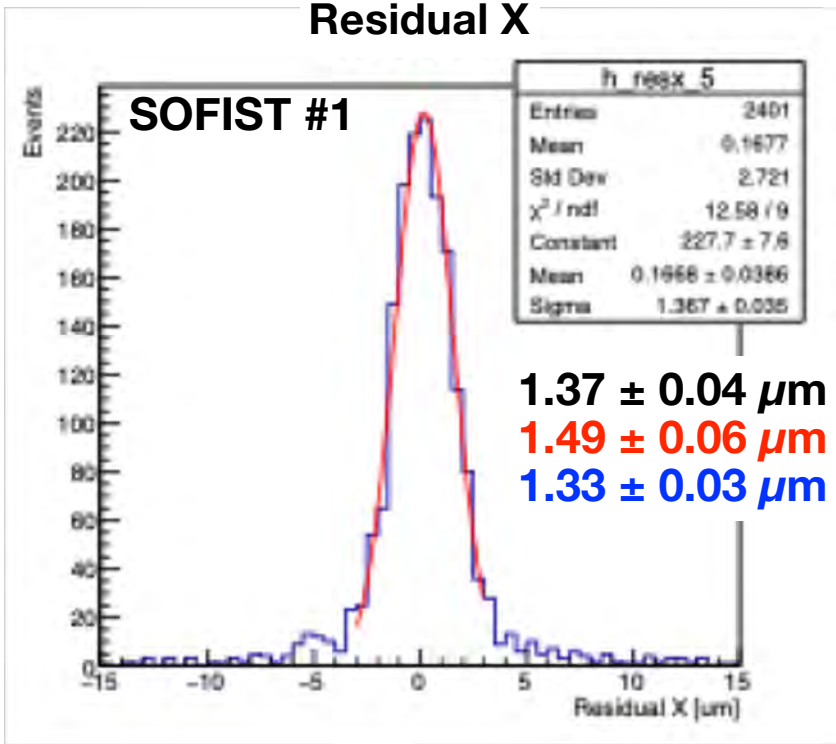
Readout and Sensor depletion layer

12-bit external ADC, 500 μm (Full depletion)

8-bit on-chip ADC, 500 μm (Full depletion)

12-bit external ADC, 200 μm (Partial depletion)

Residual X

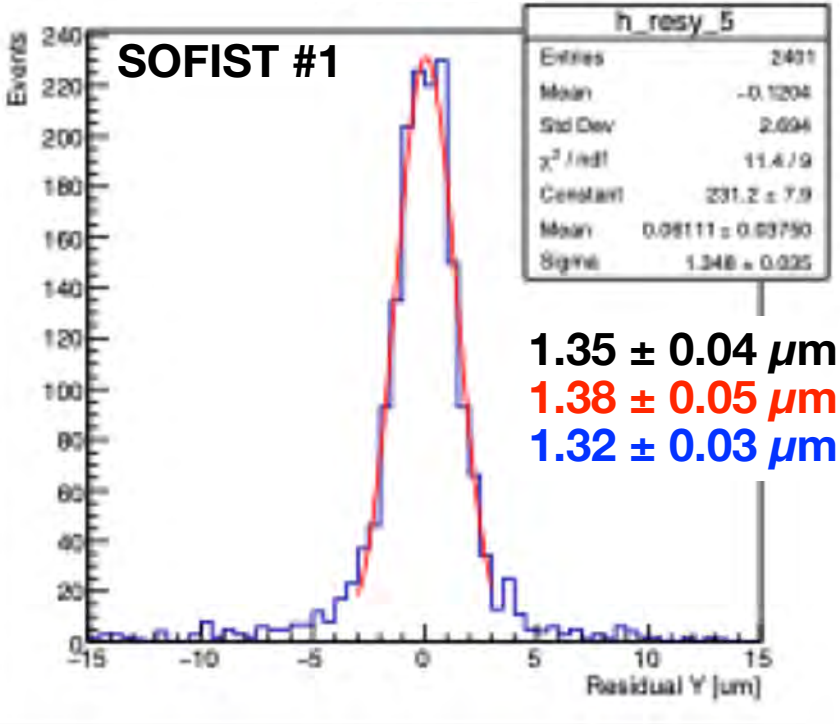


1.37 ± 0.04 μm

1.49 ± 0.06 μm

1.33 ± 0.03 μm

Residual Y



1.35 ± 0.04 μm

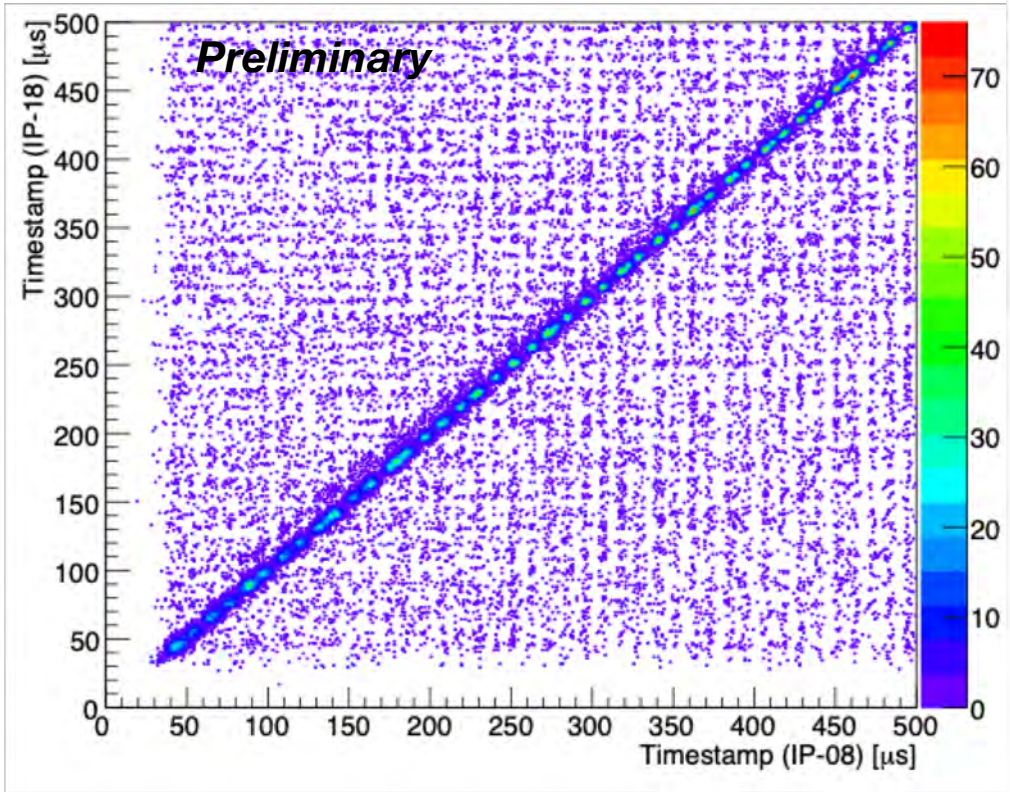
1.38 ± 0.05 μm

1.32 ± 0.03 μm

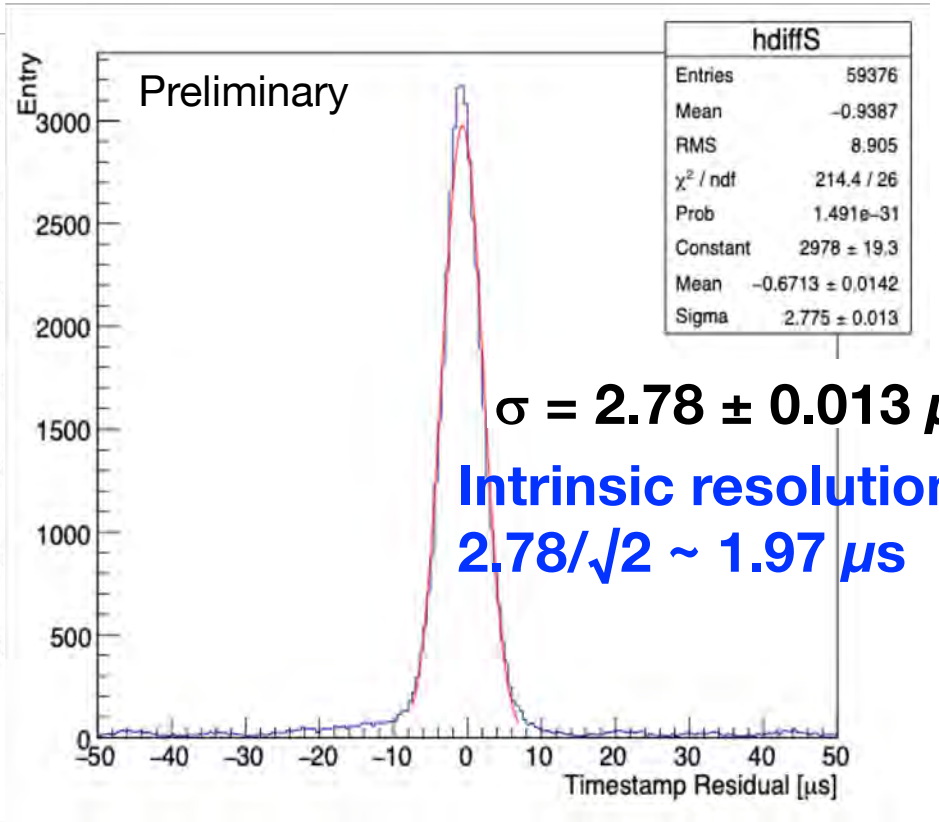
Time Resolution

SOFIST Ver.2

Timestamp correlation between SOFIST ver.2 #1 and #2



Timestamp residual between SOFIST ver.2 #1 and #2



σ = 2.78 ± 0.013 *μs*

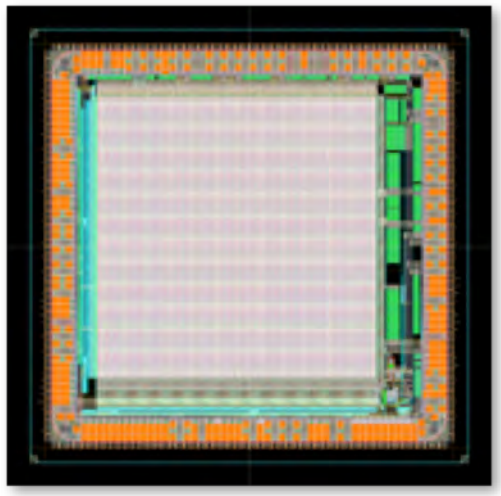
Intrinsic resolution: 2.78/√2 ~ 1.97 *μs*

Bench test resolution is about 1 μsec.

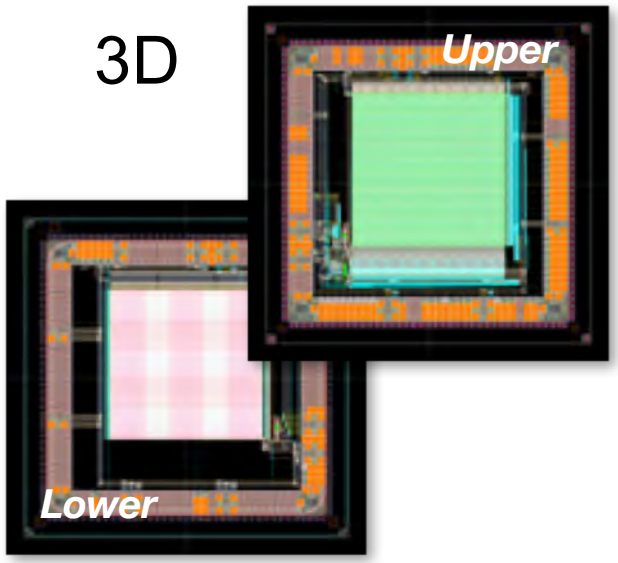
New SOFIST Chips (Ver. 3 & 4)

Designed at the same time. Same circuits.

2D



3D



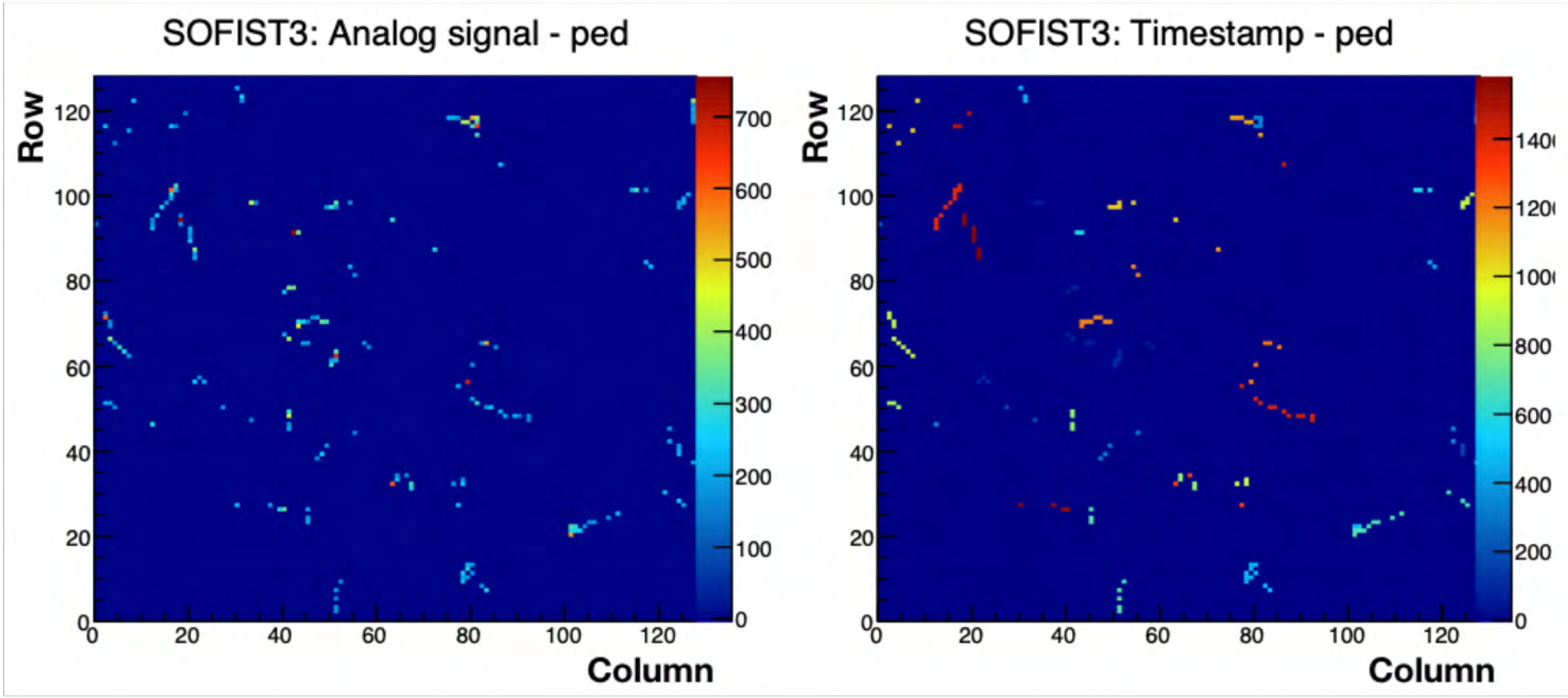
	Ver. 3 (2D)	Ver. 4 (3D)
Chip Size	6mm x 6mm	4.45mm x 4.45mm
Pixel Size	30μm x 30μm	20μm x 20μm
Pixel Array	128 x 128	104 x 104
Circuits	CSA + Comp.+ 3 Analog Mem + 3 Time Stamp Mem	
Wafer	FZ p-type (3~10 kΩ•cm) Double SOI	

Position and Time Measurement

SOFIST Ver. 3

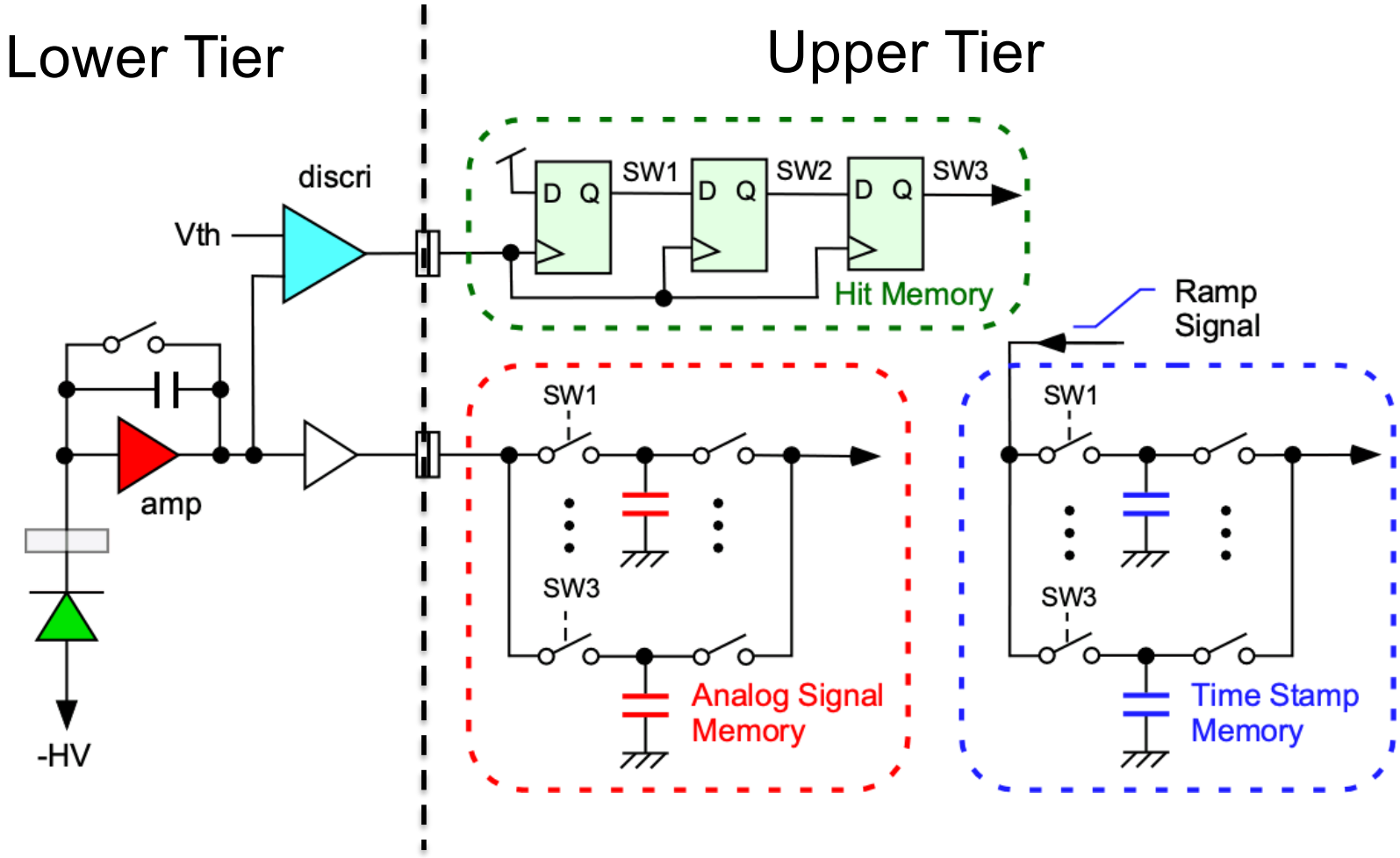
β –ray track from ^{90}Sr

Threshold: V_{th} = 950 mV, V_{RST} = 900 mV
HV = -100 V



Successfully measured Charge and Time simultaneously!

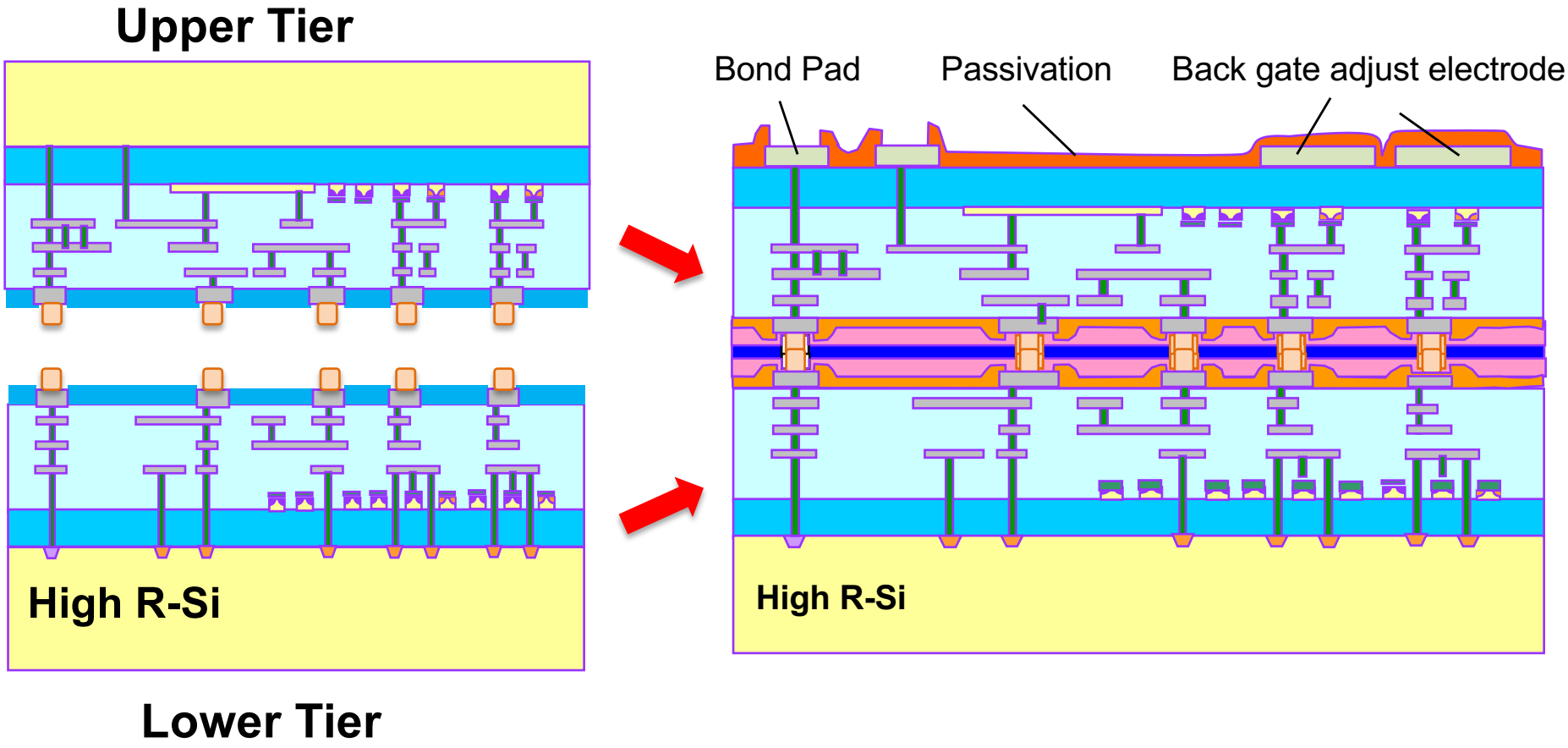
3D Vertical Integration (SOFIST Ver. 4)



3D Integration

SOFIST Ver. 4

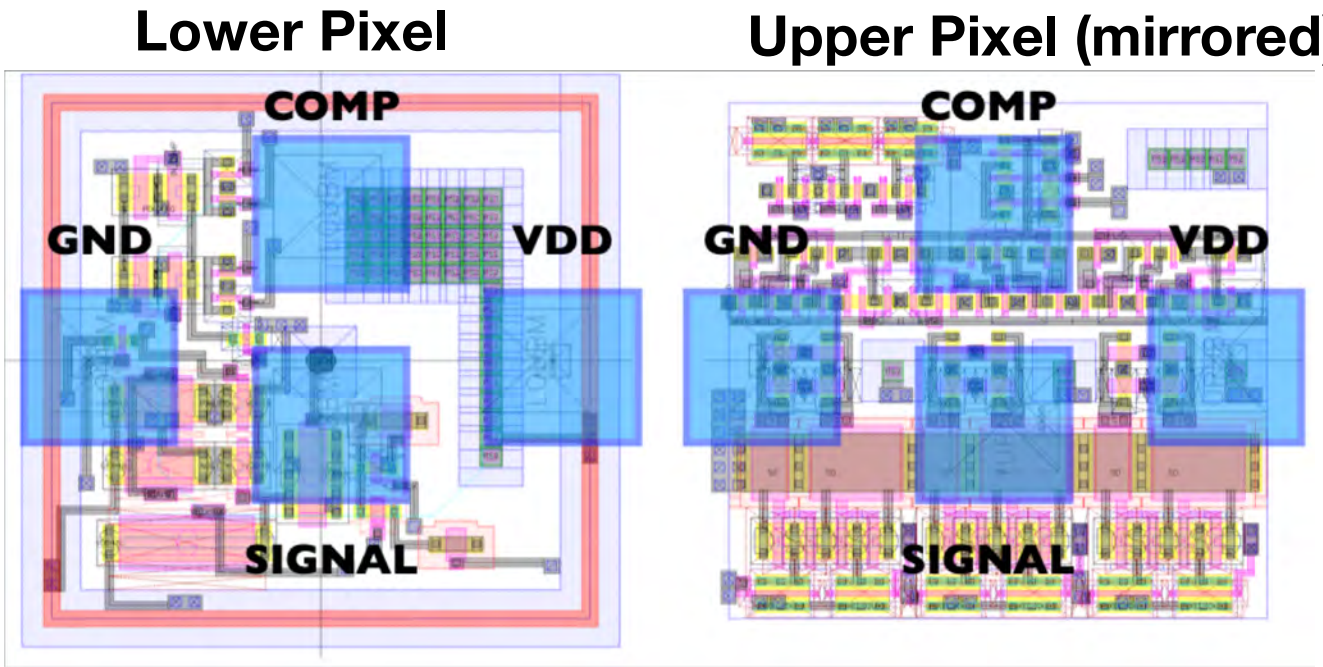
T-Micro



Upper and Lower Tier chips are produced in a same wafer and bonded chip to chip.

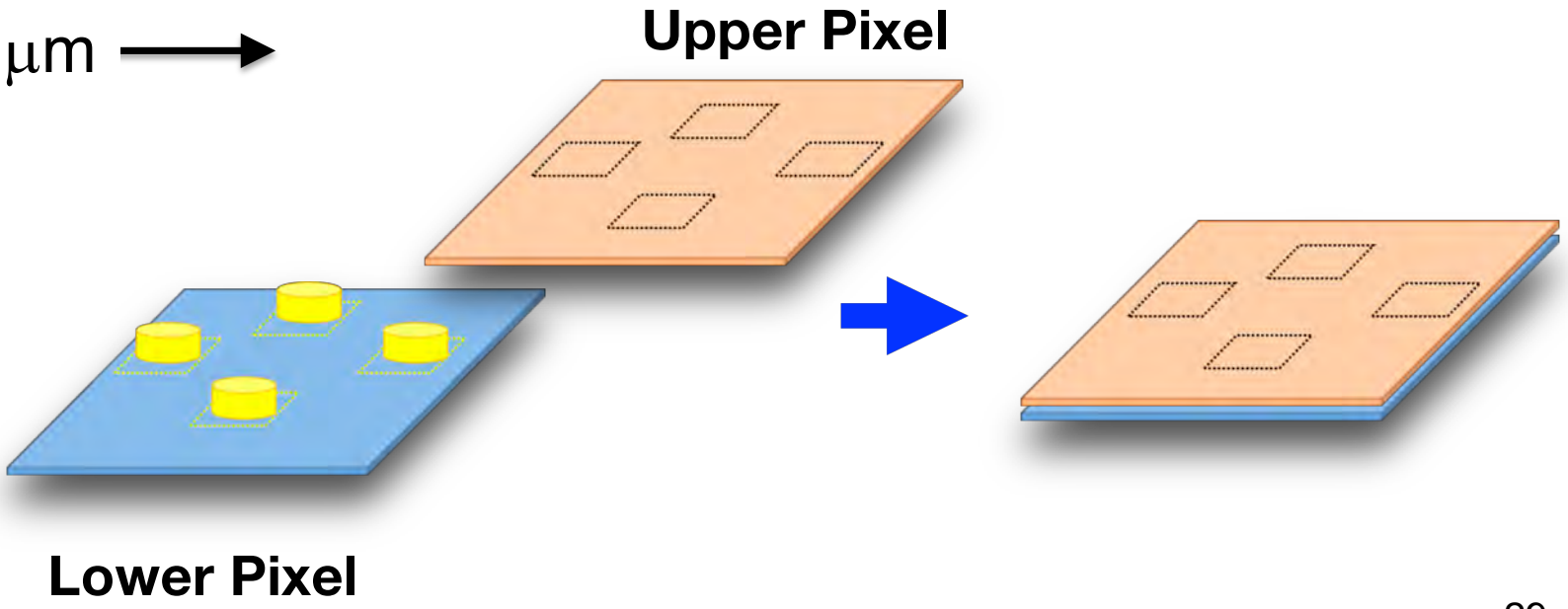
Pixel Layout

SOFIST Ver. 4

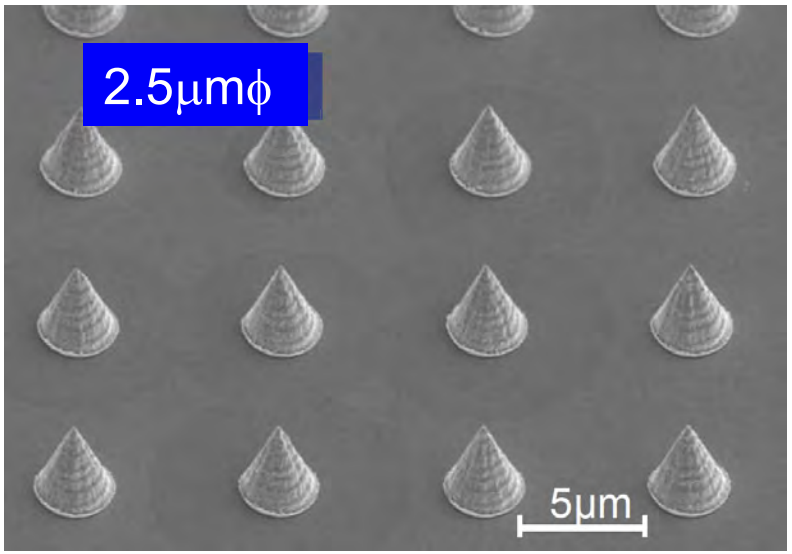


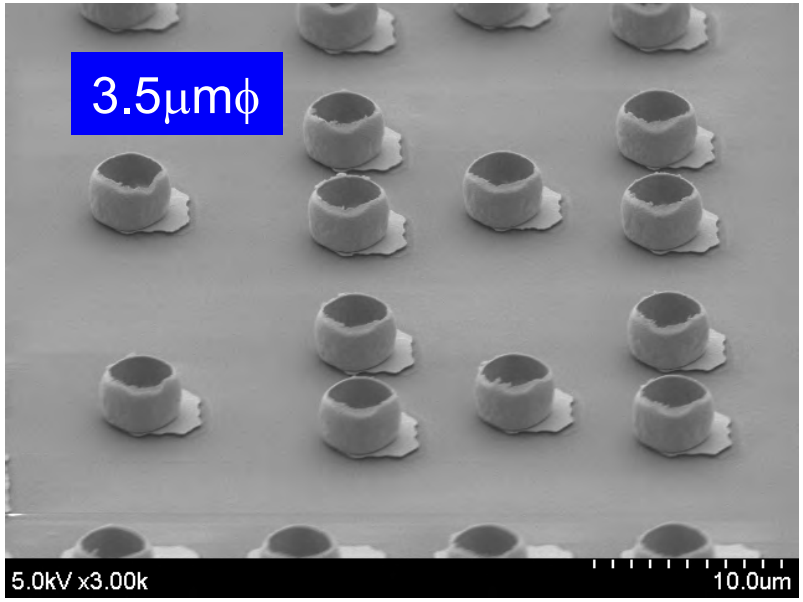
3 bumps per pixel

20 μm



Bump Shape

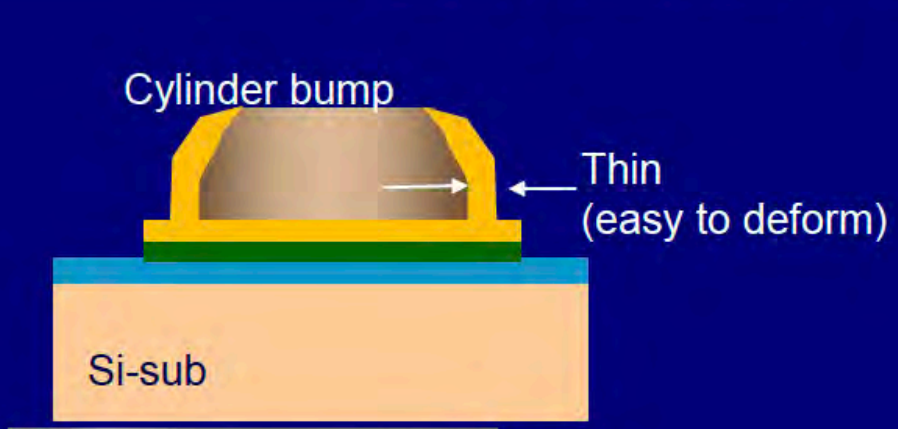


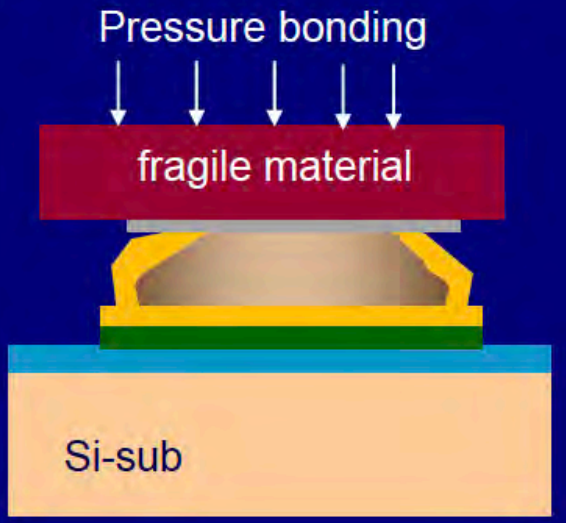


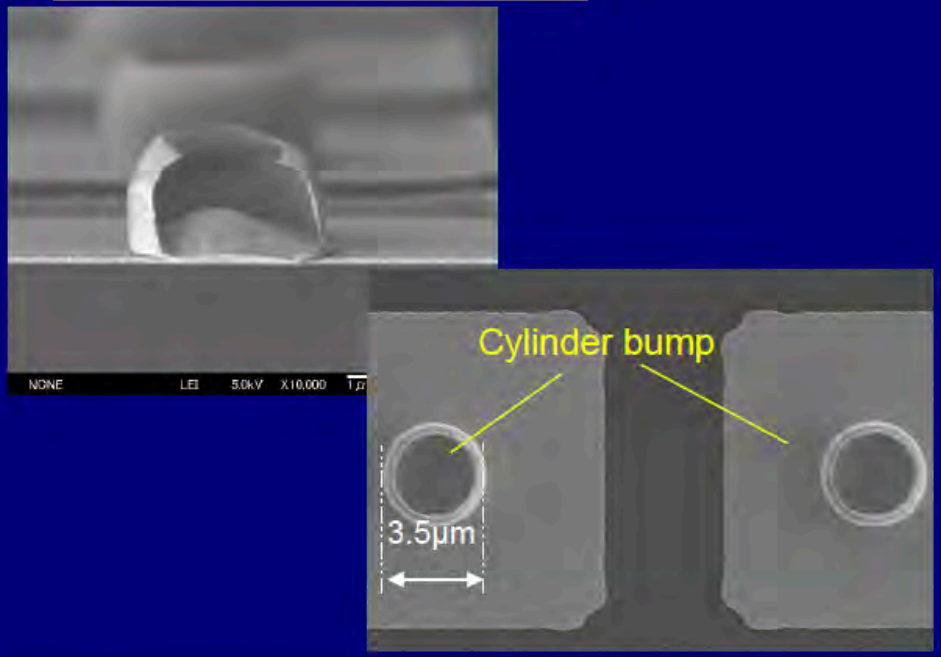
Shape	Cone	Cylinder
Min. Size/Pitch	2.5μmϕ / 5μmϕ	3.5μmϕ / 7μmϕ
Bump Resistance	~0.3 Ω/bump	~0.3 Ω/bump
Yield	Good	Very Good
Reliability	Good	Very Good
Gap	1.5 ± 0.2 μm	1.0 ± 0.2 μm
Processing Time	Very Long	Short

T-Micro

Bump bonding with cylinder Au bumps





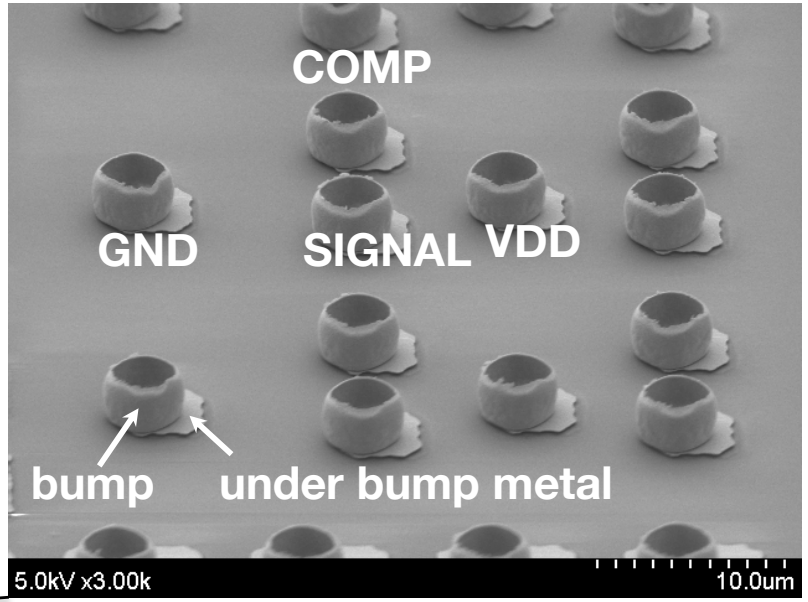


SEM cross section

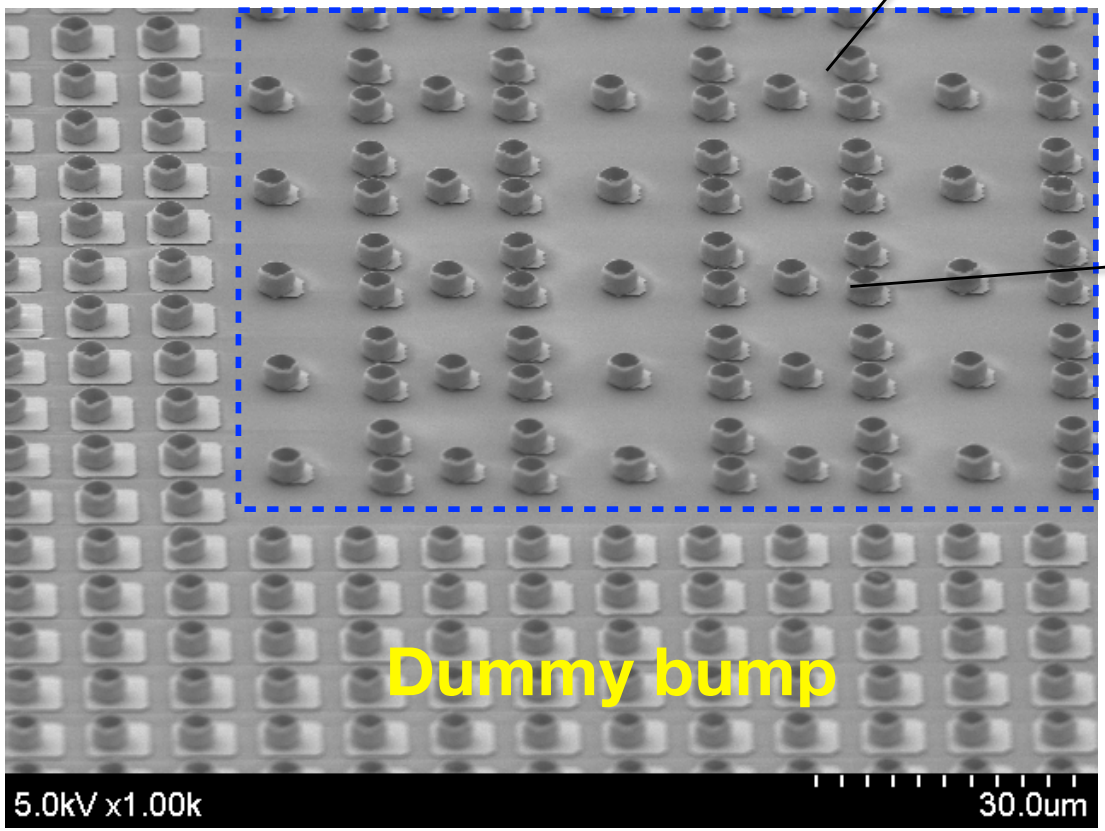
SOFIST Bump

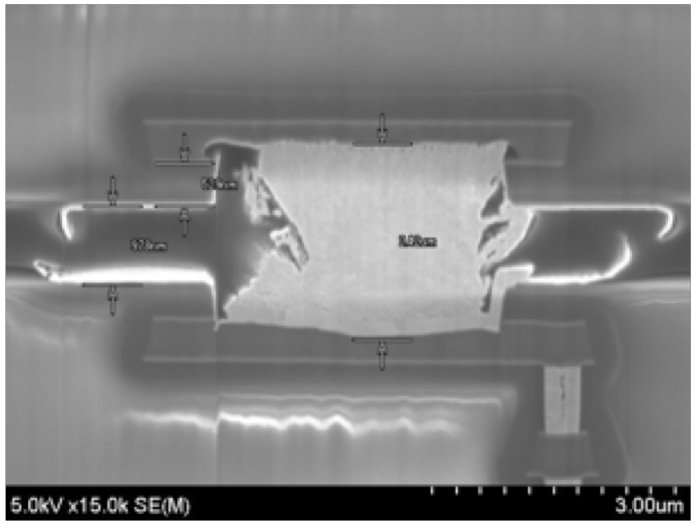
Cylinder bumps are successfully fabricated

Pixel



Pixel array





3D SOFIST will be tested soon.

IV. Summary

- SOI pixel technology has been developed for fine-resolution vertex detectors. In addition, it is widely used in many X-ray experiments.
- Back-gate, sensor-circuit coupling, and radiation hardness issues are solved by introducing Buried well, Double SOI, and PDD technique.
- SOFIST detector is under development for the ILC experiments. It almost fulfills position and timing resolution required in the ILC.
- We are also developing 3D vertical integration technology by using cylinder bump for small size high functionality pixel.

Thank You!