Some considerations on the CMOS sensors for CEPC MOST-2

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CEPC-MOST 2 Mini-workshop

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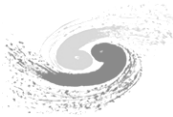
Outline



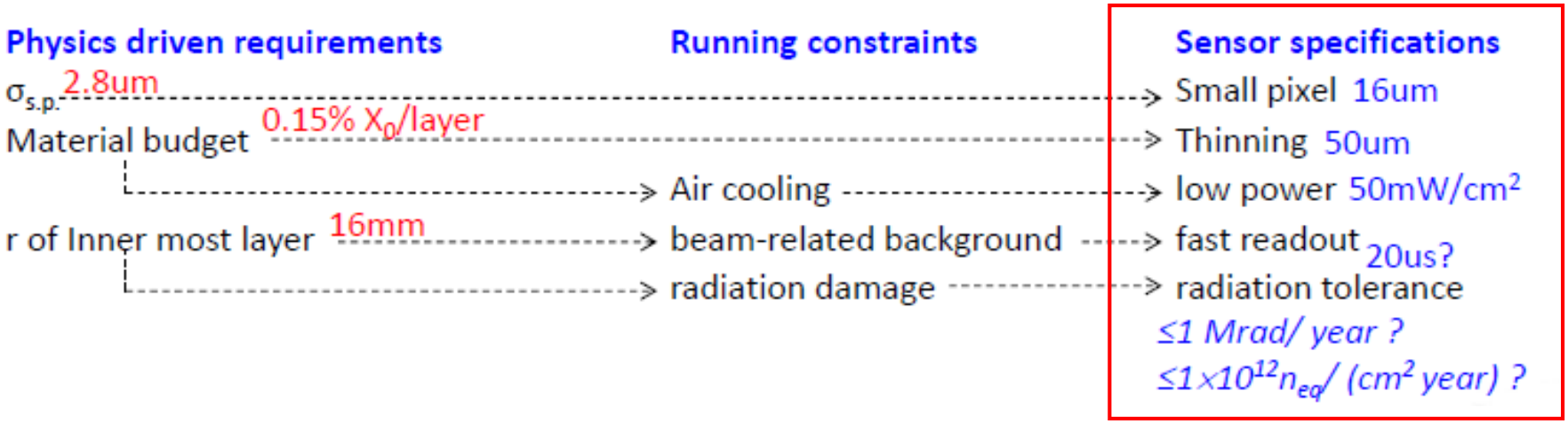
- **General requirement**
  - **Specifications**
  - **Chip architecture**
- **Overall plan of the chip design**
- **Open questions and discussion**

First questions on motivations

- **What are we going to do?**
  - **To design a chip with full functionality, and to build a prototype ladder with several layers mounted**
  - **Very limited time**
    - **5 years in total, 3.5 years for the chip final design**
  - **Therefore:**
    - **It is very unlikely that we have parallel designs (not like MOST-1)**
      - **Have to be very focused on a unique chip design**
      - **Chip design tasks might be divided into blocks**
    - **The requirement, spec., interface of the chip have to be determined asap**
      - **Real design can be initiated asap to earn time**

General requirement- from CEPC MOST 1

- To achieve S.P. resolution
  - Digital pixel ~ 16um
  - Analog pixel ~ 20um (power pulsing mode in ILC)
- To lower the material budget
  - Sensor thickness ~ 50um
  - Heat load < 50 mW/cm^2 constrained by air cooling
- To tackle beam-related background
  - 20us/frame?
  - 300krad/year & 3×10^{12}neq/ (cm^2·year)?



from Lu Y.P.

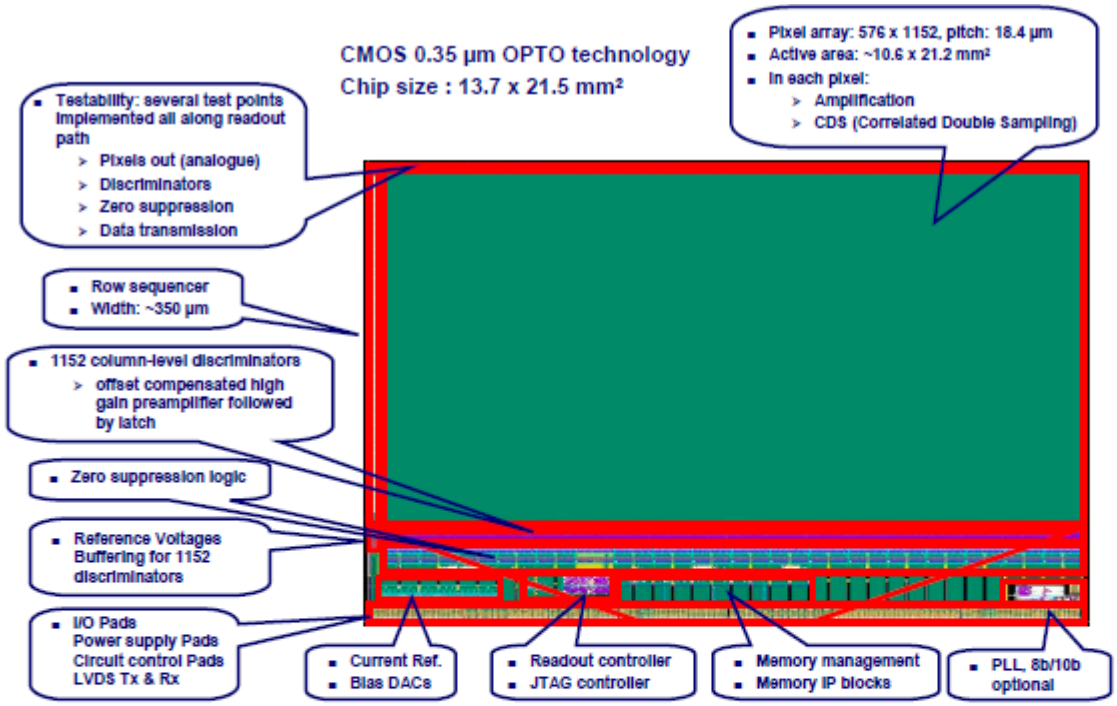
Status of CEPC MOST-1

- **Initial sensor R&D targeting on**
  - **Pixel pitch ~16 μm**
  - **Power consumption <100 mW/cm^2**
  - **Integration time 10-100 μs**
- **CPS design**
  - **More focused, with major man power**
  - **All designs on Tower Jazz 0.18μm CIS process**
    - **sharing tapeout with CERN and IPHC**
  - **two versions of tapeouts**
    - **1st ver.: only pixel sensors, analog readout**
    - **2nd ver.: in-pixel digitization, parallel design on readout scheme**
      - **rolling shutter readout (IHEP) 22μm×22μm/ async. readout (CCNU) 25μm×25μm**
      - **Chip periphery: voltage DACs, readout logic, analog chain**
- **SOI design**
  - **Develop in-pixel circuit for minimum layout area**
  - **SOI-collaboration between IHEP & KEK**
  - **Two ver. of tapeouts: 16μm×16μm in-pixel discrimination**

Experiences and comments from CEPC MOST-1

- **Pixel size**
  - **Aiming for 16μm×16μm, however very challenging in the current process (not even reported worldwide)**
    - **Achieved in the SOI efforts, but very little room left for any more func.**
- **Readout time**
  - **Aiming for a fast readout < 10us, final goal 1us?**
  - **Also very challenging under the power consumption constraints**
- **Power: aiming for 50mW/cm2 as the final goal**
  - **Less periphery block integrated (some are hot elements: LDO/ Interface)**
  - **A brief evaluation: not achieved so far**
- **Wafer thining**
  - **Not possible so far (MPW and sharing tapeout)**
- **Simulation consistency**
  - **Still needs careful test to prove**
- **Comments and questions**
  - **To meet the final goal for CEPC is really challenging**
  - **No prior success of the similar chips worldwide**
    - **most of them are done by more experienced engineers than us**
  - **Should we really be so aggressive on specs? Or maybe we should be conservative because we need to build a real ladder in very limited time**

MIMOSA-26 chip architecture

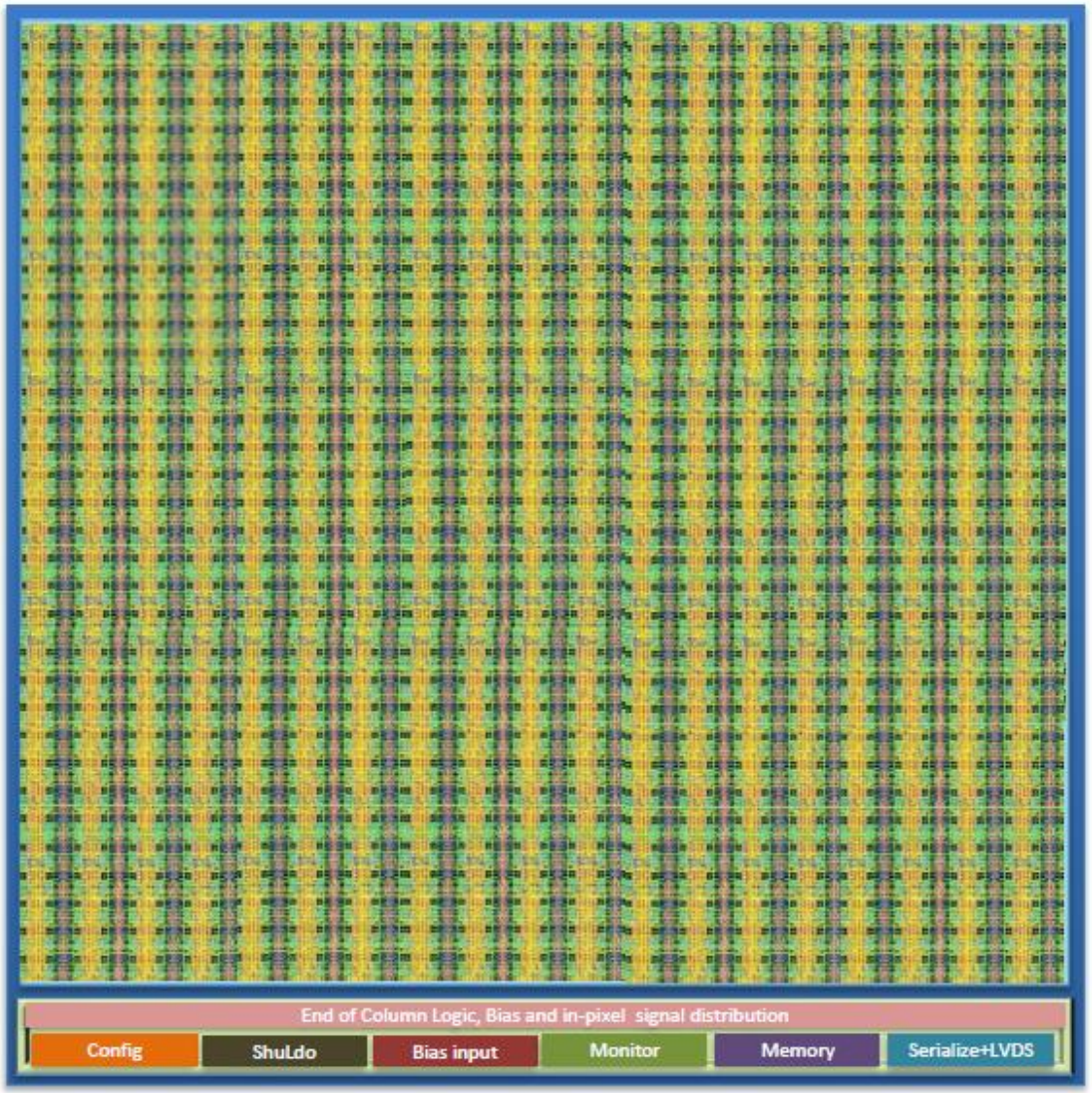


Main characteristics of MIMOSA26 sensor equipping EUDET BT:

- Column // architecture with in-pixel Amp & CDS and end-of-col. discrimination, followed by Ø
- Active area: 21.2×10.6 mm² ,1152 x 576 pixels, pitch: 18.4 µm ➔ $\sigma_{sp.}$ <~ 4 µm
- Read out time <~ 100 µs (10^4 frames/s) ➔ suited to >10^6 particles/cm²/s
- Yield ~90% (75% fully functional sensors thinned to 120 µm + 15% (showing one bad row or column)
- Thinning yield to 50 µm ~90%

[1] Hu-Guo C. ULTIMATE: a High Resolution CMOS Pixel Sensor for the STAR Vertex Detector Upgrade, TWEPP-2010

ATLAS CMOS-1 Sensor Overview



Active Matrix

- Active area 19.2 x 20 mm^2
- Each pixel contains CSA + discriminator + buffer
- Readout in double column structure either synchronously or asynchronously

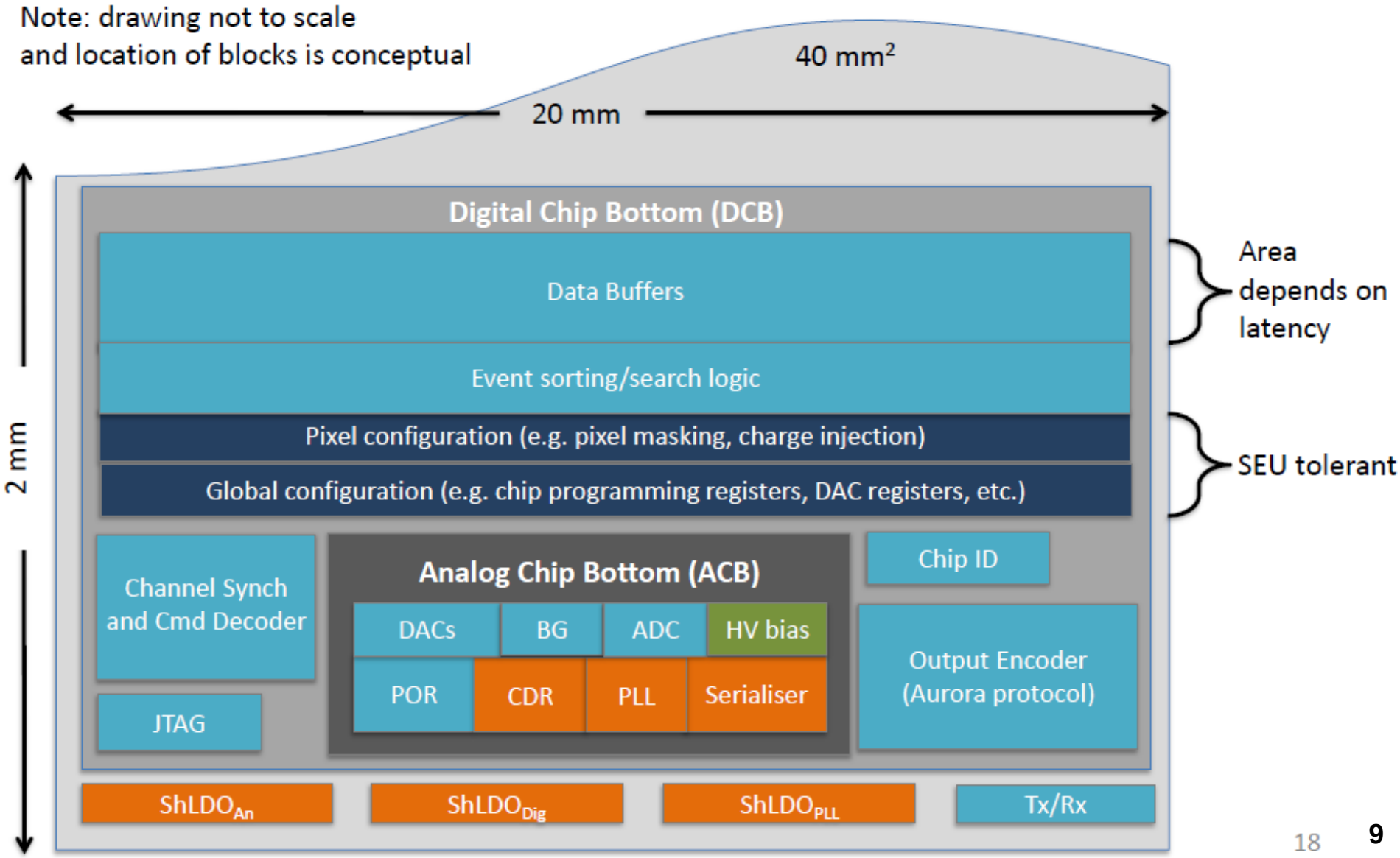
Periphery

- End of Column Logic
- Common blocks to interface to ITk

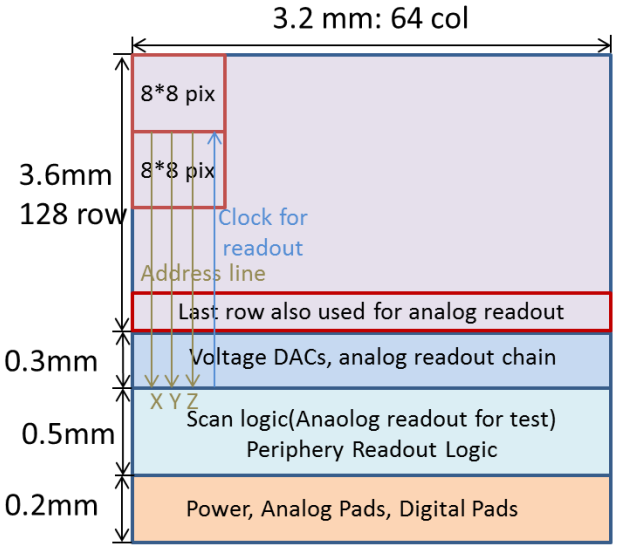
ATLAS CMOS-1 from H. Pernegger, ATLAS ITk week June 2017

From Walter Snoeys

Common Periphery Block Diagram (based heavily on RD53A)



Chip overall architecture – CEPC MOST-1



CEPC CPS v2

- Compared with the exist chips, it seems that we have almost full func. in pixels
- Current chip only integrates basic periphery blocks and basic logics
- Q: do we need more complex readout logic
  - Depends on event rate, occupancy, and bunch crossing structure
  - If high, we probably need on chip RAM and some level of trigger
- Q: do we need other commonly used blocks: LDO, PLL
  - Very likely
  - Otherwise system design less compact: on-board components
    - Material budget issues
  - On-board component tends to be less rad-hard than on-chip rad-hard design

Consideration of the CEPC MOST-2 sensor

- **A chip aiming for prototype + full funcs. + time is short !**
- **1st: Specs. need to be fixed**
  - **Better do not be too optimistic**
- **Borrow the experience and designs from MOST-1**
  - **Especially the pixel design**
  - **But it better that the pixel size be further shrinked**
- **Should we try other processes?**
  - **TJ 0.18μm:**
    - **existed experience, but pixel size limits already reached**
    - **Has to coordinate the tapeout schedule with collaborators– not good for a time limit project**
  - **XX 0.15μm or even less?**
    - **Might gain benefit to shrink the pixel size**
  - **Can we try to establish dedicated collaboration with foundries?**
    - **May get dedicated process that is optimized for CPS (even rad-hard?)**
    - **Possible to know more "secret" of the process– esp. important for sensor design**
    - **Might have free offers of tapeout**
  - **Q: do we know any proof of the rad-hardness of a new process?**
    - **When design initiates, it is very unlikely to change the process**

Consideration of the CEPC MOST-2 sensor

- **Pixel chip=pixel array(√？) + periphery**
- **Carefully think about the overall chip functionality, especially the consideration for a real prototype**
- **How the chip works?**
  - **How the pixel level data are processed?**
    - **Zero-suppression? On-chip FIFO?**
    - **Not clear, need to be decided**
  - **How the chip is readout?**
    - **A BESIII-ladder like readout?**
      - **Signals of multiple chips all routed on PCB to the edge**
      - **Quite a experience learned from BESIII**
    - **Daisy-chain readout?**
      - **Based on high speed serial link; less reliable**
    - **Or even design a dedicated "Module Controller Chip (MCC)" like ATLAS?**
      - **My comments: less likely due to the limited time**
    - **My comments: a BESIII-like readout may still be the most possible solution**

Consideration of the CEPC MOST-2 sensor

- **How we divide the design tasks among collaborators?**
  - **We will design a real prototype in very limited time, so better deliver the tasks to the collaborators with experiences on that part**
    - **Less R&D, more engineering**
  - **Chip overall design and simulation**
  - **Pixel array – better based on MOST-1**
    - **Sensor re-simulation**
    - **Pixel optimization**
    - **Column readout**
  - **Periphery Digital Pre-processing– new but somewhat independent**
    - **Functionality TBD**
  - **Common blocks in periphery – rad-hard!**
    - **Pixel array configuration (√)**
    - **PLL (existed experience)**
    - **LDO (???any report in Chinese HEP society?)**
    - **Bandgap+Bias DAC (√)**
    - **Serializer + Tx/Rx （√）**
    - **Other common blocks: JTAG, decoder**

General schedule of the chip development

- **Scheduled in 3.5y till final tapeout My worries:**
  - **2~3 MPW tapeouts, 1~2 full mask tapeout expected**

- **-0.5~0y**
  - **Can we decide the process?**
- **0~0.5y**
  - **Specifications determined**
    - **Pixel size, readout speed, power**
  - **Key interface of the chip decided**
    - **Sync or async readout, HV, Tx/Rx to PCB…**
  - **Design tasks devided and delivered**
- **0.5~1.3y: 1st MPW tapeout**
  - **Full func. digital pixel in medium pixel array**
  - **Basic periphery blocks integrated**
  - **New blocks tapeout and evacuated separately**
- **1.3~1.9y: 2nd MPW tapeout**
  - **Test of the 1st chip (3month)**
  - **Full funcationalily chip in medium pixel array**
- **1.9~2.5y:**
  - **Test of the 2nd chip (2month)**
  - **Modified 3rd MPW or 1st full mask**
- **2.5~3.1y:**
  - **Test of chip (3m for MPW/6m for full mask)**
  - **DAQ debug and ladder debug**
- **3.1~3.5y:**
  - **Final tapeout**

Related issues

- **My worries:**
  - **We really need more system level electronic designers**
    - **No man power for the chip test (from the name list)**
      - **The test setup has to be designed before hand and ready in time**
      - **Heavy job in chip test**
    - **Not easy from chip to DAQ, also need experiences on mechanical design**
  - **Time is really short, both for chip design and ladder design**
    - **Parallel tasks in the project schedule is great, but might be to optimistic: ladder design usually waits for the final chip**
    - **Also very challenging for the chip handling when thinned to 50μm**
- **Very limited considerations were proposed**
  - **Let's discuss**