Status of CMOS pixel sensor design for CEPC vertex detector R&D

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On behalf of the CEPC VTX study group

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MOST silicon project, IHEP

CMOS pixel sensor R&D activities

Initial sensor R&D targeting on

- Spatial resolution 10 μm
- Power consumption <150 mW/cm^2
- Integration time 100 μs

IHEP project

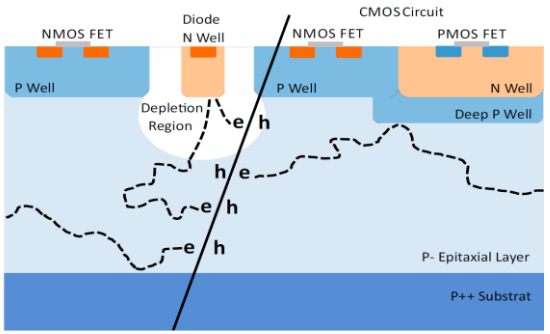
Medium-term goals

- Spatial resolution 3-5 μm
- Power consumption <100 mW/cm^2
- Integration time 100 μs

MOST1 project

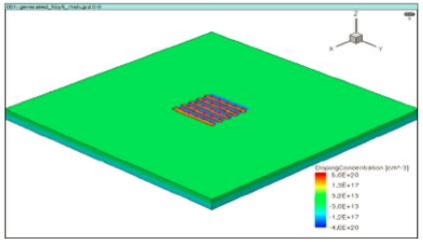
Selected TowerJazz 0.18 μm CIS process for R&D, featuring:

- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area
- Feature size of 0.18 μm and 6 metal layers: good for high-density and low power
- Thick (18–40 μm) and high resistivity (≥1 kΩ•cm) epitaxial layer: larger depletion
- Thin gate oxide (< 4 nm): robust to total ionizing dose

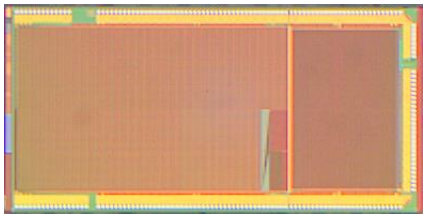


CMOS pixel sensor R&D activities

- **Sensor design & TCAD simulation**
  - Different sensor diode geometries, epitaxial-layer properties and radiation damage



- **First submission in Nov. 2015**
  - Exploratory prototype, analog pixel, rolling shutter readout mode
  - Sensor optimization and radiation tolerance study
  - Sensing diode AC-coupled to increase biased voltage



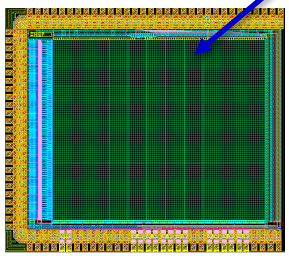
- **Second submission in May 2017**
  - Tow prototypes with digital pixels (in-pixel discriminator)
  - Tow different readout schemes: rolling shutter & asynchronous

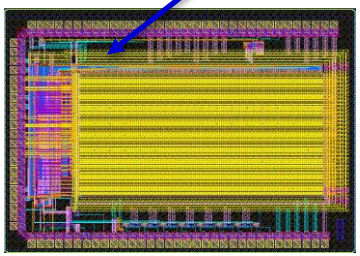
Design goals

Spatial resolution ~5 μm

Integration time < 10 μs

Power consumption < 80 mW/cm^2

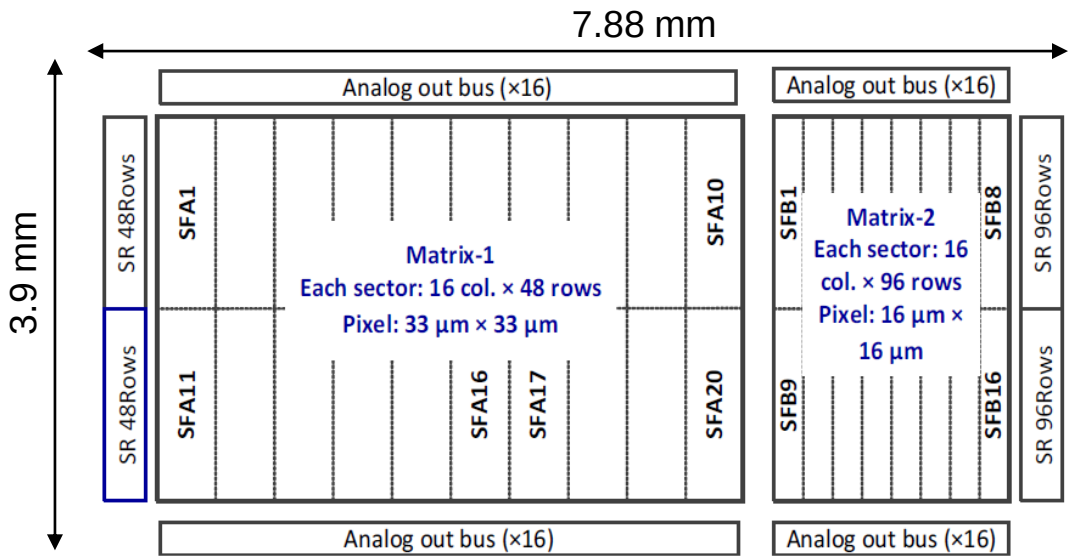




chip returned from the foundry

1st CPS prototype design

- **Goals：sensing optimization and in-pixel pre-amplifier study**
- **Floorplan overview**
  - Two independent matrices: Matrix-1 with 33 × 33 μm^2 pixels (except one sector SFA20 with 16×16 μm^2 pixels), Matrix-2 with 16×16 μm^2 pixels.
  - Matrix-1 includes 3 sectors with in-pixel pre-amplifier
  - SFA20 in Matrix-1 contains pixel with AC-coupled pixels



- TowerJazz 0.18 μm CIS process November 2015 submission
- Chip received in 2016 June, test in progress

2nd Submission: rolling-shutter mode prototype

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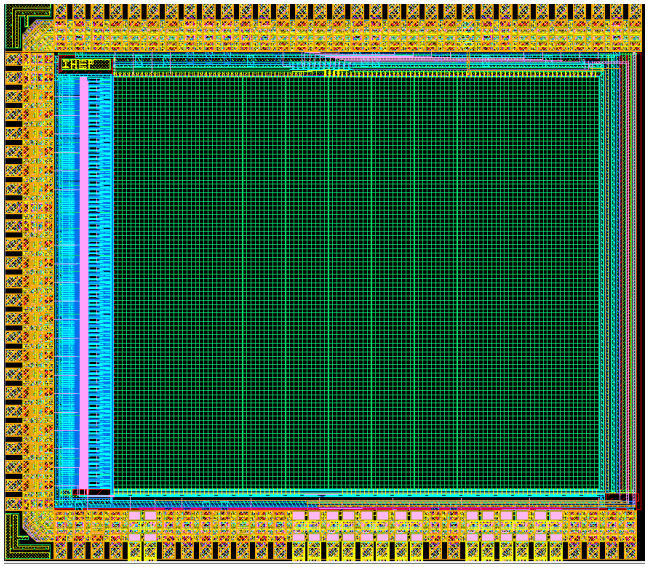
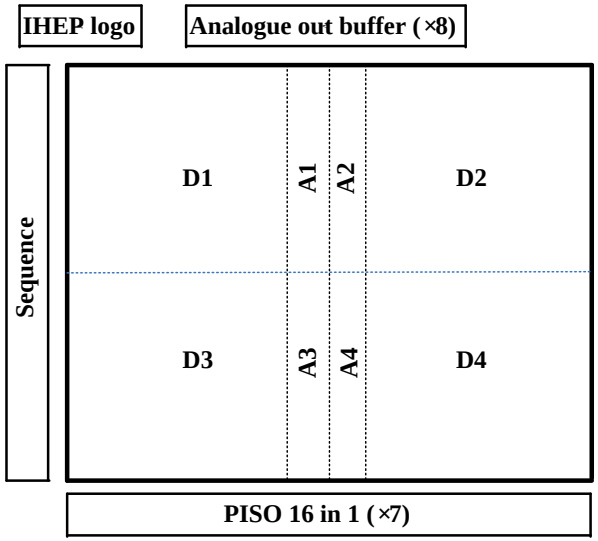




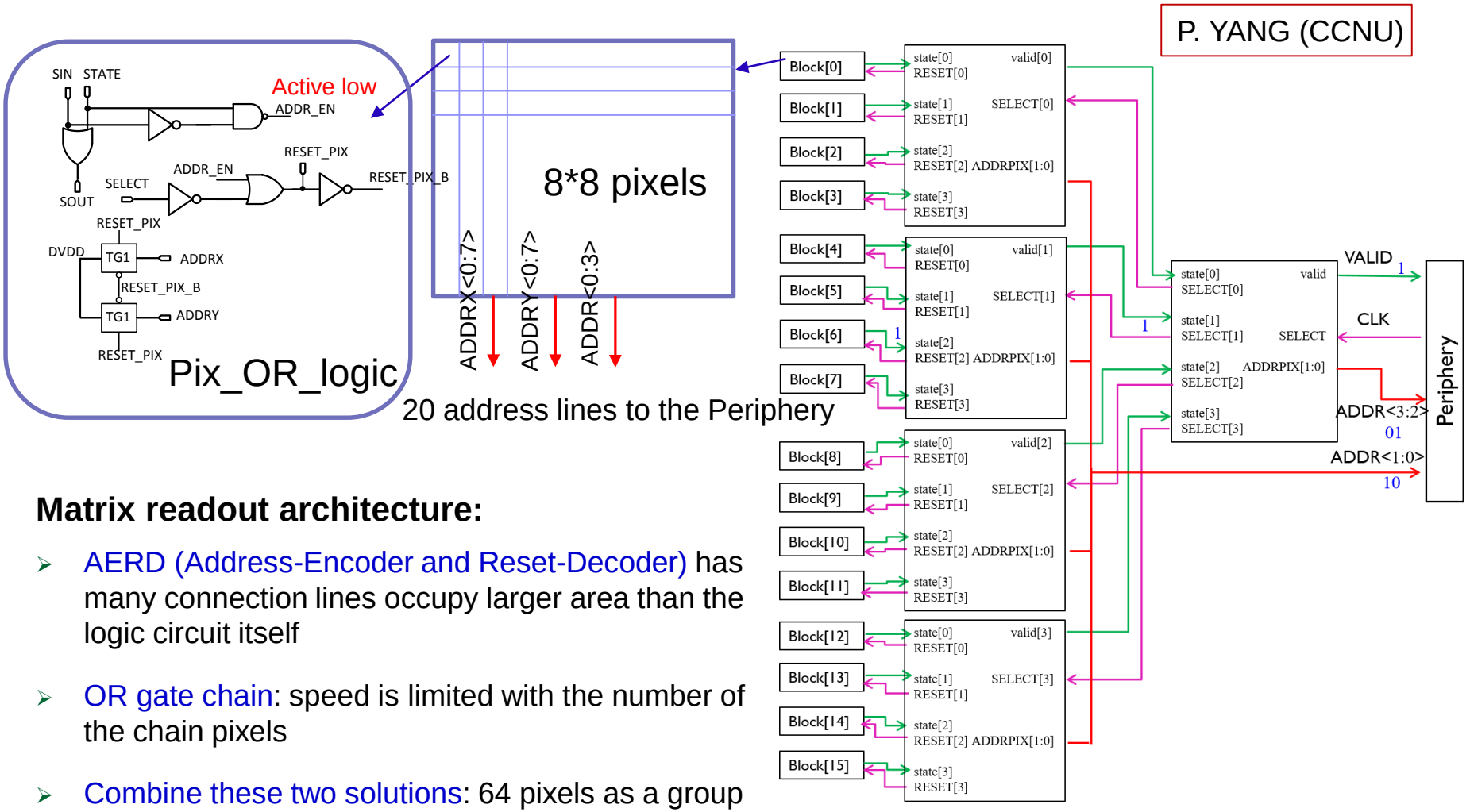
Two different pixel versions:

- Pixel size: 22 μm × 22 μm
  → 65% of ASTRAL chip (IPHC)
- Same amount of transistors;
- Offset cancellation technique;
- Version 2 has higher signal gain, but suffers "more" from "Latch" input voltage distortion.

Chip features:

- 3 × 3.3 mm^2
- 96 × 112 pixels with 8 sub-matrix
- Processing speed: 11.2 μs/frame with 100 ns/row
- Output data speed: 160 MHz
- Power: 3.7 μA/pixel (14.4 mW/cm^2 @pixel matrix)

2nd Submission: asynchronous mode prototype



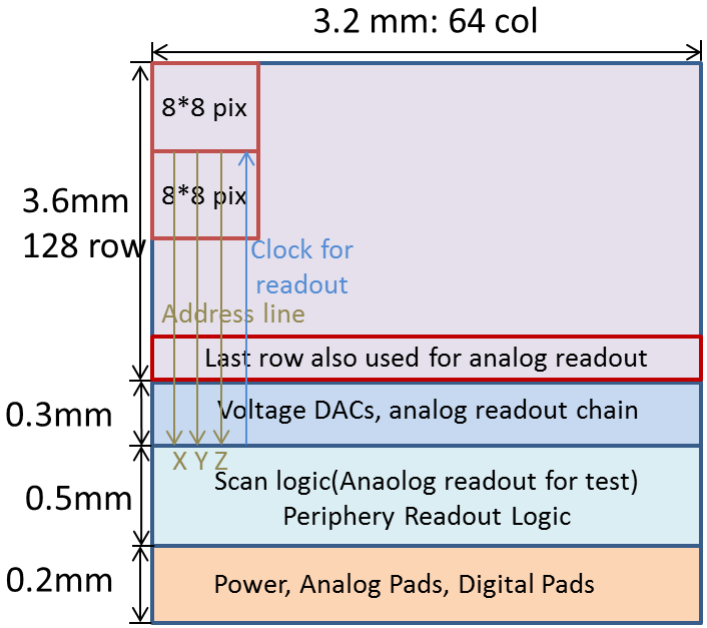
Matrix readout architecture:

- AERD (Address-Encoder and Reset-Decoder) has many connection lines occupy larger area than the logic circuit itself
- OR gate chain: speed is limited with the number of the chain pixels
- Combine these two solutions: 64 pixels as a group using OR gate chain, groups using AERD structure to readout

2nd Submission: Asynchronous mode prototype

Y. ZHANG (IHEP) & P. YANG et al. (CCNU)

- **front-end I:** same structure as ALPIDE chip
  - ENC: 8 e^-
  - Power cons.: 61 nA/pixel
  - Threshold: 140 e^-
  - Peaking time < 1 us
  - Pulse duration < 3 μs
- **front-end II:** CSA based circuit
  - ENC: 24 e^-
  - Power cons.: 50 nW/pixel
  - Threshold: 170 e-
  - Peaking time < 500 ns @ Qin < 1.5 ke^-
  - Pulse duration < 9.4 μs @ Qin < 1.5 ke^-



- 3.2 × 3.7 mm^2
- 128 × 64 pixels, pitch 25 μm
- Integration time: < 5 μs/10 μs
- Power consumption: < 80 mW/cm^2
- Chip periphery
  - Band gap
  - Voltage DAC
  - Current DAC
  - Matrix configuration
  - LVDS
  - Custom designed PADs

Summary

- **The first prototype test on-going, test system being finalized**

- **2nd CPS submission made in May 2017, focus on highly compact digital pixels and fast readout development**
  - 3 versions of highly compact digital pixels designed
  - 2 different readout architectures (rolling shutter & asynchronous) implemented
  - Chips back from foundry in Oct., test system for MIC4 chip being developed
  - more effort required for the prototype test (test system development, electrical test, irradiation test, beam test …)

Thanks for your attention !