The CPS technology study for the inner chamber upgrade of BESIII MDC

Mingyi Dong

dongmy@ihep.ac.cn

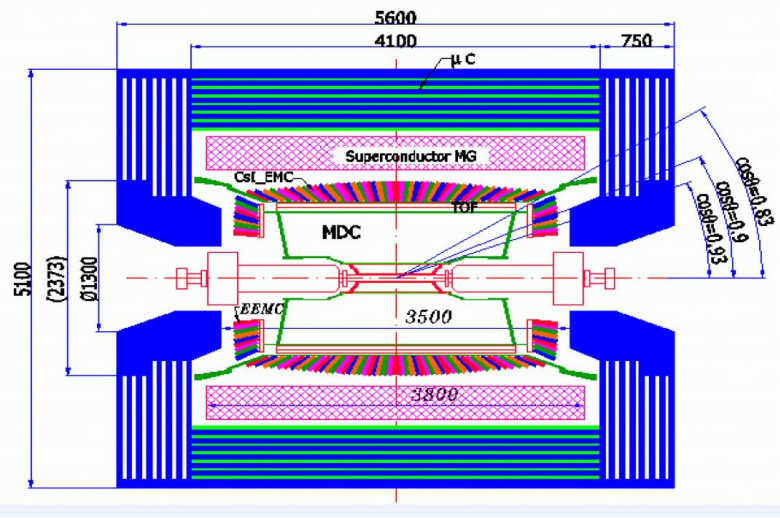
On behalf of the working group

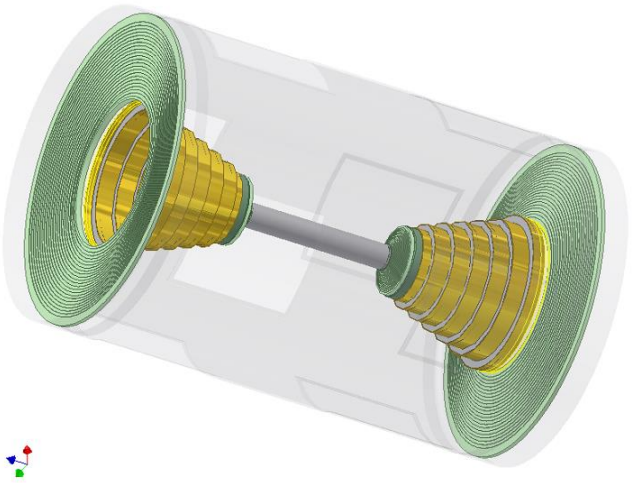
Outline

- Introduction of the CPS prototype for inner MDC upgrade
- Probe test of Mimosa28 chips
- Ladder design and assembly
- Readout electronics and DAQ
- Ladder test by radiation source
- Summary and outlook

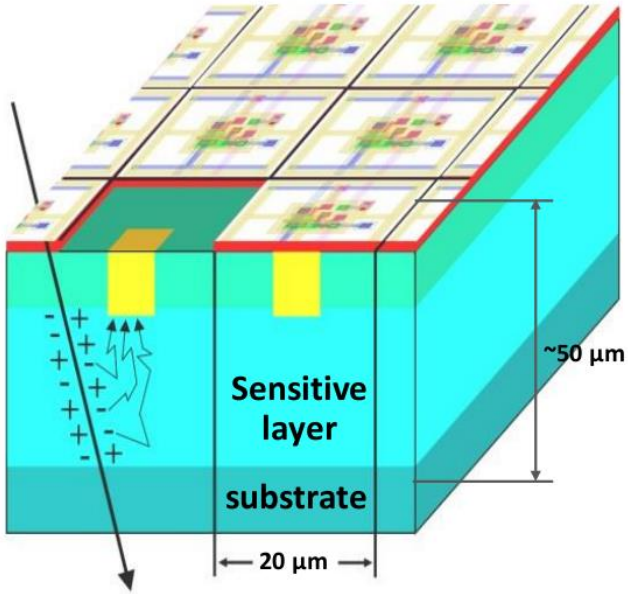
The BESIII experiment

- **The BESIII experiment**
  - general purpose detector at BEPCII, $E_{cm} \approx$ 2-4.6 GeV, $L_{peak} \approx 10^{33}/cm^2/s$
  - versatile researches in τ-charm physics
- **Main drift chamber (MDC)**
  - Key tracking detector for momentum and dE/dx measurements of the charged particles
  - Composed of an inner chamber (8 layers) and an outer chamber (35 layer), working in 1T field
  - σ_{xy} = 120μm, σ_p=0.5%@ 1GeV, dE/dx=6%
- **Aging problems of inner chamber**
  - High background encountered, reducing HV of the innermost 4 layers, gain decreased to 31% of normal one for the first layer cell
  - Cathode aging: Malter discharge
  - Anode aging: resulting in the cell gains dropped dramatically (39% for the first layer cells)
  - Performance deteriorated (the worst case) : $\sigma_{xy} \approx$ 300μm, $\varepsilon_{cell} \approx$70%





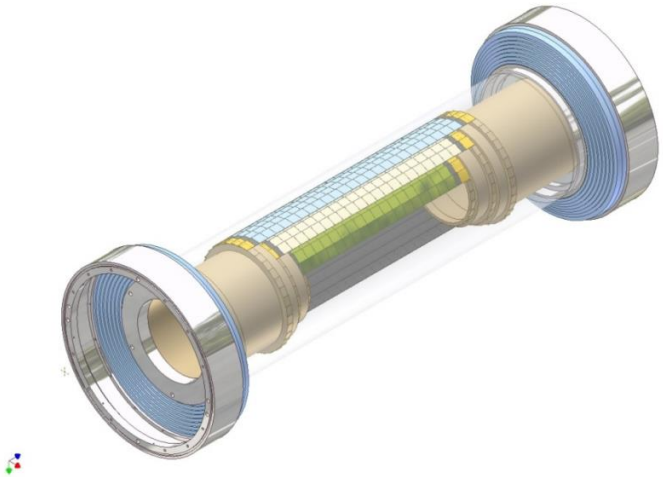
Main features of CMOS pixel sensor

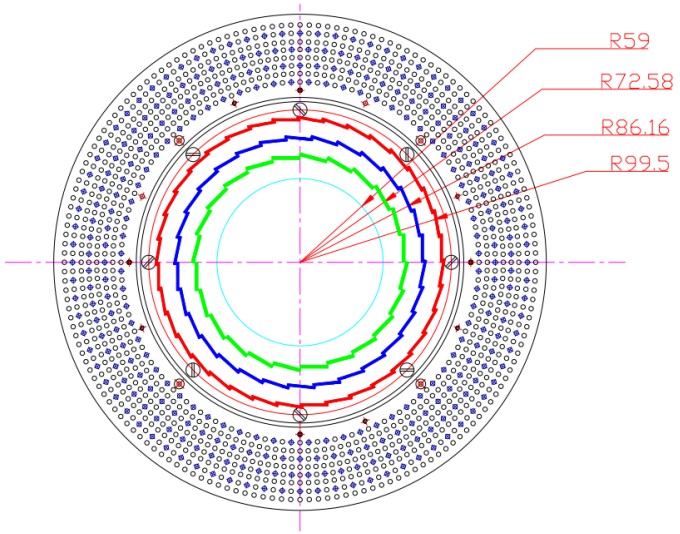


- CMOS Pixel Sensors (CPS), one kind of monolithic active pixel sensor
- First developed by IPHC at Strasbourg , France in 1999
- Mimosa28: used in STAR-PXL, derived from Mimosa26,

- Monolithic, senser+readout electronics
  - p-type Si
  - Signal created in low doped thin epitaxial layer
  - ~ 80 e^- /µm, total signal ~ O(1000 e-)
- Charge collection
  - Limited depleted region
  - By thermal diffusion
  - Charge sharing → resolution
- Flexible running conditions
  - From 0℃ up to 30-40 ℃ if necessary
- Industrial mass production
  - Advantages on costs, yields, fast evolution of the technology, Possible frequent submissions

Inner MDC upgrade with CPS



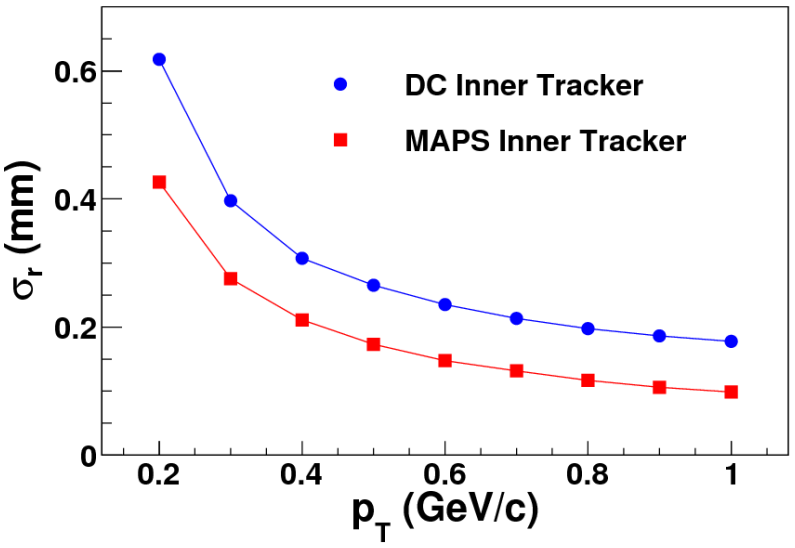


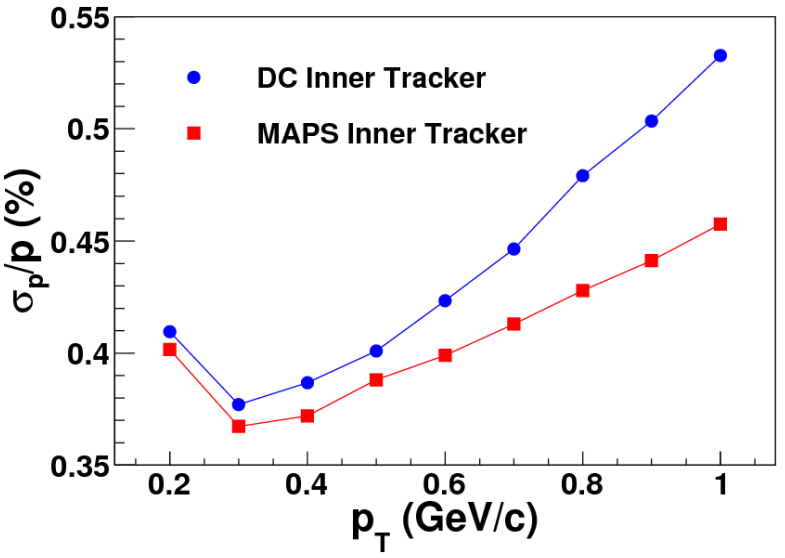
- Baseline design
  - 3 layers of single sided CPS
  - Similar ladder structure as STAR or ALICE
  - Air cooling
- R&D project
  - institutions: IHEP+ SDU

  collaboration with IPHC

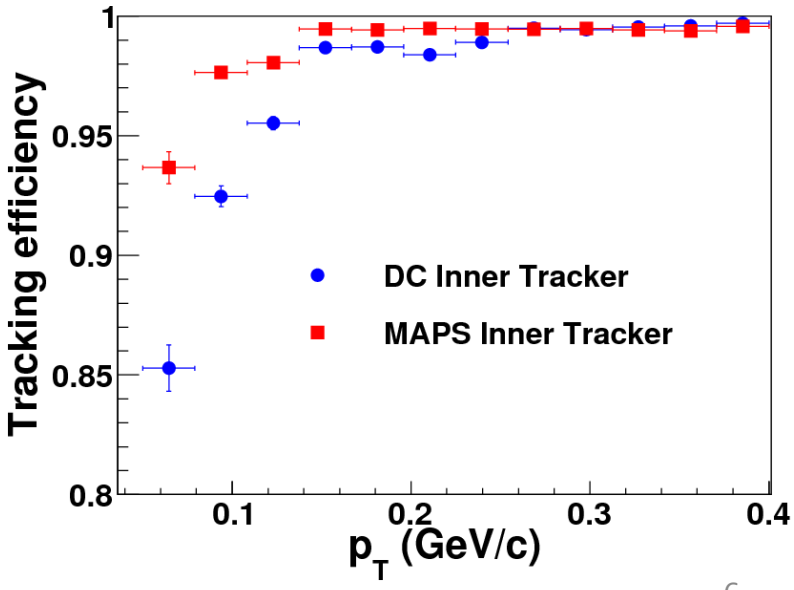
- density: ~20μm pixel pitch, ~0.9Mpixels/chip
- Spatial resolution: a few μm
- Rating capability: ~10^6Hz/cm^2
- Material budget: ~50μm thick
- Radiation tolerance: ~1 MRad, 10^{13} n_{eq}/cm^2
- Power consumption: 175mW/cm^2
- Room temperature operation

Simulation of Inner tracker with CPS

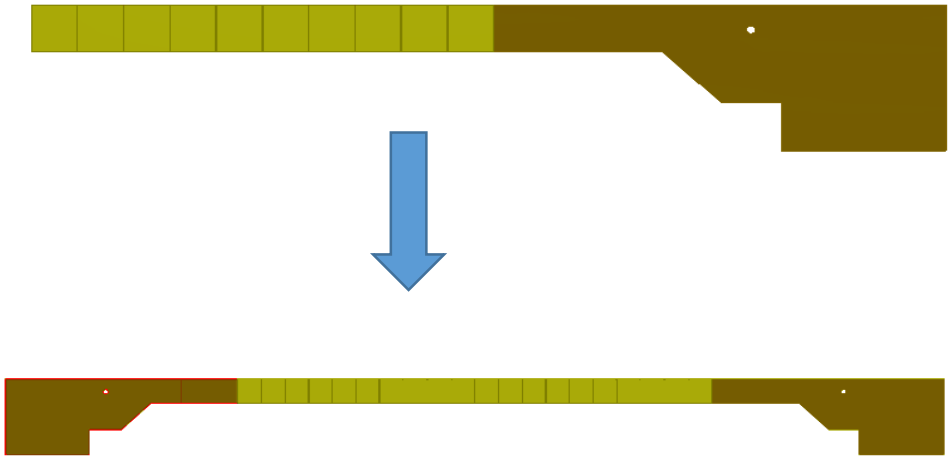


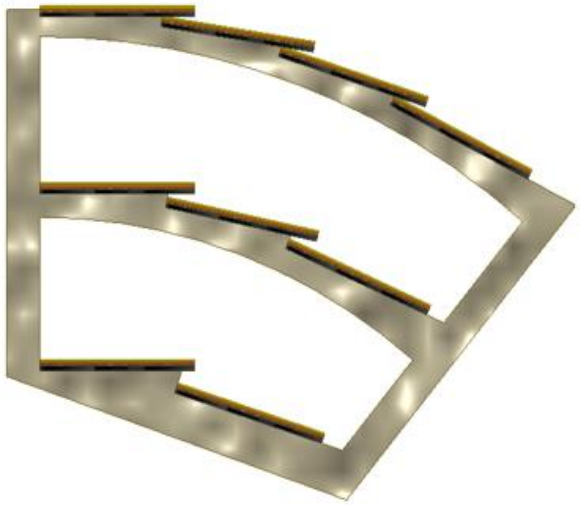


- Simulation to estimate the performance of the whole tracker with CPS inner tracker
- Improvement of the spatial resolution
  - σ_{xy} : 0.18mm → 0.10mm @ 1GeV/c
  - σ_z : 1.6mm → 0.12mm @ 1GeV/c
- Improvement of the momentum resolution
- Improvement of the tracking efficiency



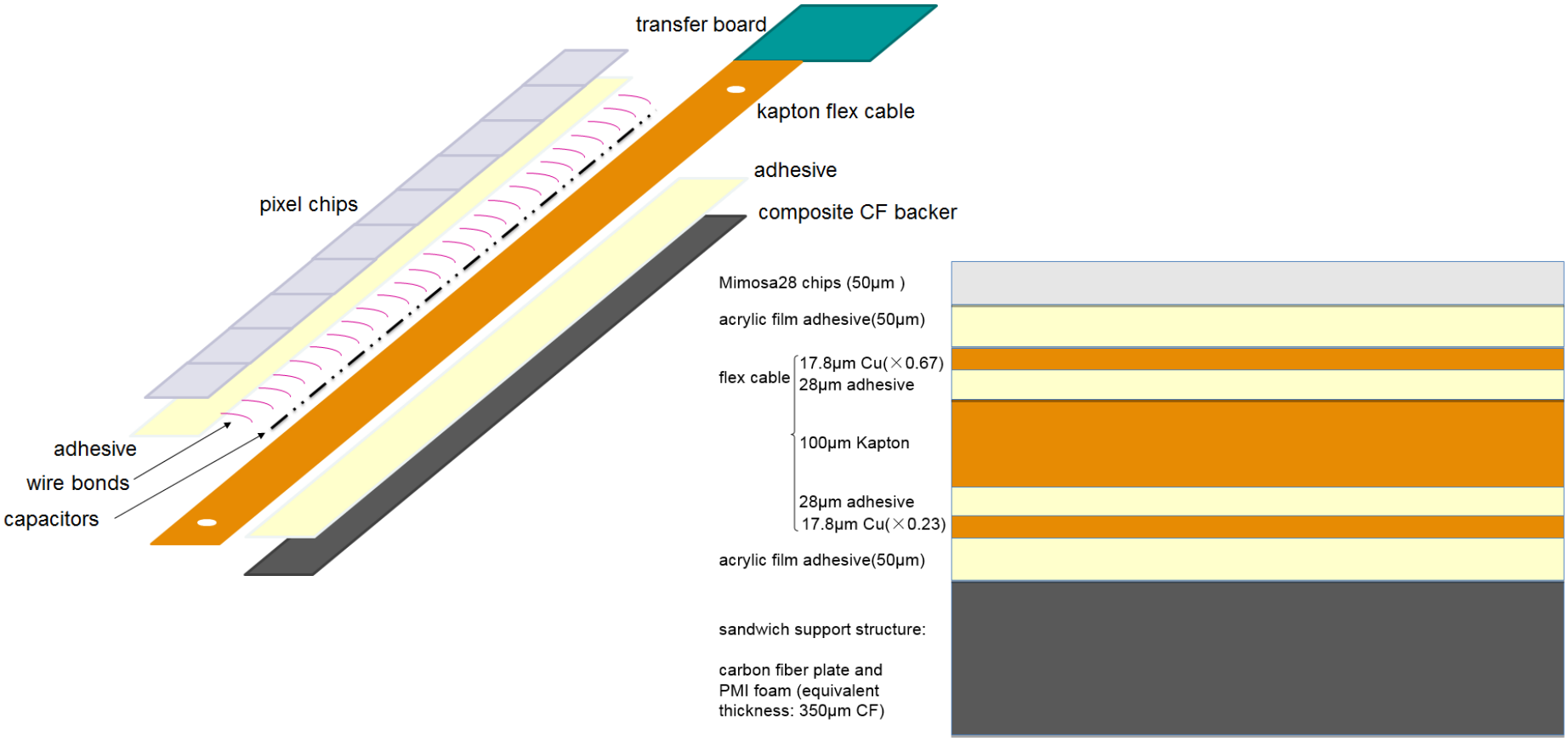
R&D target: a CPS prototype





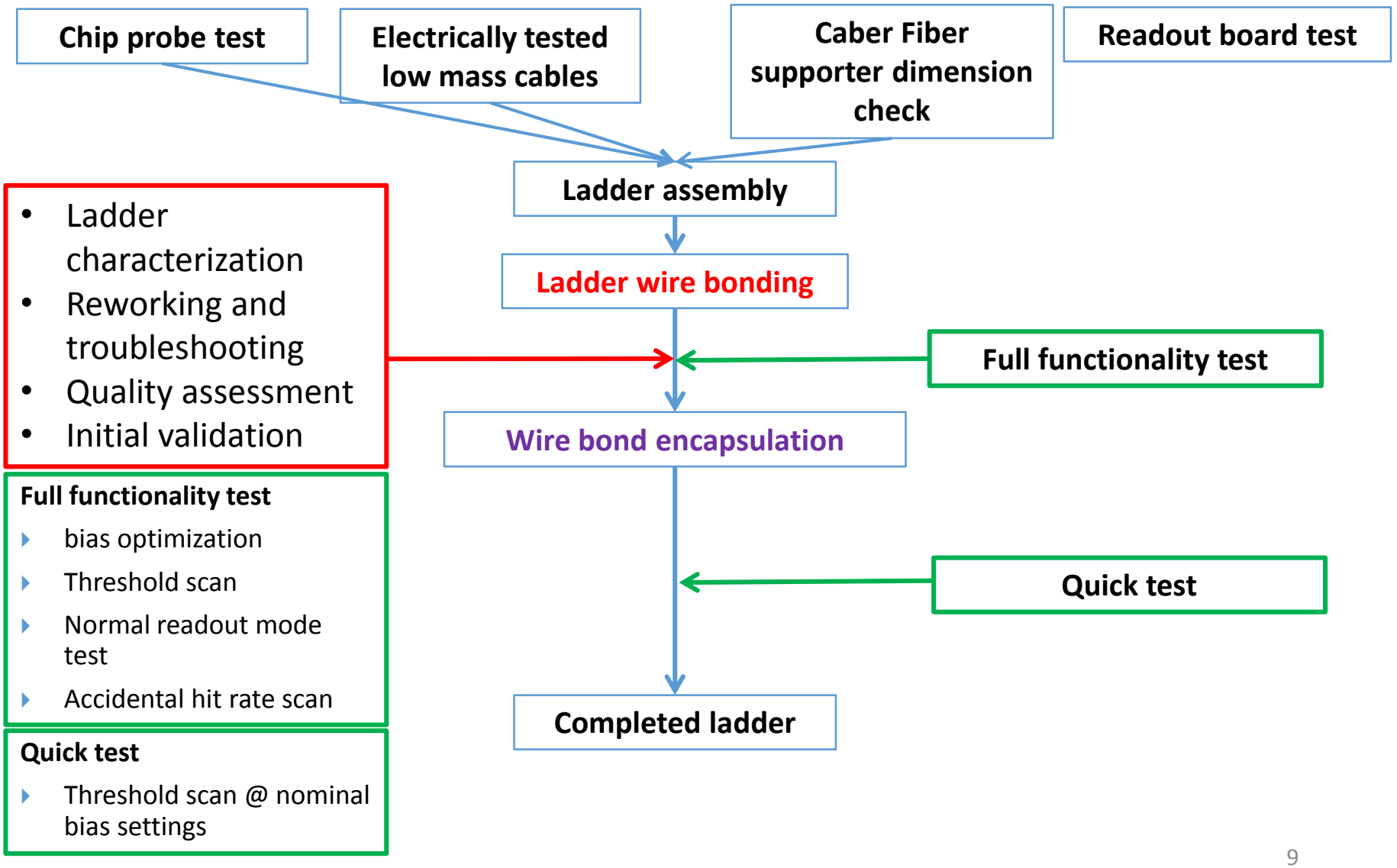
- Prototype layout
  - 1/10 Coverage of the inner tracker (~ 720cm^2→180 chips→180M pixels)
  - ϕ direction: 2 , 3 and 4 ladders for the 1st, 2nd and 3rd layer respectively
  - Z direction: 2 sets of ladders each layer
  - 10 Mimosa28 chips with dimension of 2cm × 2cm in each ladder
- chip →ladder →sector → layer →prototype

Ladder design

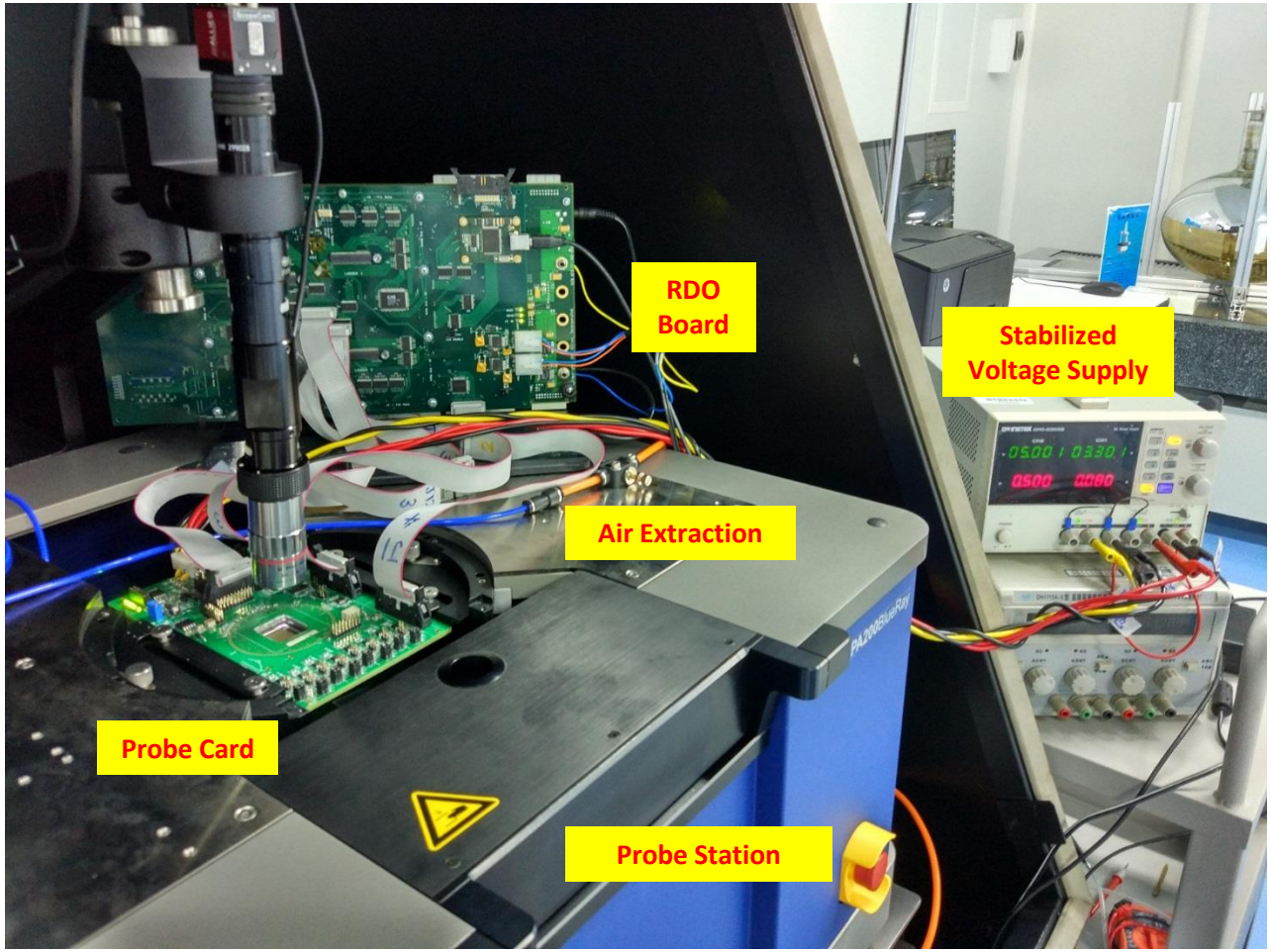


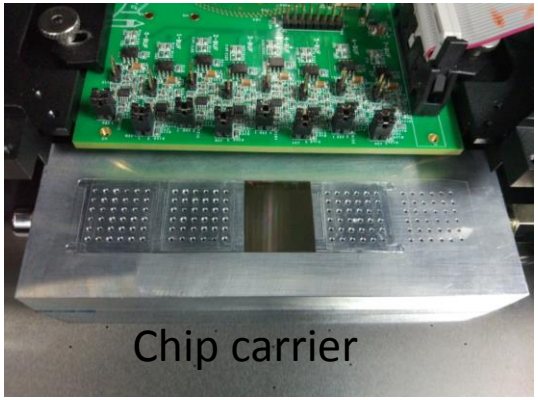
- Ladder: the basic building block of the detector
  - 10 Mimosa28 chips (thinned to 50μm)
  - A flex cable
  - A carbon fiber supporter

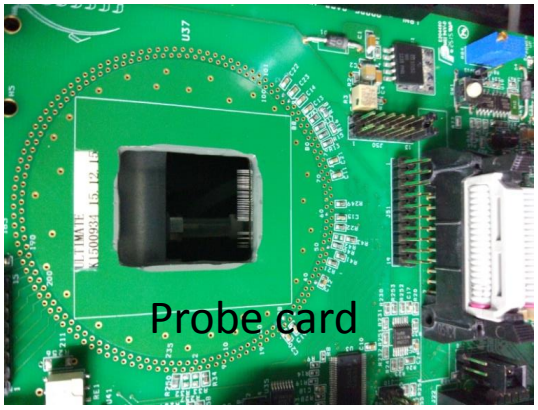
Ladder assembly procedure

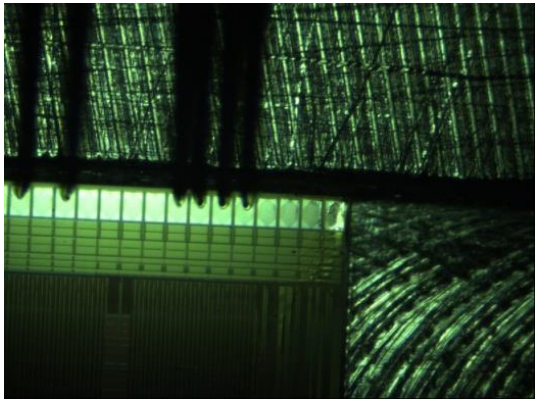


Chip probe test









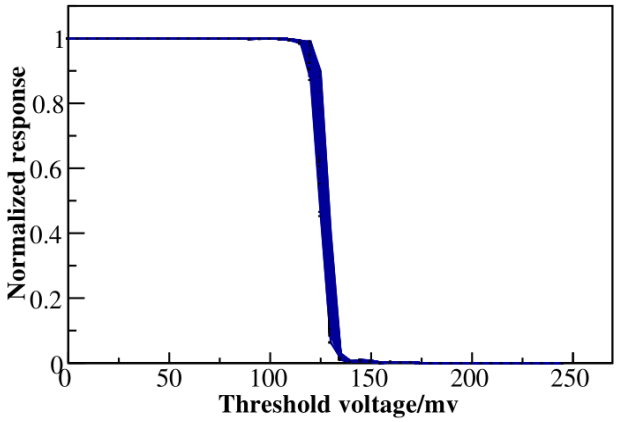
- A probe testing system was set up for the chip functional verification and preliminary performance test

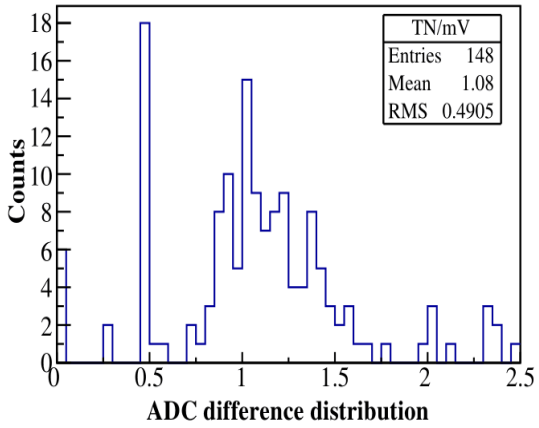
Probe test content

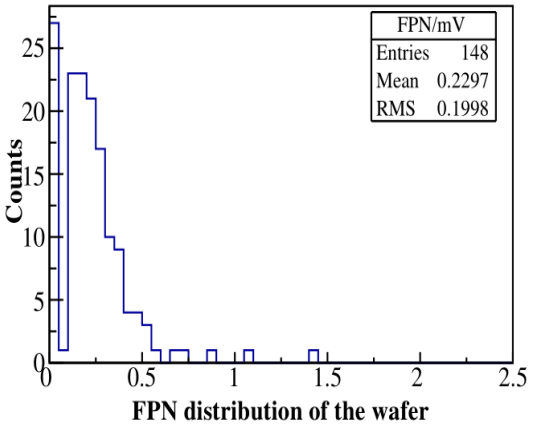
Test	Description
1_contact_test.bat	Check pin-pad touched and JTAG
2_test.bat	Test the power consumption
3_pattern.bat	Check the number of header and trailer
4_pattern2.bat	Compare the output data with the reference data in normal mode
5_vclp_scan.bat	pixel clamp voltage scan
6_threshold.bat	Threshold scan

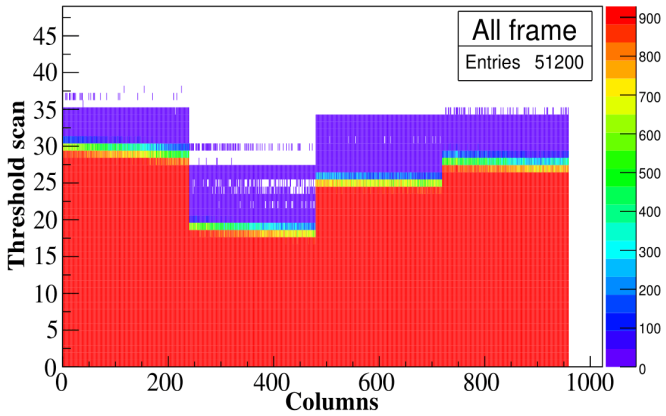
Test	Preliminary Judgment for Bad Chips
1	JTAG is wrong
2	Reset:i_vdda>100 or i_vddd>25; Start:i_vdda>1500 or i_vddd>1000
3	Headers or Trailers < 200
4	data do not match
5	DAC Range out of (75, 100)
6	Bad pixels > 80%

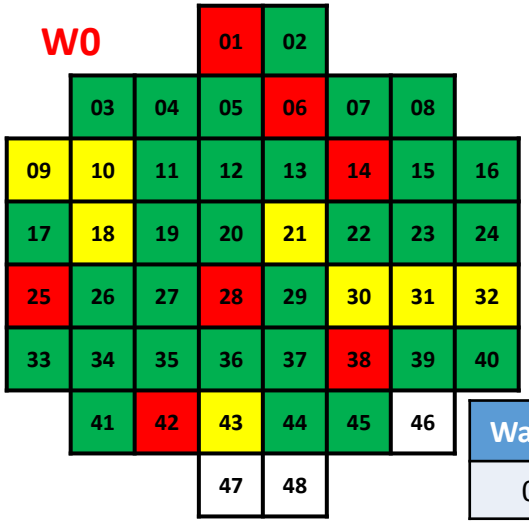
Probe Test Conclusion









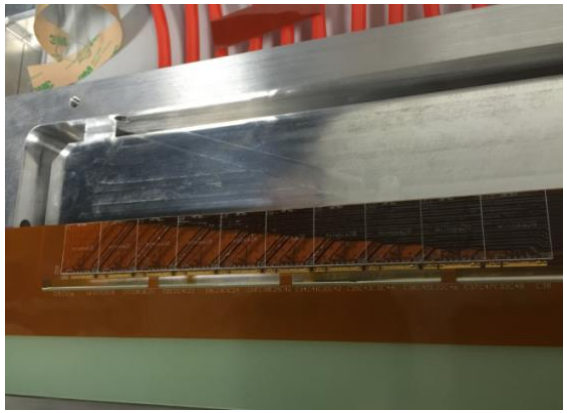


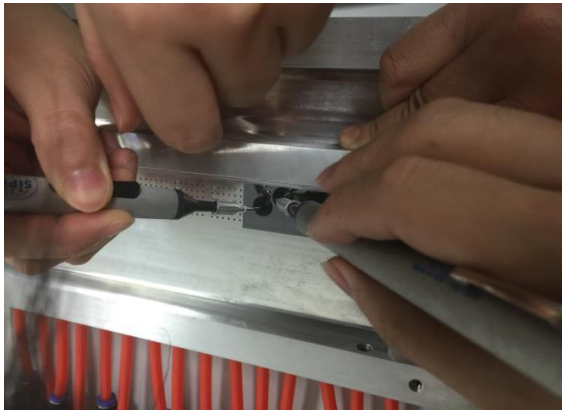
Not Test
Dirty Pads
Good Chip
Bad Chip

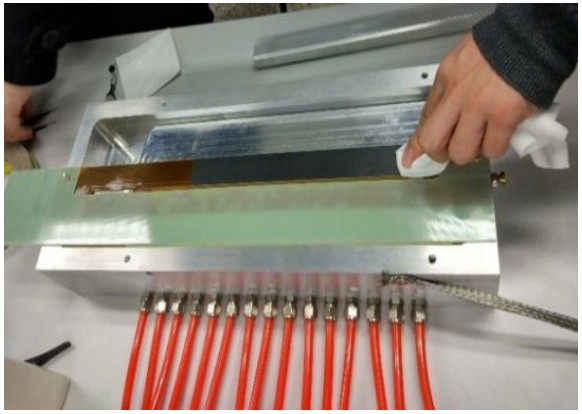
Wafer	Chips	Good	Bad	Dirty
0	45	30	15	8

- 6 wafer chips were delivered, 4 wafer chips were tested
- Typical yield is about 65%

Ladder assembly

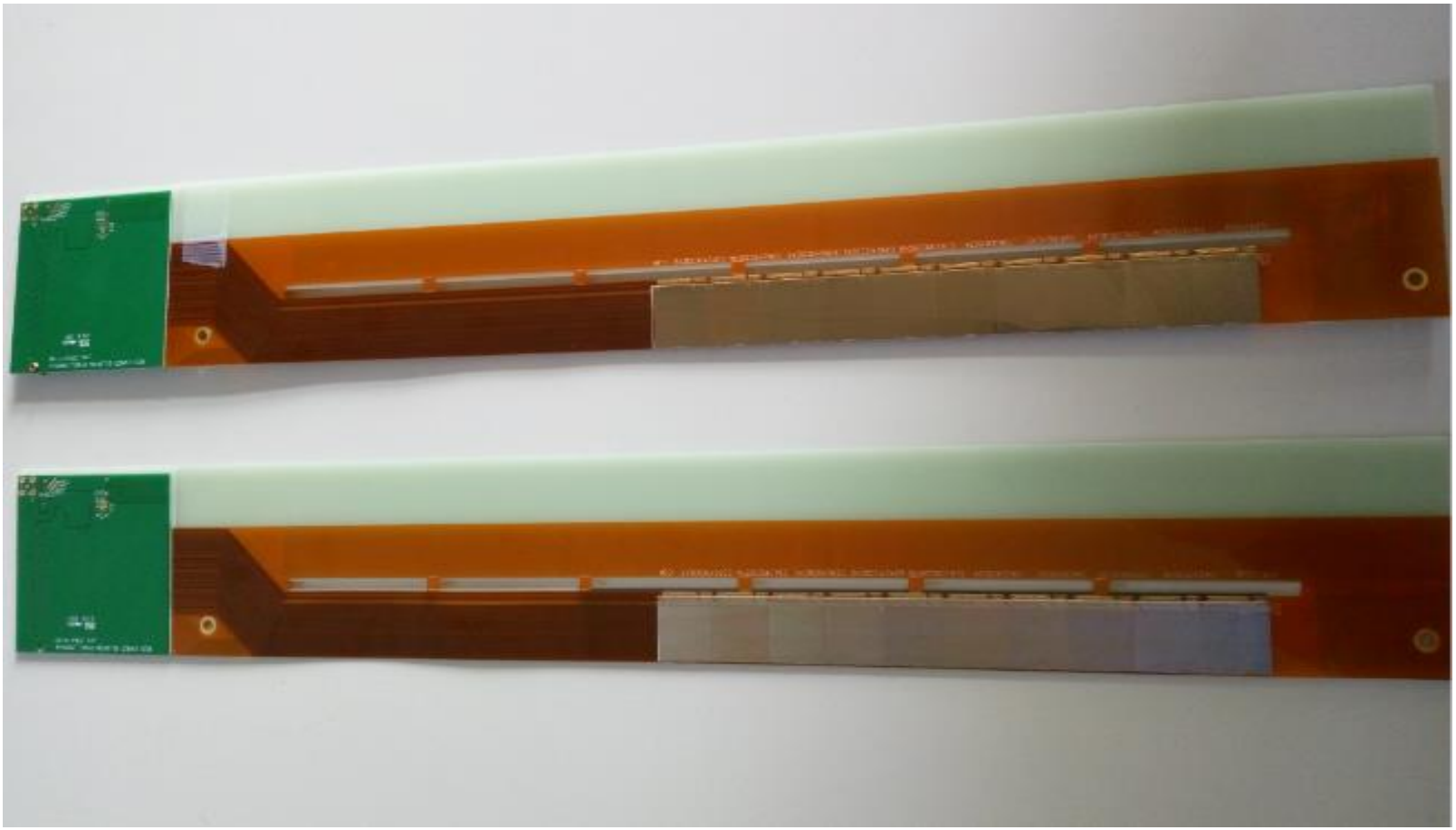




- Ladder assembly was operated at a special platform to ensure the location accuracy of the chips

Ladder assembly

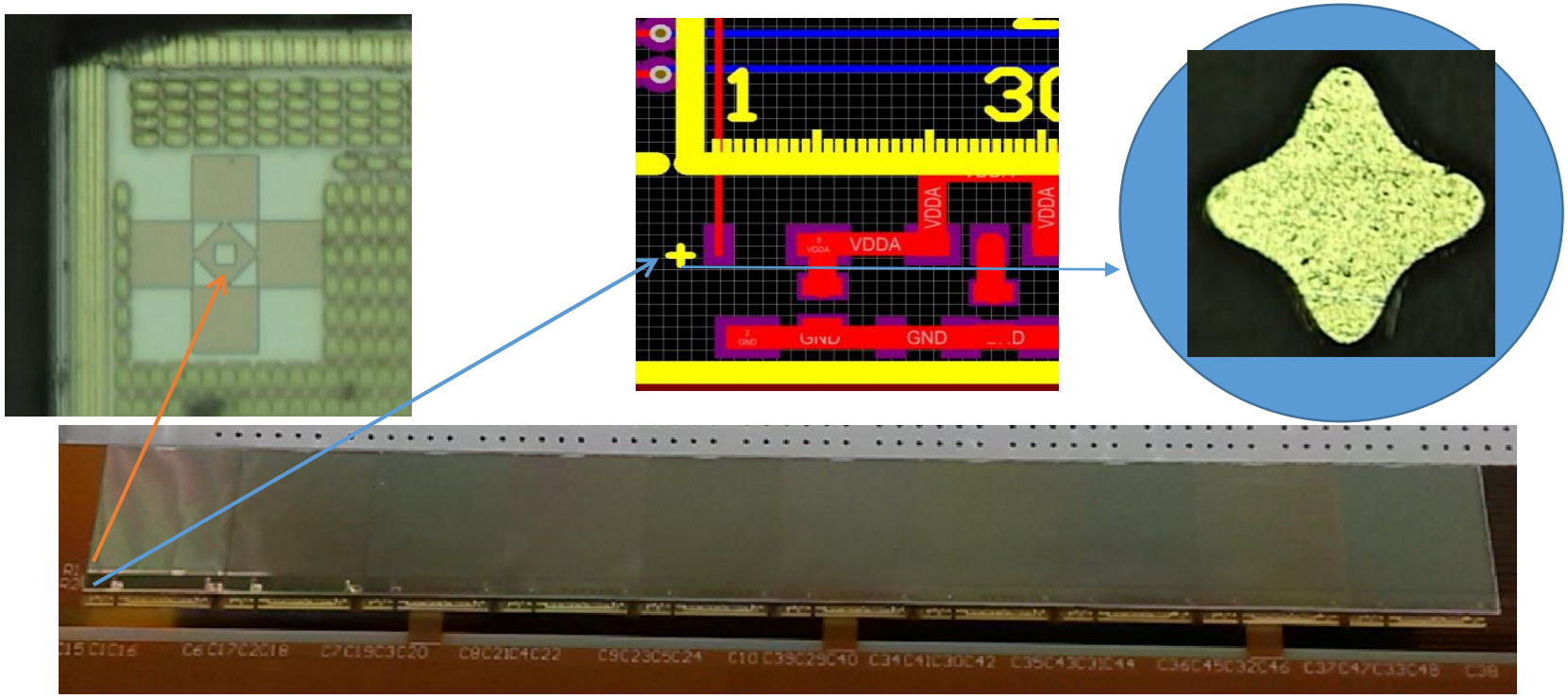


Material budget

layer	material	Thickness (μm)	Density (g /cm^3)	X_0(cm)	% of X_0
sensor	Si	50	2.33	9.36	0.053
	Acrylic adhesive	50	1.2	34.5	0.014
cable	Cu	17.8×0.67	8.96	1.43	0.083
	Adhesive	28	1.2	34.5	0.008
	Kapton	100	1.42	28.6	0.035
	Adhesive	28	1.2	34.5	0.008
	Cu	17.8×0.23	8.96	1.43	0.029
backer	Acrylic adhesive	50	1.2	34.5	0.014
	Carbon fiber	350	1.72	28	0.125
Support beam	Acrylic adhesive	50	1.2	34.5	0.014
	Carbon fiber	350	1.72	28	0.125
total of ladder					0.369
total all					0.508

- Ladder: about 0.37% X_0
- Detector prototype: 0.51% X_0 /layer (ladder + CF supporter)

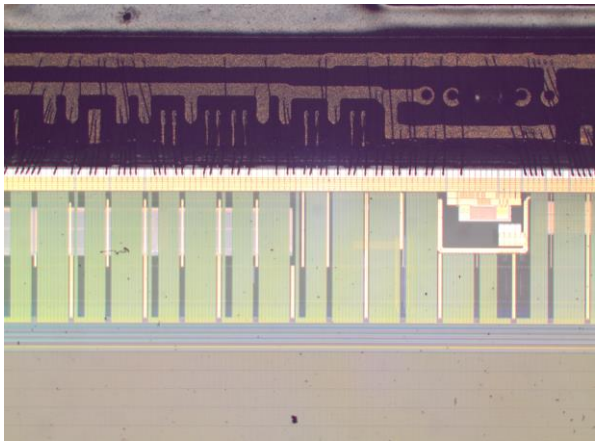
Location of the chips on the ladder

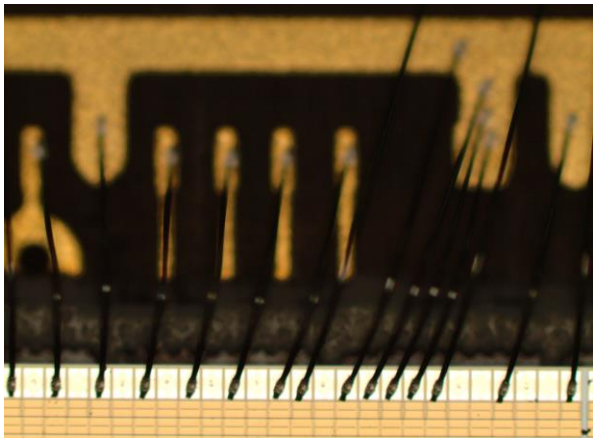


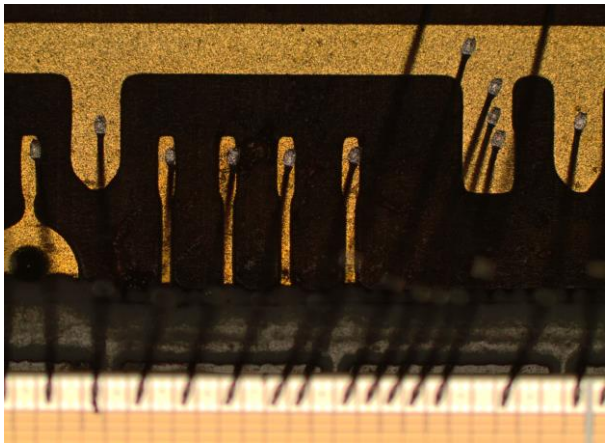
芯片编号	chip1	chip2	chip3	chip4	chip5	chip6	chip7	chip8	chip9	chip10
Δd2(μm)	7.6	9.9	-1.6	-13.4	3.4	-15.3	0.2	6.1	2.7	10.0

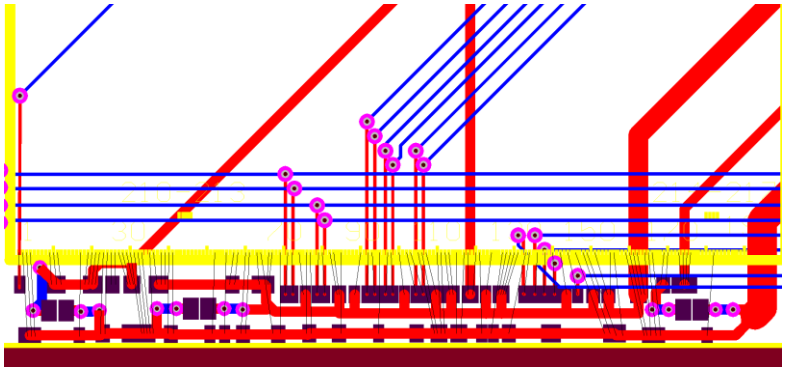
- The distance between the left mark on the chip and its corresponding mark on the PCB was tested by a imaging machine
- The location precision is better than 10μm or even better after the assembly process optimization

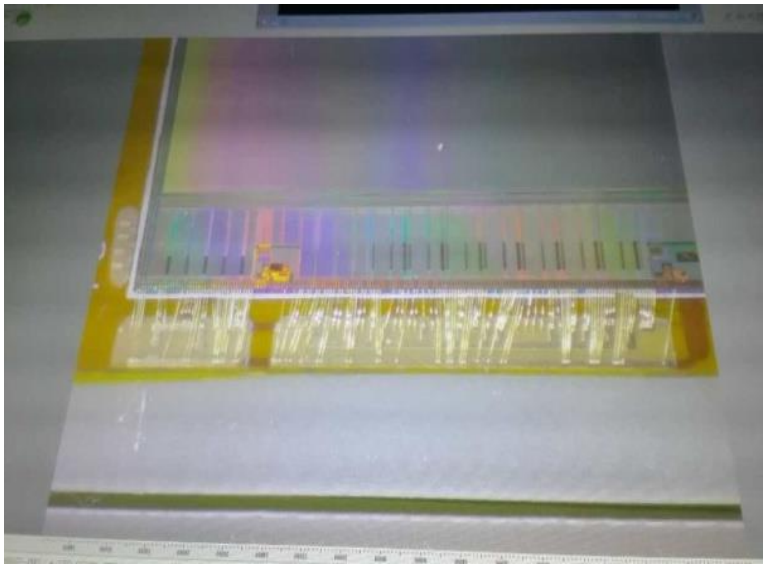
Wire bonding





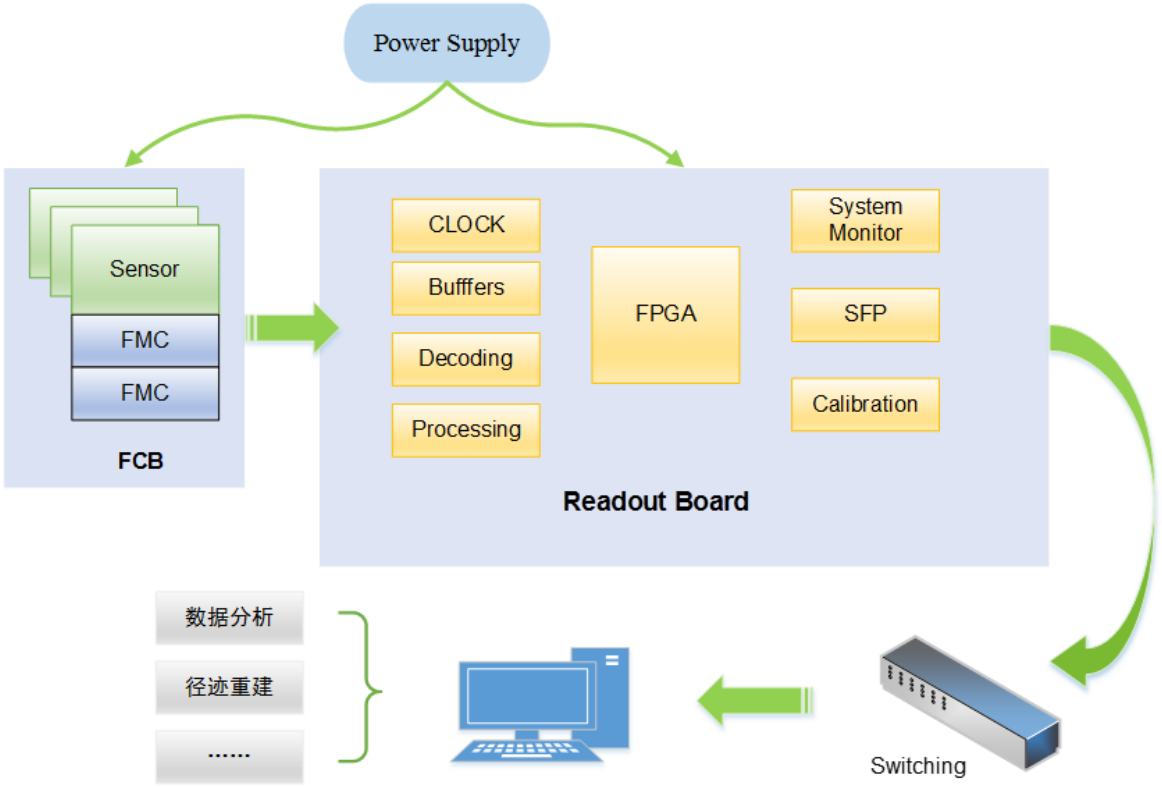


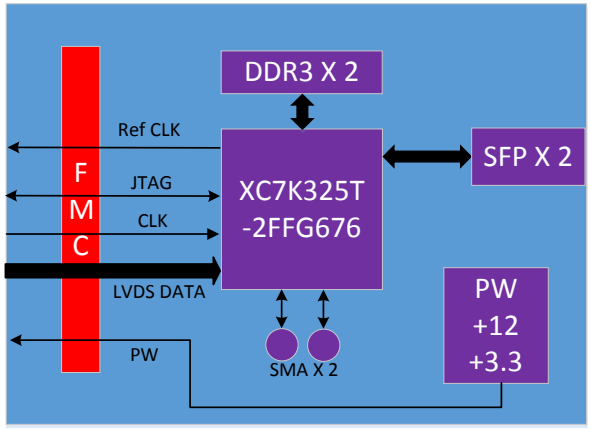




- 102wires/chip
- Bonded with 25µm aluminum wire
- Tooling for fixing ladder

Schematic of the readout electronics

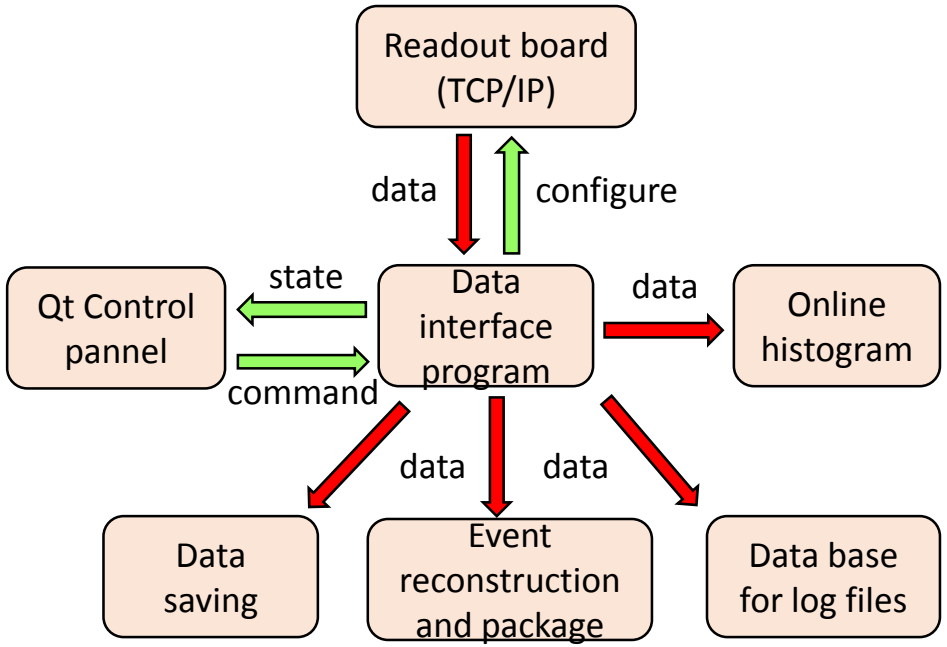


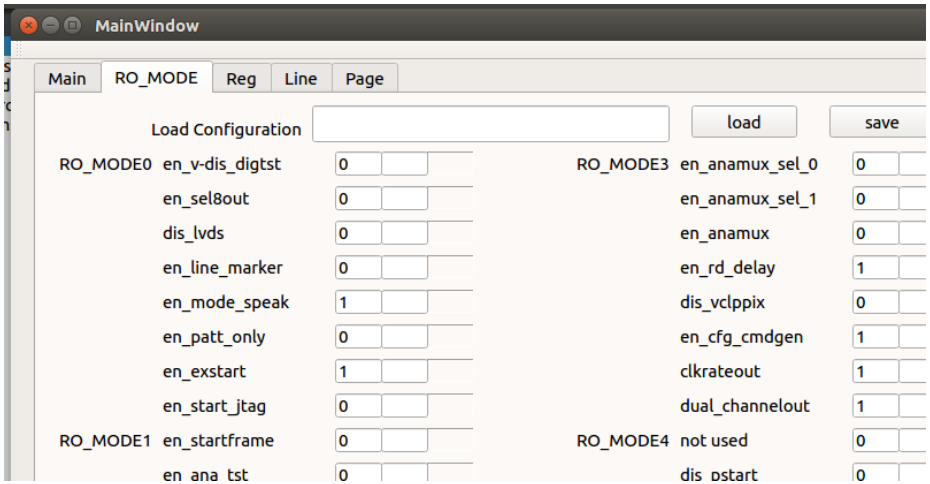


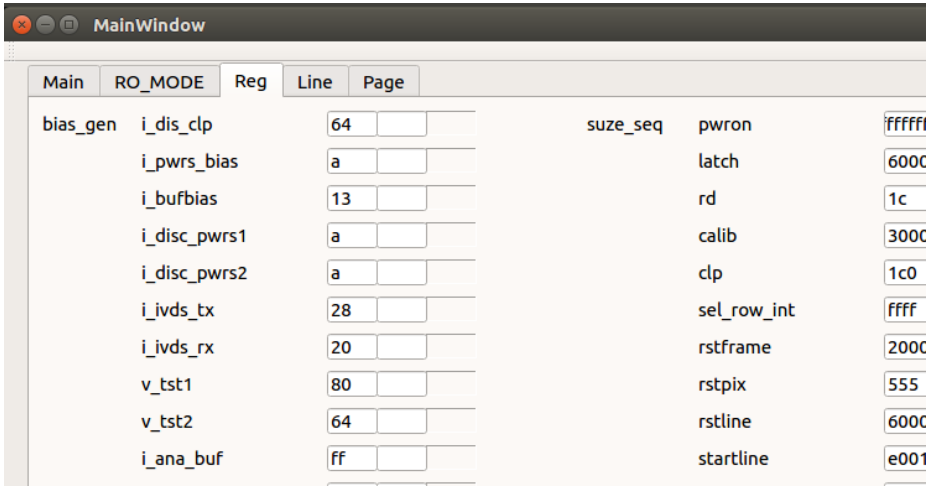
- Distributed system
- Ladder → FCB → Readout Board → Switching → PC
- SiTCP： implementation of a hardware TCP/IP on Xilinx FPGA device, high-speed and highly reliable data transmission

DAQ

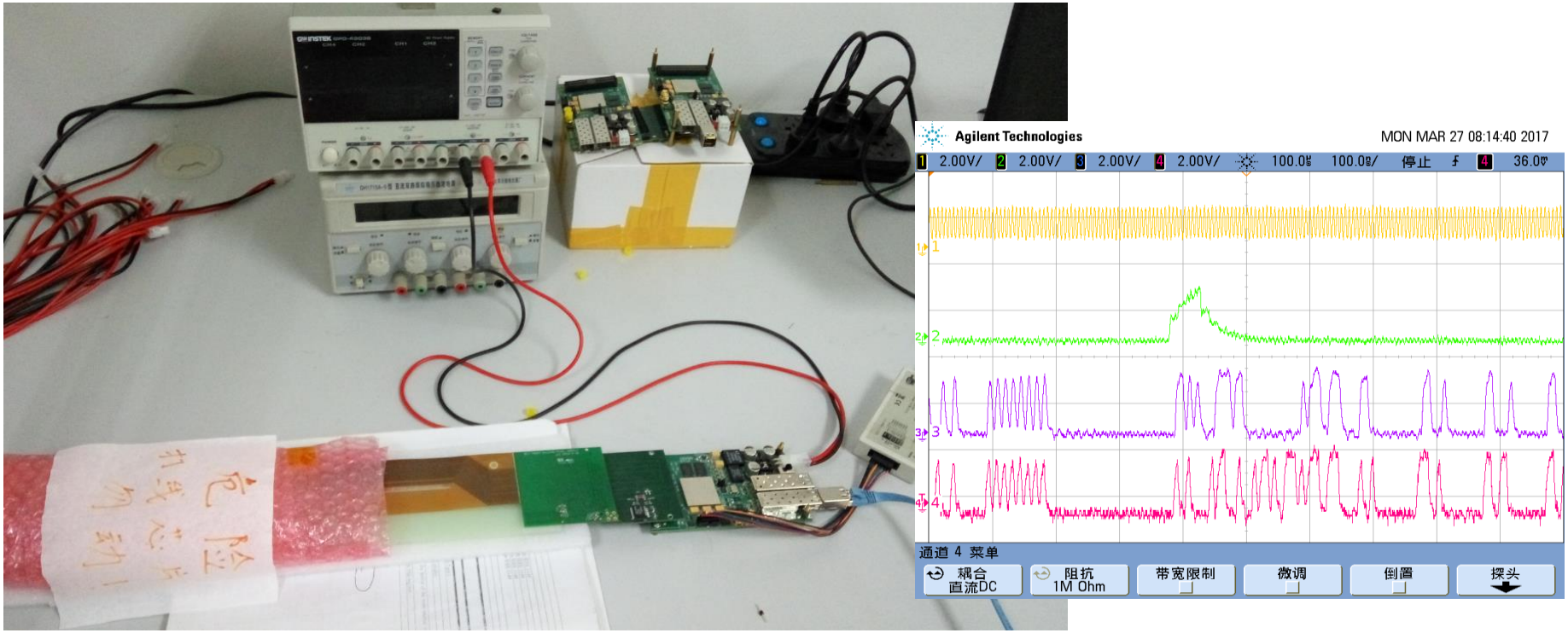
- Data transmission based on SiTCP
- Meet the requirement of maximum of the ladder readout speed: 30~40MB/s
- Developed by Qt software (linux), including 7 functional modules





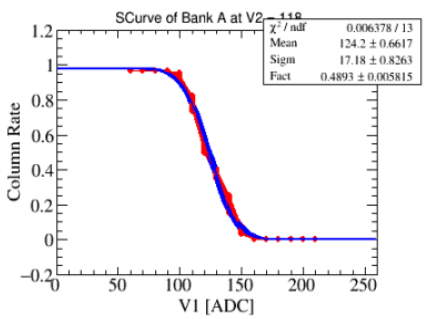


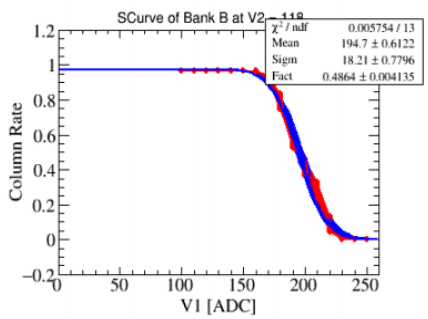
Ladder test

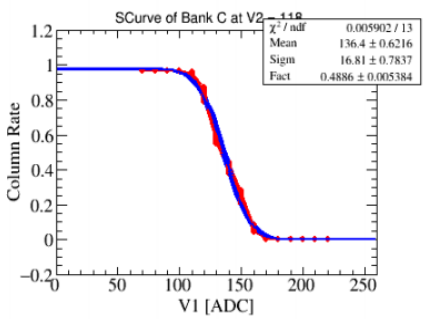


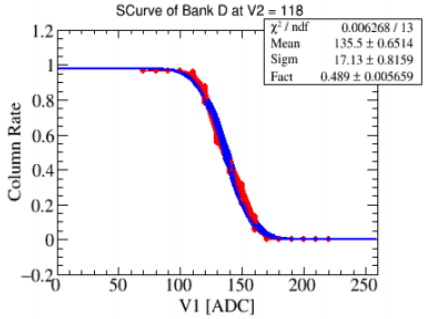
- The ladders together with the readout electronics were test by ^{55}Fe X rays and ^{90}Sr β rays
- The threshold scan, the crosstalk, the imaging performance, and the hit reconstruction algorithm were studied.

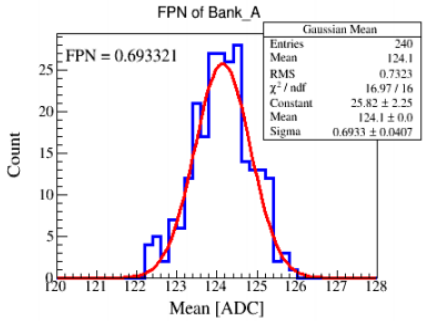
S-curve scan

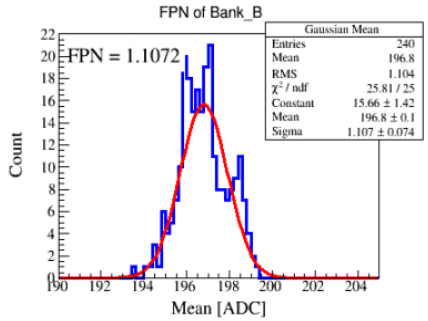


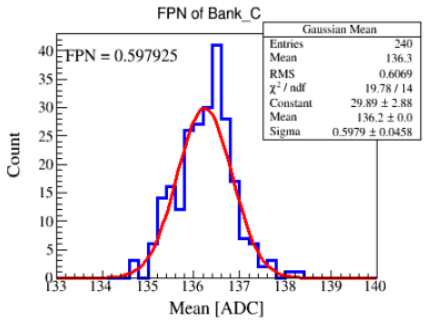


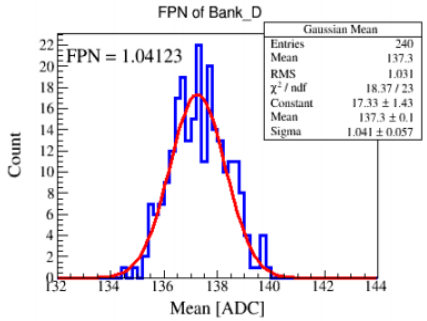


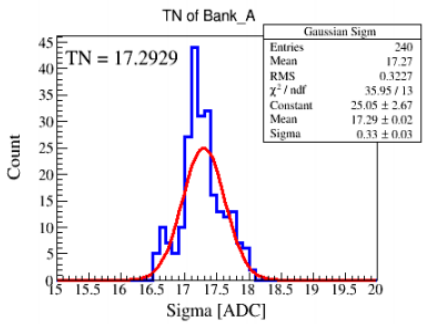


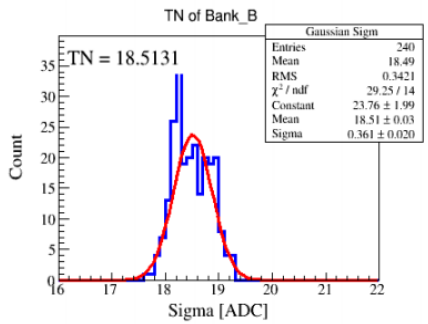


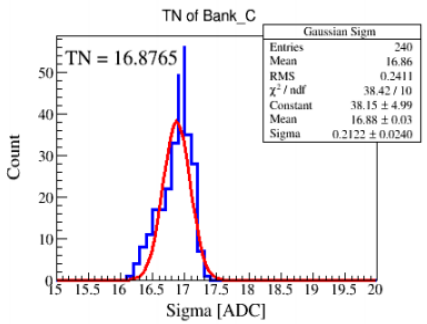


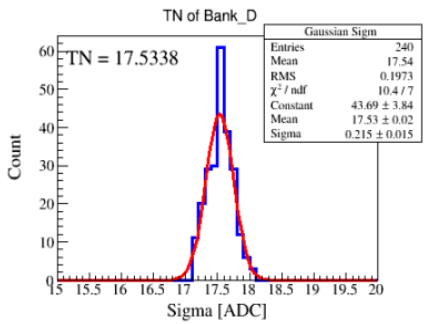








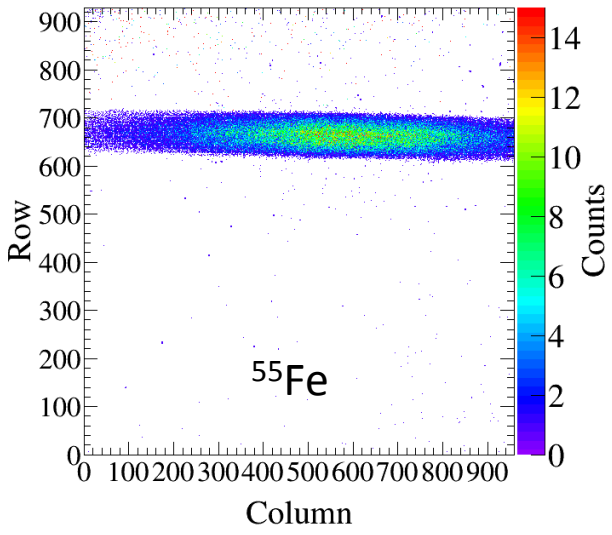


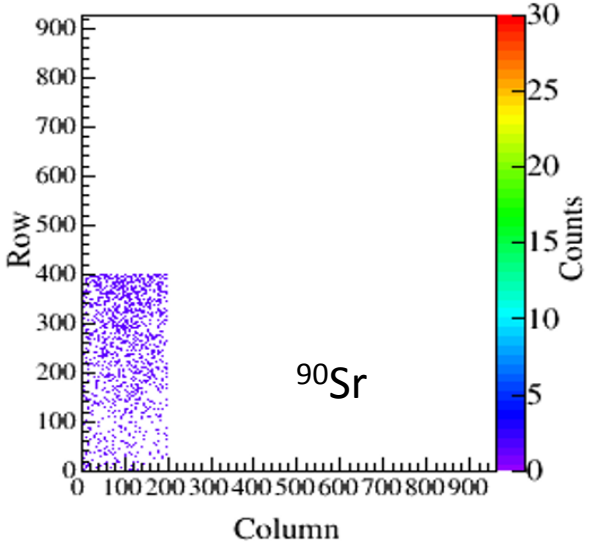


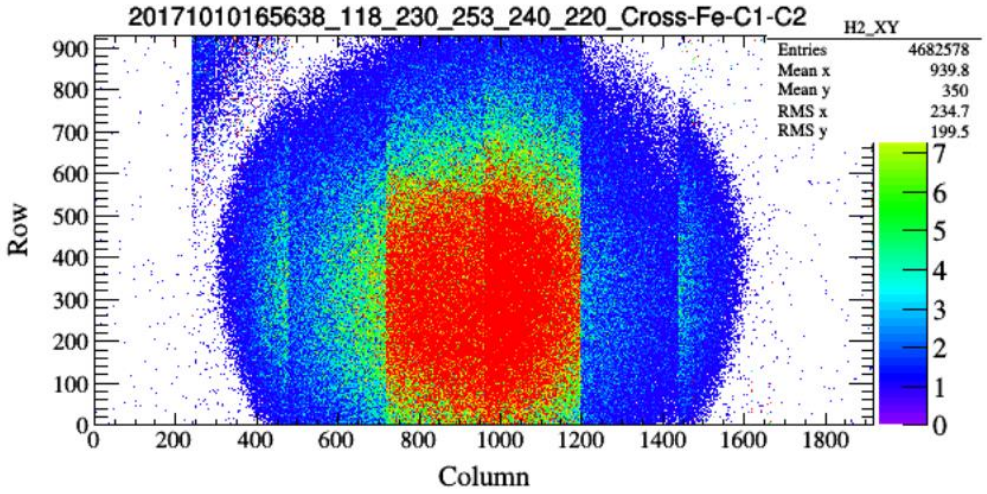
- S-curve scan by column and by pixel
- PFN~1mV, TN, ENC~ 15-20e, Threshold ~(3-4)σ

Test by radiation sources

- Pixel response test by ^{55}Fe X rays and ^{90}Sr β rays
- Crosstalk between two neighboring chips test
- Impact of the chip temperature on the noise level



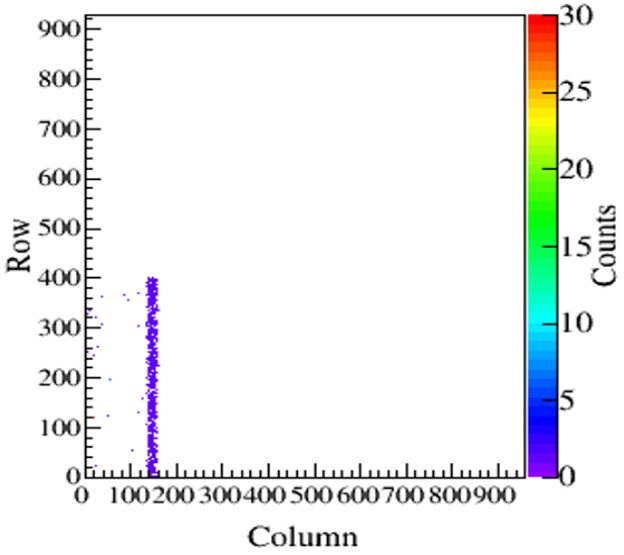


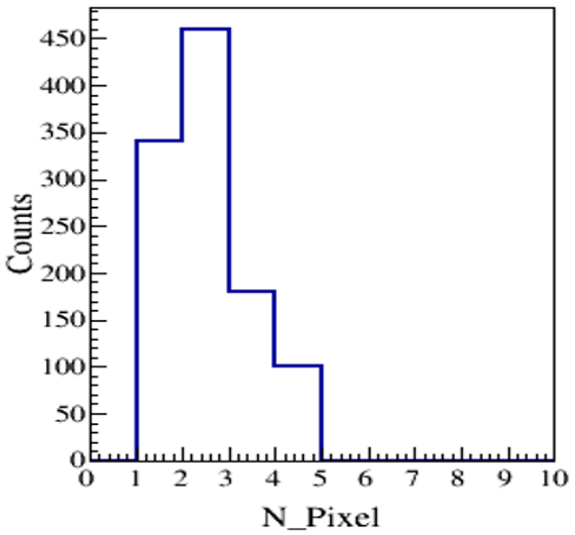


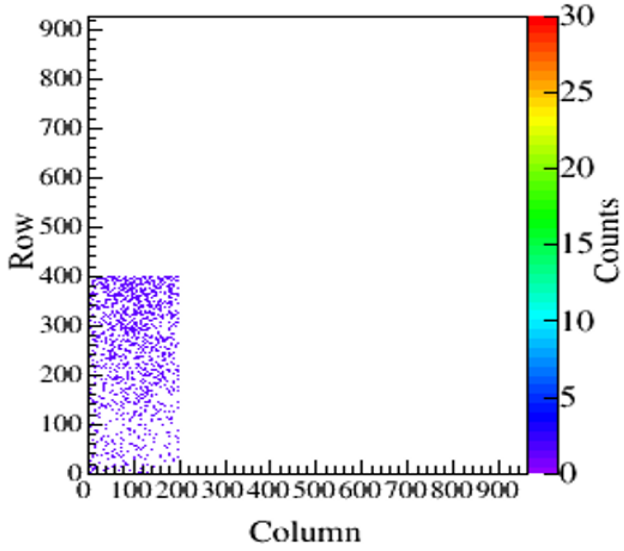
Crosstalk between two neighboring chips test

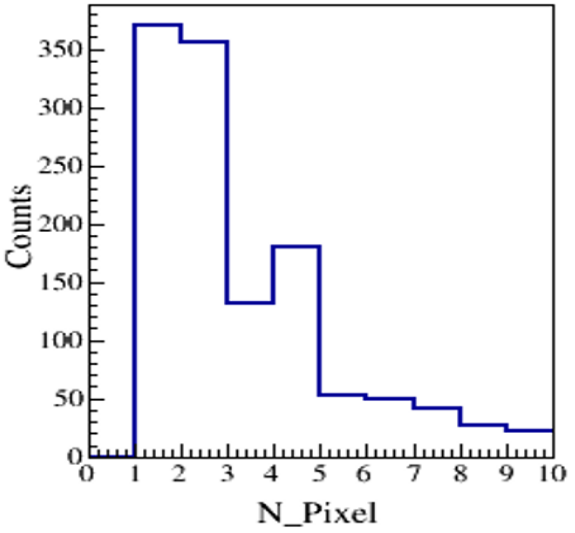
Hit reconstruction algorithm

- Charge collection by thermal diffusion
- Charges induced by one hit can be sharing with several pixels, be benefit to special resolution
- Digital readout: no seed signal
- Reconstruction algorithm : comparison method









Summary and Outlook

- The study of a CPS prototype
- Development of the ladder, electronics, DAQ, and software
- Preliminary test by radiation source, beam test will be carried out next year

- The research focus on the key technology and method of the pixel detector, not only for the BESIII inner tracker upgrade, but also for the pre-research of the CEPC vertex detector
- Double-sided ladder was considered and designed preliminary, supported by funding of key lab of nuclear detection and electronics
- Some issues for MOST2: trigger, cooling……

Thanks for your attention !