Introductory remarks
Pixel Detector Prototype
(MOST 2)

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Goals of Meeting

- Plan the Silicon Prototype project of MOST 2
  - Review any flaws of pre-application
  - Establish a plan for final application
    - Review input from different sources, including MOST 1 project
    - Define “conservative” project for MOST 2 application
    - Discuss extended goals for project beyond minimal requirements
    - Identify shortcomings and problem areas

- Application deadlines
  - Pre-application
    - Due: December 1, 2017
    - Version due to CAS on November 27, 2017
  - Application:
    - Due: December 31, 2017

MOST 2 Guidance

- 高能量加速器上高分辨探测技术验证。完成内层硅径迹探测器原型机，通过束流试验验证主要设计指标，空间分辨3-5微米（um）；设计总电离剂量为1 MRad的硅探测器；

- Verification of high resolution detecting technology on high energy accelerator. Complete the **prototype** of inner silicon track detector, verify the main design parameters through beam test, spatial resolution is **3-5 microns (μm)**; Design a silicon detector with **1 MRad** total ionization dose;

Deliverables:

- Silicon prototype
- Beam test

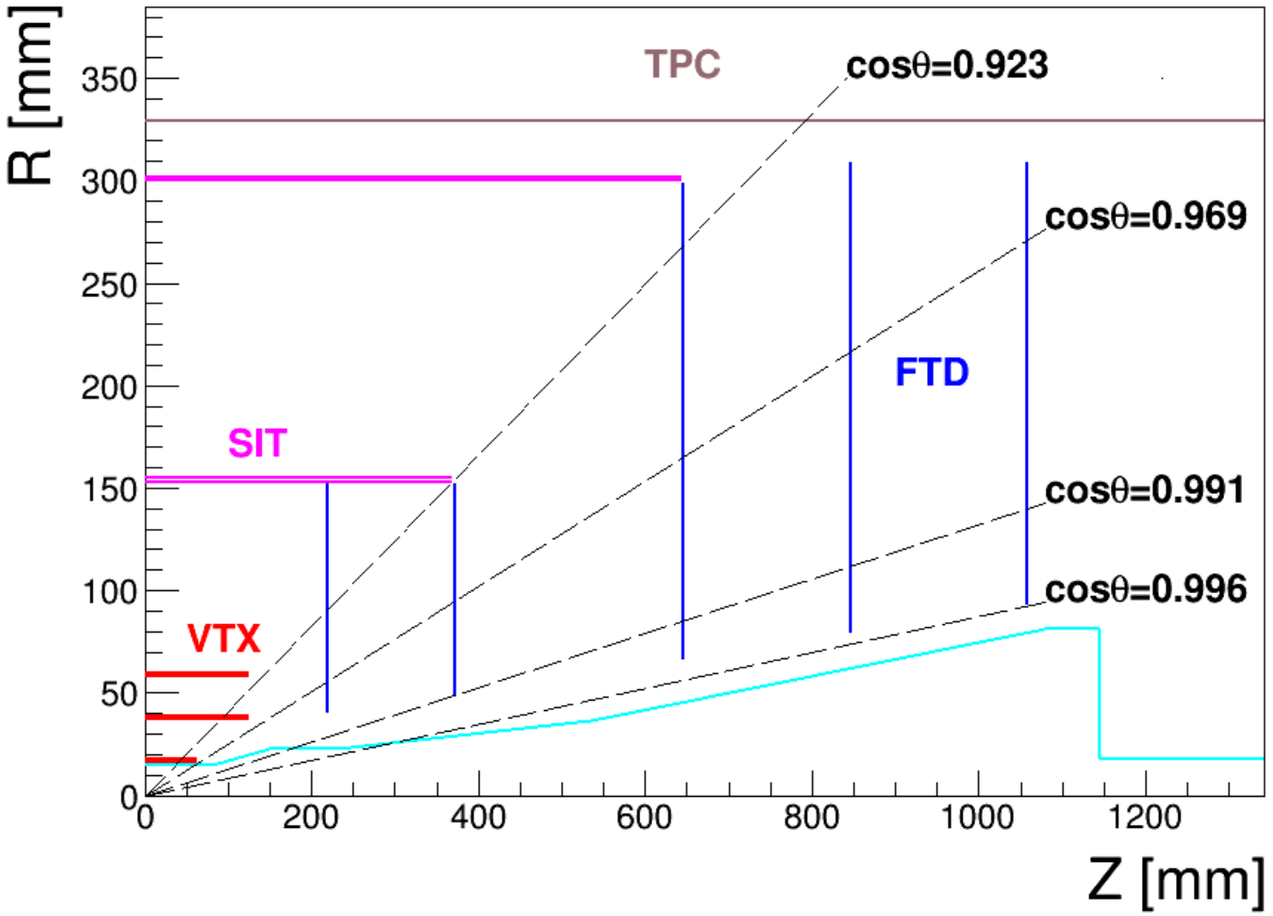
Key assessment parameters:

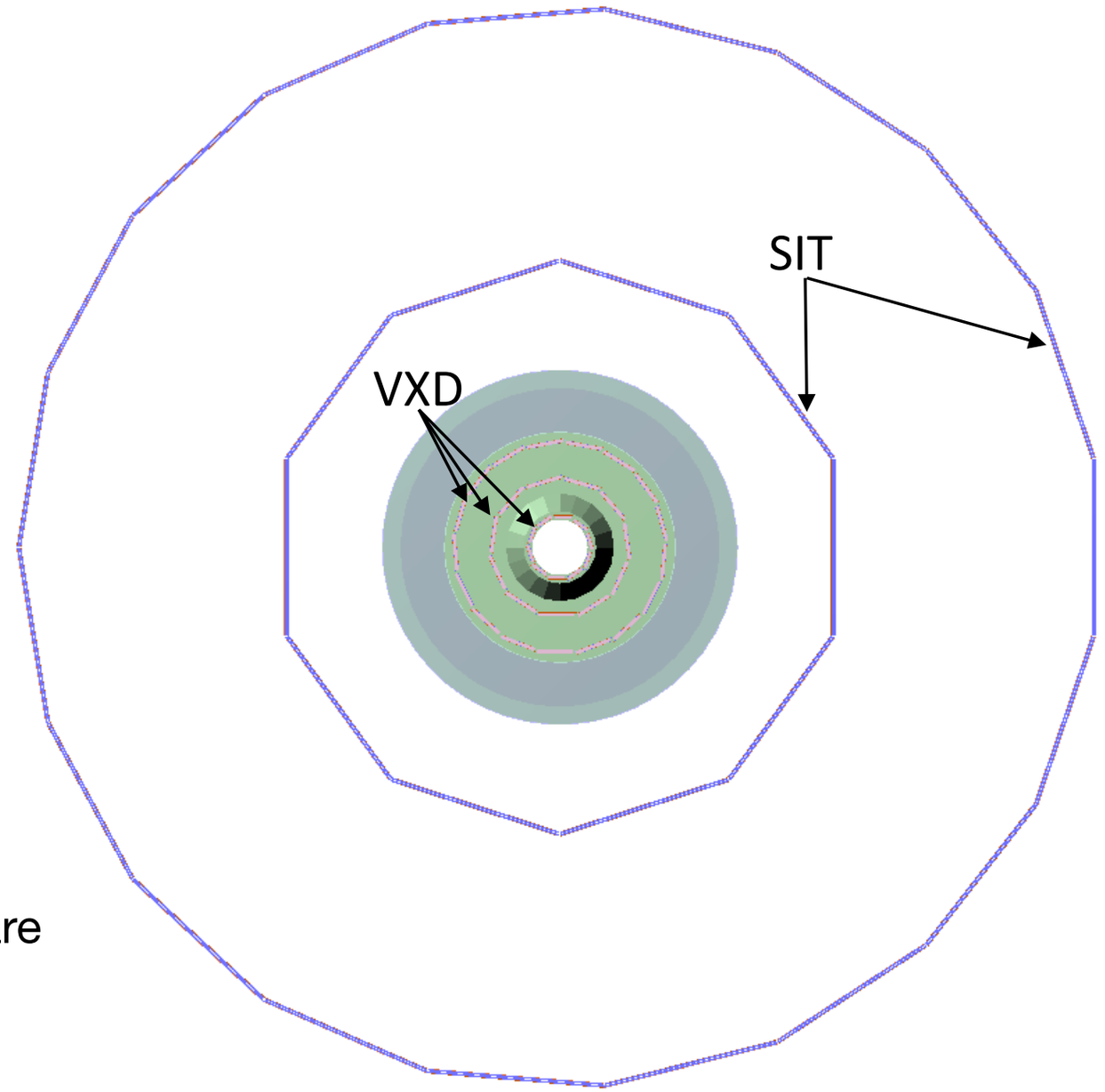
- 3-5 μm resolution
- 1 MRad total ionization

What are we building?

Current Silicon Layout in CEPC Simulation/CDR

double-layer SET with 24 ladders
at radius of 1.811 meters

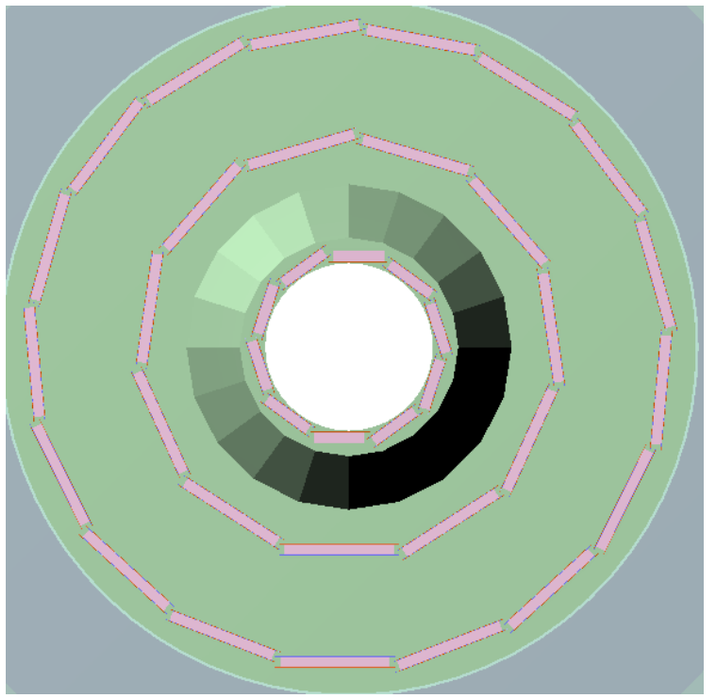




- Currently in simulation we have:
  - Vertex detector, SIT, TPC and **SET** at barrel, and FTD at endcap.
  - Vertex detector, SIT and **SET**, ladder structures are included
  - But ETD has not been included

What are we building?

Current Silicon Layout in CEPC Simulation/CDR



	$R(mm)$	$\|z\|(mm)$	$\|cos\theta\|$	$\sigma(\mu m)$	$Readout\ time(us)$
Layer 1	16	62.5	0.97	2.8	20
Layer 2	18	62.5	0.96	6	1-10
Layer 3	37	125.0	0.96	4	20
Layer 4	39	125.0	0.95	4	20
Layer 5	58	125.0	0.91	4	20
Layer 6	60	125.0	0.90	4	20

Table 4.1: Vertex detector parameters

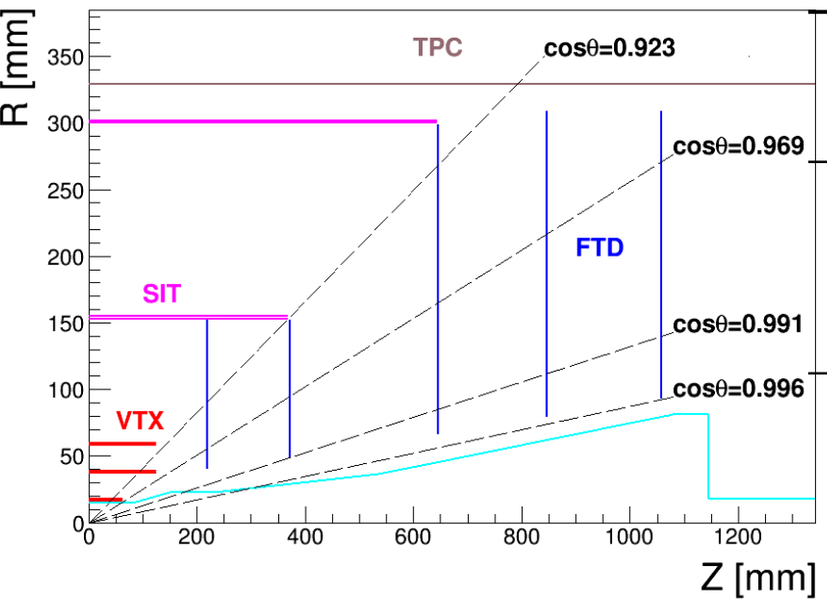


Table 5.2: Main parameters of the CEPC silicon tracker.

Detector		Geometric dimensions			Material budget $[X/X_0]$
SIT	Layer 1:	$r = 153$ mm,		$z = 371.3$ mm	0.65%
	Layer 2:	$r = 300$ mm,		$z = 664.9$ mm	0.65%
SET	Layer 3:	$r = 1811$ mm,		$z = 2350$ mm	0.65%
FTD	Disk 1:	$r_{in} = 39$ mm,	$r_{out} = 151.9$ mm,	$z = 220$ mm	0.50%
	Disk 2:	$r_{in} = 49.6$ mm,	$r_{out} = 151.9$ mm,	$z = 371.3$ mm	0.50%
	Disk 3:	$r_{in} = 70.1$ mm,	$r_{out} = 298.9$ mm,	$z = 644.9$ mm	0.65%
	Disk 4:	$r_{in} = 79.3$ mm,	$r_{out} = 309$ mm,	$z = 846$ mm	0.65%
	Disk 5:	$r_{in} = 92.7$ mm,	$r_{out} = 309$ mm,	$z = 1057.5$ mm	0.65%
ETD	Disk:	$r_{in} = 419.3$ mm,	$r_{out} = 1822.7$ mm,	$z = 2420$ mm	0.65%

What are we building?

Silicon Inner Tracker Vertex Detector Prototype

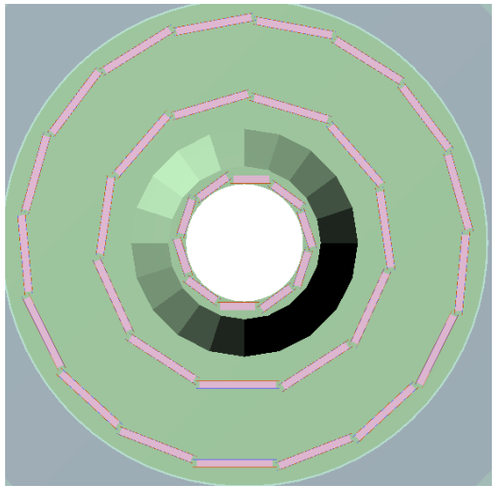


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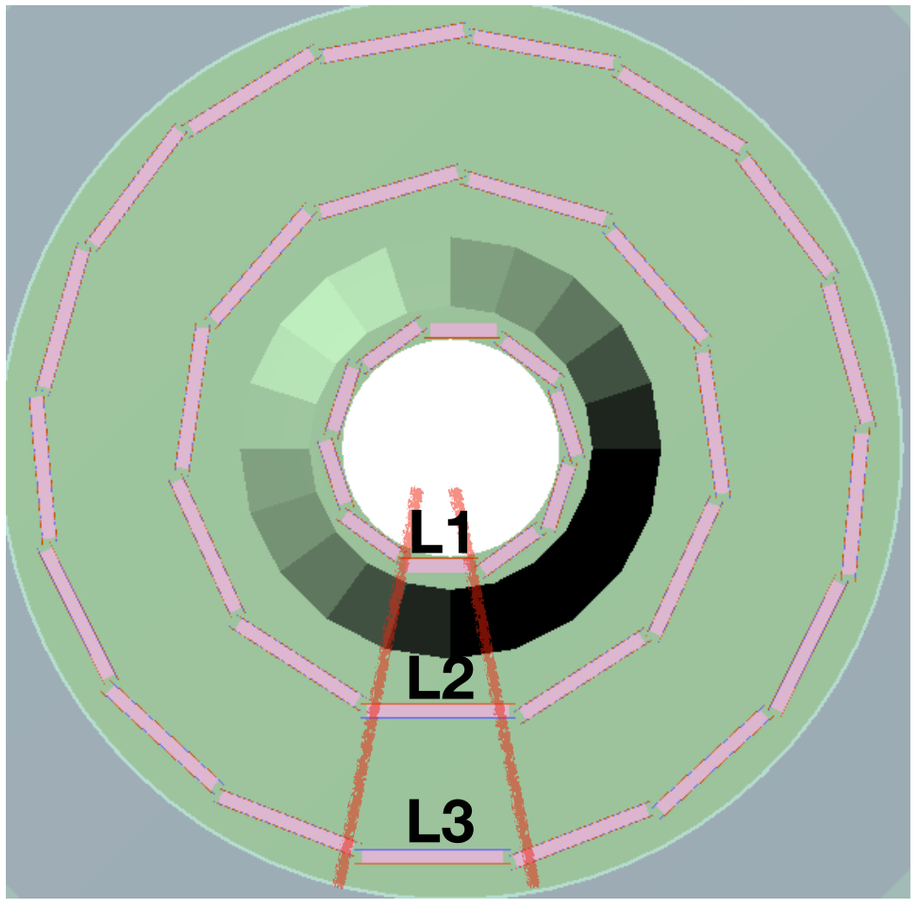
Table 4.1: Vertex detector parameters

3-layer sector



Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

L1

L2

L3

3-layers
same size
same chip

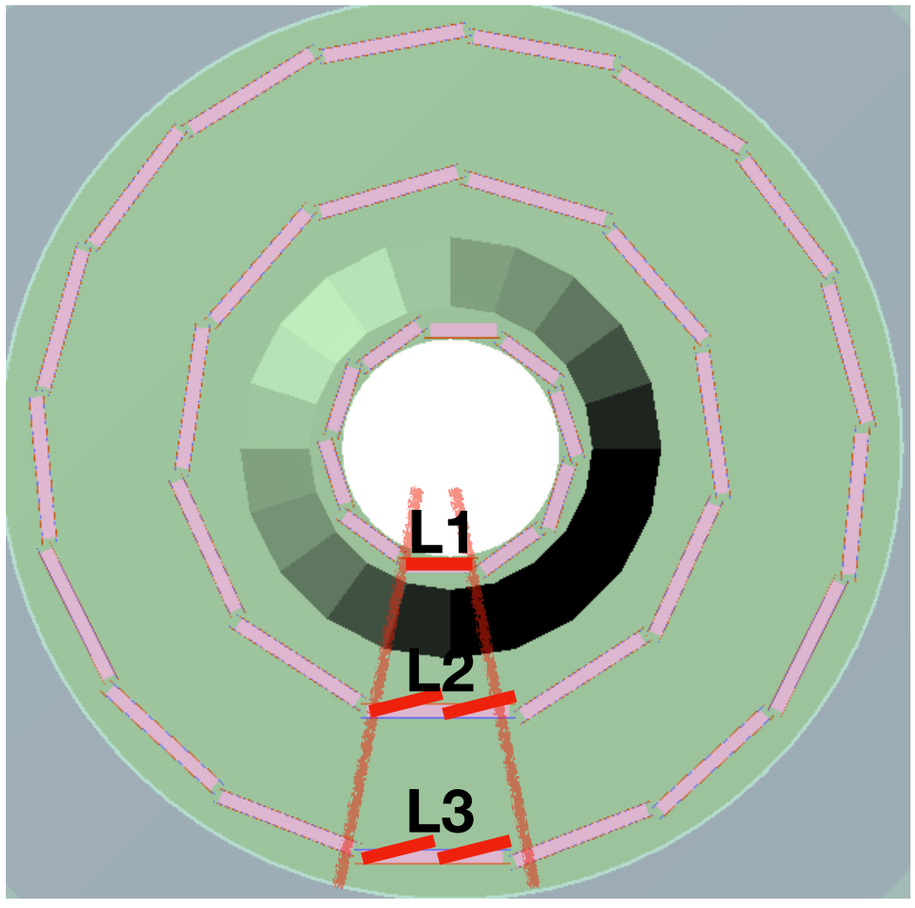
What are we building?

Silicon Inner Tracker Vertex Detector Prototype

Extended goals if manpower and technical knowledge available
Get closer to a real detector prototype

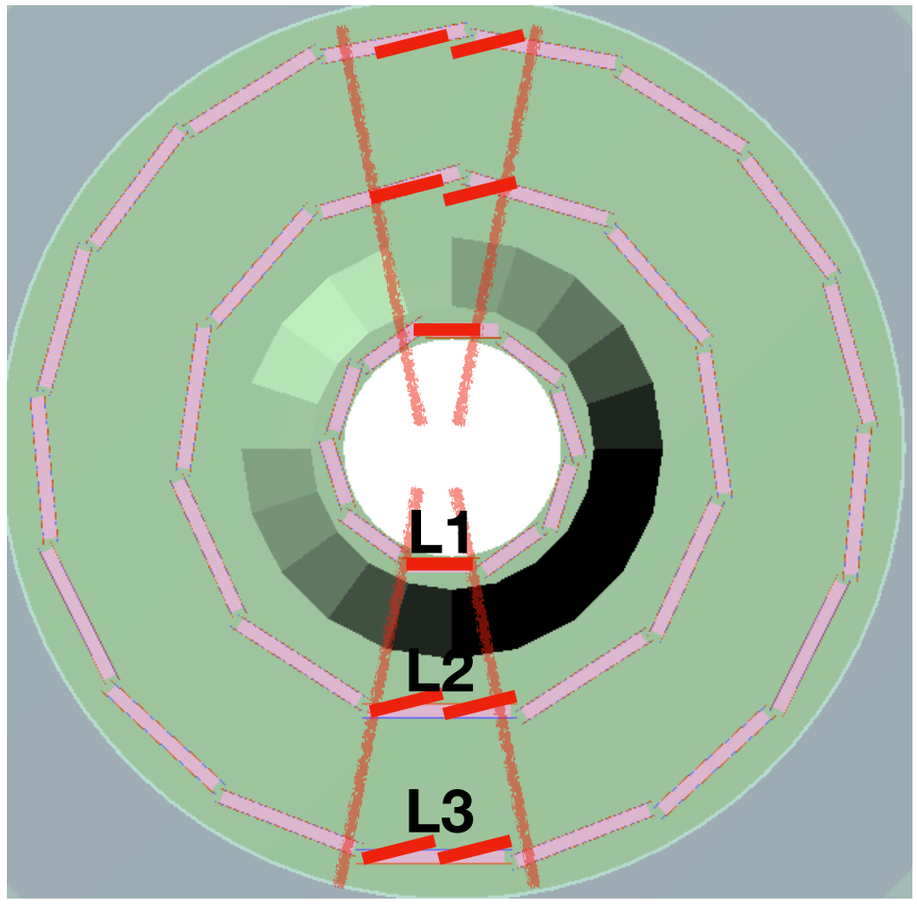
3-layer sector
with multiple ladders per layer

Requires study/simulation of new layout



Full mechanical prototype
with subset of ladders instrumented/readout

Requires study/simulation of new layout



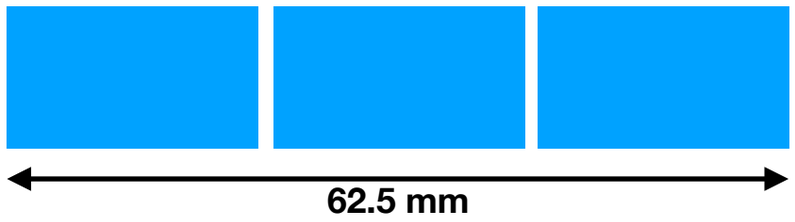
Chips size and number

Layer 1 (11 mm x 62.5 mm)

Chip size: 11 mm X 20.8 mm

Chip Number: 3 X 2 layer = 6 chips

Half barrel design

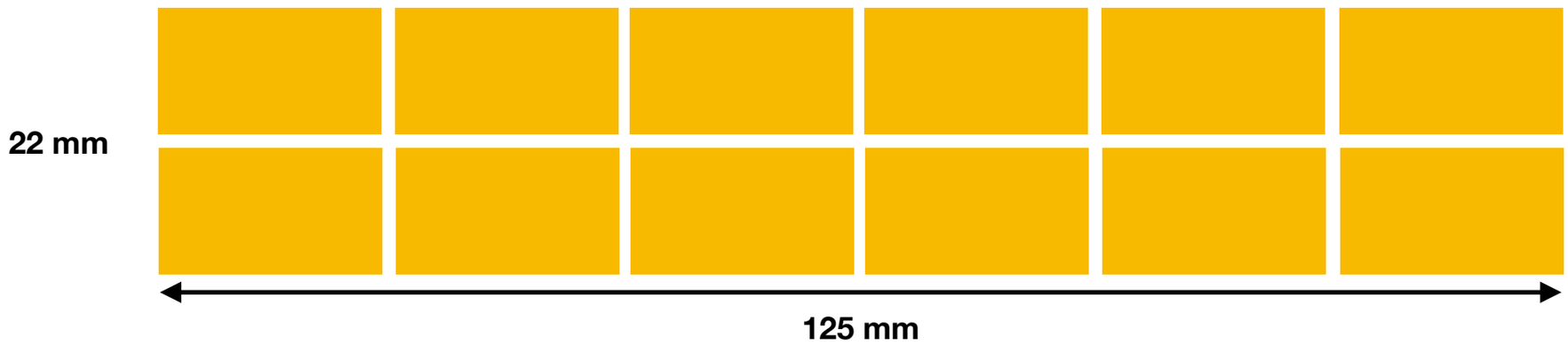


Double sided ladder

Layer 2 and Layer 3 (22mm x 125mm)

Chip size: 11 mm X 20.8 mm

Chip Number: 6 X 2 rows X 2 layer = 24 chips



Double sided ladder

Total number of chips = 6 + 2 * 24 = 54 chips/wedge for 3 layers prototype

Project outline: Task 3

- Sensor design to reach single-point **3-5 micron spatial resolution, 1 MRad TID**
  - On-sensor design of readout circuitry (CMOS) with low-power consumption, 50 mW/cm^2
  - Testing of sensor/chip prototypes on bench tests/source tests and test beams
- Realistic layout of full pixel (silicon tracker?) taking into account low-material budget
- Design and construction of double-sided silicon ladder with CMOS chips
- Final test beam to demonstrate full prototype
  - Assemble series of ladders or sensors at correct distances —> Need to decide on number of layers
  - Design full readout electronics for ladders/system

List of tasks (1)

- Sensor
  - Single pixel geometry layout (n-well size …)
  - Amplifier design
  - Charge injection calibration loop
  - Readout architecture
    - Readout clock design
    - Pixel array address encoding design
  - LVS and DRC design
  - Test structure design (passive pixel, standalone amplifier , pMOS..)
  - Global layout
  - TCAD simulation on sensor performance and irradiation hardness
  - Sensor Irradiation
  - Testing
    - I-V ,C-V and inter-pixel capacitance
    - Fe-55 source tests (to verify signal-to-noise)
    - Laser charge injection tests

List of tasks (2)

- Ladder
  - Design Single-chip Readout board for MPW runs
  - Design ladders for multi-chips readout
  - Mechanical design for ladder core support structure and alignment
  - Electronic design for ladder
  - DAQ for ladder
  - Cooling design for the ladder, if needed
- Tracker Prototype
  - Mechanical design for framework holding three layer
  - Alignments between ladders
  - Multi-channels power supply crate
  - Multi-channel readout crate
- Testbeam
  - Design on beam type and beam test location
  - Mechanical setup up the beam test (equipment, reservation of beam time)
  - Alignment with telescope
  - DAQ and synchronize with triggers and telescope
  - Data taking and Data analysis

Schedule

	Layout	Chip/Sensor	Readout	Prototype
Year 1	– Define detector/ladder layout and chip size	– Determine process for chip design and chip size – Expand chip schematics to full size pixel – MPW 1	– Development of readout motherboard for MPW1 – Secure DAQ system for single chip – Start ladder electronics and readout syst. design	– Mechanical and electrical construction of small first prototype ladder
Year 2	– Optimize ladder layout – Mechanical design of support structure	– MPWs 2 and 3	– Development of readout motherboard for MPWs – Design DAQ system for ladder readout	– Optimization of ladder assembly procedure with dummy chips
Year 3	– Finalize ladder mechanics	– 1st engineering run	– Complete DAQ system for ladder readout; Test it – Develop DAQ system for full prototype readout	– Production of ladder with first engineering run chips
Year 4	– Finalize full prototype mechanical structure	– 2nd engineering run by middle year	– Full readout of single ladder achieved – Complete and test DAQ system for full prototype readout	– Production of final ladders – Testing of ladders – Full readout of single ladder achieved
Year 5		– Production chip/sensor testing	– Full readout of ladder with final chips achieved – Full readout of all prototype achieved – Test beam	– Finish mechanical assembly of full prototype – Test beam – Results

Manpower (incomplete)

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International Collaboration

- Barcelona (Sebastian Grinstein)
  - Experience in HV CMOS pixel design, 3D pixel design
  - 1 professor, 1 chinese student, 1 engineer?
- University of Liverpool (Yanyan) — CMOS design?, ladder design
- Oxford University (Tony Weidberg, Ian Shipsey, Daniella) — ladder, mechanics
- Rutherford Labs — could help with many aspects
- Strasbourg (Marc Winter) — CMOS design (TowerJazz)
- Marseille University (Marlon Barbero, Patrick Pangaud)
- University of Geneva (Peppe) — CMOS design?
- DESY (Marcel Stanitzki) — test beam

Open/Critical Items

- Sensor technology to use?
  - Should try to keep project relevant 5-year from now, but also realistic!
  - Follow MOST1?
  - TowerJazz **180**/130/(115) nm, HVCMOS 130/**65** nm
  - Attempt production in China?
  - Attempt to reach true CEPC design goals on power consumption, material budget (thin sensor)

- Size of CMOS chip

- Size of ladder for layers 2 and 3
  - Most likely we will not define the size in the MOST application

- Readout electronics
  - Chip testing level
  - Full ladder and prototype level

- Schedule extremely tight

Current budget: 18.8 MRMB (see Zhijun's talk)

PROPOSAL:
Key scientific problems, key technologies and research targets to be solved

2. 研发满足 CEPC 的物理要求的高精度径迹探测的硅像素技术。研制空间分辨达 $3-5\,\mu m$、总电离辐照剂量为 1Mrad 的强抗辐照的硅像素传感器。研发硅径迹探测器样机，重点研究高速读出电子学和探测器模块支撑结构，建造大面积的硅径迹探测器样机，并通过束流实验验证其空间分辨力达到要求。

Develop the silicon pixel technology for high-precision tracking detection which meets the requirement of CEPC. Design the large area silicon sensor with high spatial resolution of 3-5 \mum and high radiation resistance with the total ionizing radiation of 1 MRad. Research and produce the silicon tracker prototype. Produce a silicon tracker prototype, the high speed readout electronics and the support structure of detector module are the key research points. Then verify the spatial resolution of the silicon tracker prototype through the test beam results.

PROPOSAL:
Project research content, research methods and technical routes

本课题研发重点在于硅像素传感器芯片、探测器模块电子学以及硅径迹探测器原型的集成。探测器样机包含了由多层硅像素传感器和高速读出电子学构成的探测器模块，力学支撑结构及数据获取系统。研究方案如下：设计大面积高分辨的单片式硅像素传感器，研究前端电子学与传感器芯片的集成；调整传感器与前端电子学的结构，设计抗总电离剂量为1MRad 的抗辐照传感器；研究探测器模块的高精度组装方式，通过调整读出架构优化模块电子学设计，提高读出带宽；设计并生产用于模块与径迹探测器样机的轻型坚固支撑结构，以满足高能环形加速器对低质量材料的物理要求。联合国内外团队研制硅径迹探测器样机，通过束流试验验证主要设计目标，空间分辨精度达到$3-5\ \mu m$的设计要求。

PROPOSAL:
Project research content, research methods and technical routes

The key R&D point is on the chips, electronic and the integration of prototype. Silicon tracker prototype includes the multi-layer silicon tracker modules which consist of several pixel sensor chips and high speed readout electronic, mechanic support structure and DAQ system. The research plan is listed below: Design the silicon sensor with large area and high resolution, and develop the integration of front-end electronic on sensor chip; By optimizing the design of frontend electronics and sensors, we will design a sensor which can tolerate 1 Mrad total radiation dose; R & D on the assembly technique of the detector module, by optimizing the electronic architecture and the electronics readout design, we will increase the bandwidth of data readout in the module; Design and produce light and rigid support structures for the multi-layer silicon tracker prototype, satisfying the physics requirements of the CEPC; We will cooperate with both domestic and international teams to research and produce a multi-layer silicon tracker prototype. The major design parameters will be verified through test beam results, spatial resolution reach the requirement of 3-5 \mum .

PROPOSAL:
Innovations

所研发的硅径迹探测器样机具有国际先进水平。创新设计大面积多通道硅传感器；通过计算机模拟芯片辐照后性能，优化传感器工艺参数与几何结构，设计具有超高的空间分辨率（$3-5\,\mu m$）和抗辐照性能的传感器；通过自主研制的读出架构和电路实现数据高速读出和低能耗；设计轻型坚固支撑结构。

The silicon tracker prototype we develop will reach the international advanced level. Novel design of large area, multichannel silicon sensor; Use computer program to simulation radiation hardness, and Optimize the design and geometry of the sensor, and then design a sensor with high spatial resolution ($3-5\,\mu m$) and high radiation resistance performance; New readout circuit architecture design to accommodate the large number of pixels with high-transmission rate and low power consumption; Design Light material support structure.

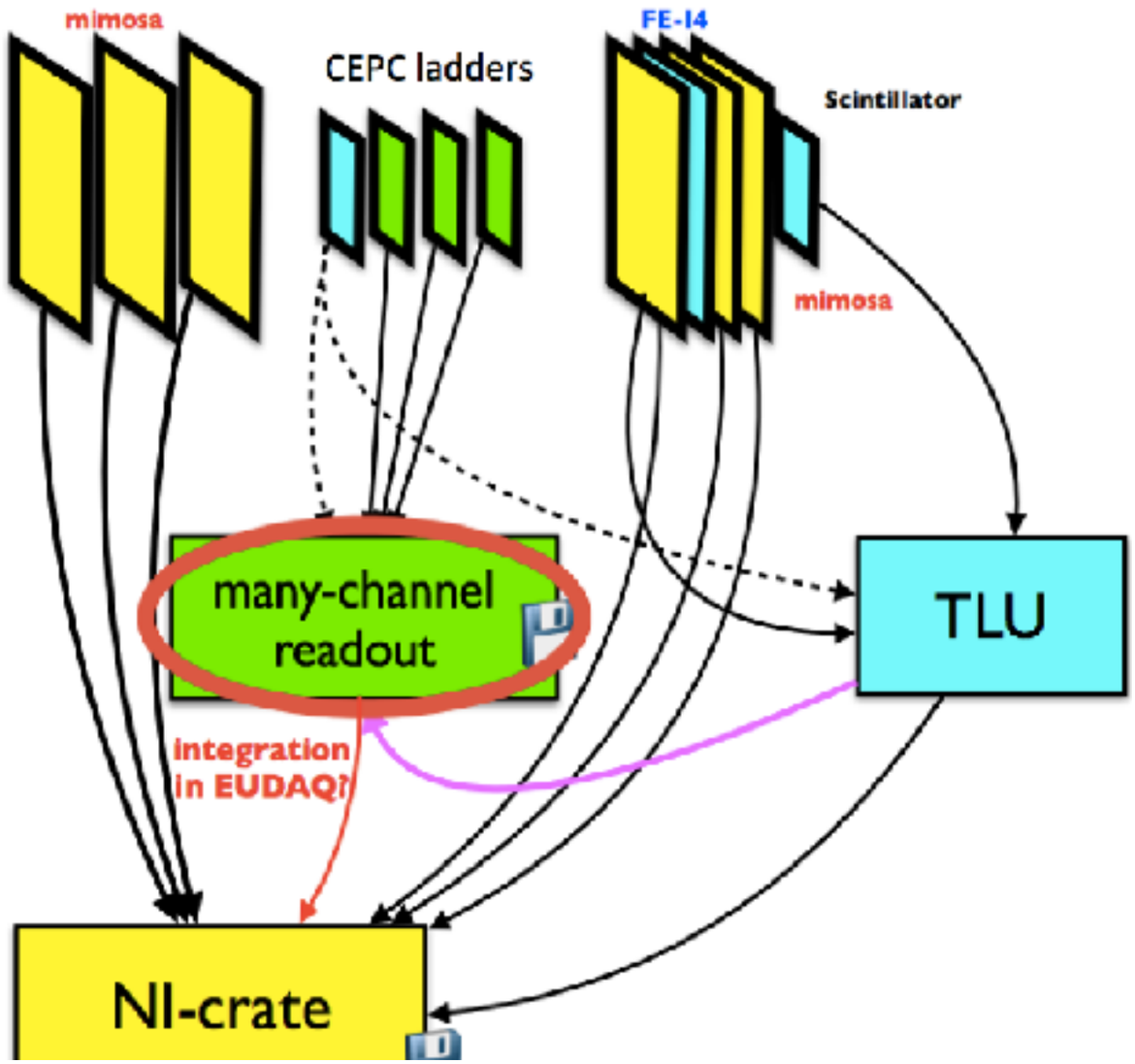
Backup

Overall design possibilities

- Wafer 6” should give 25 chips 2x2 cm^2. Assume 80% yield.
- Layer 1: 62.5 mm — double layer
  - Chips: 2 layers x (1.1 cm x 2.08cm) X 3 chips = 6 chips/ladder
  - Build two ladders = 16 chips
  - Prototype:
    - layer 1 = 2 ladders; layer 2 = 2 chips; layer 3: 2 chips (20 chips)
    - layer 1 = 1 ladder; layer 2 = 1 ladder; layer 3 = 1 ladder (24 chips)
- Layer 2: 125 mm — double layer (make 120 mm)
  - Chips: 2 layers x 2 cm x 6 chips = 12 chips/ladder
  - Prototype:
    - layer 1 = 1 short ladder; layer 2 = 1 long ladder; layer 3 = 1 long ladder (32 chips)
    - (need two wafers)

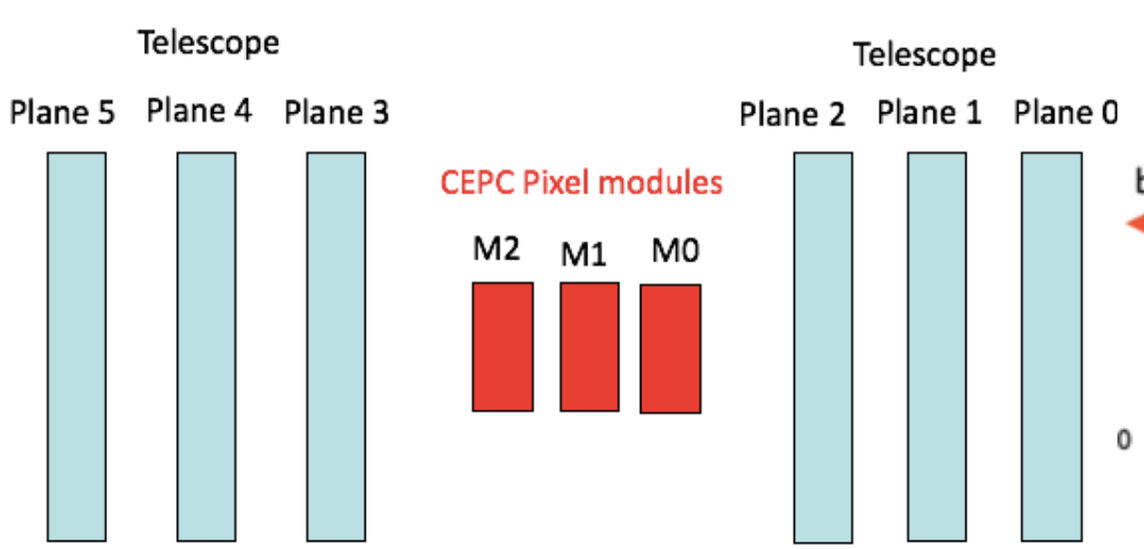
Test beam setup

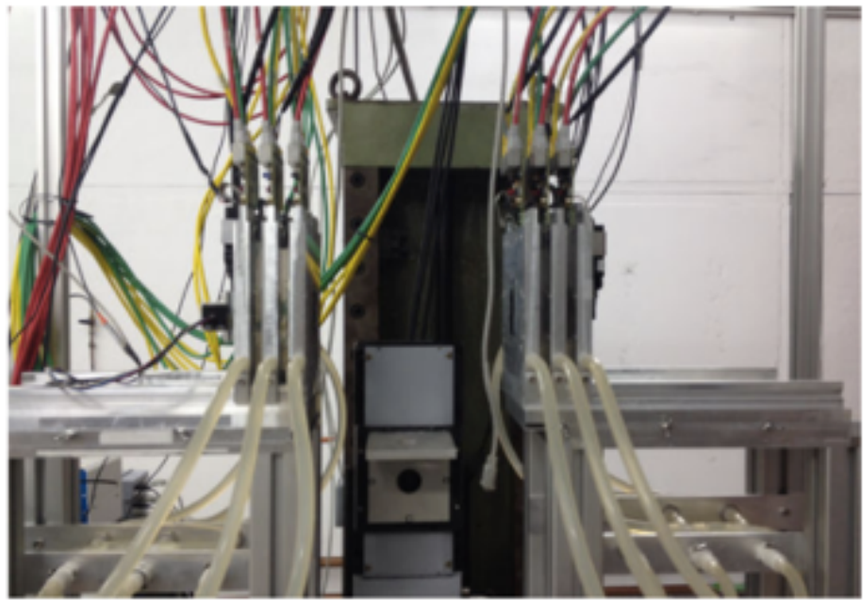
- CERN H6 beam line , 180 GeV pion beam
  - Expected beam rate : 10kHz
  - Expected beam time: one week
- EUDAQ-Mimosa telescope.
  - added one FEI4-IBL pixel layer for trigger, if we need more than 8kHz
  - Resolution of this telescope is less than 5um



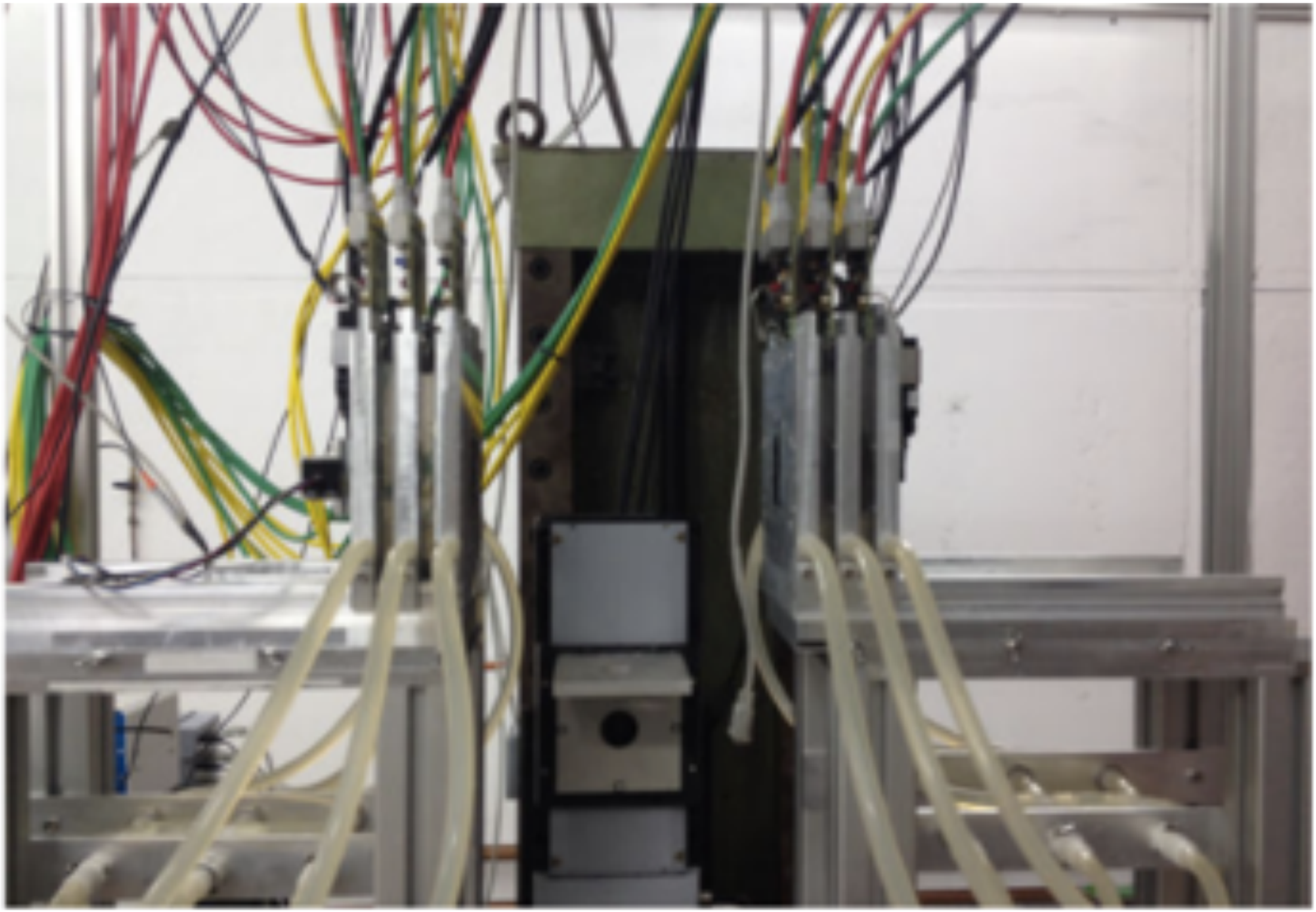
Test beam setup

- the weight of the DUT: It is 8 kg in total, thus, minus 0.6 kg if using the angle and minus 0.94 kg if using the rotation stage.
- the spacing between the upstream and downstream telescope plane is in maximum ~0.5 m (Z direction)
- The active area in X-Y plane is about “1cm X 1cm”.





Test beam setup



Schedule Discussion

- 2018.7-2019.6:
  - design the CMOS sensor geometry and readout architecture for large sensor.
  - submit MPW runs
- 2019.7 - 2019.6:
  - design and implement the DAQ setup for single sensor testing.
  - Testing performance of the sensor after irradiation
  - Refine the CMOS chip design
- 2019.7-2020.6:
  - Finalize the design of full-size sensor, do engineering run submission.
  - design the ladder electronics and mechanical structure.
- 2020.7-2021.6:
  - Integrate the CMOS sensor chip into ladders.
  - Commissioning the ladders
  - 1st Test beam at CERN to verify the ladders performance
- 2021.7-2022.6
  - Manufacture 3 ladders, and integrate them into one tracker prototype
  - 2nd Test beam at CERN to verify the tracker prototype performance

Manpower (incomplete)

Name	*personnal certification*	*Ranking*	*institute*	*email address*	*task*	*load*
Joao Guimaraes da Costa	project leader	Professor	IHEP	guimaraes@ihep.ac.cn		
Zhijun Liang	Key member	Assoc. Professor	IHEP	liangzj@ihep.ac.cn	Ladder construction/Testing	
Gang Li	Key member	Assoc. Professor	IHEP	ligang@ihep.ac.cn	Detector Simulation	
Chengdong Fu	Key member	Assoc. Professor	IHEP	fucd@ihep.ac.cn	Detector Simulation Layout	
Mei Zhao	Key member	Assoc. Professor	IHEP	zhaomei@ihep.ac.cn	Sensor and chip design	
Wei Wei	Key member	Assoc. Professor	IHEP	weiw@ihep.ac.cn	Chip design	
Ying Zhang	Key member	Assoc. Professor	IHEP	zhangying83@ihep.ac.cn	Chip design	
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LIU Qingyuan		PhD student	SDU	liuqy@hepg.sdu.edu.cn	detector simulation	
LI Long		PhD student	SDU	lilong@hepg.sdu.edu.cn		
Ming Qi	Key member	Professor	NJU	qming@nju.edu.cn		

Task List from Wang Meng

- Sensor simulation (SDU) - postdoc
- Chip design and tapeout (SDU) - Zhang
- Chip test (probing, electronic, radiation, …) (SDU) -Zhang
- Chip test electronics (SDU) - Jianing
- Ladder/prototype simulation and optimisation (SDU) - student
- Ladder/prototype mechanical design
- Ladder/prototype assembly (SDU)
- Ladder/prototype lab test (SDU)
- Ladder readout electronics (SDU) - Jianing
- Alignment
- DAQ (ladder + prototype)
- Beam test (chip, ladder, prototype) (SDU)
- Irradiation test (SDU)
- Data analysis (SDU)