CEPC 环形正负电子对撞机 Circular Electron Positron Collider

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Status of readout electronic design in MOST1

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On behalf of the Trigger Group (IHEP)

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Outline

- Introduction on readout electronics in MOST1
- R&D activities
  - -Data acquisition with oscilloscope
  - -Data acquisition with ADC
- Summary and future plan

R&D activities

- Two versions of daughter-board designed and fabricated
- Two versions of mother-board (1st designed and fabricated ,2nd in process)

– Single analog readout channel verified with oscilloscope and ADC sampling

– FPGA Firmware Design

– Digital controlling （IP is under packaged）

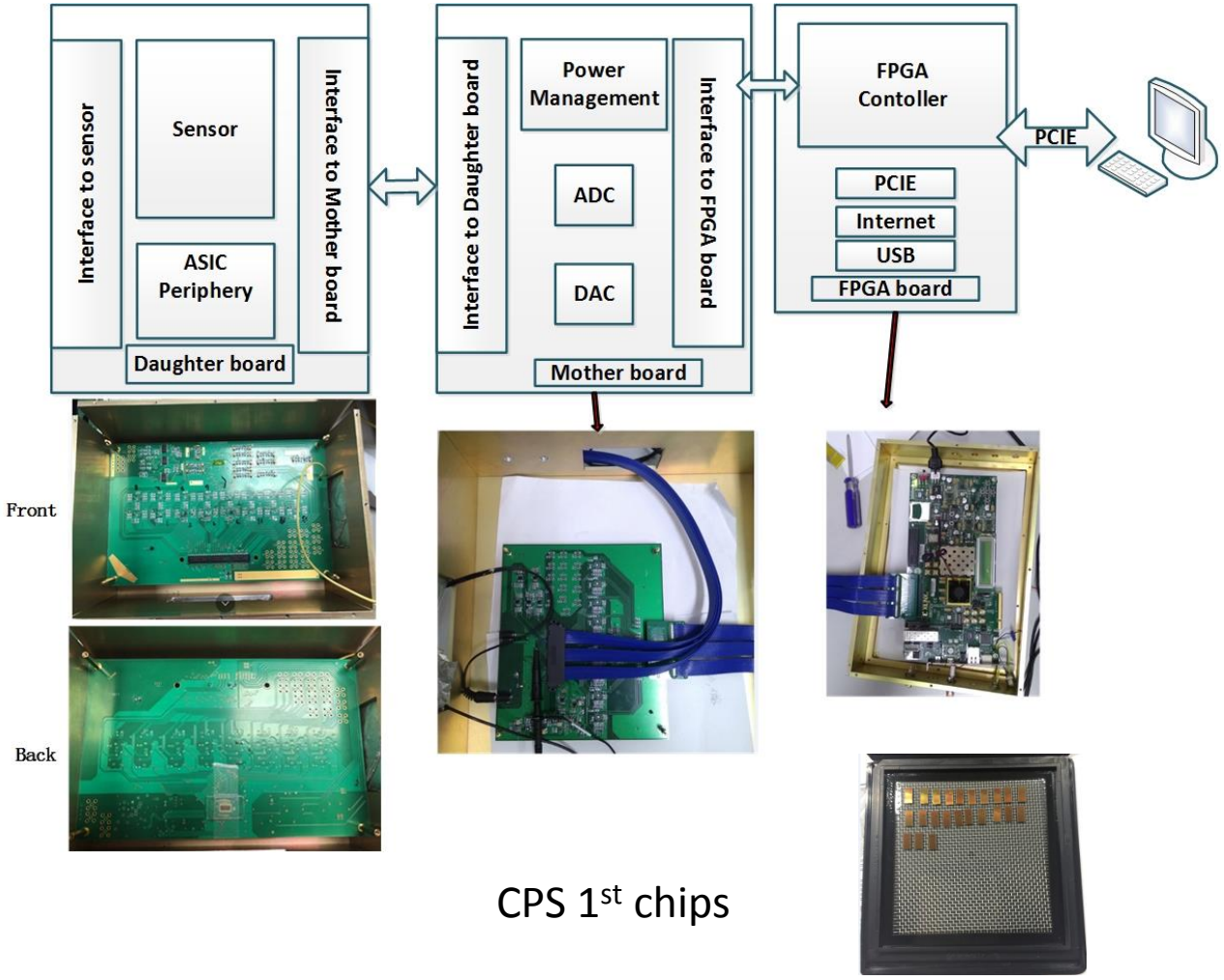
Introduction on the readout electronics

- Measurements of the prototype pixel devices
- To validate their usefulness for future application
- 1st CPS Prototype Characterization
  - ✓ Verification of basic electrical parameters
    estimation of the collected charge
    Noise, signal dynamic range
    response of the device to the light pulses
  - ✓ Tests using ^{55}Fe radioactive source

Daughter Board → Mother Board→ FPGA board

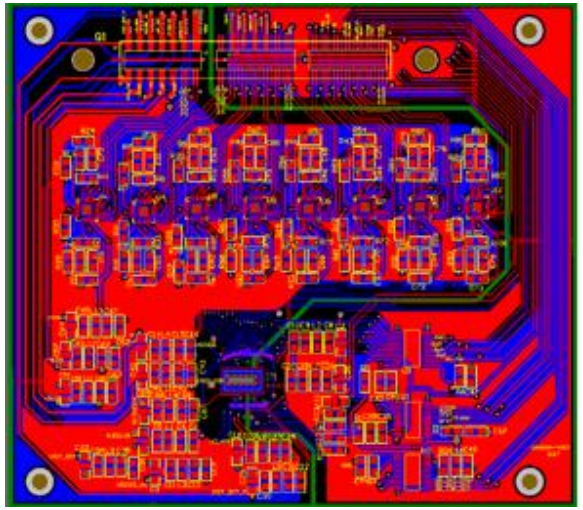
Mother Board ADC sampling.

16-bit ADC resolution

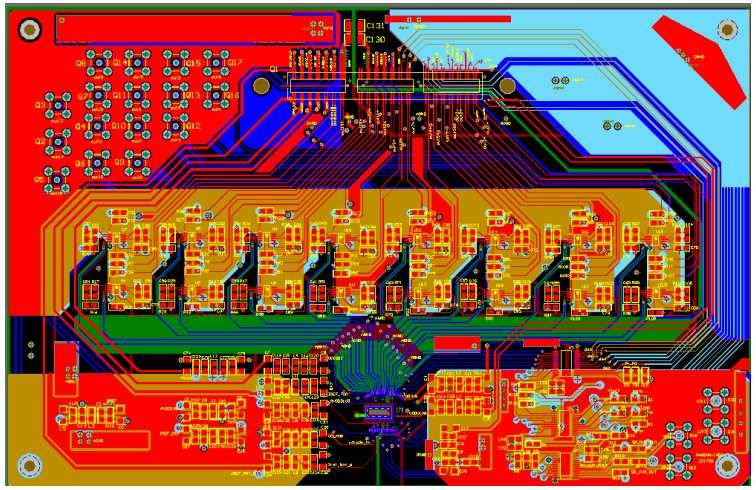


CPS 1st chips

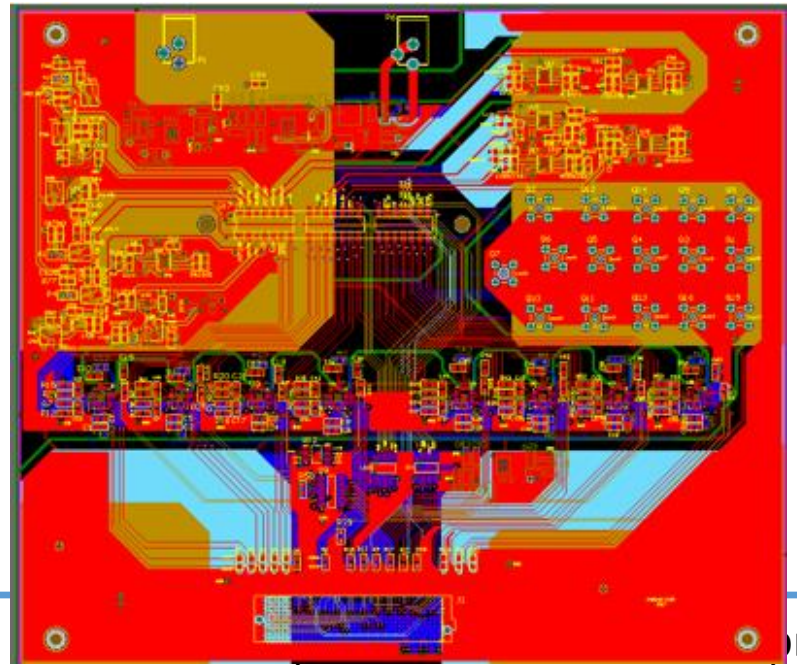
Two versions of daughter and mother board



Daughter board:1st to 2nd fabricated and tested



- Daughter →Mother board design.



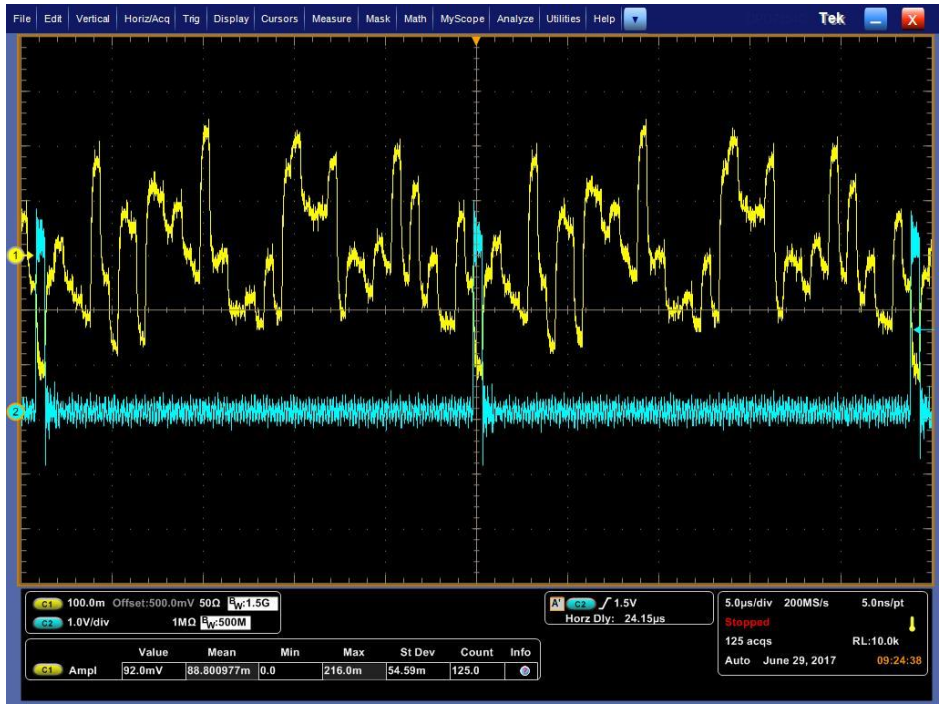
Mother board:
1st , fabricated and tested
2nd under designed

Interface to mother board：
- power supplies ,read-out clock
- address and other controlling signal
- read-back synchronization signal
- 16 pairs of differential analog and digital output

Interface to NI chassis：
- 16 analog output
- clocks and synchronization signals

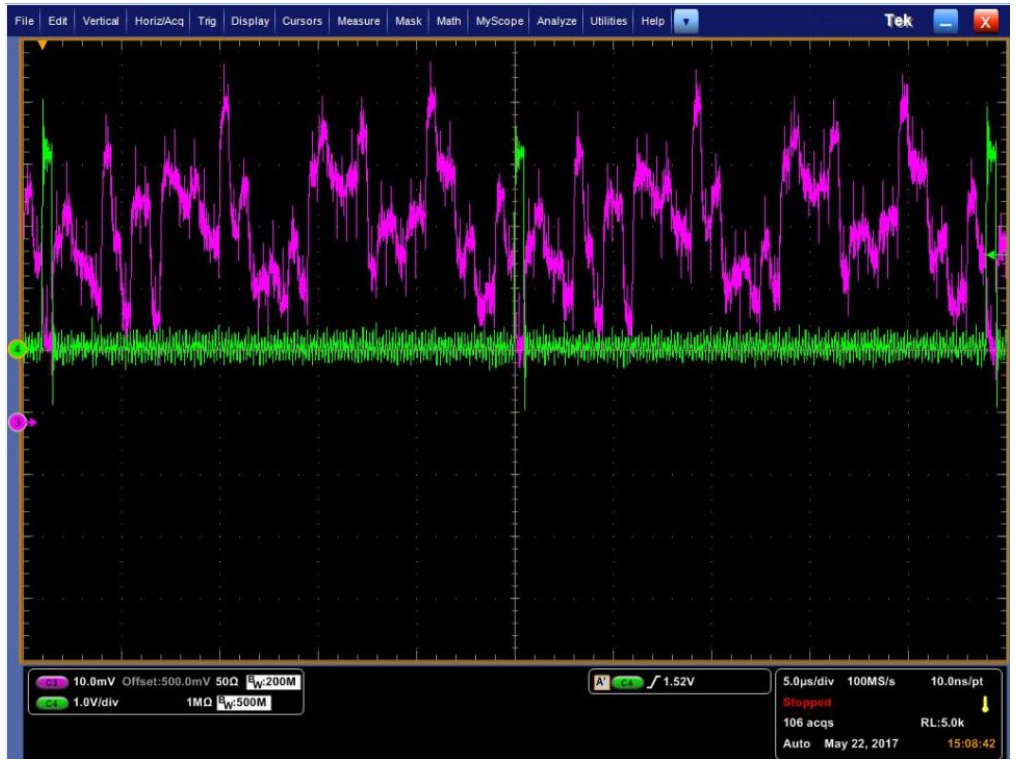
Signal dynamic range

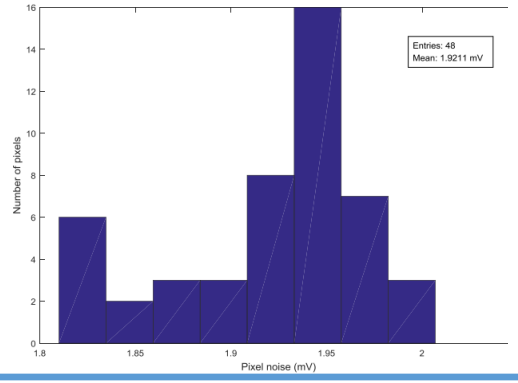
- Single input ,differential output
- Low noise amplification of the signal (multiplied by 3 ~10)
- Dynamic range(e.g. 50mV Vpp→500mV Vpp)

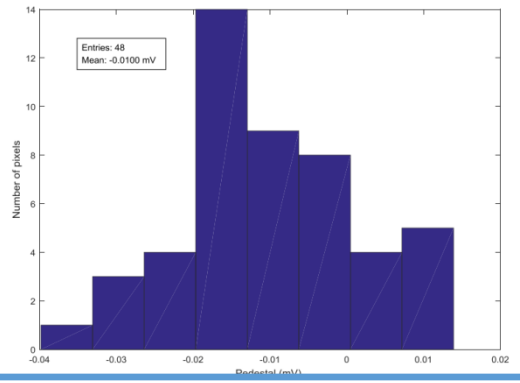


Data acquisition with oscilloscope

Data acquisition with oscilloscope







- Sensitive to visible light

data acquisition：

- Oscilloscope data acquisition and storage 2 frame/pic，2M clock
- 5000 point data

Data processing：

- Remove oscilloscope background noise
- Pixel output noise：

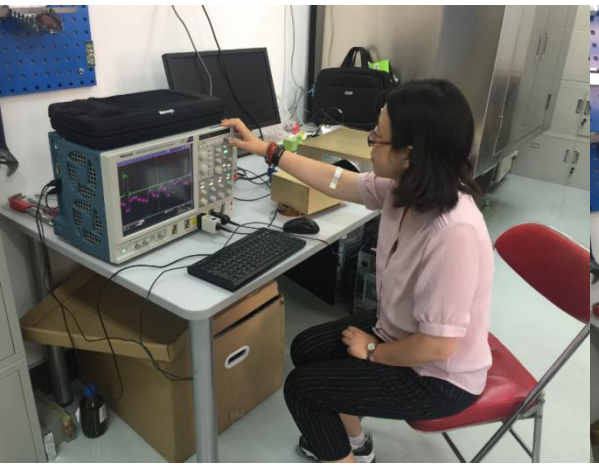
  1.6mV

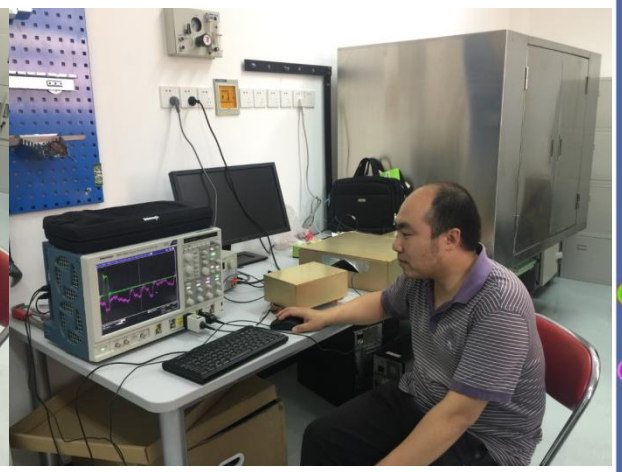
simulation pixel charge gain 20uV/e,

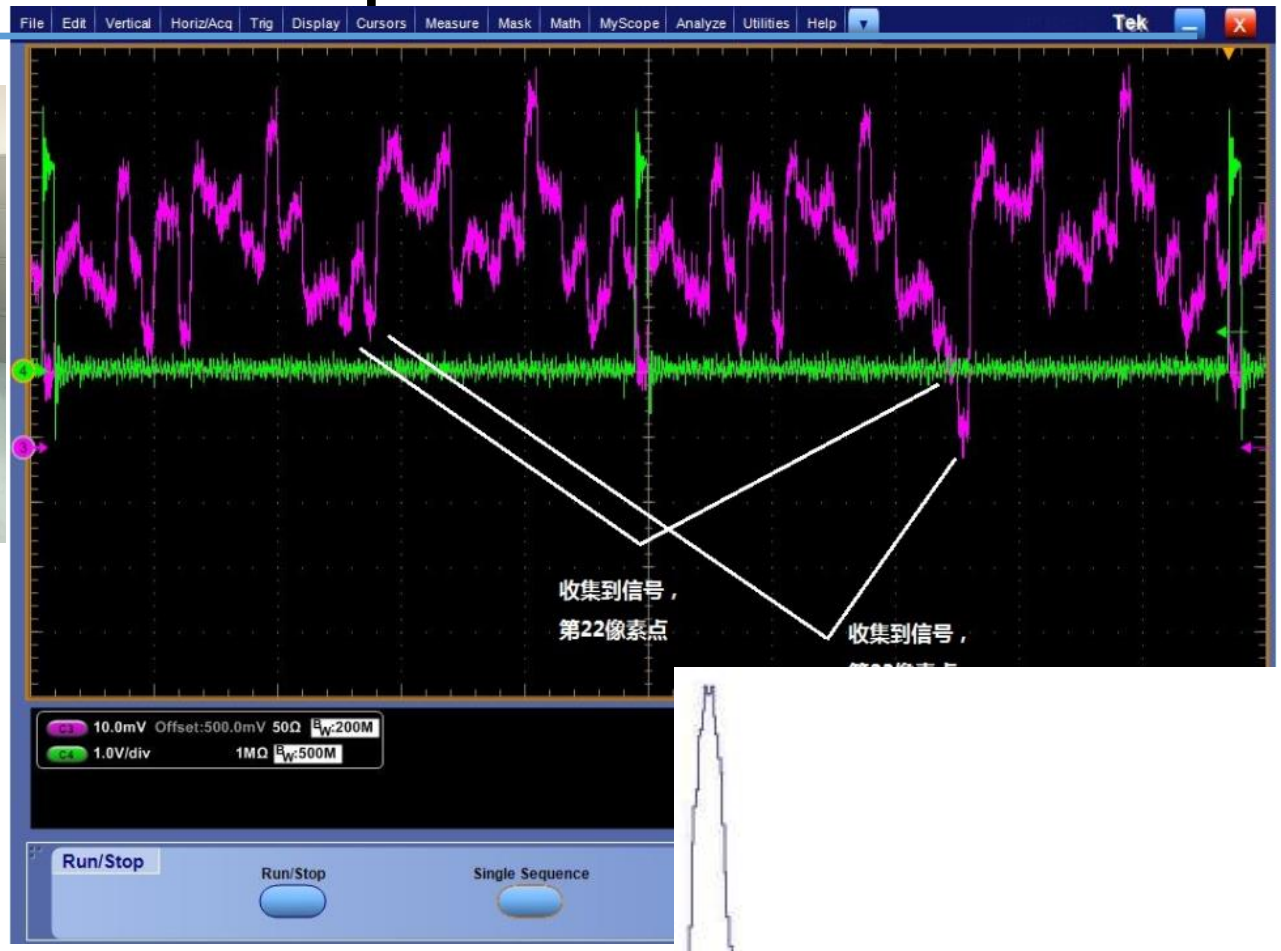
equivalent noise charge, ENC-- 80e –

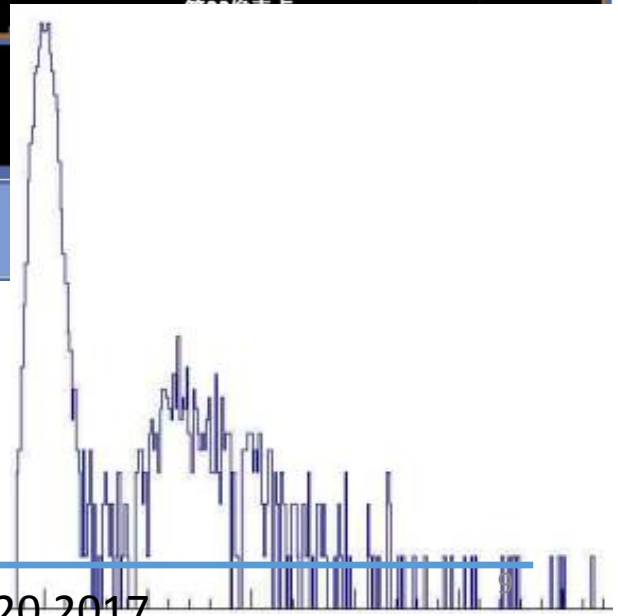
- 48 rows noise and background distribution

Data acquisition with oscilloscope









- ^{55}Fe Radioactive Source ：

  5.9 keV X-ray source

Observed signals :

  2M clock,2 frames/pic

- Multi event trigger mode selection,10G raw data for processing

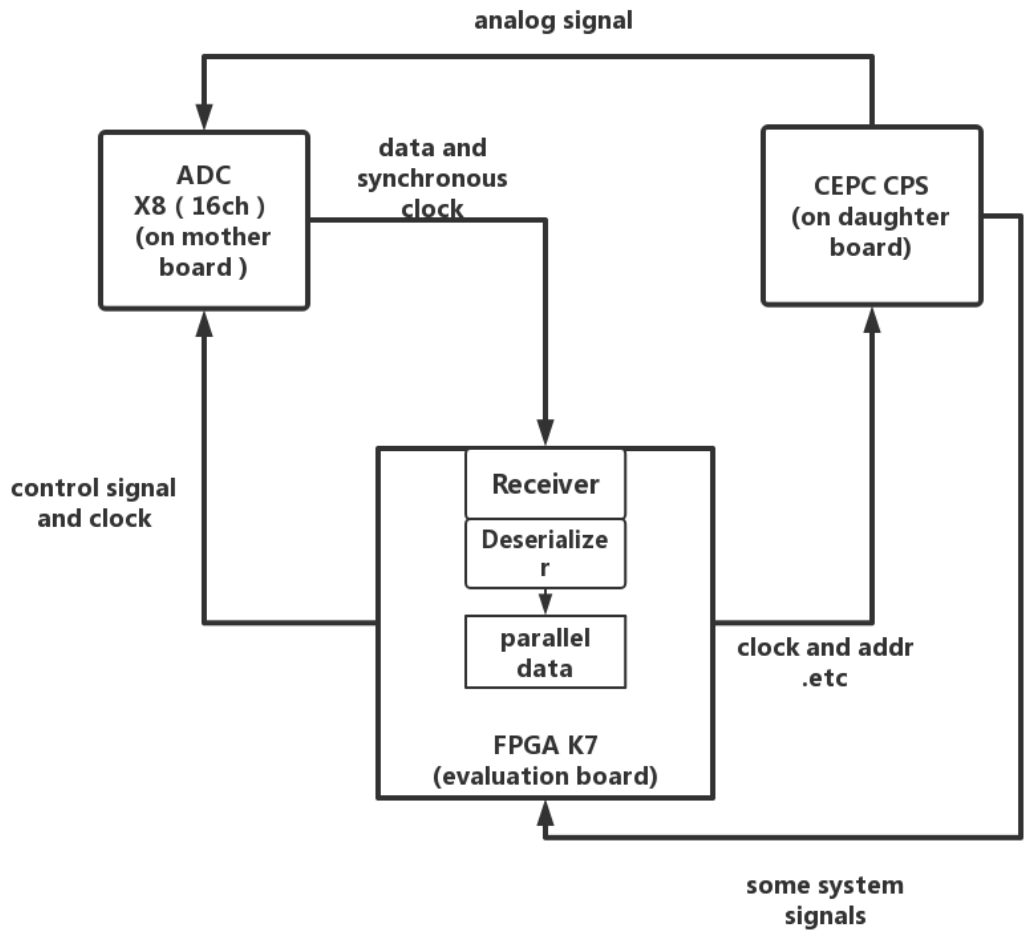
Data acquisition with ADC sampling

Digital controlling--FPGA firmware design

Digital controlling Block diagram
based on Xilinx KC705

- CEPC CPS control:
  -clock selection:2M,4M
  -address set :A0:A7

- ADC control
  - clock
  -enable
- ADC data read out
  -readout clock



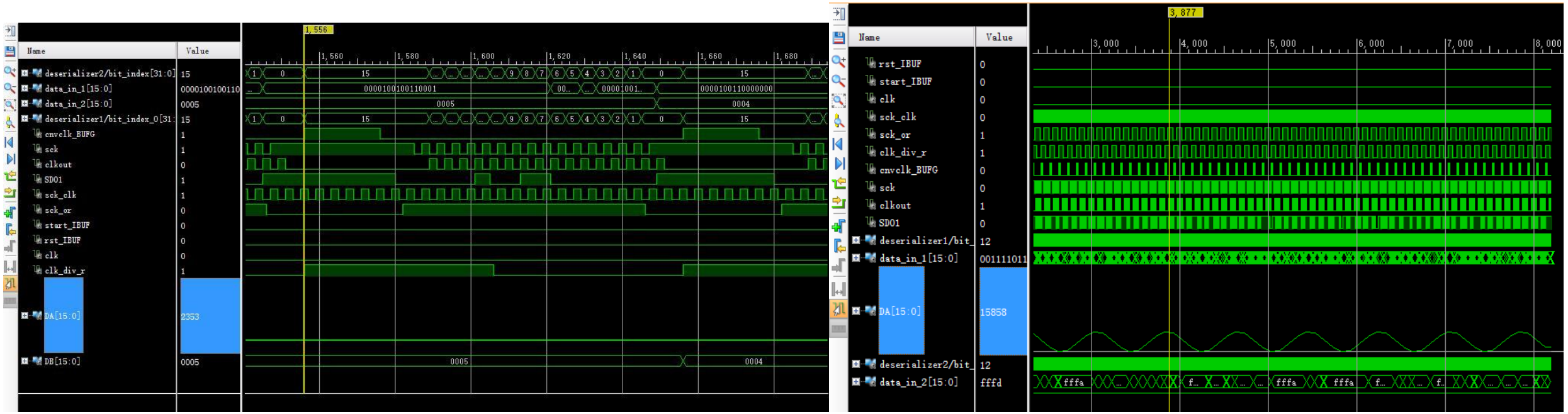
- Data pre-processing
  --Serial parallel conversion storage in local memory (in progress)

Digital controlling—ADC verification

ADC Characterization verifying

--ILA captured data 1.5VDC SDO is the same as the oscilloscope's waveform

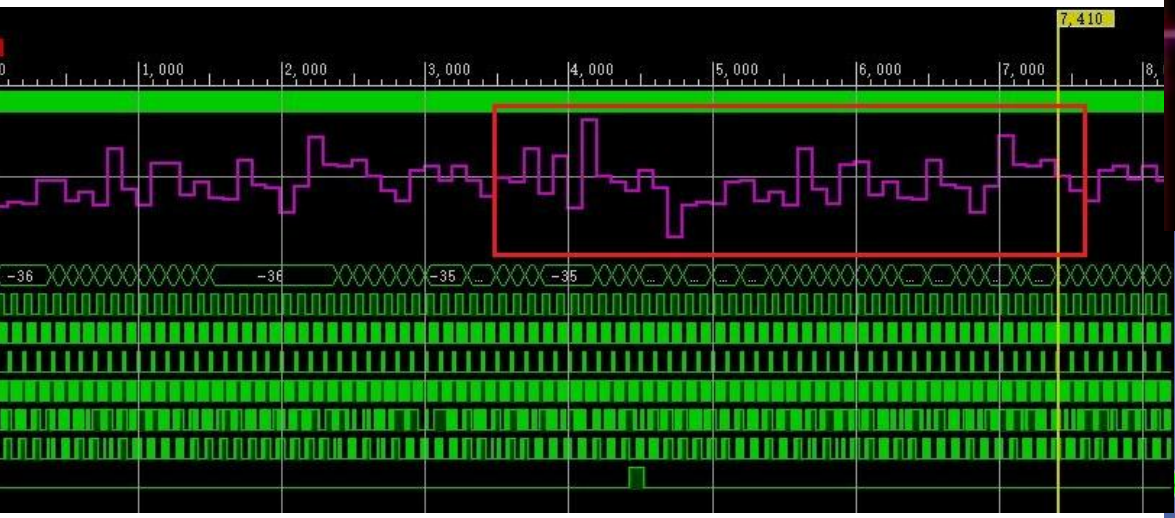
--ILA captured data 250KHz 4Vpp 2VDC offset Sine wave (signed decimal)



Data acquisition ADC sampling

VIVADO ILA captured data
(displayed in analog style)

One channel data read out



Oscilloscope captured
waveform

Summary and future plan

Accomplished：

- Read-out system for MOST-1 , single channel data aqquisition and transmission

  basic characteristic-signal dynamic range

  -noise performance

  -the digital controlling for chip and FPGA

  --single channel data CDS （48rows in one selected column）

Future plan：

- Read-out system:16 channel*16bit *clock data convention and transmission， storage in local memory

CEPC CPS1 prototype chip testing plan

1.Tests under Infrared Laser -- Time of Charge Collection

（time properties of charge collection , undepleted epitaxial layer ）

-- spatial resolution and detection efficiency

2. Tests with Soft X-rays （^{55} Fe source） -- Temporal noise and spatial non-uniformities in pixel responses

-- Charge Collection Efficiency and Cluster Signal Distribution

-- Soft X-ray spectroscopy

-- Charge Distribution

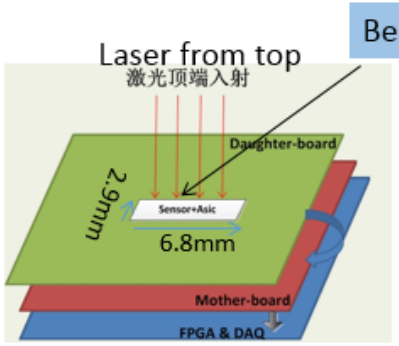
3.Radiation testing:

TID anti-radiation testing

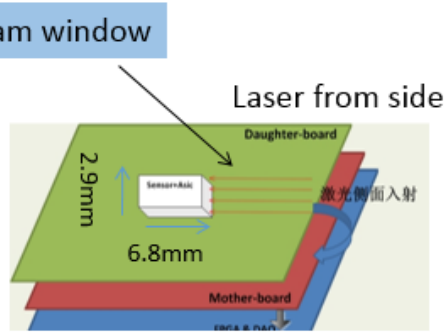
Single event effect

Displacement effect testing

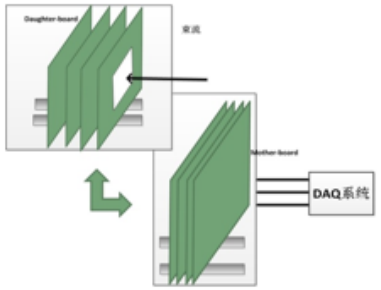
(Neutron irradiation)



1st step



2nd step



Beam test

Thank you!