Chapter 4

General comments:

- Not particular to Chapter 4, but in general I am a bit confused about the CDR structure. Usually these documents follow something on the line of:
  - Physics motivation → requirements (for example, to obtain such measurement with such statistical error one needs such luminosity, or to study such Higgs decay mode such b-tagging efficiency is needed).
  - Detector Layout (initial layout needed to be able to do performance studies...)
  - Performance → detector requirements (for example: such position resolution requires such pixel size, and such luminosity such radiation hardness)
  - The last step, detector requirements to specifications, is done in a later stage, much closer to actual construction, since detailed specifications can limit the technical options at some level.

  The Vertex chapter should then start with the detector requirements, as it is indeed done in 4.1. However, I have not been able to find the motivation for such requirements, which thus seem arbitrary. The later section on "Jet flavor tagging" on Chapter 11 does not provide requirements.
- In the line of the comment above, I would think that the section 4.3 "performance of the baseline [vertex detector]" should not belong to Chapter 4, but on the performance chapter. While Chapter 4 focuses on the technical options, the current and future R&D activities.
- The fact that the same layout as for the ILD has been adopted with no real justification (??) gives a poor impression.
- The work already done within the CEPC effort so far (CMOS, SOI2) is missing some detail. This can be added in a concise manner, with short text and references.
- I think the technology section needs to be updated.
  - It mentions DEPFETs in a positive light (I think they are not an option). It mentions the R&D of ALICE as "gaining momentum", when is is already well done and in production.
  - Contrary to what it says, ALPIDE reached the power dissipation of 40mW/cm2, but the radiation hardness is in fact on the edge (0.6 Mrads, but not sure if this is the limit of the technology or the tests).
  - Also HV/HR CMOS are lately collectively called depleted-CMOS (since technologies tend to offer different resistivities anyhow). The classification is now small or large fill factors.
  - The SOI paragraph can be improved and the "HV-CMOS" text is not correct anymore.
- Is the vertex detector replaceable? Was wondering if this could be an alternative for a technology not so radiation hard, but with other advantages...
- What is the assumed composition of the beam pipe? Does it include Au coating?
- I would recommend including a section in Ch4 that explains the common "front-end issues" of the devices. Trigger operation mode, electronics in pixel, etc.
- If readout speed is a concern, then depleted sensors (like SOI2 or depleted CMOS), are a better option than technologies that collect change by drift.

Detailed comments on Chapter 4:

- Page 11, introduction. "… the need for a vertex detector with low material budget and high spatial resolution." I think the order should be reversed, the important issue is the position resolution, low material budget is a consequence of this.
- Page 11, introduction. "As required for the precision physics program, the CEPC vertex detector is designed to achieve excellent impact parameter resolution...". I think this is not really justified so far in the document. It is not clear which is the target impact parameter resolution.
- Page 12, section 4.1. reference power-pulsing
- Page 12, section 4.1. "..readout time shorter than 20us...". Where does this number come form?
- Page 12, section 4.1. Need to add TID and NIEL limits
- Page 12, section 4.2. "...exactly as that of the ILD detector.". Again, does not read well.
- Page 12, section 4.2. What is the distance separating the two layers on the same ladder? Has it been optimized?
- Page 12, section 4.2. "the impact parameter resolution can reach the requirements by using the single point resolutions provided in the table". Which is the impact parameter resolution required?
- Page 13, section 4.2. "The preliminary studies for optimization to evaluate the sensitivity of the results on the chosen parameters had been done, for the purpose of assessing the impact of the detector geometries and material budgets on required flavor-tagging performance." I am not sure I understand the sentence.
- Page 13, section 4.3.1. "ambitious impact parameter resolution". Not sure what it the target of this vaelue.
- Page 16, section 4.5. Suggest: "The history of silicon pixel vertex detector can be traced back to LEP era, when it was introduced in the DELPHI experiment [5]. Significant progress has been made over the last 20 years [6]."
- Page 16, section 4.5. "mild compared to the ILC"… but it is not mild, it is of the same order.
- Page 16, section 4.5. "To fulfill...the vertex detector must be..."
- Page 16, section 4.5. "practical" → feasible
- Page 17, section 4.5. I think the paragraph on DEPFETs is too optimistic for the technology. DEPFETs are not rad hard, not fast(20us/frame is slow) and need extra electronics… The figure also seems odd for a technology that is probably discarded.
- Page 17, section 4.5. "The HR-CMOS" section based on ALICE needs to be updated (see general comments above).
- Page 17, section 4.5. SOI:
  - while I agree SOI2 has great potential, I would not say that the isolation issues have been solved until the radiation hardness is studied. Or it has been already? If so, then must add the sentence and reference.
  - I have my doubts that 3D integration is really an option on the current relatively short timescale of the CEPC.
  - Note that HV-CMOS is not longer proposed in ATLAS for AC coupled devices, but good results have been obtained on fully monolithic AMS productions (though with high power dissipation ~100mW/cm2). Also note that TJ 180nm with process modification to ensure a larger drift area, is being pursued in ATLAS.
- Page 18, section 4.6. "another pixel chips layer" → "...with another sensor pixel layer."
- Page 18, section 4.6. "So a suitable cold plate, which is coupled with..."

- Page 19, section 4.6. STAR-PXL. It says that the PXL system uses air cooling with 170mW/cm2, but for the CEPC 50mW/cm2 are needed? Why the difference?
- Page 19, section 4.6. So for CEPC vertex detector, the suitable cooling method will be determined according to the sensor option and the power consumption. → actually, since the cooling adds material, it is part of the overall optimization, sensor technology, power, cooling…
- Page 19, section 4.6. “Simulation and module prototype studies should be carried out to find suitable designs that can meet requirements of stability, cooling and the performance of the vertex detector.” Unclear to me what “designs” mean.
- Page 19, section 4.7. “The technology options in Section 4.5 are able to meet each individual requirement” → “Each technology option in Section 4.5 is able to meet some of the requirements of the CEPC vertex detector (low material, …).”
- Page 19, section 4.7. Again, not sure if 3D integration will be ready in the current time scale of the project.
- Page 20, section 4.7.1 I think this section can be improved with some concrete results and references. Some corrections.
  - ...have started chip design using… → ...have started chip designs using…
  - one uses simple 3T analog… →one uses the simple three transistor (3T) analog amplification circuit…
- Page 20, section 4.7.2. Here is says 2.8 um resolution, but in other places just 3 um.
- Page 20, section 4.7.2. to be resistive to the TID → to be able to sustain the expected TID dose…
- Page 20, section 4.7.2. “When it comes to...low power design” → this paragraph mentions the modification of the TJ process (reference needed) but seems to repeat the SOI2 process that was mentioned before (in 4.7.1), so it is future or current?

Chapter 5

General comments:

- Again, no clear requirements presented for the tight
- Why 50um thickness for CMOS? This is a large area detector, thinning to 50um may have yield implications.
- There are some contradictions regarding the cooling strategy. While the simulation seems to assume air cooling, the text mentions micro channel cooling. In but are micro channels realistic? I think micro cooling might not be an option for the CEPC, given the large area of the detector.
- The chapter mentions DC-Dc converters for powering? But DC-DC converters are very bulky, would introduce material budget. Both ATLAS and CMS adopted serial powering for the HL-LHC update.
- How to address large area CMOS sensors (otherwise restricted to reticle size of 2x3cm2)? Should the chapter include a few words in this aspect.

Chapter 6

General comments:

- Looks like the Calorimeter chapter has too many details and options.
  - May be better to present a realistic baseline and options?
- Again, missing link between physics motivation and physics requirements
- The first option presented, the PFA, looks a bit like an overkill
  - Is cost realistic for the Silicon option
    - I would estimate a 10EUR/cm2 cost just for silicon
    - Charlie checked that for the SID they predicted 3$/cm2
    - But 1 mm thick silicon is likely to be more expensive (?)
  - 20 ps resolution would have to be justified
    - Note that 20 ps is not realistic for standard silicon (or not proven yet)
    - While ~50 ps has already been demonstrated by CMS HGCAL (see Alberto´s slides)
- Inconsistencies between slides and Fig 6.8
- Right now, it looks like the requirement of 3%-4% for jet energy resolution is not achieved.

Chapter Muon

- May be too many options for the muon system. Concentrate on RCP and uRWell technologies? Other options could be mentioned briefly, but no need to cover them all in the CDR.

Chapter Magnet

- What is the advantage of the active shielding scenario vs the default one?
- Charlie estimated 60km of cable for the HTS option. How does it compare with other systems already built?

Big discussion on structure of CDR

- Currently, Ch 6 gives the impression that dual calorimeter is a plug-and-play option for the PFA approach, however in reality, we are talking about two detector concepts. This should be more clearly presented in the CDR
- Consider to restructure along the following lines
  - Introduction (executive summary of the full project)
  - Physics motivation
  - Detector concept A (vtx+TPC/all si + PFA...)
  - Detector concept B (vtx´ + drift chambers + dual…)
  - Performance (of baseline)
  - Summary

Overall recommendation (mail Joao from reviewers)

- Better interaction between simulation and performance
- More manpower… also specific to CDR preparation (editorial team)