Digital Design and Verification of the Front-end readout chip of ITk Strip for ATLAS Phase II upgrade

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On behalf of ITk Strip ASIC community

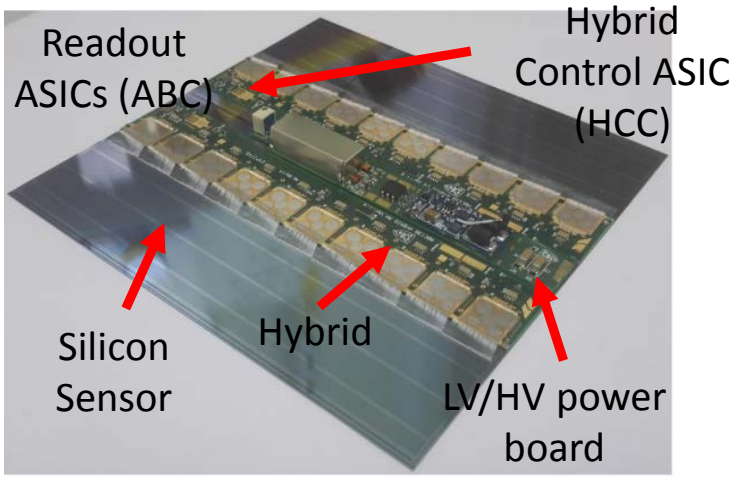
Dec. 8, 2017

Outline

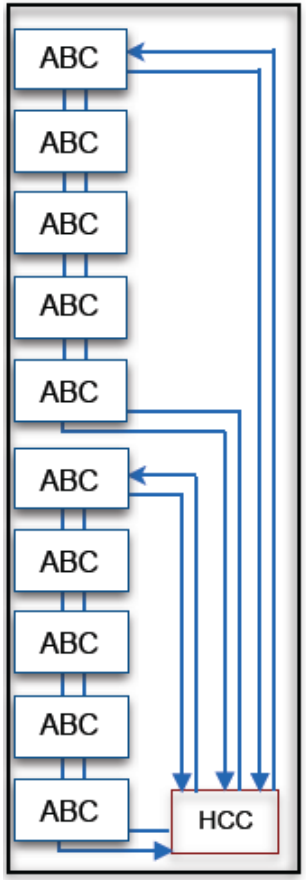
- Star chips for ITk strip upgrade
- New design features of ABCStar
- Functional Verification
- Other blocks and current status

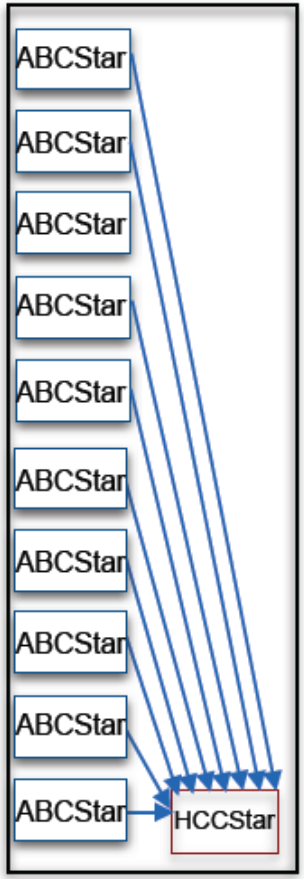
Star chips for ITk strip upgrade

Star chips for ITk Strip



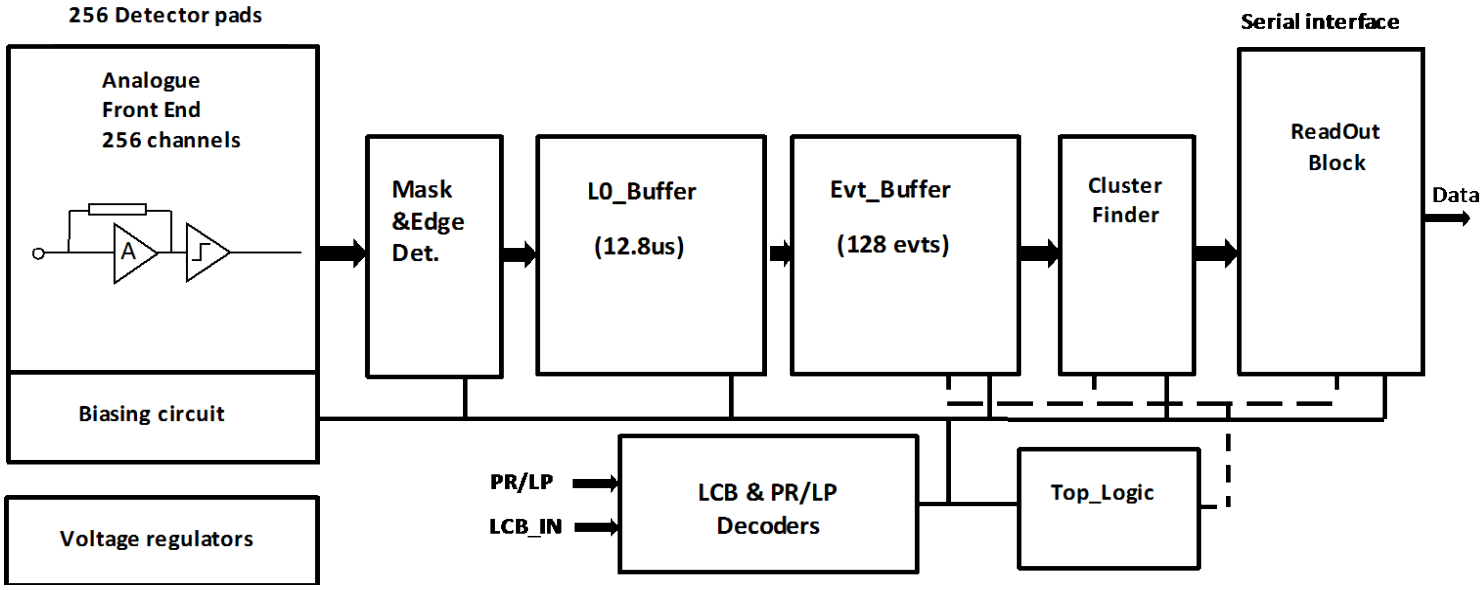
- Challenge for ITk Strip upgrade
  - Higher luminosity , finer granularity, larger scale, harsher radiation…
- Chip set on module
  - ABC--ATLAS Binary Chip
  - HCC--Hybrid Control Chip
- Interface for higher trigger rate
  - Increased trigger rate->1MHz L0
  - shorter latency
  - From serial transfer to star connection





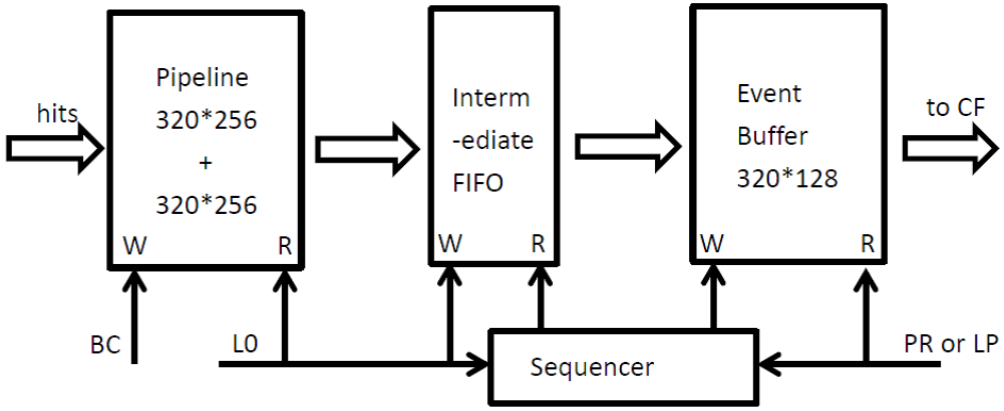
New design features of ABCStar

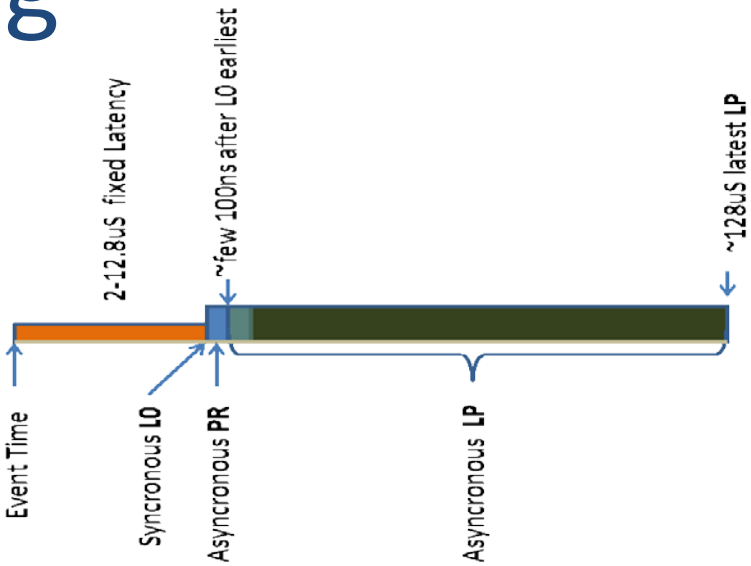
ABCStar ASIC



- It uses the standard binary readout architecture
- Data path: amplifier, discriminator, input register block, pipeline, event buffer and a cluster algorithm to compress data for output
- It is being designed to support various trigger modes
- It will be built in GF130nm technology

buffering

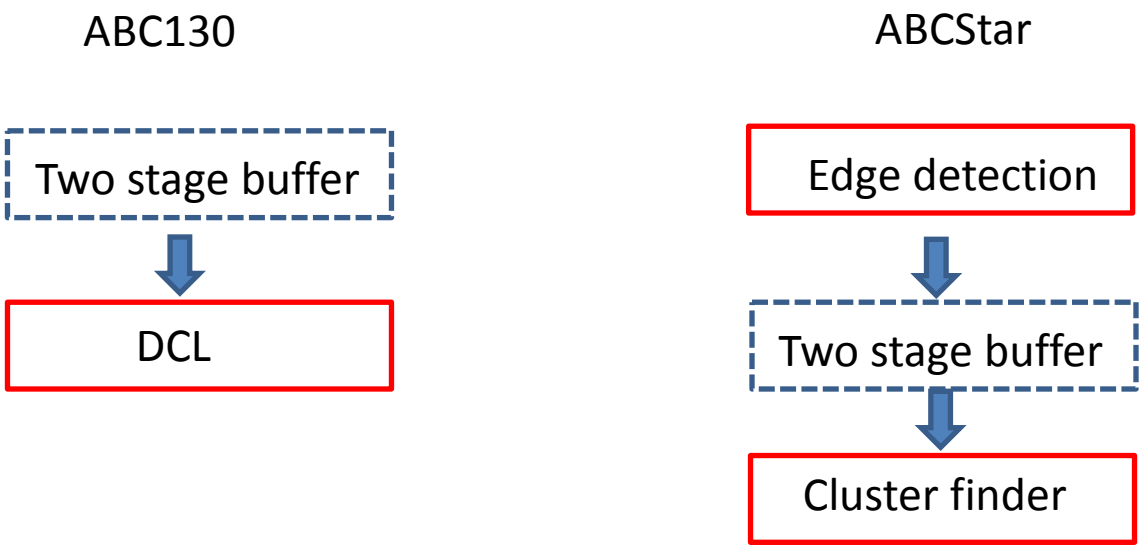




- The two stage buffers: Pipeline(L0Buffer) and EvtBuffer
- Transfer 1 event per L0 from Pipeline to EvtBuffer(instead of 3)
  - Less RAM
  - Simpler logic
- Modification of buffer size
  - Pipeline(L0Buffer)extended to 512bit length
  - EvtBuffer reduced to 128bit length(128 events)
- Basic memory IP: single port RAM+ in case of consecutive L0s

  -->Intermediate FIFO to give the priority to EvtBuffer read operation

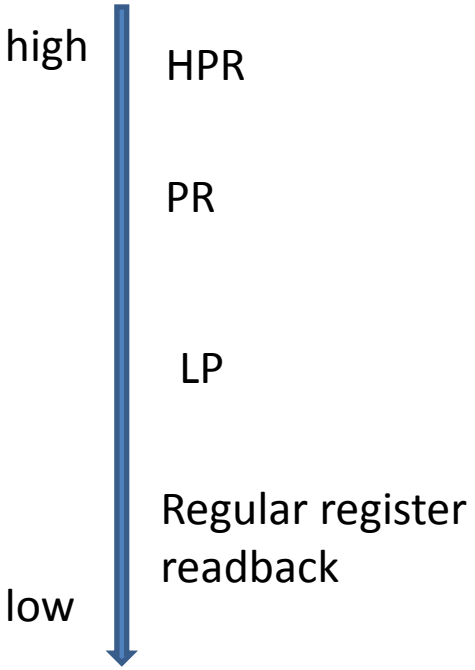
Data compression



- Edge detection circuit before pipeline
  - Extract only the leading edge information
  - To compress the data in terms of time by factor of 2
- Cluster finder after eventbuffer
  - Data reduction in terms of space, creating a cluster byte for channels found with hits
  - takes in 256 bits of strip data and reports out 12 bit clusters at 40MHz

Priority readout

- Physics data
  - PR trigger has higher priority over LP trigger
- Register readback
  - 32 positions Register Data FIFO
  - Two cases of conditions independent of read register command
- HPR
  - The content of the 32 bits register called “HPR” (for High Priority Register) is transmitted periodically after powerup, a HardReset, or a RegisterReset fast command, or in case of the lcb_lock bit being false, indicating the LCB circuit has lost its synchronization with the LCB signal frame.
- TopLogic
  - Sequencer for the control of EvtBuffer, ClusterFinder and ReadOut



interface

- LCB
  - The L0A/CMD/BCR - signal transfers triggers (L0A), fast-commands, register read-writes (CMD) and bunch-counter-reset (BCR) to the HCCStar and then onto the ABCSTAR
  - The signal is 6b8b encoded and sent at 160Mbps over an LVDS bus
  - 16 bits frame extending over 4BC
- Data packets
  - 68 bits fixed length readout packet format
  - 160Mb/s readout rate was rather chosen to reduce the transmission latency for L1-track

Start Bits	Header	Payload	Trailer
3	16	48	1

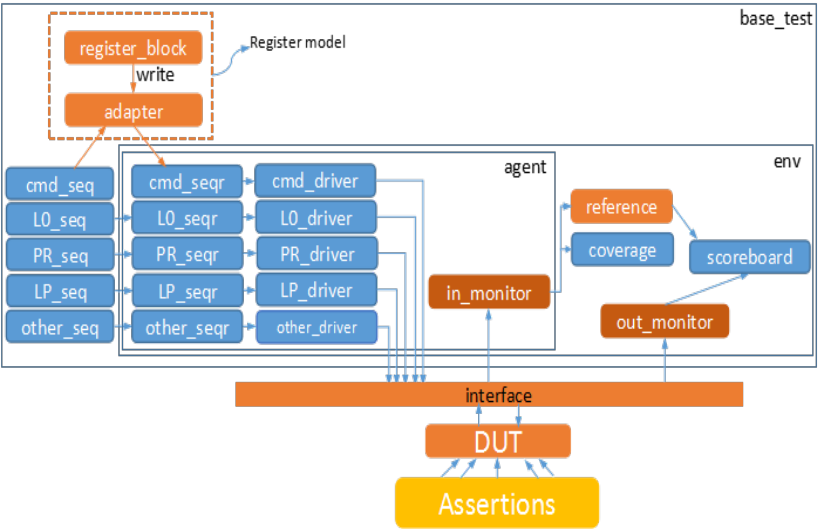
Robust design

- L0tag insertion in LCB
  - Improve reliability by remove sensitive L0ID counter
- Deglitcher for external asynchronous resets
- Radiation hard design
  - TMR for key logic and registers
  - Hamming coded state machine
- …

Functional Verification

UVM setup

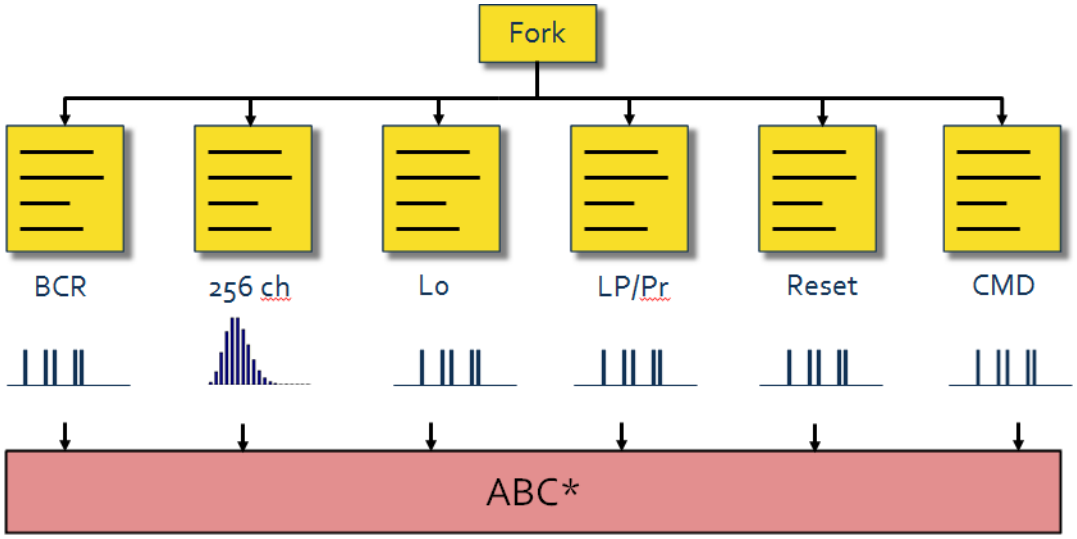
- A top verification setup based on (UVM)Universal Verification Methodology was built for ABCStar.
  - Functional coverage with customized random stimulus
  - Result comparison with reference model through scoreboard
  - SystemVerilog assertions for validating key design features
- to verify the current design under several possible trigger conditions
  - different rate, latency and distribution model of triggers



Trigger mode	description	Example tests with UVM setup
L0	Capture and readout at L0 rate	L0@1MHz, LP@1MHz
L0/LP	Capture data at L0, send requested data at LP rate	L0@4MHz, LP@1MHz
L0/PR/LP	Capture data at L0, send data with priority at PR rate, send remaining requested data at LP rate	L0@4MHz,LP@1MHz,PR@100KHz; L0@1MHz,LP@400KHz,PR@100KHz

SystemVerilog setup

- Unit tests
  - RTL level tests
  - Done at the module level
- Directed random tests
  - ABCStar golden model, SystemVerilog description of the ABCStar specs
  - Independent parallel process with random distributions & payloads.



List of test for ABC*

This document describes the list of unit test to be developed for ABC*

- Mixed signal simulation of analog blocks ADCs regs 0x01 to 0x07
  - DAC's
  - Ref bias
  - Mux
  - ADC's
- Data[0:255] and Mask[0:255] verify that masking works for all bits - full coverage of all individual bits of Data & Mask
- Functional test of test mode TM[0:1] with full coverage of all option and random input pattern Data[0:255]
- Registers read, write and reset as well as write disable
- Hit counter until complete fill + Fast commands Start, Stop, Enable
- L0 buffer, Event buffer full coverage of all positions LP/PR enable and full coverage of latency.
- Test of output sequencer and priority HPR, Register with RR mode, LP, PR
- HPR functional test start stop mask reset and payload
- Calibration pulse length polarity
- Pad current drive in mixed signal
- BC offset check with full coverage of latency
- Max cluster full coverage
- Edge detection mode 0 to 30 consecutive BC's and sequence of random hits

Other blocks and current status

Analog frontend

Supporting blocks

- Power options for TID current bump mitigation
  - extend the range of digital voltage regulator, lower voltage down to 1 volt for the digital part
- eFuse for chip identification
  - an individual chip identifier programmed with eFuses
- Analogue monitor of voltage and temperature
  - an analogue monitor circuit like in the HCC to measure regulated VDDs, and temperature

Pads and layout

Summary

- In order to meet new challenges, many new features are adopted for ABCStar design, especially in the digital part
- rtl designs are close to the end, a lot of verification work ahead
- Analog blocks almost fixed, the layout has started

Thanks for your attention !