CMOS Strip Sensor Characterization for the ATLAS Phase-II Strip Tracker Upgrade

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On behalf of IHEP ATLAS Group

Many thanks for ATLAS CMOS Strip Calibration
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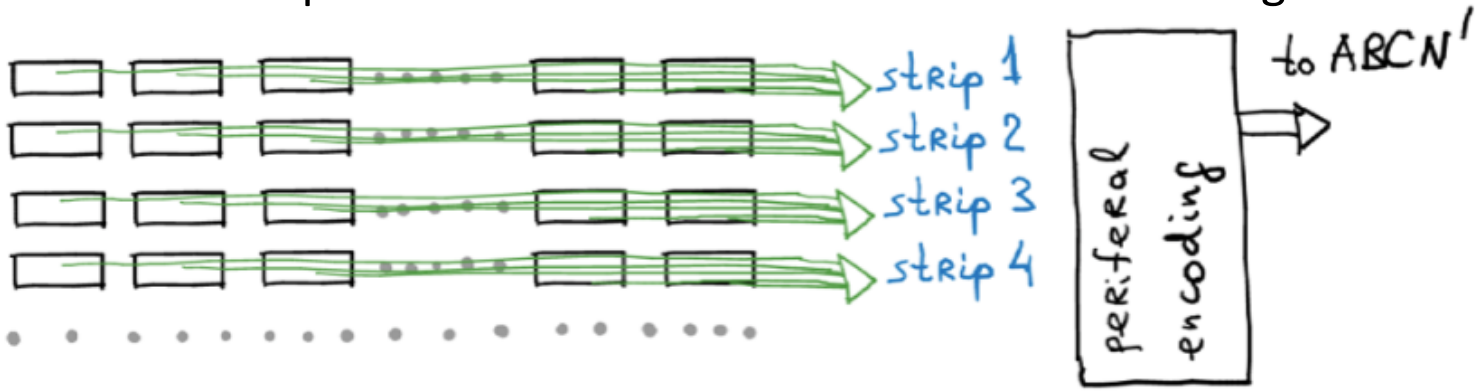
Outline

- **Introduction of CMOS Strip**
- **Primary test results of OverMOS**
- **Test results of the Chess 2 in-pixel electronics**
- **Conclusion**

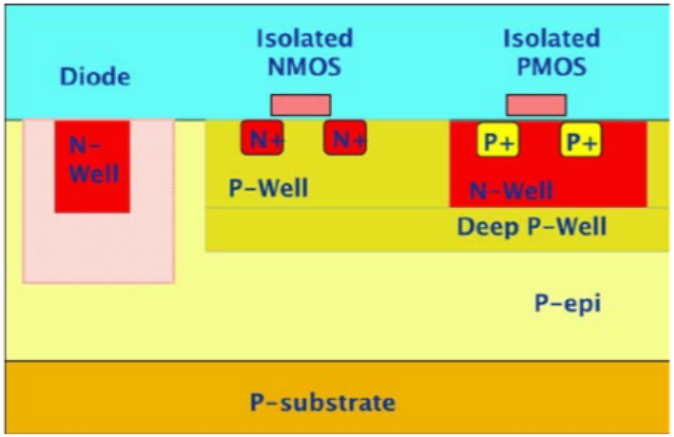
CMOS Strips Introduction

- ATLAS evaluate HV/HR CMOS technologies for strip region
  - "Strip" is composed from pixels with individual readout
  - Similar readout chain: sensor (Analog FE + comparators)->ABCN'->HCC'
- Possible improvements compared to present strip sensor:
  - Significantly lower material budget
    - eliminate the need for bump bonding or other challenging interconnect methods
    - can be thinned to less than 100um
  - Smaller pixel size
    - not limited by bump bonding
  - Lower costs
    - can be implemented in standard commercial technologies

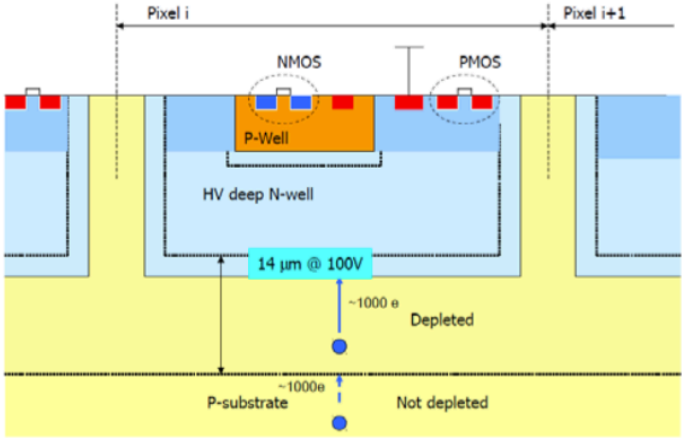


HV/HR-CMOS Technology

- Depleted CMOS benefits from HV/HR technology
  - $Q_{MIP} \propto d \propto \sqrt{\rho \times V}$
- High-Resistivity CMOS technology
  - Developed for image applications
  - Depletion zone ~10-20um
  - High resistivity: up to kOhm*cm
  - TowerJazz-OverMOS 1 -> TowerJazz OverMOS 1.1
- High-Voltage CMOS technology
  - Standard n-in-p sensor
  - Depletion zone ~10-20um
  - High bias voltage: ~100 V
  - Challenging for hybrid pixel readout electronics
  - AMS-Chess1 -> AMS-Chess2



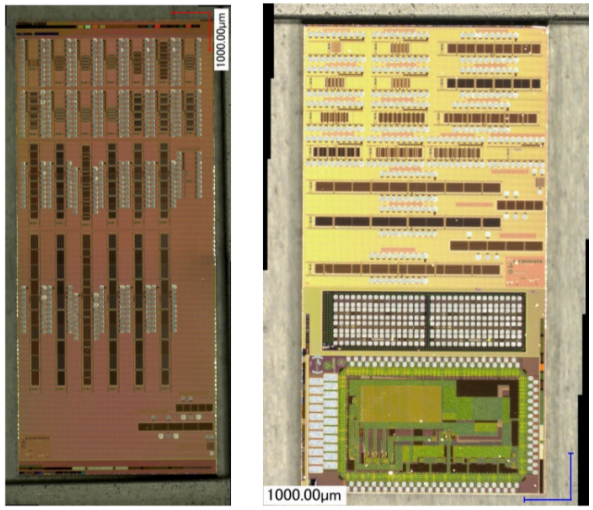
HR-CMOS Layout



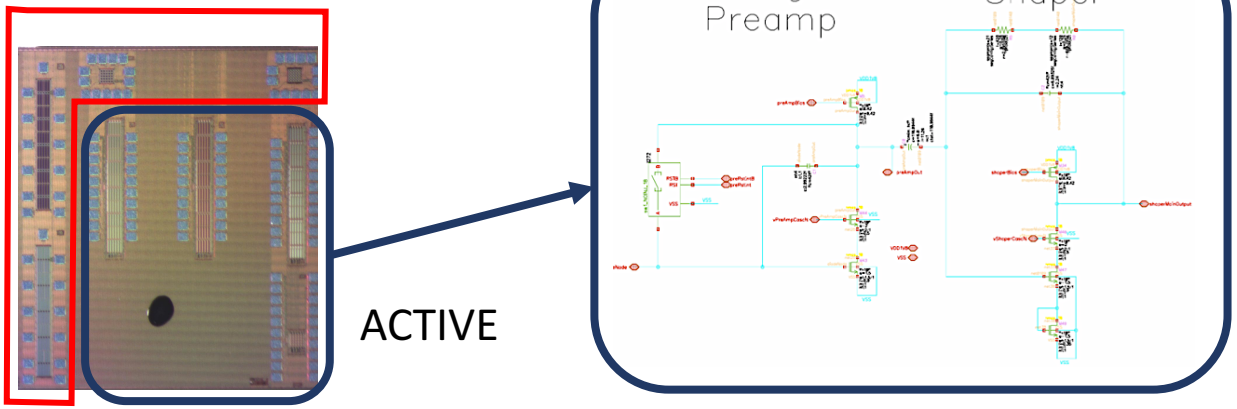
HV-CMOS Layout

Introduction of OverMOS

- OverMOS 1.0
  - P and n type substrates
  - Numbers of topology of the collecting n-wells
  - But it has shortage problems
- OverMOS 1.1
  - similar structure, but collection n-wells surrounded with P-type rings
  - Passive pixel arrays (40X40um^2, 40X400 um^2)
  - Active pixel arrays: AC/DC coupled with In-pixel electronics (40 X 400 um^2)

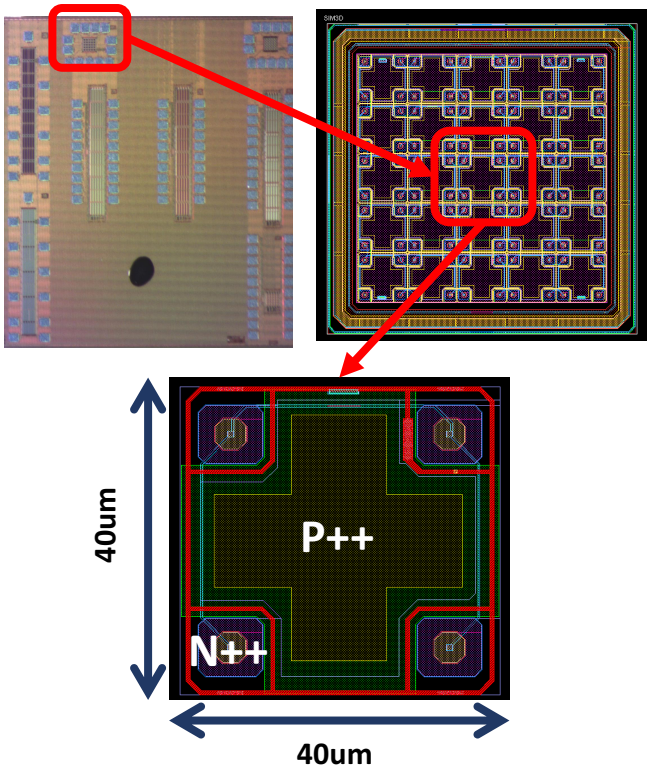


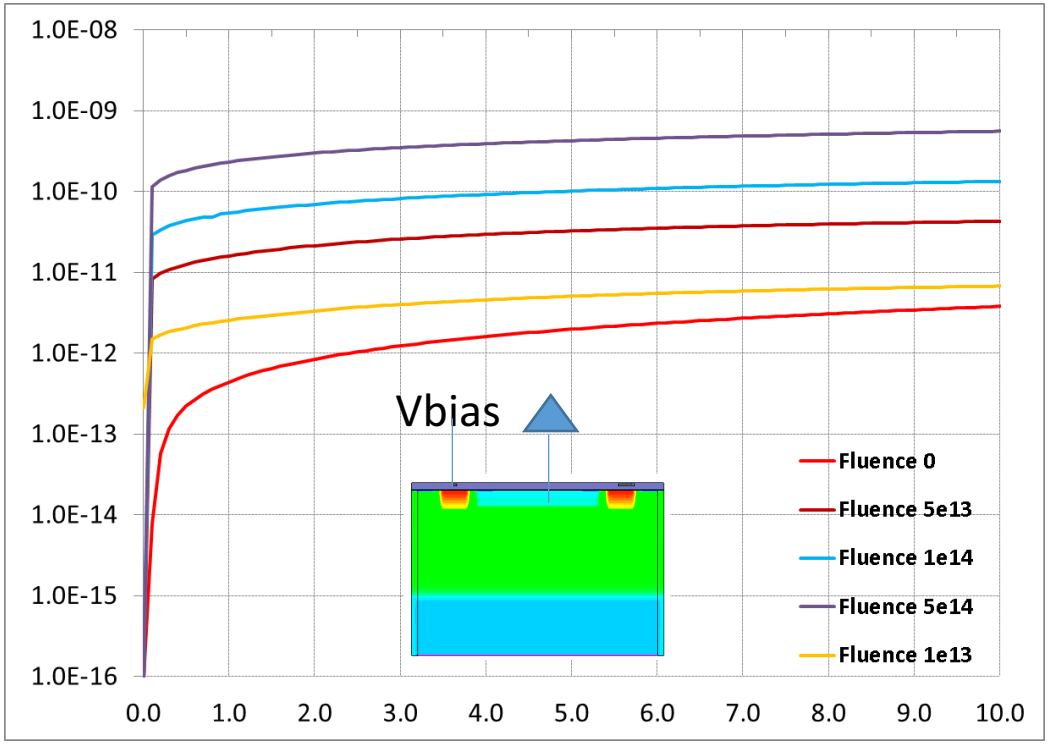
OverMOS 1 with p/n type sub



OverMOS 1.1 with p type sub

Passive Pixel DC Properties

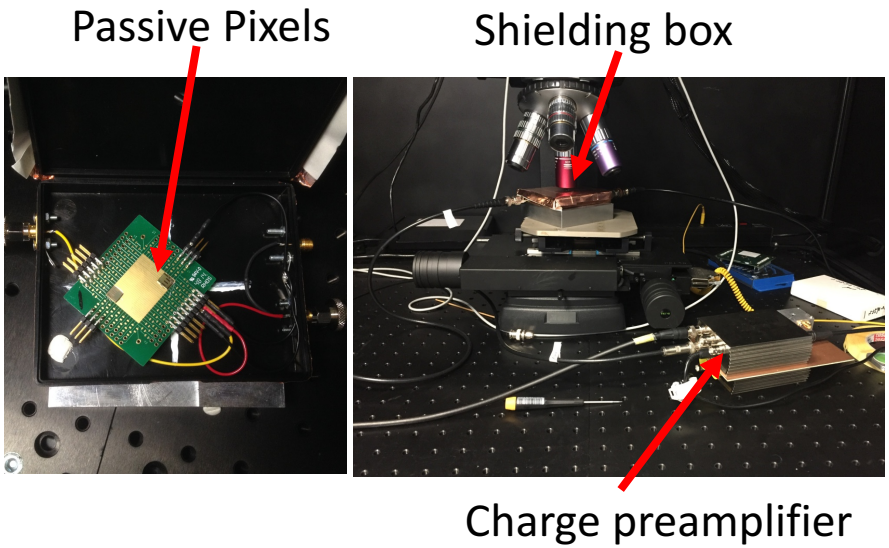


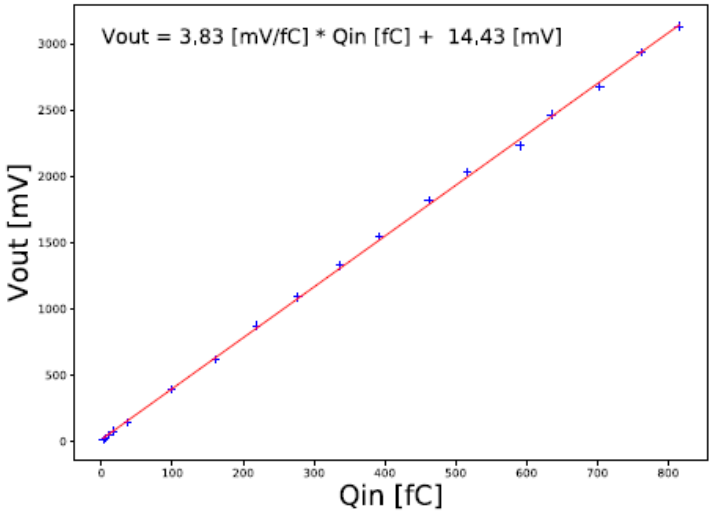


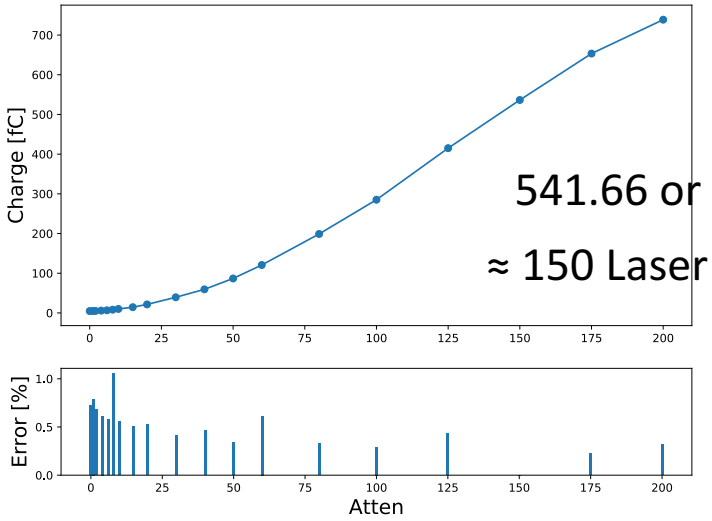
- Probing the central pixel (40X40 um^2): HV bias voltage applied to n-well and p-well grounded
- Irradiated at Ljubljana in October 2017: 1e13, 5e13, 1e14 and 5e14 n_{eq}/cm^2

Laser Injection on Passive Pixels

- Signal of the sensor amplified with an external preamplifier (A250CF coolFET Charge preamplifier)
- Bias voltage applied through the port of A250CF
- Laser information:
  - ND filter: 1.3 + 3 (decrease intensity)
  - Lo_IR (1064 nm)
  - Shutter: 4.5x4.5 um^2





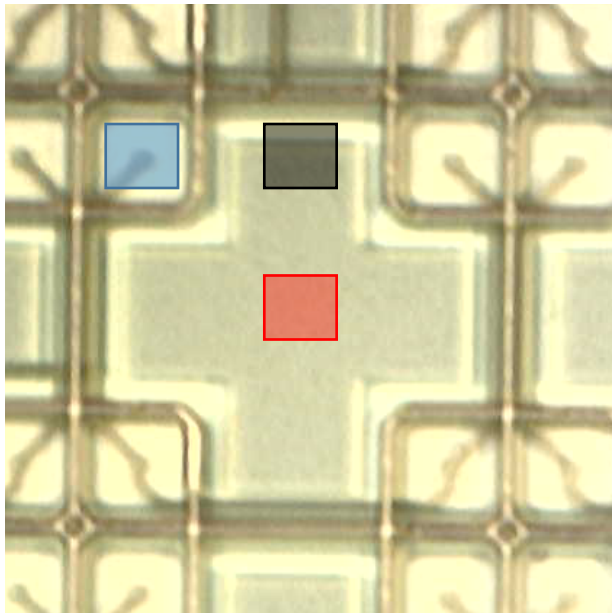


541.66 or 1.805 fC/um

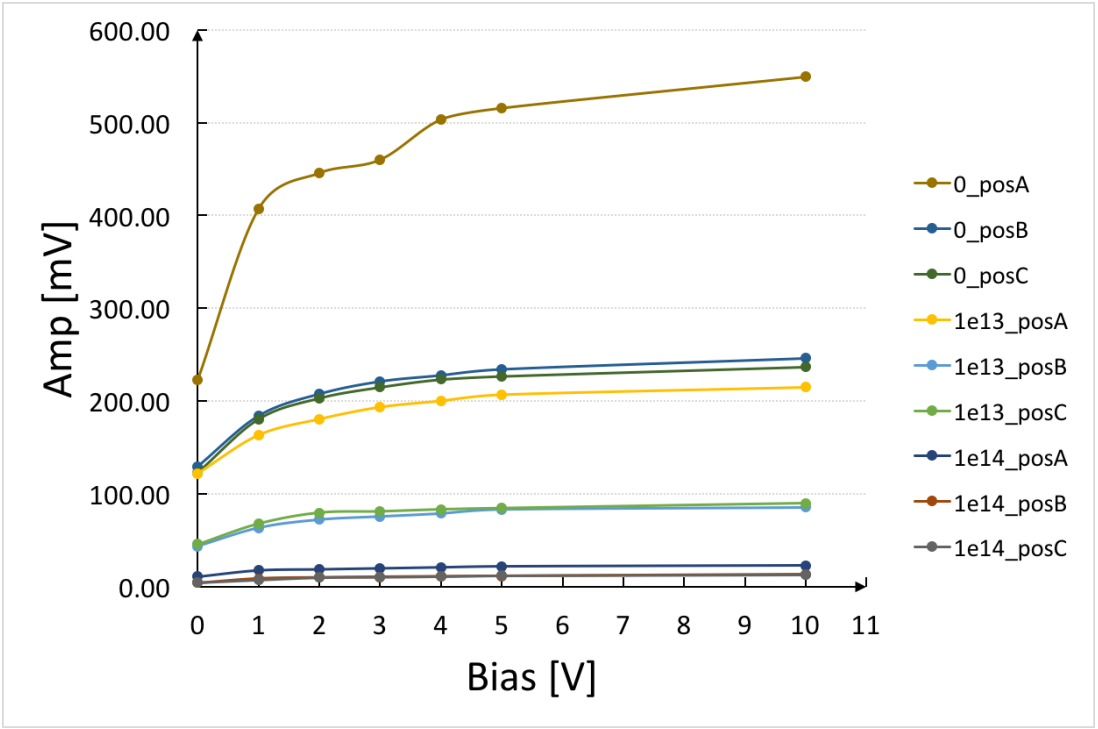
≈ 150 Laser attenuation

Laser Response of Passive Pixels

- Total collected charge vs. Vbias , points A,B,C. Integration time 400 ns
- <Q injected> = 1.805 fC/um
- HVbias provided through the A250CF, via a 400 Meg resistor chain

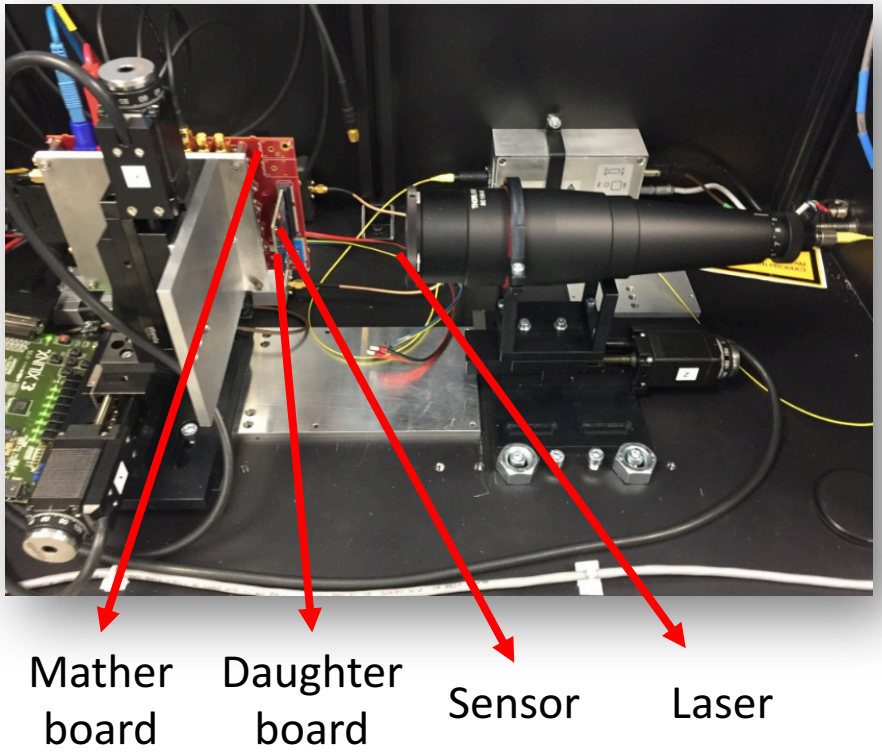


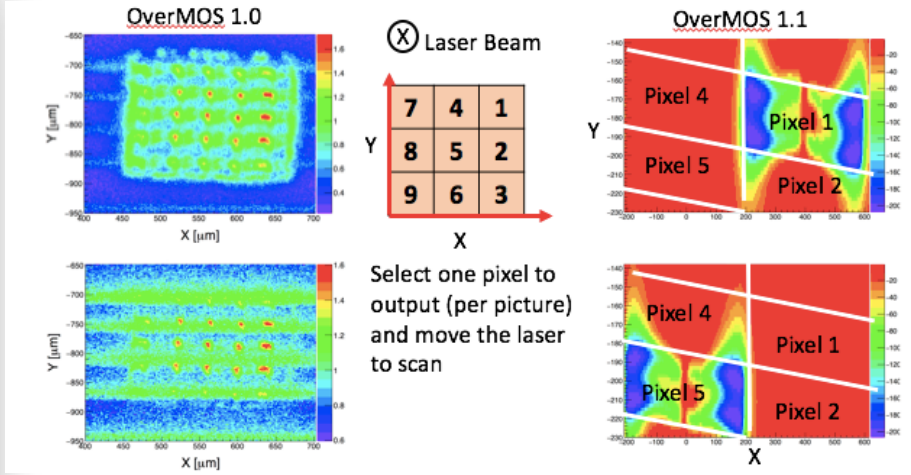
Pos A: Blue	(0,0)
Pos B: Black	(15,0)
Pos C: Red	(15,-15)



TCT Measurements on Active Pixel Arrays

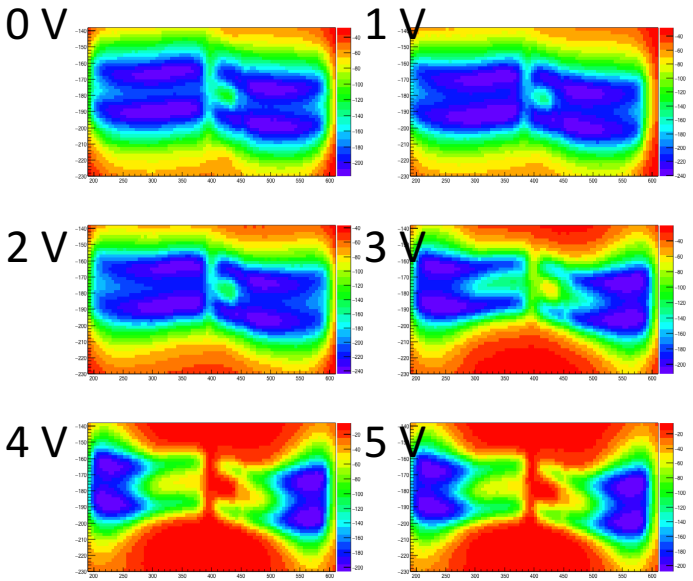
- TCT scanning on active pixel arrays confirm that the shortage problem have been solved
- The diodes are isolated by P-rings in OverMOS 1.1, so only the hit channel does show a significant response with negligible crosstalk comparing to OverMOS1.0

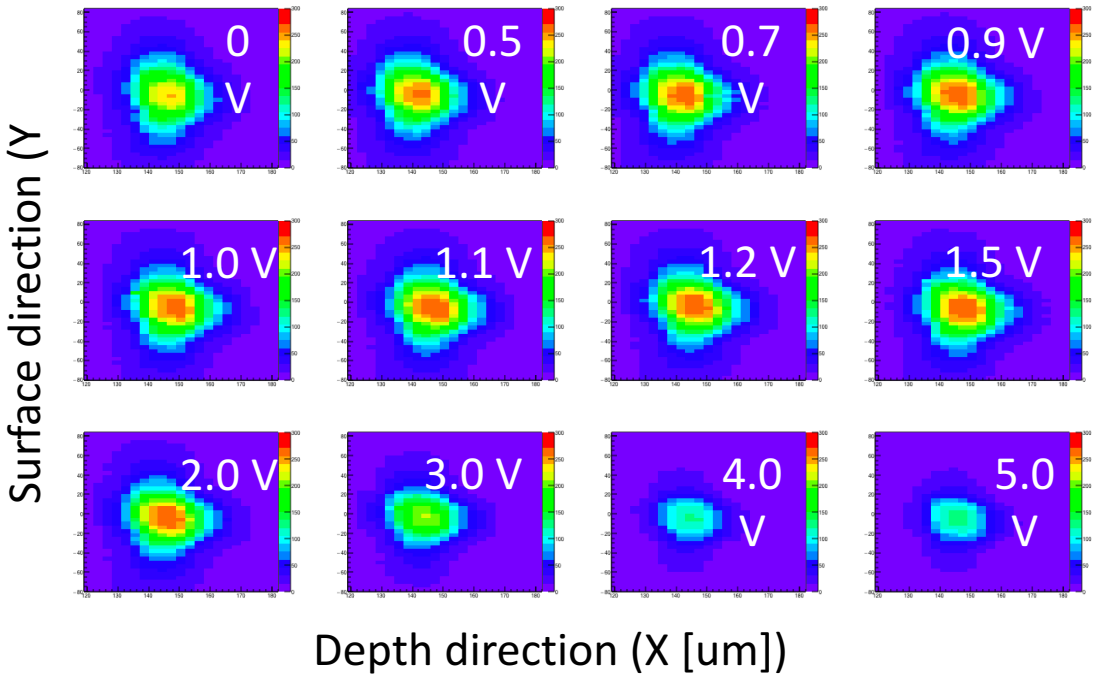




Top-TCT/Edge-TCT

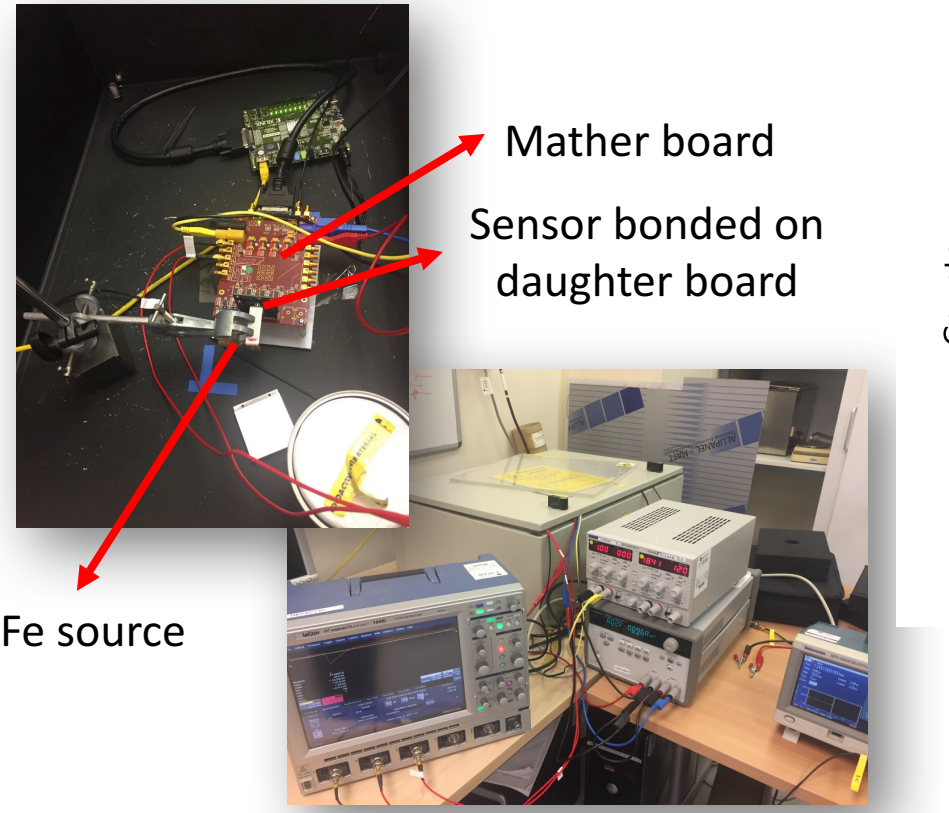
- Top-TCT and Edge-TCT scanned indicate the bias strange behavior

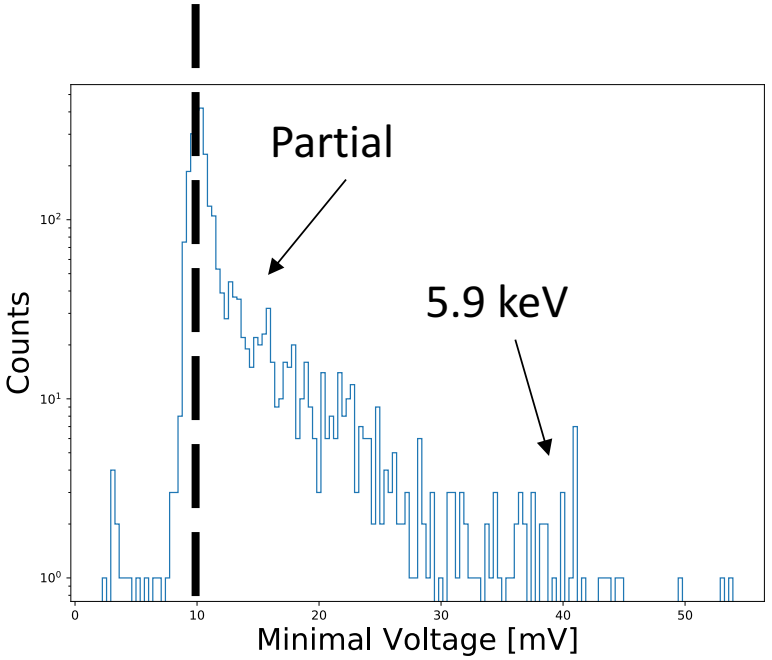




^{55}Fe Experiment

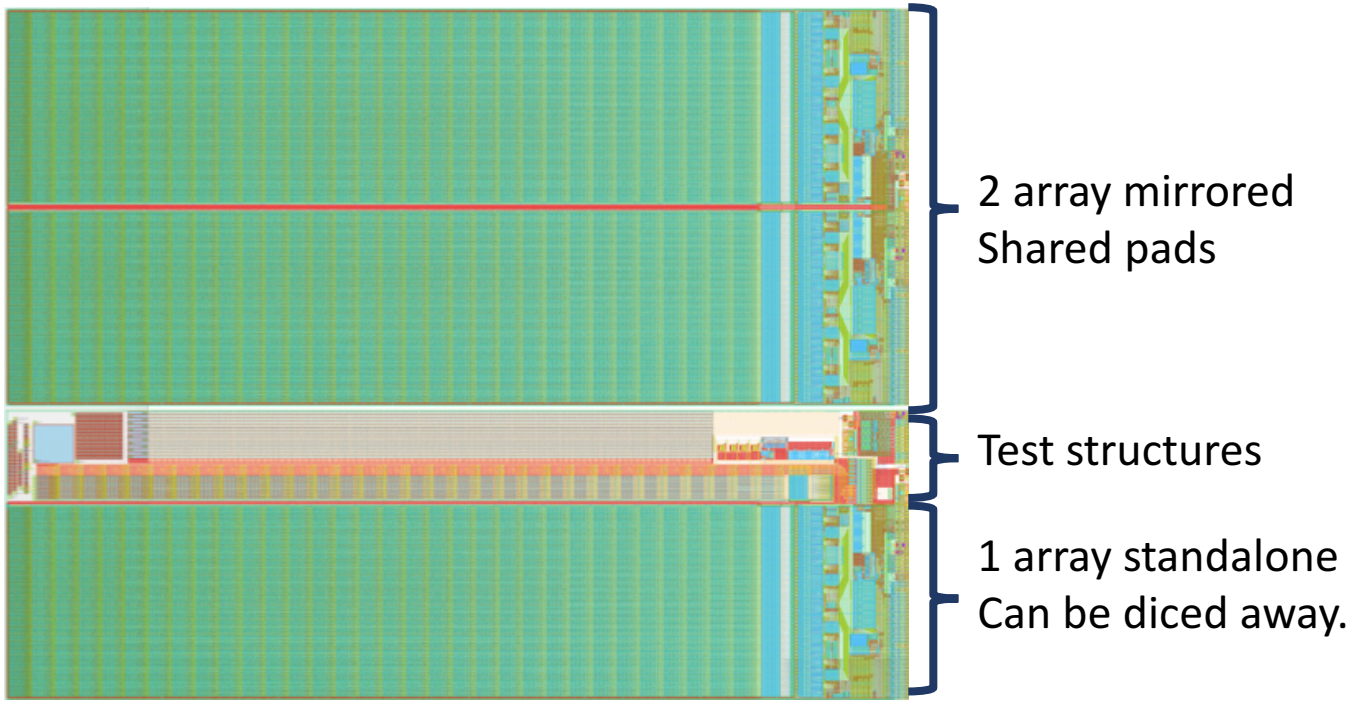
- ^{55}Fe5.9 keV/3.6 eV ≈ 1640 e^-
- Not very clear spectrum due to low statistic





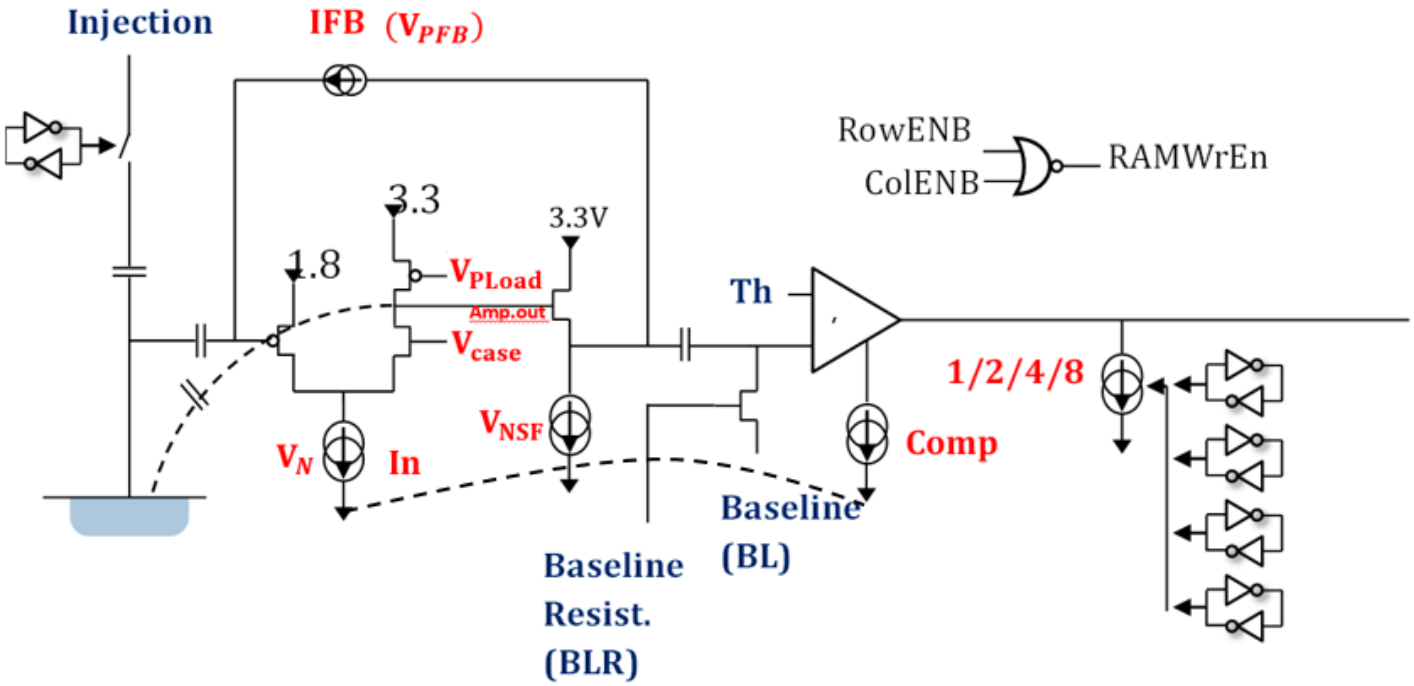
Introduction of AMS-Chess2

- Designed at UCSC and SLAC, manufactured in the AMS-H35 technology by AMS after being successful in porotypes HV-CMOS Chess1
- n-in-p with 4 substrate resistivities (20 – 1000 Ω·cm)
- Full reticle monolithic demonstrator chip
- 3 fully digital striplet arrays + 1 test filed with analog test structures
- IHEP (Yubo) attend the test of in-pixel electronics



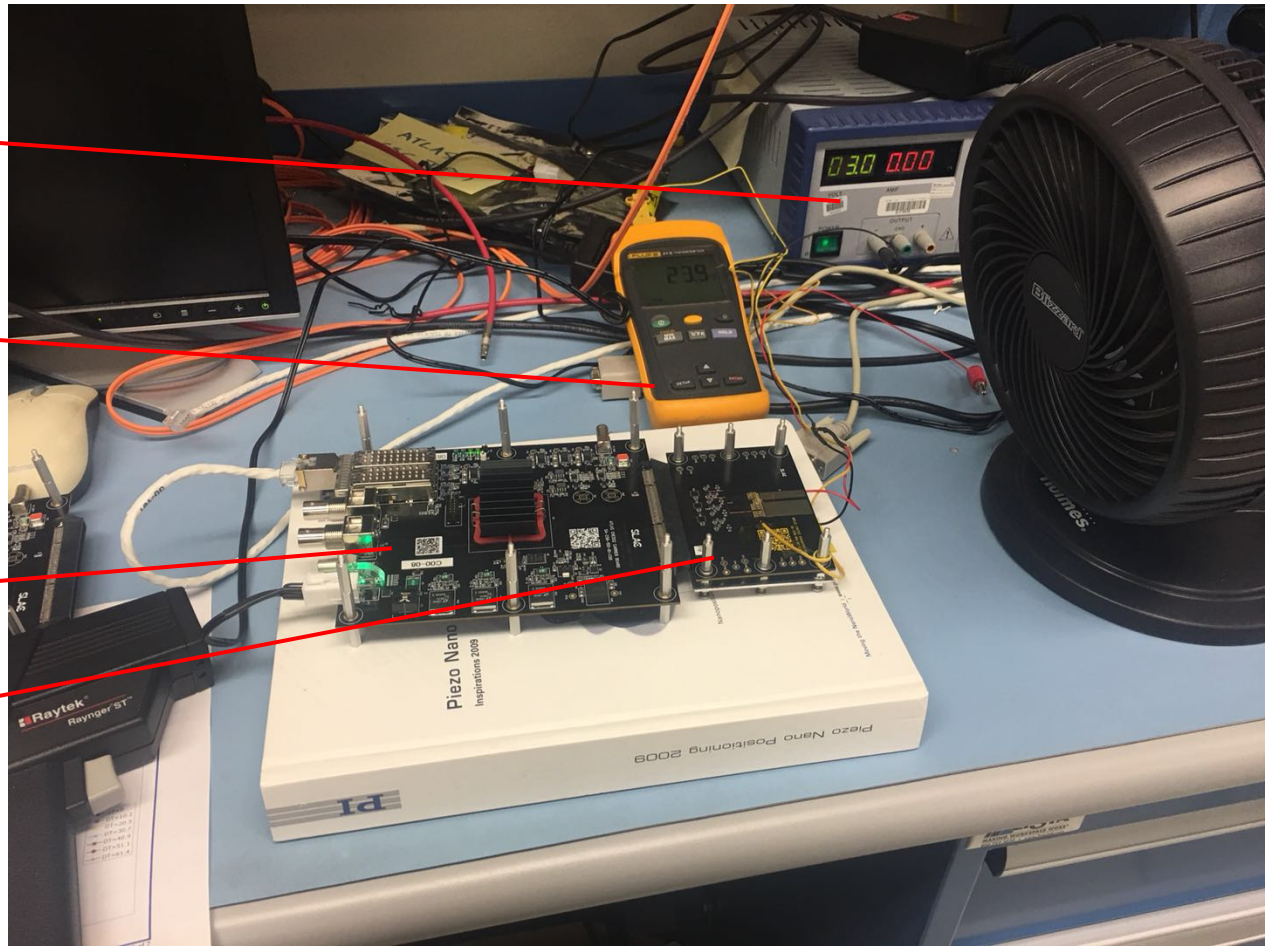
In-pixel Electronics

- Charge preamplifier and comparator are implanted in pixels
- Challenging in adjustment to make the electronics work stable



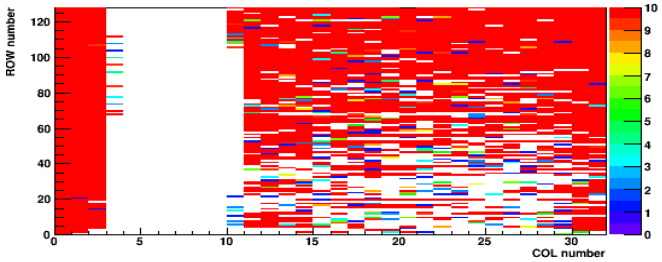
Test on ASICs

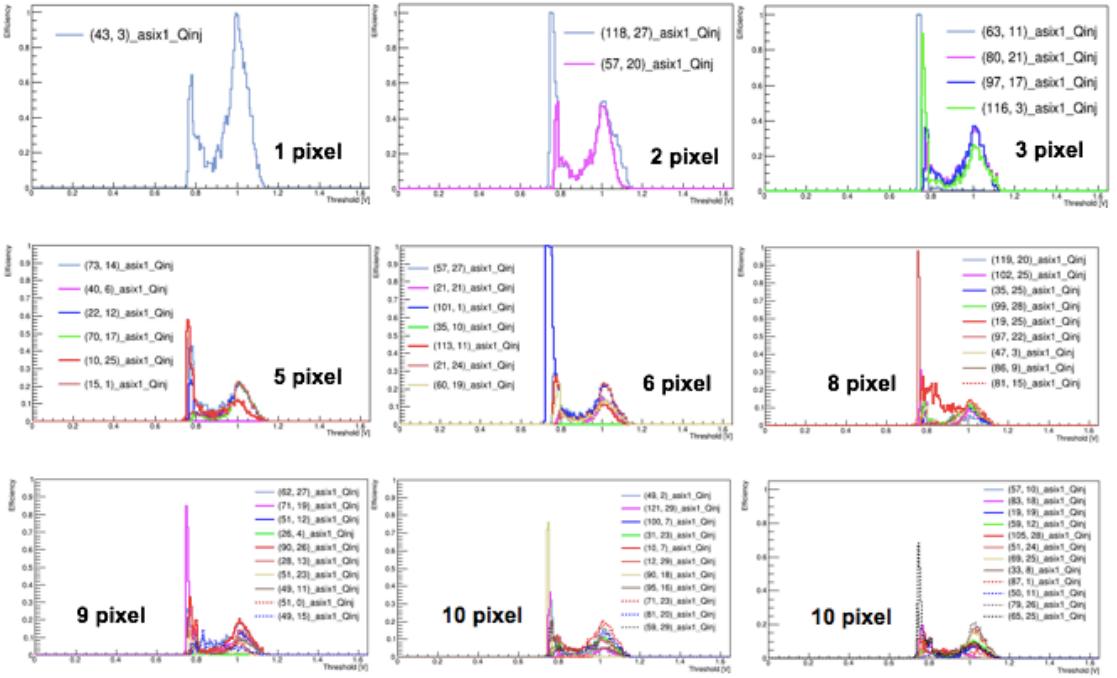
- Cooling module added to reduce the noise
- Acquire stable results with good BL/threshold linearity
- Update firmware to enable external pulse injection



Test Results of Chess2

- Average efficiency of multiple pixels @ different external pulses injected
- Beam test is on gonging after enable bias the board





Conclusion

- ATLAS commenced R&D effort to evaluate depleted CMOS pixels (HV/HR)
- IHEP attend most test of OverMOS 1.1 and Chess 2 in-pixel electronics test
- Better understanding of HR-CMOS sensor before/after irradiation and HV-CMOS in-pixel electronics