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DRX-II chip for the optical links upgrade of the ATLAS Pixel Detector

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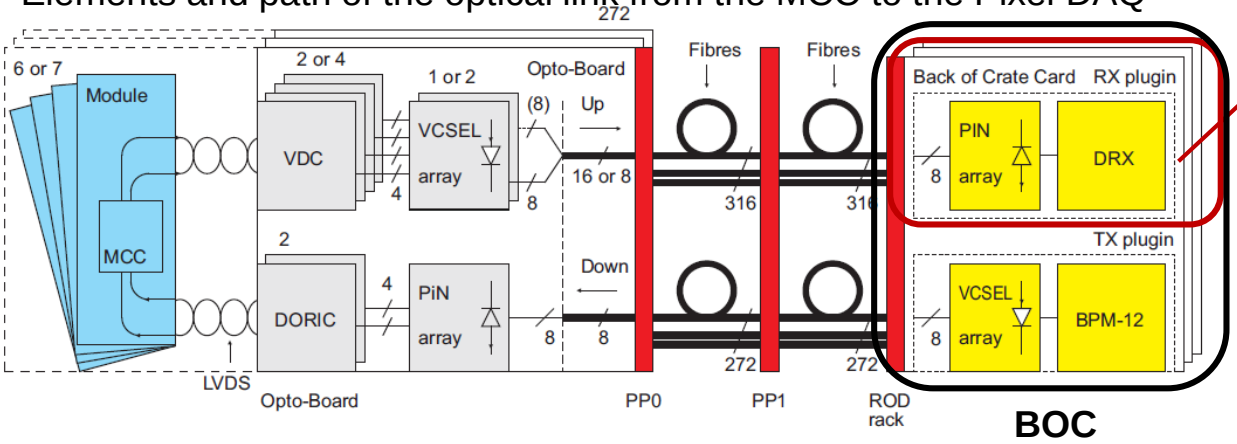
ATLAS Pixel Detector optical links

Elements and path of the optical link from the MCC to the Pixel DAQ



Rx plugin (optical receiver)

- Receiving signals from optical fiber
- Converting optical signal to electrical signal
- Recovering the electrical signal

- Optical readout of the L1/L2 will suffer from bandwidth limitation after LS1
- A wider range of threshold setting will help operations
- Option is to use new BOC for pixel operation
- Commercial optical receivers can NOT cope with NRZ signal
- Old Rx design has different connector, and old DRX chip is NOT available anymore

New Rx plugins needed

Link occupancy at 75 kHz L1 Trigger					
	μ	B-Layer	Layer 1	Layer 2	Disks
50 ns	37	39%	34%	52%	30%
25 ns; 13 TeV	25	35%	31%	48%	27%
	51	53%	59%	66%	39%
	76	71%	73%	111%	64%

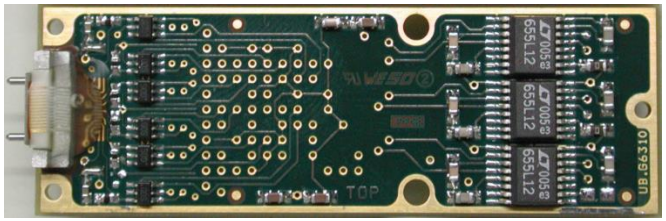
Link occupancy at 100 kHz L1 Trigger					
	μ	B-Layer	Layer 1	Layer 2	Disks
50 ns	37	51%	45%	69%	40%
25 ns; 13 TeV	25	47%	42%	65%	37%
	51	71%	67%	88%	52%
	76	95%	97%	148%	75%

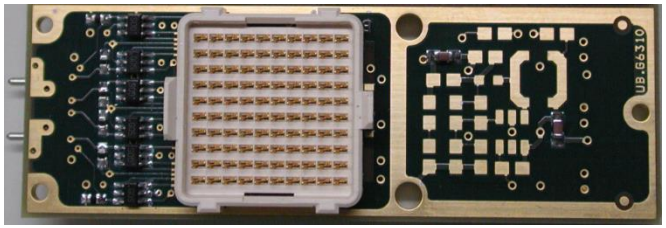
Project requirements

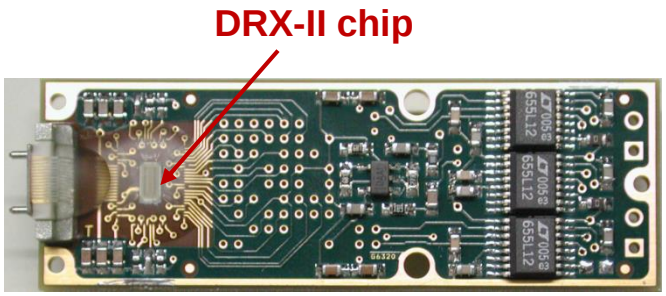
- Should operate with NRZ signals (as in Pixel operations) at 80Mbps, high stability for low frequency is needed
- Have stable operation over a wide range of light power received/input current: from 10 μA up to few mA
- Have independent thresholds for all 12 channels
- Have a BER < 10^{-11} after aging
- Should be able to perform a measurement of the input current/light power in order to monitor the stability of the on-detector VCSELS

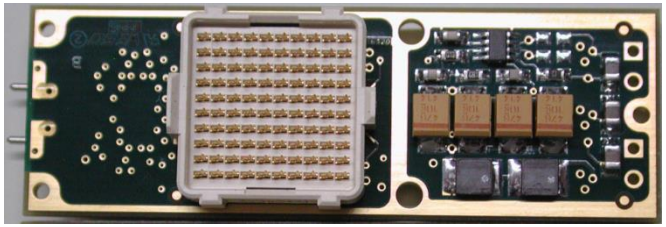
Rx plugin designs

- **Two alternative designs developed: sharing the same optical package, mechanical package and dimensions, but with different data receiver solutions**
- **Discrete solution (P. Lutz, BERN)**
  - **Commercial discrete components**
  - **Using a pull-up resistor and a discriminator**
  - **No amplification applied**
- **ASIC solution (Y. ZHANG, IHEP)**
  - **Full custom design integrated circuit**
  - **Two amplification chains**
  - **Optimized at 80 MHz**





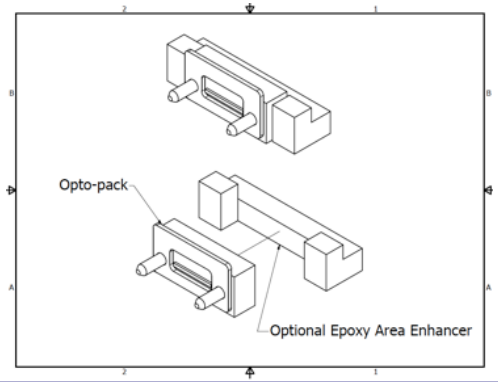


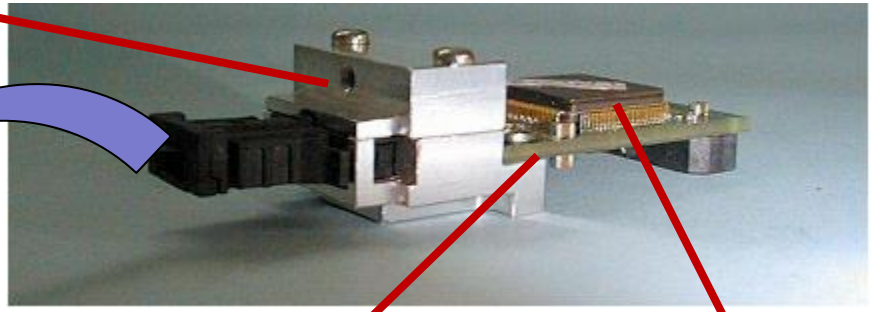


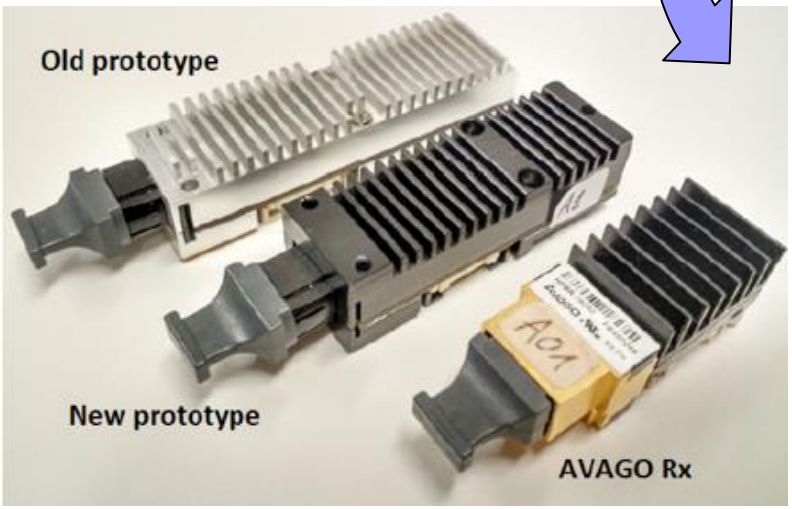
Rx prototype

Optopackage:

provided by OSU







PCB + connector

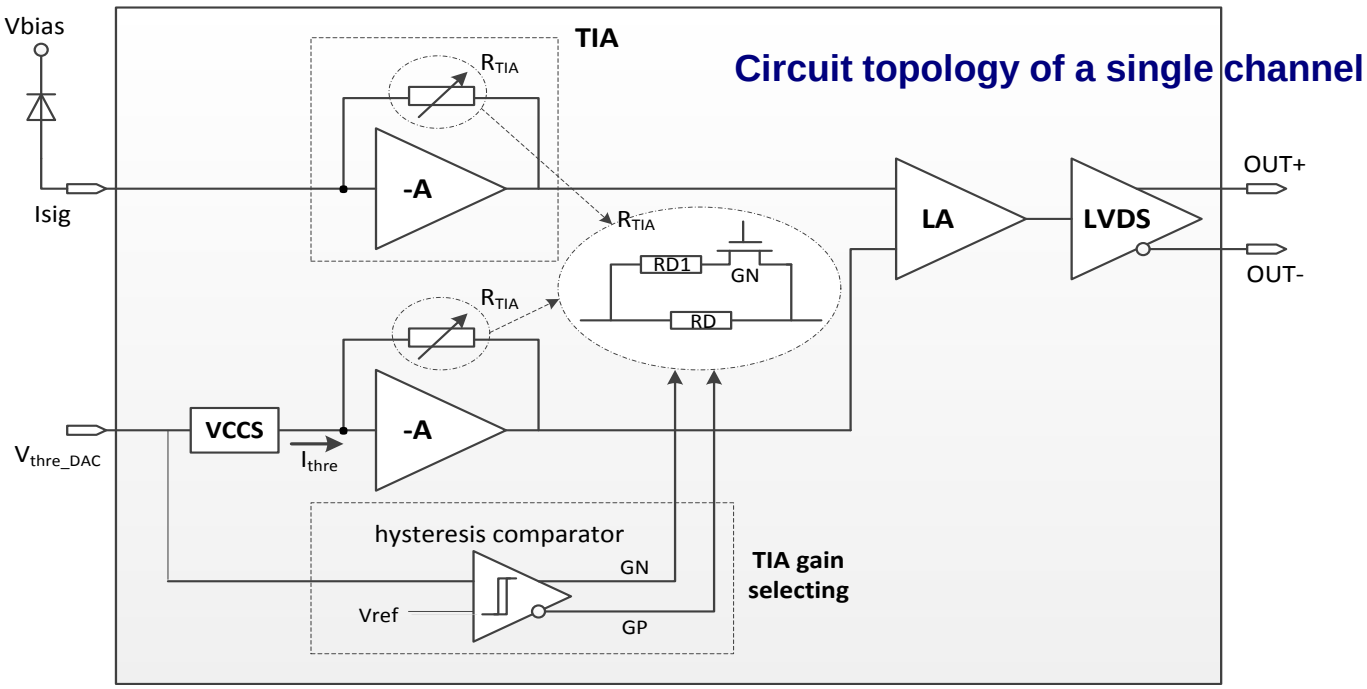
Designed, loaded, and tested in Bern

Readout electronics:

DRX-II chip (IHEP) or

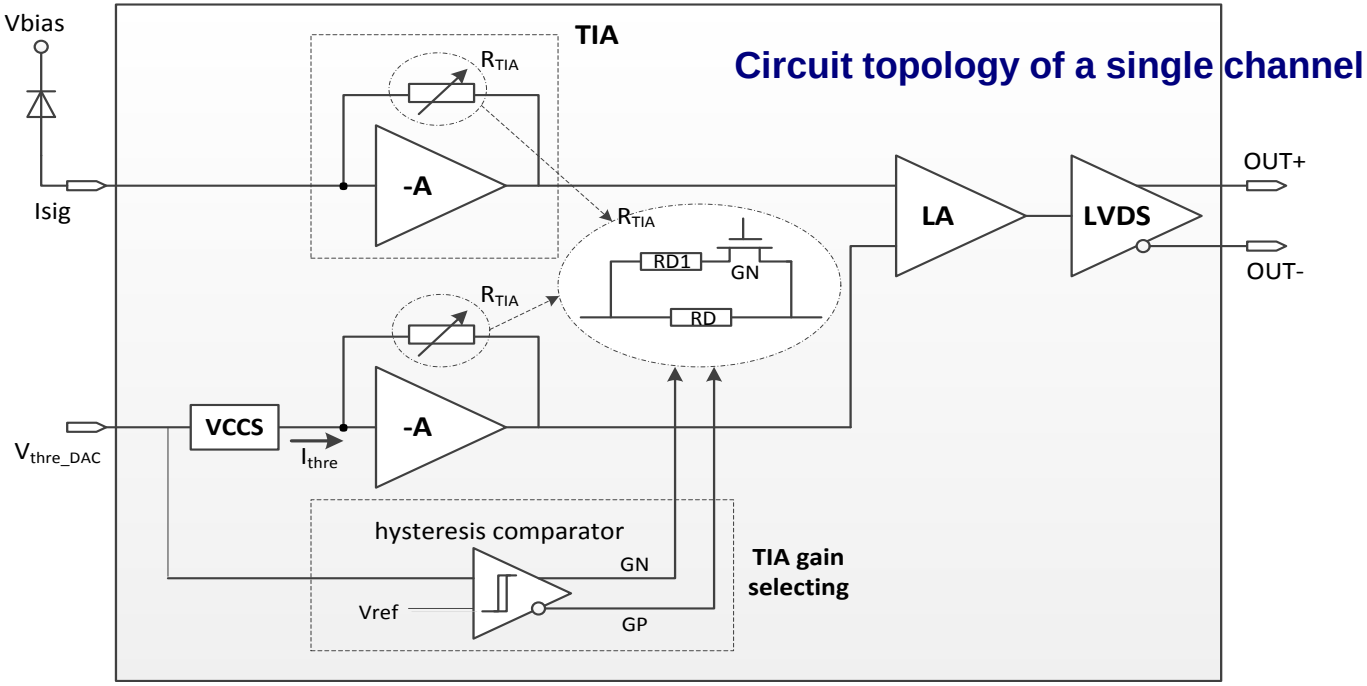
Discrete components (BERN)

DRX-II chip design (1)



- A single channel consists of two transimpedance amplifiers (TIAs), a voltage-control-currents block (VCCS), a comparator, a limiting amplifier (LA), and an LVDS output driver.
- One TIA amplifies the photocurrent produced by the PIN diode. The other TIA is to offer a reference voltage. Two identical TIAs are used to minimize the difference on the baseline due to the process mismatch and variations.
- A two-gain TIA is proposed to extend the effective dynamic range → good linearity over the complete input current range of 10 μA to 2.4 mA.

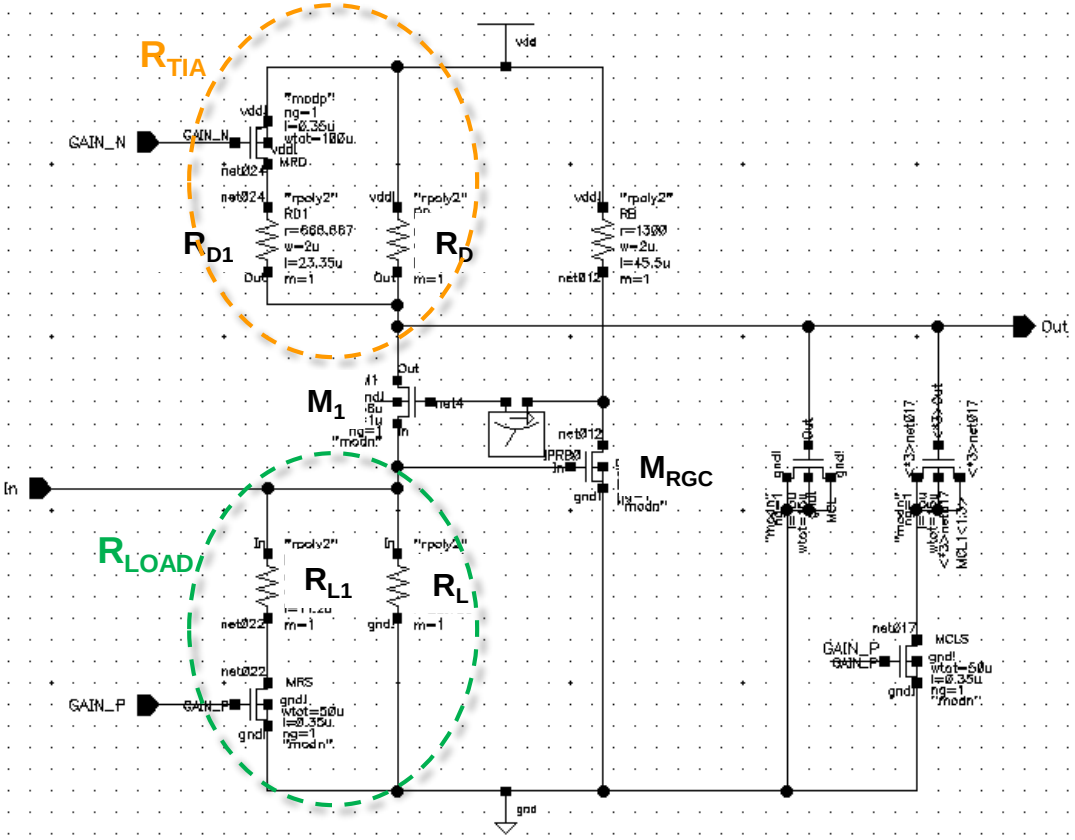
DRX-II chip design (2)

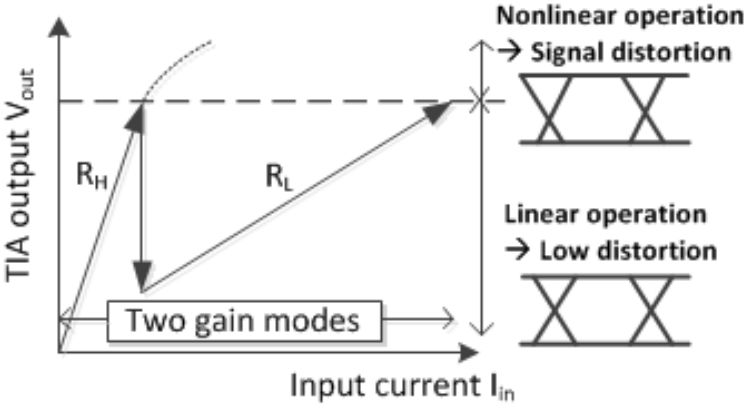


- **Gain selection is made by measuring "input signals". The individual threshold for each channel, normally half of the signal current, indicating the input current amplitude. By comparing the threshold current with a reference voltage, which defines the range of the high gain of the TIA, the comparator decides if the TIA needs to reduce its gain.**
- **The gain of the TIAs is chose during the calibration phase and will be fixed during the operation phase. Forward system free from stability problem.**
- **The chip is designed in AMS 0.35 μm CMOS process.**

DRX-II chip design (3)

- **TIA with two gain modes**
  - **TIA core: RGC (Regulated-Cascode) topology, featuring low input impedance**
  - **Two alternative transimpedance gain controlled by switched**





High gain $R_H = R_D$

Low gain $R_L = R_D \parallel R_{D1}$

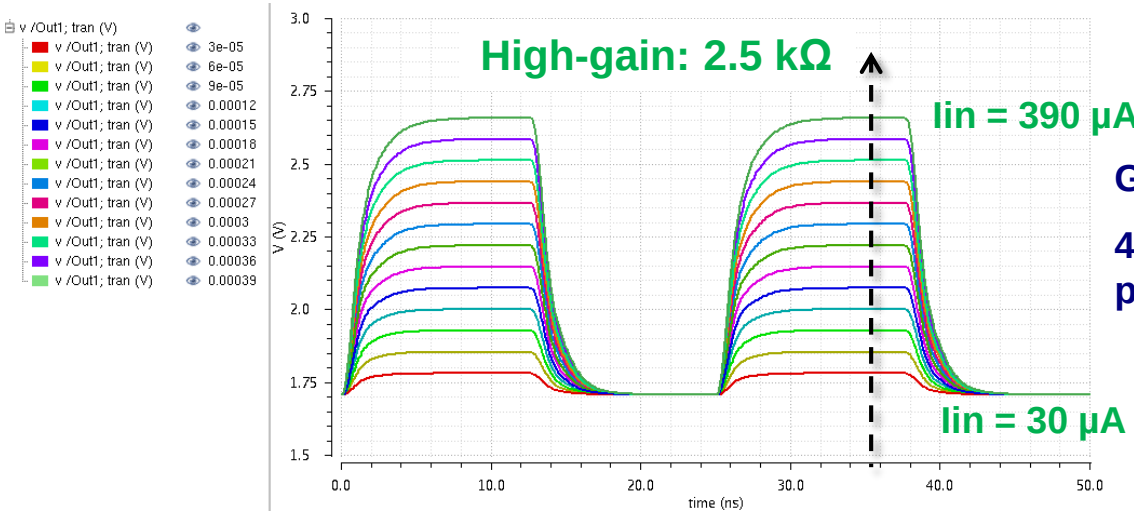
For stable operation in each gain mode, the load resistance linked with the transimpedance gain is also changed.

High gain $R_{LOAD} = R_L$

Low gain $R_{LOAD} = R_L \parallel R_{L1}$

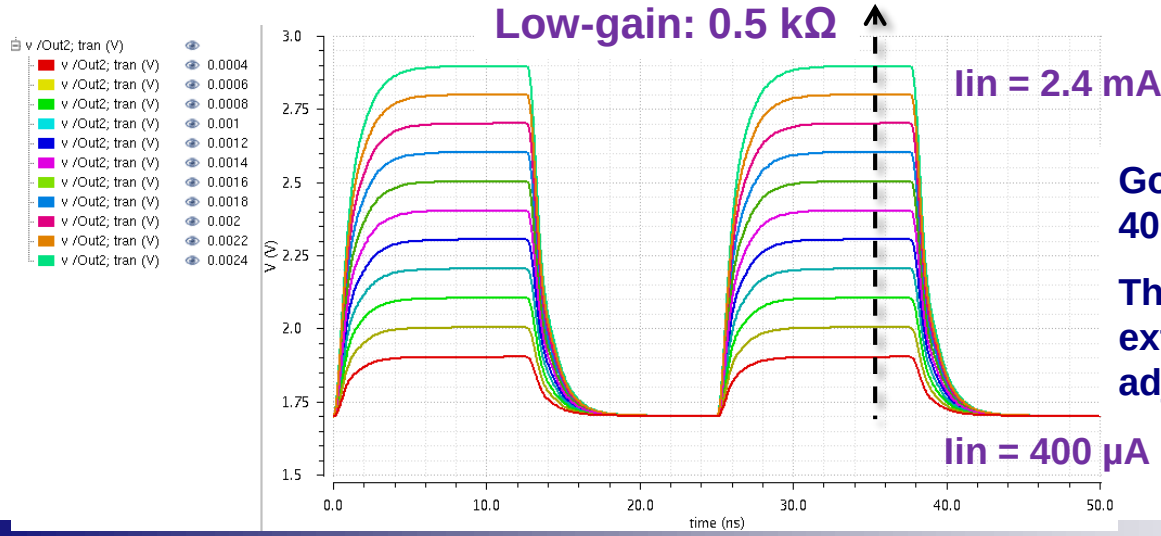
DRX-II chip design (4)

- **Transient response in two gain modes: good linearity & sufficient dynamic range**



Good linearity (±1%) for Iin < 600 µA

400 µA was chose as the gain change point in simulations

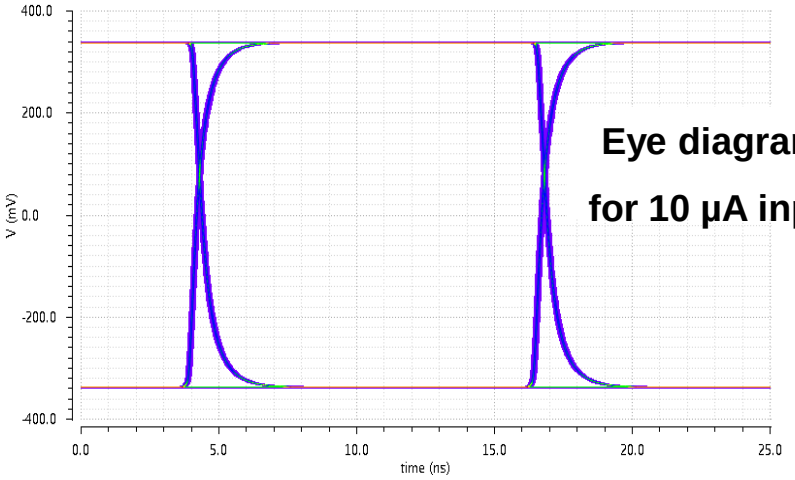


Good linearity (±1%) in the range of 400 µA to 2.4 mA

The gain change point is defined by an external reference voltage, which is adjustable

DRX-II chip design (5)

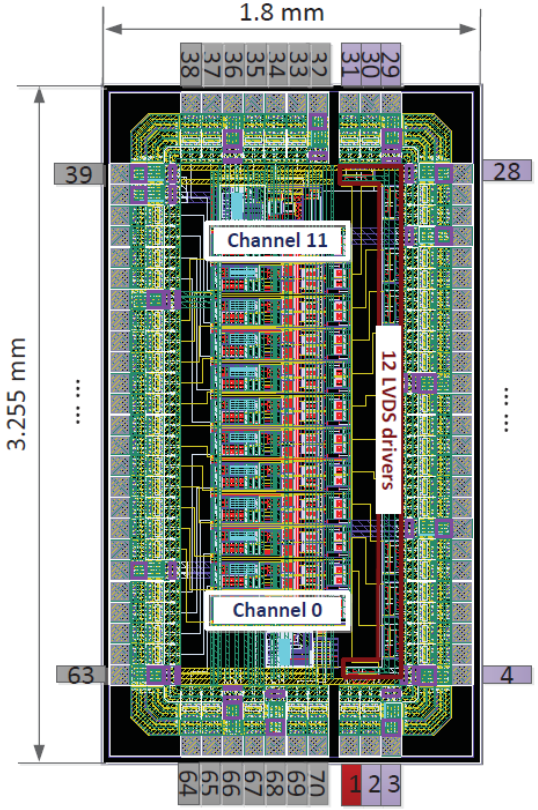
- **Simulated performance of a single channel:**



Eye diagram @ 80Mbps

for 10 µA input with noise

Symbol	Parameters	Typical value	Unit
VDDA/VDD	Power supply	3.3 ± 10%	V
I_p	Supply current	154 to 178	mA/Chip
R_{LOAD}	Output loading	50	Ω
V_{thr}	Individual threshold voltage	0 to 2.5	V
V_GS	TIA gain transition reference voltage	0.45	V
R_T	TIA transimpedance gain	2.5/0.5	kΩ
I_{in}	Linear dynamic input range	10 to 2400	µA
	Data rate	80	Mbps
J_p	Output jitter peak-to-peak	340	ps

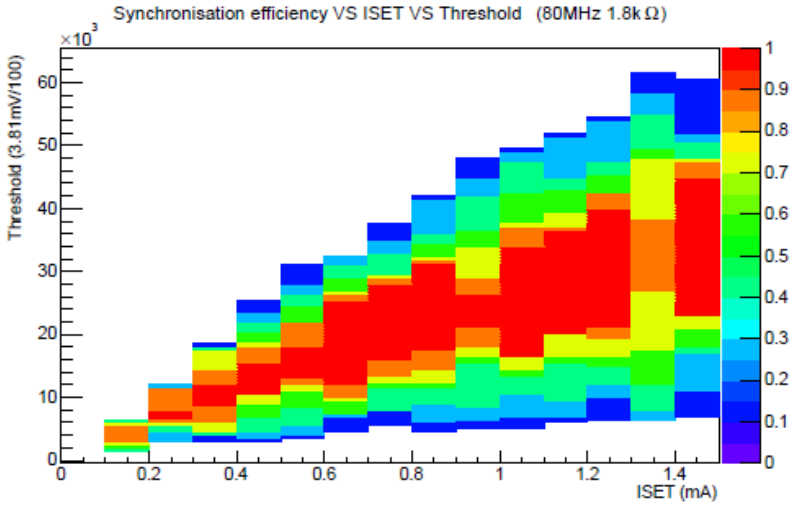


Designed in 2014, using the AMS 0.35 µm CMOS process

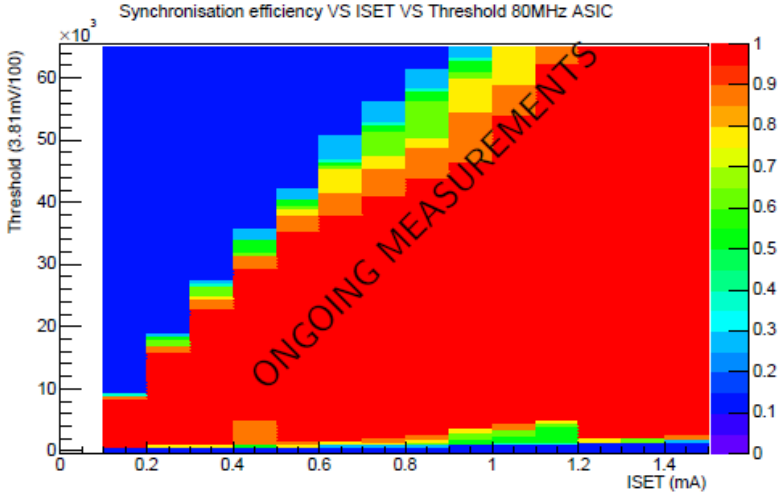
Test results (1)

- **Synchronization test: the BOC over samples the received signals in order to be able to synch its clock with the incoming signal**
- **Keep on sending an idle word and trying to synchronize on it, scanning thresholds of the prototype and the optical power of the optoboard**
- **synchronization efficiency = No. of synchronized channel/No. of total ch.**

Discrete



ASIC Synch

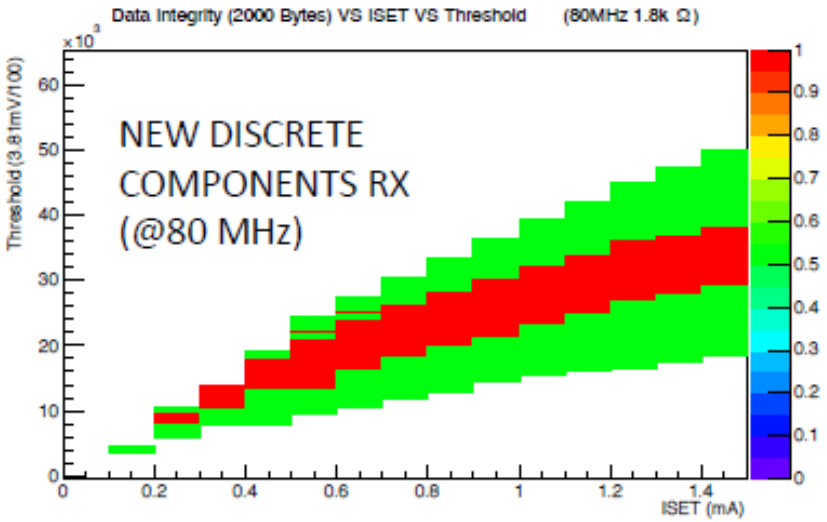


Range of the ASIC significantly broader than the discrete design

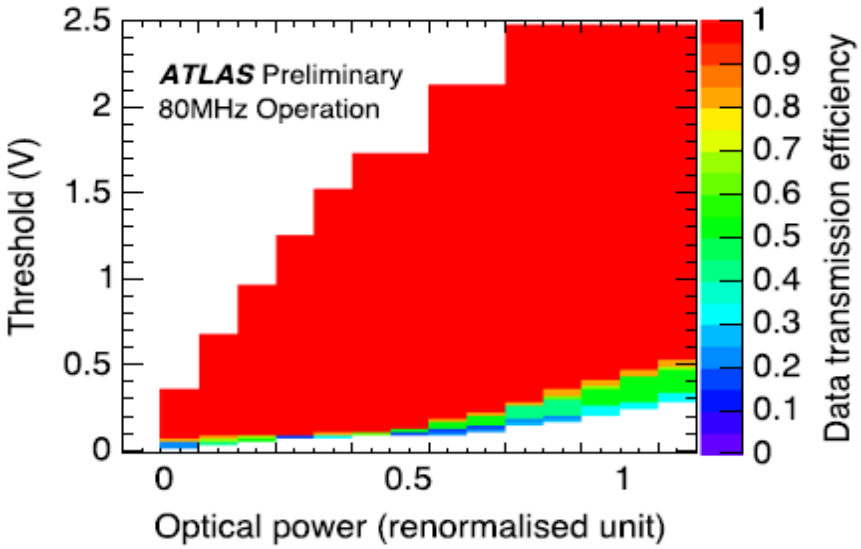
Test results (2)

- **Data integrity test: in the region where the BOC synchronized, scan sending 10 bytes 8b/10b encoded, including start and end of frame words, 200 times for a total of 2000 bytes**
- **Data integrity efficiency = No. of working channel/No. of total ch.**

Discrete



ASIC



Range of the ASIC significantly broader than the discrete design

Test results (3)

- **BER test of the Rx plugins with ASIC :**
  - **Input current of 1.2 mA**
  - **Transmitting 8b/10b encoding data at 80 Mbps**

RX channel	Transmitted Bits	Errors
9	1,036,438,631,340	0
10	1,026,958,157,490	0
11	1,026,956,151,805	0
12	1,026,958,190,122	0
13	1,026,957,957,358	0
14	1,026,953,952,342	0
TOT	6,171,223,040,457	0

BER of the Rx plugins with ASIC less than 10^{-12}

DRX-II chip for L1/L2 upgrade

- **Due to the better performance, DRX-II chip has been selected as the baseline design for the L1/L2 upgrade**

NUMBER OF LAYER 1 RX PLUGINS:	152
NUMBER OF LAYER 2 RX PLUGINS:	104
MINIMUM AMOUNT OF SPARES:	24
TOTAL WORKING RX PLUGINS:	280

- **Chip characterization performed by OSU, Rx plugin mass production made by OSU and BERN**
- **Layer2/ Layer1 has been upgraded during Dec. 2015/2016**

- **Running status ?**

Summary

- IHEP designed a ASIC chip (DRX-II) for the optical links upgrade of the ATLAS Pixel Detector (L1/L2)
- DRX-II meets the requirement well, and offers better performance than the alternative solution.
- DRX-II chip has been used in the new Rx plugins, which have been installed in the Pixel Detector upgraded readout during 2015 to 2016