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Nuclear Instruments and Methods in Physics Research A



journal homepage: www.elsevier.com/locate/nima

Review

R&D paths of pixel detectors for vertex tracking and radiation imaging $\stackrel{ au}{\sim}$

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ARTICLE INFO

ABSTRACT

Article history: Received 4 December 2012 Received in revised form 8 March 2013 Accepted 22 March 2013 Available online 30 March 2013

Keywords: Semiconductor pixel sensor Radiation hardness Vertex trackers at future colliders This report reviews current trends in the R&D of semiconductor pixellated sensors for vertex tracking and radiation imaging. It identifies requirements of future HEP experiments at colliders, needed technological breakthroughs and highlights the relation to radiation detection and imaging applications in other fields of science.

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^{*}This paper was prepared under the auspices of the ICFA Instrumentation Panel and submitted to the European Strategy Preparatory Group for the CERN Council Open Symposium on European Strategy for Particle Physics, Krakow, September 2012.

^{0168-9002/\$ -} see front matter @ 2013 Elsevier B.V. All rights reserved. http://dx.doi.org/10.1016/j.nima.2013.03.040

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1. Introduction

Semiconductor pixel detectors for vertex tracking have provided the much needed technological breakthrough to make decisive advances in the collider exploration of the TeV energy domain and precision heavy flavour physics. Exceptional progress has been made over the last two decades. Comparable improvements in performance in the next two decades for upgrades and future colliders are becoming increasingly more difficult. Since the design of the LHC detectors. Si pixels have become the standard for vertex tracking in the proximity of the interaction region [1]. This report reviews current trends in the R&D of semiconductor pixellated sensors for vertex tracking and radiation imaging. It identifies requirements of future high energy physics (HEP) experiments at colliders, needed technological breakthroughs and highlights the relation to radiation detection and imaging applications in other fields of science. Applications of pixel sensors beyond vertexing, for the main tracker and high granularity calorimetry are also of great interest and are being actively explored, but will not be discussed here. In the following, we consider the LHC luminosity (HL-LHC) and energy (HE-LHC) upgrades and lepton colliders at the intensity (superKEKB and SuperB flavour factories) and energy (ILC, CLIC and Muon Collider (MuC)) frontiers. There is a broad spectrum of other applications of semiconductor pixel technologies developed towards the specifications of these experiments. Their number and diversity is growing, as new facilities put emphasis on specifications, such as frame rate, radiation tolerance and space-time resolution, which are the primary focus of the HEP-driven R&D. Examples of the fields where pixels developed from results of R&D for collider experiments include imaging at light sources [2–4] and free electron lasers (FELs) [5], including hybrid [6] and DEPFET [7] technologies, transmission electron microscopy (TEM), with hybrid [8,9] and monolithic sensors [10,11], plasma diagnostics, biological imaging [12], auto-radiography, with hybrid and monolithic CMOS [13] and DEPFET [14] pixels, fluorescence microscopy, with monolithic pixels [15], and medical imaging, with hybrid pixels [16], beam monitoring and diagnostics for future accelerators, ion-beam analysis [17] and real-time dose delivery assessment and quality assurance in hadron therapy [18,19]. There are also examples of returns of these developments to the benefit of HEP applications, as discussed in Section 5. In the next chapters we identify some key R&D areas to enable the next generation of collider experiments and then review major trends in semiconductor technology relevant to sensor fabrication, readout electronics, services and system-level issues and the availability of test facilities to support the R&D effort.

2. Requirements and R&D perspectives

The main purpose of Si pixel sensors in collider experiments is the accurate reconstruction of the trajectories of charged particles in the proximity of the beam collision point. The discovery of a light, Higgs-like particle by the ATLAS [20] and CMS [21] experiments at LHC places special emphasis on the identification of b-, c- and τ -jets in the physics program at high energy collider experiments.

2.1. Charged particle extrapolation resolution

The standard figure of merit for vertex tracking accuracy is the accuracy on the impact parameter, σ_{IP} , defined as the distance of closest approach of the particle track to the colliding beam position. This can be parametrised as: $\sigma_{IP} = a \oplus (b/p \sin^k \theta)$, where *p* is the particle momentum, θ the track polar angle and k=3/2 for the $R-\Phi$ and 5/2 for the *z* projection. The identification of hadronic jets

originating from heavy quarks is best achieved by a topological reconstruction of the displaced vertex structure and the kinematics associated to their decays. The ability to reconstruct the sequence of primary, secondary and tertiary vertices depends on the impact parameter resolution. This is related to the single point resolution of the sensors and their geometry. The figure of merit for the resolution is the distribution of the impact parameter values for charged particles originating from *b* hadron decays. It is useful to recall that the impact parameter does not depend, to a first approximation, on the *b* hadron energy, since the angle of production of the track in the lab frame $\propto (\beta \gamma)^{-1}$, which compensates the $\beta \gamma$ term in the b hadron decay length. The average impact parameter value is \sim 220 µm, with a 0.15 (0.24) fraction of tracks having impact parameter below $15(35) \mu m$. The asymptotic resolution *a* is typically proportional to the sensor point resolution, the tracking lever arm and, to a lesser extent, the radial position, R, of the first layer. The multiple scattering coefficient, b, scales $\propto \sqrt{dR/p}$, where d is essentially the material thickness of the beam pipe and the first layer. The tracking lever arm is constrained by detector volume, number of electronics channels and cost. The minimum detector radius is typically defined by radiation or particle density conditions from particle fluence and beam-induced backgrounds and it is accelerator dependant. This was 63 mm at LEP and 25 mm at SLC, is 30-50 mm at the LHC, with plans to further reduce it and should be 15-30 mm at future lepton colliders.

2.2. Radiation hardness

At hadron colliders the location of the detector closest to the collision point depends on the radiation levels and their effects on the sensors and readout electronics. The radiation levels for the inner layers of ATLAS, CMS and LHCb upgrades with neutron equivalent fluences beyond 10¹⁶ n cm⁻², or an ionising dose of 10 MGy, significantly degrade traditional sensors of several hundreds μm thickness and require novel approaches. In the case of ALICE, with doses of about 10^{13} n cm⁻² and ~7 kGy, the limitation comes from safe operation of LHC. Radiation effects in silicon detectors can be distinguished in two main categories, depending on the type and energy of particles impinging on the sensors: ionising and non-ionising effects. Ionising radiation affects the surface oxide layers of sensors and electronics with the creation of conductive electron accumulation layers, lateral isolation oxides of MOSFET transistors and buried oxides in SOI devices. In sensors, these can be compensated by the deposition, under the oxide, of a p-doping layer commonly called p-spray. This effect is dominant in detectors used for X-ray imaging, electron microscopy or diagnostic at synchrotron light sources but its effects are present as well in vertex detectors at colliders. Non-ionising radiation effects consist in damage to the crystal lattice of the Si bulk and its primary consequence is the generation of defects in the material formed by the combination of vacancies and interstitials with dopants and impurities present in its lattice after the sensor processing. When the radiation environment is made of particles of different species and energies, it is customary to express the fluence normalised to the equivalent effect of 1 MeV neutrons.

2.2.1. Hadron colliders

The radiation levels at hadron colliders increase with luminosity and decrease with the radial distance from the beam. In the scenarios of energy upgrades, the dose scales with the inelastic cross-section within the geometrical acceptance and the expected damage increases proportionally to particle multiplicity, which rises logarithmically as function of the beam energy, when beam related backgrounds are not the dominant source of damage. Vertex detectors at the LHC will be exposed to a fluence, mostly due to charged hadrons, ranging from 1 to 3×10^{15} 1 MeV neutron equivalent cm⁻² after an integrated luminosity of 300 fb⁻¹ up to $\sim 10^{16}$ n cm⁻² after ~ 3000 fb⁻¹ at a radius of 32 mm in the general purpose experiments and for the innermost tip of the LHCb VELO upgrade detector after 100 fb⁻¹.

Neutron and charge hadron irradiation introduce defects at different band-gap depths which can be positively or negatively charged. The dominant radiation induced defects in the middle of the Si bandgap are negatively charged and affect most of the macroscopic silicon sensor parameters. These defects can act as efficient generation centres and affect the space charge as acceptors. In n-type bulk, after a fluence which corresponds to an introduction rate equivalent to the original doping concentration the bulk is fully compensated. In this condition, typically obtained at a fluence of $2-3 \times 10^{13}$ n cm⁻², the full depletion bias voltage is reduced to a minimum. For even larger fluences, the negative space charge from the radiation-induced deep acceptors prevails and the bulk becomes type-inverted. The consequence is the presence of a double junction and an increase of full depletion bias voltage. Oxygen homogeneously diffused in the material has shown to slow down this effect [95]. Beneficial and reverse annealing have also been observed and the latter is also affected by the presence of oxygen [96]. Above 1×10^{15} neutronequivalent cm⁻², the dominant effect is charge trapping [97,98]. In ptype silicon the net effect is an increase of negative space charge at high fluences, after a mild initial decrease therefore without type inversion and double junction.

Concerning the non-ionising radiation effects, many macroscopic bulk parameters of Si detectors change due to irradiation. These include increased leakage current and negative spacecharge build-up. Space-charge build-up controls the reverse bias voltage needed to generate the *E* field across the device. At high doses, high electric fields appear at both electrodes and the electric field in the centre of the sensor is significantly reduced. at reasonable values of the applied bias. Together with charge trapping, this ultimately limits the signal efficiency of the detector. The most important parameter for an irradiated detector is the amount of collected charge as a function of the bias voltage, which is affected by the increase of the charge trapping due to the radiation induced trapping centres that partially remove charge carriers. The density of traps is assumed to increase linearly with fluence. The effective drift length, which expresses the length a carrier can drift before being trapped by a defect, is proportional to the carrier's trapping time and its drift velocity, which reaches a saturation value of $\sim 10^7$ cm s⁻¹. This length is $\sim 50 \,\mu\text{m}$ for electrons at 5×10^{15} n cm⁻². Operation at high electric fields leads to a consequent reduction of the carrier trapping probabilities and consequently to higher signal efficiency. In addition faster signal is achieved by collecting the electron current which have larger mobility. Pixel sensors readout from the n + implant (n-in-n or nin-p geometries) provide noticeably higher charge collection than standard p-in-n detectors after irradiation, as discussed in Section 3.2. Radiation damage effects on the detector operation include: (i) depletion voltage, which in traditional planar sensors rises above 600 V and reaches ~1000 V for 5×10^{15} n cm⁻² in the case of the ATLAS IBL pixel detector layer 32 mm away from the LHC beam. (ii) Charge trapping which reduces the signal. (iii) Increase in leakage current with consequent increase of the noise and the power dissipated by the module. This could trigger a positive feedback effect that forces the module into thermal runaway and requires operation well below 0 °C. (iv) Reverse annealing, where negative space charge builds up after irradiation. This effect can be controlled by oxygenating the silicon bulk and, again, by keeping the sensors below 0 °C. The cause of reverse annealing is presently not completely understood.

At present, the most effective way to improve the radiation hardness of Si sensors is by engineering their geometry to allow the highest possible electric field to be applied across their sensitive region. This includes thin and 3D sensors, the latter offer a larger signal charge for perpendicular tracks although at the price of a larger pixel capacitance. The comparable small bias voltage has the potential for lower power dissipation in the sensor, which otherwise would become comparable to that of the readout circuitry at the expected radiation levels. The ATLAS experiment will install 3D detectors in parts of the inner layer during the first LHC long shutdown, and obtain valuable operational experience with these devices. Other materials, like diamond, could also be considered for their better noise performance, as discussed in Section 3.5. Finally, the charge multiplication phenomenon observed after neutron and hadron irradiation in both planar [99] and 3D sensors [104], interpretable as the onset of a high electric field region where signal charge is multiplied through impact ionisation, could be used to the advantage of enhanced detector operation, if it can be controlled. An additional challenge specific to the LHCb detector and forward physics experiments is the highly non-uniform distribution of the dose on the detectors, inserted in a secondary vacuum perpendicularly to the beam axis, leading to radiation associated annealing effects at one edge of the sensor but not the other, while high voltages have to be applied to extract charge from the irradiated side of the sensor.

2.2.2. Lepton colliders

The radiation environment is radically different at lepton colliders, where it is the hit density from the beam background and not the deposited dose to define the position of the innermost layer. At the ILC, there is an estimated 1.5×10^{12} hits cm⁻² year⁻¹ of low momentum background electrons at a radius of 15 mm, corresponding to 1.5 kGy for a three-year operation period, or a non-ionising radiation fluence of $\simeq 2 \times 10^{11}$ 1 MeV n-equivalent cm⁻² [22]. At superKEKB and SuperB, the equivalent fluence is 2×10^{12} and 5×10^{12} n cm⁻² year⁻¹, respectively. These low doses allow the possible implementation of a rich array of technologies which cannot be considered in the hadron collider radiation environment. Still, radiation damage needs to be considered, in particular for monolithic pixel technologies, which have been tested up to doses of several tens kGy and fluences in excess to 10^{13} n cm⁻² [23–27].

2.2.3. Applications beyond HEP

These developments extend the applicability of pixel sensors to other fields, such as electron microscopy and imaging at XFELs, where conventional imaging devices, such as CCDs, have limitations due to the radiation conditions and readout speed. In TEM, radiation tolerance requirements depend on the mode of operation. For example, operating in diffraction mode, may induce large numbers of electrons to be contained in a limited number of Bragg spots, causing large doses to be received over small areas. Given that a very intense bright field image could deposit order of 0.1 Gy s⁻¹ pixel⁻¹, a target radiation tolerance of at least a few tens of kGy enables the use for more than one year. At the European XFEL, the expected dose is quite comparable, reaching up to \sim 30 kGy per year of operations. One important difference compared to HEP applications is the absence, or the reduced importance, of bulk damage given the small energy transferred by the soft X-rays and electrons.

2.3. Space-time granularity

The two main drivers for the sensor pixel pitch, *P*, are the single point resolution, which scales as *P* and the local occupancy, which scales as the pixel area (i.e. $\propto P^2$ for square pixels) times the readout time. The first pixellated Si device used for vertex tracking

in a particle physics experiment was the CCD doublet installed next to the target in the ACCMOR experiment at CERN [28] in 1985. It had the pixel density foreseen for the next generation of vertex trackers at the STAR HFT at RHIC and at lepton colliders, but on a surface three orders of magnitude smaller. This was motivated by both the expected track density next to the target and the required extrapolation resolution to study charm decays.

2.3.1. Pixel pitch

At collider experiments, the single point resolution has played so far a major role in determining the pitch of microstrip detectors adopted at LEP [29-33] and the pixel size of the CCD at SLC [34]. With a track density of just 0.004 tracks mm⁻², the LEP detectors could adopt microstrips at a readout pitch of 50 μ m, resulting in an occupancy of \sim 0.02 and 1D single point resolution of \sim 7 μ m. At LHC, where the local track density was estimated to be an order of magnitude larger in pp. and up to two orders of magnitude in central PbPb, collisions with an average *b*-jet energy within a factor of two compared to LEP, the size of the pixel was similar to the LEP pitch in one projection, achieving a comparable asymptotic track extrapolation $a \simeq 20 \,\mu m$, while the other projection was optimised accounting for occupancy and surface available for the front-end electronics and the detector thickness to avoid broken clusters for inclined tracks. For the LHCb VELO upgrade [35], the target pixel size of $55 \times 55 \,\mu m^2$ is still determined by the tracking resolution requirements to resolve the oscillations of neutral B mesons, with a decay time resolution of the order of 50 fs. For the upgrade planned for 2018 ALICE aims at an *a* value of \sim 2.5 µm, requiring a point resolution of ~4 µm and an inner radius of ~25 mm. The evolution of the pixel density vs. year of start of operation is summarised in Fig. 1.

Since the typical charge carrier spread is ~7 µm in a 300 µm-thick fully depleted pixel and ~15 µm in 15 µm of an undepleted CMOS sensor, there is limited interest in pushing the pitch much below 10–20 µm, except for imaging applications, where pixels of 5 µm are used in electron microscopy, thinner depleted sensors or CCDs. At these sizes, pixel sensors have already obtained single point resolutions of 1–2 µm. owing also to good signal-to-noise values, [36,37], corresponding to an asymptotic extrapolation resolution \leq 5 µm. Track density is expected to become relevant in driving the pixel space granularity.

At LHC displaced decay vertices and high track density in the core of highly boosted jets already lead to merging of hits in the pixel layers. The further increase in rate with the LHC upgrades and the



Fig. 1. Evolution of the pixel density vs. the year of start of operation of Si pixel vertex trackers. High density detectors motivated by point resolution were developed over small surfaces in the early years. The subsequent trend towards increasing pixel densities is driven by occupancy and it will match the requirements of high point resolution for future collider projects. The total detector surface, indicated by S, in given in cm².

short bunch spacing, or large continuous background flux, at high energy lepton colliders, such as CLIC and a MuC respectively, push the design of the sensors to be located closest to the interaction region towards smaller cells, driven by both occupancy and two-track separation, which again scales $\propto P$. At a linear collider, both background and physics track density are important. The innermost radius of the vertex tracker is determined by the density of incoherent pairs produced and deflected in the e.m. interaction of the two bunches. Two-track separation is challenged by particle density in the core of boosted hadronic jets where the minimum distance between two contiguous hits on the first layer of the vertex tracker has a most probable value of ~400 µm in $e^+e^- \rightarrow H^0Z^0 \rightarrow b\overline{b}q\overline{q}$ events at $\sqrt{s} = 500 \text{ GeV}$ and just $\sim 240 \text{ µm}$ in $e^+e^- \rightarrow H^0 A^0 \rightarrow b\overline{b}\overline{b}\overline{b}$ events at $\sqrt{s} = 3$ TeV. Typical two-track separation is $2-3 \times P$, depending on the cluster size. In the case of flavour factories, the advantages of pixels over short strips, or "striplets", are found in the more reliable performance in high background scenarios thanks to their lower occupancy and are therefore the technology of choice for BELLE-II and SuperB at full luminosity. A study performed for SuperB compares the physics sensitivity in time-dependent analyses normalised to the number of reconstructed physics events for striplets and pixels of equal thickness and resolution. The relative degradation of the sensitivity for pixels is a factor five lower compared to that for striplets, assuming a background rate up to five times the simulation expectation to include a safety factor [38]. An example of extreme requirements in terms of pixel size to limit occupancy, without exploiting fast readout or time stamping, is offered by the Fine Pixel CCD (FPCCD) concept proposed for the ILC vertex tracker, based on fully depleted, $5 \times 5 \,\mu\text{m}^2$ pixels with multi-port, low-noise readout [39].

2.3.2. Time stamping

More in general starting with the current LHC detectors, fast time-stamping, required by occupancy, has become part of the overall optimisation and we have to consider the space-time granularity as the appropriate parameter space for any future vertex detectors. New approaches, such as ultra-fast timing exploiting charge multiplication in thin sensors, are being investigated. Fast time stamping is of special importance in occupancy reduction at accelerators with long trains of closely spaced bunches, such as a linear collider. This has obvious benefits beyond HEP for applications such as fourth generation light sources and FELs. In these applications there is comparable interest in reducing the pixel pitch from the current 100–500 μ m down to ~50 μ m or even less. The burst-mode time structure of the European XFEL imposes to store images in the detector front-end during the full bunch train for subsequent readout during the inter-train period. The area required for memory puts severe limits on the minimum pixel size that can be achieved. This limitation will be eased by the reduction in feature size of the CMOS processes and by accessing 3D integrated technologies, discussed below.

2.4. Sensor thickness

In collider experiments a reduction of the detector thickness is highly desirable because it minimises the amount of multiple scattering experienced by charged particles, in particular in the first layer(s) of the vertex tracker, as well as the number of radiation lengths of material placed in front of the calorimeters. This has implications on the precision of extrapolating (mostly soft) particles back to their production vertex and on the amount of energy loss by radiation before the calorimetric measurements.

2.4.1. Multiple scattering

The track extrapolation resolution for several Si vertex detectors is given in Fig. 2. It is interesting to observe that even at multiTeV collision energies there is a sizable fraction of final state hadrons which do not exceed a few GeV in momentum. As an example, the fraction of charged particles originating from a Higgs boson decay to a pair of *b* quarks and having a momentum below 2.5 GeV/*c* ranges between 0.24 and 0.19 for pp collisions from $\sqrt{s} = 8$ TeV to 30 TeV and between 0.26 and 0.19 for e⁺e⁻ collisions from $\sqrt{s} = 0.5$ TeV to 3 TeV. At flavour factories and in heavy ion collisions, most of the decay products from heavy hadrons are soft particles. Thinner sensors are also less susceptible to δ -ray emission, resulting in a displacement of the collected charge w.r.t. the particle point of impact. Sensor thickness accounts for only part of the total material budget of vertex tracking systems, with support structures, cooling and other services often being the dominant contribution.

2.4.2. Hybrid pixels

In the sensitive part of the ATLAS pixel detector the sensors with their readout electronics account for 17% of the total material, the largest contribution being due to the mechanical structure and cooling components at 58% [40]. The present ALICE pixel detector is the lightest vertex detector among the LHC experiment with a total material budget of 1.14% X_0 /layer, where the contribution of the sensor and front-end electronics (FEE) chip amounts to 33%. Still, the availability of thin sensors is important to precision vertex tracking. In particular, this is the case in experiments where high flavour tagging efficiency, such as high-energy lepton colliders, or reconstruction of low momentum short-lived hadrons, such as *b*-factories and heavy ion experiments, is of paramount importance to their physics program. Thin sensors are also valuable to imaging applications, for example in TEM where the reduction in multiple scattering improves the point spread function (PSF).

The practical thickness is tightly linked to the amount of signal charge collected for a minimum ionising particle. This has to be compared to the intrinsic single pixel noise in terms of the achievable signal-to-noise ratio (*S*/*N*). The *S*/*N* determines the detection efficiency, taking into account charge sharing on neighbouring pixels, discriminator threshold setting and threshold variations, and also the single point resolution, in particular if analog readout with charge interpolation is used. The efficiency starts to degrade for *S*/*N* values below 20 per pixel. A minimum ionising particle generates in Si a most probable value of ~80 e⁻ µm⁻¹. With a typical noise of less than 200 e⁻ ENC, taking into account the minimal threshold of the readout chip which allows stable operation, including threshold variation, a 250–300 µm thick hybrid pixel sensor, as those employed in the ATLAS and CMS vertex trackers, the resulting *S*/*N* ensures a comfortable margin for detection efficiency, but imposes a multiple



Fig. 2. Extrapolation resolution vs. track momentum for past, present and future Si vertex detectors.

scattering burden of almost 2% X₀, when also the readout chip is accounted for. This is becoming more important for the next generation of vertex trackers. The reduction in material, obtained by shifting inactive components out of the sensitive region and reducing the contribution of cooling and flex cables, in the upgrades brings the attention back to the active components. In CMS, the sensor+readout-chip will contribute 56% of the material of a single ladder, up from 42% for the current detector. The readout chip contributes significantly to the material budget and a main limitation to its thinning has been the bending at the high temperatures used for re-flow during the flip chip process. In the case of the current FE-I3 ATLAS pixel chip, with an area of 0.8 cm², a thickness of 190 µm is adequate, but the 4 cm^2 FE-I4 chip had to be supported by a handle chip substrate to safely bond it at a thickness of 150 µm. New flip chip techniques have been developed for the next generation of hybrid pixel modules for LHC upgrades to reduce the chip contribution to the material budget [40]. To further reduce material electromechanical integration and interconnect are under extensive study. One area of research are silicon through vias (TSVs) which allow a direct connection from the bump bonded readout ASIC to the back side of the silicon. This avoids wire bonds, increases geometrical acceptance and allows a leaner electro-mechanical architecture (see Section 3.4).

2.4.3. Monolithic pixels

Much thinner active lavers can be afforded by monolithic CMOS and DEPFET technologies, introduced in the R&D for the linear collider, where the pixel cell measures $\mathcal{O}(10 \times 10) \,\mu\text{m}^2$ with a typical capacitance of $\mathcal{O}(1)$ fF and 10–40 e⁻ ENC of noise. An active thickness of 15-20 µm is sufficient for achieving a detection efficiency \geq 99% with CMOS pixels, even at operating temperatures in excess to 40° [41]. Back-thinning technologies available as commercial service, such as grinding and chemical etching, have been successfully applied to make 40-50 µm-thick CMOS sensors for the STAR HFT at RHIC [42] and in the R&D for the linear collider [43] and are foreseen for the SuperB [44] vertex detector. The ALICE upgrade baseline design is also based on monolithic pixels for an overall material budget $0.3-0.4\% X_0$ /layer with the sensor contributing $\sim 15\%$ [45]. DEPFET sensors can be thinned to $< 100 \,\mu m$ in the sensitive region, using a wafer bonding technology, retaining a frame which ensures the stiffness of the mechanical module [46]. Thin DEPFETs are under development for BELLE-II, where the target thickness is 75 μ m, and first results have been obtained for prototypes successfully thinned to 50 µm [47,48]. Given that the reverse bias voltage, V_d , required to depleted a given thickness *d* scales as d^2/ρ , where ρ is the Si resistivity, a modest V_d of $\mathcal{O}(10 \text{ V})$ is sufficient to fully deplete a thin layer of high resistivity Si. Sensors of this thickness are compatible with the needs of *b*-factories and for achieving a material budget of ~0.1% X_0 /layer, needed to meet the value of b~10 μ m for the multiple scattering contribution, identified as a requirement at a linear collider. For sensors of this thickness, the ladder support is of major importance for counteracting the chip warping and insuring the module stability and planarity. In the design of thin ladders for applications at *b*-factories, STAR and the linear collider with thin sensors, as well as those for an LHC upgrade, the Si ceases to be the largest single factor in the overall layer material budget which becomes the cable routing signals, power and clocks. The PLUME collaboration is addressing some of these challenges [49]. In order to progress towards thinner modules, sensor stitching, with clocks and signals routed on metal lines in the chip, appears a promising path. The development of very light double-sided ladders, which are advantageous mechanically and offer hit correlation to reject low energy particles from beam background, appears promising.

2.4.4. Applications to TEM and soft radiation

Progress with thin sensors benefits other applications involving soft radiation, where multiple scattering and δ -ray production is an issue. In TEM, replacing phosphor-coupled CCDs with direct detection on CMOS sensor is the latest trend in imaging [10,50,11], to decrease the PSF and enhance the detection guantum efficiency and imaging contrast ratio. Multiple scattering in the sensor is a major limitation, since the typical electron energy is in the range 60–300 keV. CMOS sensors, with a \simeq 15 µm-thick sensitive volume, thinned to 50 μ m improve the contrast ratio by a factor 1.5 and the PSF by 1/3 compared to 300 um-thick sensors of the same design [11]. Thin monolithic sensors are well suited for the detection of soft X-rays and charged particles in applications from XFEL to solid-state dosimetry by thinning the sensor to the boundary of the sensitive layer (depleted or epitaxial) and using it in backillumination configuration [51–53]. Thinning is important to open transparent windows to soft radiation but the thickness of the readout chip is not limited in these applications as for vertex tracking. Therefore the possibilities offered by the 3D ASIC developments, discussed in section 3.4, can be fully exploited.

2.5. Energy resolution

Typical HEP applications do not place emphasis on the resolution of the energy deposited in the pixels. However, there are examples of the use of dE/dx measured in the Si trackers for improving momentum resolution [54] and performing particle identification [55] at low momenta, also applicable to proton tomography [56]. Pixellated semiconductor sensors may offer energy resolution comparable to that of commercial spectroscopy detectors with the added benefits of spatial resolution. Fully depleted CCD on high resistivity substrate [57], developed mostly for astronomical applications, have an energy resolution of ~150 eV FWHM at 5.9 keV and are successfully applied in imaging and XRF analyses at light sources and for plasma diagnostics [58]. Similarly, pnCCDs have demonstrated excellent energy resolution and are used at LCLS [59]. The very low input capacitance and in-pixel charge to current conversion of monolithic pixel sensors are advantageous in terms of pixel noise and makes them attractive for applications requiring good energy resolution at relatively high frame rate. DEPFET sensors, derived from R&D for the ILC vertex tracker [60], have demonstrated singlepixel energy resolution of 130 eV at 5.9 keV. They are being developed for use in satellite missions for X-ray astronomy [61] and planetary observation [62] and X-ray light sources [7]. SiC pixels have obtained an energy resolution of 196 eV at 5.9 keV [63] and CMOS LePix sensors gave 143 eV [65]. Pixels in SOI technology are also being developed towards applications in X-ray detection. Their noise performance is not yet a match to the examples above, due to the larger pixel capacitance and leakage. However, there are promising R&D avenues to make these sensors applicable to X-ray astronomy [66]. In addition, back-plane post-processing to create a thin entrance window, offering enhanced spectral sensitivity to soft X-rays has been demonstrated [53].

3. Semiconductor technology trends

Recent developments in the field of microelectronics are leading to a performance leap for detector systems, in particular pixel sensors, thanks to an aggressive scaling of the feature size of CMOS technologies.

3.1. CMOS process feature size

Commercial silicon foundries have been able to offer a density advantage of a factor of two at every 18-month generation, and are now capable of offering high volume technologies with features well below 100 nm, with the main goal of increasing performance and density of large digital systems. The industrial road-map foresees the introduction of processes below 15 nm by 2015, accompanied by the further development of many special technologies, such as vertical integration, integration of special features such as bipolar, germanium-doped or power devices. SOI devices and many others. Microelectronic design based on CMOS scaling has to tackle bottlenecks, such as the length of interconnections. Many of these have already been overcome through engineering creativity and, of course, investments. In the future, for thin oxides gate leakage and voltage swing become a concern. particularly for monolithic CMOS active pixels. 3D integration of two or more vertically interconnected layers of CMOS circuits promises to help by shortening connection paths and by increasing functional density [67,68]. 3D techniques can be exploited in the fabrication of multilayer electronic devices, where each layer is based on a different technology and optimised according to its function (sensing, analog and digital signal processing, storage and data transmission).

The CMS phase-1 upgrade [69] is still in 250 nm technology but 65 nm CMOS is foreseen for the phase 2 and the development of readout chips for the LHCb [35] and ATLAS upgrade (FE-I4) [70] are in 130 nm technology. The design of complex embedded trigger logic for more intelligent vertex trackers are in 65 nm and with obvious advantage of high-speed logic such as that needed in fast data links [71]. Validating such technologies requires assessing their reliability in high radiation environments and great progress has recently been made in proving the robustness of commercial 65 nm CMOS [72]. Nonetheless, still more work will be necessary and should be funded to assess the potential of 45 nm and below. The densities and feature size offered by these technologies will vield more functionality and better analog and digital performance. The time and costs of developing and perfecting chips in these new technologies are felt to be a limiting factor. The boom and bust cycle, which dominates particle physics in terms of long development times alternating with experiment construction, leads to great difficulties in developing ASIC with the performance necessary for future experiments (see Fig. 3). To this end experiments and R&D collaborations support the diversification of applications between particle physics, medical applications, instrumentation of beam lines, surveying detectors and so on, in order to make the incremental steps necessary to master new semiconductor technologies.

3.2. Hybrid pixels

3.2.1. Planar sensors

Fabrication technologies for planar pixel sensors have been well established for several decades. P-on-n pixels were first introduced and are the simplest to fabricate, since they require a single side technology without need for surface isolation layers between p-type pixels. As an example, they are currently used in the ALICE experiment at the LHC [73]. P-on-n pixels have also been fabricated on epitaxial silicon, an interesting solution in case thin active layers are required [74], with promising features of higher radiation hardness, as demonstrated by studies on pad detectors [75]. The two main options currently available for planar pixels are those featuring n-side signal readout, i.e. n-on-n and n-on-p, to exploit the higher mobility of electrons with respect to holes, which results in faster signals and higher radiation tolerance [76]. N-on-n pixels were developed in the 90's and were finally the sensors choice for the ATLAS and CMS pixel detectors [77,78]. The entire pixel side (front side) is kept at ground, so there is no risk of micro discharges between the sensor and the readout chip after bump bonding. Isolation between n-type pixels is achieved by surface p-type implantation (p-stop, p-spray or moderated p-spray) [79,80]. The back side must also be patterned to have a sufficiently wide gap (often hosting floating guard rings) between the main junction where the reverse bias voltage is applied and the cut edge of the sensor, that must be at ground. Thus, a double side fabrication process is required, with impact on costs. N-on-n pixels with slim edge ($200 \ \mu m$) made on $200 \ \mu m$ thick substrates have been recently adopted for the production of the planar pixels for the ATLAS IBL [81].

An interesting and less expensive alternative are n-on-p sensors, that need a simpler, single-side technology (only the pixel side is patterned). This option has been considered since p-type detector grade silicon has become routinely available and n-on-p pixel sensors are currently developed at different facilities in view of the upgrades at the LHC [82]. Comparable performance have indeed been observed for n-on-n and n-on-p sensors in terms of charge collection efficiency after large radiation fluences [76]. A disadvantage of n-on-p sensors is that the edge on the pixel side is at same potential as the bias and can be very high for irradiated devices. To avoid risk of micro discharges between sensor and readout chip, special passivation treatments of the sensors are required (e.g. a benzocyclobutene layer [83]). Another disadvantage with the "n-on-p" approach is the lower design flexibility for reducing the dead area at the edge, because the guard rings are on the same side as the pixels. The minimum edge so far achieved with "n-on-p" hybrid pixel sensors is 450 µm [84].

3.2.2. 3D sensors

3D pixel sensors [85] have been the object of extensive R&D in the past years and will play a major role in future experiments at large luminosity colliders. The successful fabrication of more than 300 3D sensors compatible with the FE-I4 readout chip for the ATLAS IBL has also demonstrated that 3D sensor technology is suitable for medium volume productions [86].

Two different 3D processing options exist, single-side and double-side. The first was originally fabricated at SNF (Stanford



Fig. 3. Time elapsed between concept, prototyping and application at a collider experiment for various semiconductor pixel detector technologies, ranging between 10 to over 20 years. With the progress in semiconductor technologies the time from concept to first demonstrator decreased, while the detector complexity and the reduced number of experiments have lengthened the time required to the deployment in collider detectors.

U., CA, USA) [87] and is now also available at SINTEF¹ [88]: column etching is performed by DRIE (Deep Reactive Ion Etching) all through the substrate from the front side of the sensor wafer for both types of electrodes, at the same time implementing active ohmic trenches at the edge, whereas the bottom side is oxide bonded to a support wafer. This requires extra steps to initially attach and finally remove the support wafer. The second option is a double-side process, independently developed by CNM (Barcelona, Spain) and FBK (Trento, Italy) in slightly different versions: junction columns are etched from the front side, ohmic columns from the back side, without the presence of a support wafer. In CNM sensors, columns do not pass through but stop at a short distance from the surface of the opposite side [89]. This was also the case for the first prototypes of FBK sensors [90], but later the technology was modified to allow for passing through columns. Also for 3D sensors, both single-side and double-side, n-type collection electrodes are preferred, and n-type pixels are isolated by surface p-type implantation (p-spray or p-stop) to isolate the nelectrodes after radiation which induces an electron layer at the silicon oxide interface. Double-side 3D sensor fabrication is simpler and faster because it avoids the support wafer and related process steps, with the additional advantage of having the backside accessible to apply the bias voltage. On the other hand, in the absence of the support wafer, active edges cannot be obtained. The active edge has dopants which have been either implanted or diffused on the entire edge lateral surface to properly terminate the electric field lines. In this case the dead area at the edge can be as short as the implant thickness (few microns) and there are no guard rings. As an alternative, slim edge solutions have been implemented. A slim edge is shorter than the sensor thickness and the edge can be either passivated or guard rings [91] or guard fence electrodes [92] are used to control the electric field bulge to reach the edge. The dead area at the edge is of the order of 200 µm or lower for optimised designs.

3.2.3. Future directions

Future directions for pixel sensors involve lower material budget (lower thickness), very slim edges and higher radiation tolerance. On the fabrication side, substrate thicknesses in the order of 150 µm are still suitable for production with standard equipment. Lower thicknesses can be obtained either by local thinning of the substrate [93] or by using a support wafer which is later removed [94]. As an alternative, in epitaxial wafers the heavily doped substrate can act as an intrinsic support wafer and can finally be almost completely removed [74]. In all these cases, the possibility to pattern the back-side is limited if not absent, in case of epitaxial. Thin planar sensors involve dealing with higher capacitance (noise) and lower signals. An interesting solution to improve the signal-to-noise would be to exploit charge multiplication processes, as those observed in heavily irradiated strip sensors with n-side readout biased at very large voltages $(\simeq 1000 \text{ V})$ [99]. Ideally, charge multiplication should be controlled by design and take place at lower voltages. Special designs involving additional implants or other structures enhancing the electric field are presently under consideration [100].

As for the very slim edge objective, there are a few possible approaches. Scribe-Cleave-Passivated (SCP) technique is being investigated, involving wafer scribing and cleaving to produce fewer defects than standard dicing saw, and edge surface passivation, e.g. by means of an alumina layer, that is suitable for p-type substrates due to its negative fixed charge [101]. This method could push the dead area at the edge down to $\leq 100 \,\mu$ m and it can be applied as a post processing step regardless of the specific

technology. It has already been proved with good results on few samples using a manual equipment but still needs to be extensively tested after irradiation and fully automatised for volume production. The process of stealth dicing based on a laser generating a stress layer inside the wafer can provide even narrower edges².

Planar pixel sensors with active edge, derived from the original 3D sensor technology [102], might offer the best performance [103], with full signal sensitivity up to a few microns from the physical edge, but the radiation tolerance limits of these devices have not yet been assessed. On the technological side, the main issue is the support wafer removal step that is very challenging in the presence of etched trenches, and still needs to be properly engineered. In addition, to ease assembly, the insulating layers on the back side should also be locally etched and a metal should be deposited in order to apply the bias voltage. In this respect, using epitaxial wafers might offer an advantage, because a good ohmic contact could be made on the back side directly depositing a metal over the remaining substrate layer after its etching.

Similar considerations apply to 3D sensors: using the support wafer, the single side option comes with the active edge and can easily be scaled to lower active thickness, that would actually ease the electrode etching and filling steps, thus allowing for a significant process simplification. Narrower electrodes could also be obtained, with better signal efficiency and lower capacitance. Again, support wafer removal is the main concern, and could be even more difficult for thin active layers. Conversely, for double-side 3D sensors, reducing the thickness below 200 μ m will be very complicated, particularly in terms of wafer breakage risk during processing. As for the slim edge, novel termination designs have been proposed that could allow for a \simeq 50 μ m dead area, but also the SCP approach could provide a good solution.

Charge multiplication has also been observed in irradiated and non-irradiated 3D sensors at voltages of about 200 V [104], and, if properly controlled, would be appealing for thin 3D sensors, aimed at compensating signal reduction due to the thinner substrates and to charge trapping after heavy irradiation. The feasibility of charge multiplication after irradiation depends on the high electric fields close to the junction electrodes because of the large density of radiation-induced traps, further enhanced by tip effects for nonpassing-through columns. Before irradiation, it is unlikely that charge multiplication might occur unless very high voltages are applied. In fact, high electric fields can also be obtained by adopting new designs with closer electrode spacing, that would become feasible in case of thin substrates with narrow electrodes. TCAD simulations show promising results with charge multiplication gain of up to about seven at reasonably low voltages (100-120 V) [105].

3.2.4. Applications beyond HEP

Two dimensional pixellated detectors have long played crucial roles in photon science. Phosphor screens, fiber-optically coupled to CCDs have been work horse X-ray detectors. Increasingly, these are becoming replaced with direct detection, semiconductor detectors. Hybrid pixels are becoming ubiquitous for hard X-ray applications, such as macromolecular crystallography. Originally used as photon counters, whereby a incident X-ray would fire a discriminator and increment an in-pixel counter, integrating pixels are also finding application, particularly with free electron lasers (FELs). The PILATUS [3] detector system, and its successor EIGER [4], for imaging in synchrotron radiation experiments stems out of the CMS pixel R&D at PSI, Villigen and it is widely employed on beam-lines world-wide. It offers single photon counting, fast

² Hamamatsu Photonics, Japan.

readout, superior PSF compared to CCDs, fluorescent suppression by in-pixel energy threshold and no readout noise. The detector is commercially available.³ A similar development took place also at CPPM, Marseille.⁴ The Adaptive Gain Integrating Pixel Detector (AGIPD) R&D at DESY targets applications at the European XFEL with a dynamic range of more than 10^4 photons, possibility of single photon sensitivity at high gain and operation at 4.5 MHz speed [106]. Most of the ongoing developments for instrumentation at FELs are also based on hybrid pixel detectors, using silicon as the sensor laver, such as the Cornell-SLAC Pixel Array Detector (CSPAD) architecture [107]. Fully depleted CCDs on high resistivity Si [57] and pnCCDs [59] are used at light sources and retain some advantages, when frame rate and radiation hardness are not a limitation, as at LCLS. Looking towards emerging applications, 3D sensors with active edge appear particularly well suited to the fabrication of micro-dosimeters with a well defined volume at cellular level, a known tissue equivalence factor, and the ability to use in-vivo. They are applicable to measurements and control of radiotherapy treatments, such as brachytherapy and hadron therapy. Furthermore, in cancer hadron-therapy, the combination of TOF-PET and leading neutrons and gamma detection, possible with 3D sensors, would help the precise determination of the total dose delivered to the patient. For these applications Boron- and Lithium-enriched or high Z converters can be used to fill the central region of 3D electrodes, thus increasing the total neutron detection efficiency.

3.3. Monolithic pixels

Hybrid pixel detector technology has reached a certain level of maturity and allows unambiguous hit reconstruction in two dimensions. Bump bonding limits the pitch except for advanced (3D) interconnect technologies enabling chip-to-chip assembly at extremely small pixel pitches ($< 10 \ \mu m$).

The emergence of monolithic pixel sensors from the late nineties was driven by the necessity to reach material budget and granularity performances well beyond the current LHC standards, combined with the capability to cope with high hit rates. CMOS active pixel sensors exploit the industrial CMOS technology for microcircuits. These also profit of significant industrial technology progress for camera sensors, such as OPTO processes. Some of the CMOS fabrication processes include the deposition of a lightly doped silicon layer on the standard, highly doped, substrate, prior to the micro-circuit lithography, in order to improve the insulation of the micro-circuits from the substrate. The low doping of this "epitaxial layer" favours charged particle detection as the electrons generated by traversing ionising particles exhibit a mean free path large enough (~100 µm) to reach regularly implanted sensing nodes with marginal recombination. If the thickness of the epitaxial layer exceeds typically $10 \,\mu$ m, the signal generated at a rate of about 80 e-h pairs μm^{-1} becomes sufficient to result in a signal-to-noise ratio ensuring high detection efficiency.

Monolithic detectors are considered for very small pixel pitch in the inner layers and also for the cost benefit in outer layers, but for that the power per pixel has to be much better than for hybrid detectors. Monolithic pixels offer less mass than hybrid pixel detectors, lower *C*, and a single chip solution without bump bonding [108,109]. The fact that monolithic CMOS pixels combine particle detection and the FEE in the same device is a prominent advantage, but turns into a limitation as their industrial manufacturing relies on procedures optimised for commercial items which may depart substantially from those needed for charged particle detection. CMOS industry has however evolved in a direction which allows CMOS pixels to progressively approach their real potential.

Monolithic CMOS pixel sensors in future vertex detector systems rely on the advances in the CMOS technology to cope with the demanding requirements of future collider experiments. To this purpose, many R&D paths are being pursued in the vertex detector community. The shrinking of the feature size of CMOS transistors is the most apparent outcome of the evolution of microelectronics. This is being exploited in the design of new pixel systems where advanced functions can be performed in the circuitry implemented in each pixel to provide the required signal-to-noise ratio and to handle the high data rate. These functions include amplification. filtering, calibration, discriminator threshold adjustment, zero suppression (also called data sparsification) and time stamping. CMOS sensors for particle tracking were initially designed following the classical guidelines of the NMOS-only 3-transistor cell of image sensors to collect the charge generated in an almost field-free epitaxial layer. Thanks to CMOS scaling, more functions are being included in the pixel cell, including correlated double sampling and hit binary information from a discriminator. This leads itself to achieve zero suppression at the pixel level, which is a highly desirable feature given the large number of channels foreseen and the fast readout of the pixel matrix. New strategies are also being devised in terms of the needed readout architecture, introducing a higher degree of parallelism to speed up the transfer of information from pixels to the chip periphery. Another way to comply with a high hit rate is to adopt the solutions developed for hybrid pixel sensors. This requires that the classical continuous-time analog signal processing chain (charge-sensitive preamplifier, shaping filter) is integrated in the pixel cell, together with the digital blocks needed for a high-speed sparsified readout of the matrix [110]. The implementation of complex circuitry in the pixel cell requires a technique to insulate the transistors from the collection volume, to avoid parasitic charge collection. This can be done using large deep N-well electrodes as sensing elements or by profiting of the thin oxide insulating layer of the silicon-on-insulator (SOI) technology [111,112] to use full CMOS capabilities, without degradation of the charge collection efficiency. These technologies make it possible to implement advanced readout architectures, that can be tailored to different applications. Special care needs to be taken to avoid analog-digital coupling. In the last few years, successful results have been reported for the 130 nm CMOS technology node [113] and the 200 nm SOI process [112]. Recently, the 180 nm CMOS process featuring a nearly 20 µm thick epitaxial layer with resistivity exceeding 1 k Ω · cm, 6–7 metalisation layers and additional Pwells offers the possibility to use both types of transistors inside the pixels thus allowing for a substantial increase of the in-pixel microcircuit complexity[114]. The 90 nm and 65 nm CMOS technology nodes are currently being evaluated as a promising solution to the integration of high density circuitry and high speed functionalities in a small pixel. High-voltage CMOS pixels [115] were pioneered several years ago with a larger feature size process [116] and their development is currently pursued on smaller feature size in the perspective of tracker upgrades at LHC.

It is worth mentioning that, besides device scaling, advanced CMOS technologies bring along other desirable features that pixel R&D projects are presently exploring. Metal interconnections are isolated by low-*k* dielectrics to reduce parasitic capacitance and time constants of transmission lines. This may be exploited by minimising the electronic functions in the pixel cell and by connecting each pixel to signal processing blocks in the chip periphery. Thanks to the very high integration density of the CMOS process, this peripheral readout strategy may require just a small silicon area outside the pixel matrix itself. New strategies are also being devised in terms of the needed readout architecture,

³ Dectris Ltd., Baden, Switzerland.

⁴ imXPAD SA, La Ciotat, France.

introducing a higher degree of parallelism to speed up the transfer of information from pixels to the chip periphery.

3.3.1. Fully depleted sensors

The use of a moderate- to high-resistivity substrate enhances the amount of collected charge in monolithic pixel sensors without compromising their competitive thickness. Operating the detector fully depleted has advantages both in terms of signal charge and of collection time, thus improving the performance after irradiation by more than an order of magnitude. This can be achieved either with specialised CMOS processes featuring a resistivity in excess of $1 \text{ k}\Omega$ cm, or with the SOI process on high resistivity handle wafer. Both approaches have been successfully exploited in monolithic pixel R&D ensuring signal-to-noise values of 30–40 from minimum ionising particles at room temperature. Sensors based on high resistivity CMOS pixels thinned to 50 µm, are installed in the beam telescope developed within the EUDET EU project [117]. They provide a \sim 3 µm single point resolution at a rate of $\sim 10^4$ frames s⁻¹ over an active surface of about 2 cm² paved with 670,000 pixels and can cope with particle rates exceeding $10^6 \text{ cm}^{-2} \text{ s}^{-1}$. Based on a more specialised technology, DEPFET pixels have been developed since the late 80's [118] and integrate a p-MOS transistor in each pixel on the fully depleted bulk. Electrons, collected in the internal gate, modulate the transistor current. Their low input capacitance ensures low noise operation and makes them suitable for a broad range of applications from collider detectors [119] to X-ray astronomy [61].

3.3.2. Applications beyond HEP

Monolithic pixel sensors are being successfully applied to several fields of imaging. In electron microscopy, cameras based on a monolithic CMOS pixel sensors are becoming commercially available. In particular, a reticle size 16 M pixel sensor with 5 µm pitch and a frame rate up of 400 Hz, originating from the linear collider vertex R&D, has been jointly developed by LBNL, UCSF and Gatan Inc. and it is currently available as a commercial product.⁵ For soft X-rays, where single photon energies are below hybrid pixel thresholds, low noise, monolithic detectors are being developed. Here, challenges include low noise, and thin entrance windows in order to ensure high quantum efficiency at low energies. Aiming to scientific applications at XFELs, the PERCIVAL (Pixellated Energy Resolving CMOS Imager, Versatile and Large) project developed by a collaboration of RAL, DESY and Elettra uses monolithic CMOS technology to achieve a frame rate in excess to 100 Hz for full frame readout, dynamic range from 1 to 10⁵ photons, single-photon counting capability with low probability of false positives in a mega-pixel detector. CMOS sensors are becoming attractive in intra-oral dental radiography where they offer several advantages including dose reduction and are commercially available.⁶

The low material budget, high granularity and the capability to deal with large particle fluxes afforded by CMOS pixels makes them well suited as high performance devices in beam monitoring. Sensors developed for the EUDET telescope and the STAR HFT detector are being prepared as a new generation of hadron beam monitors replacing gas chambers and in telescopes for fast on-line proton images.

3.4. Interconnection

The interconnection between the sensor and the front-end ASIC in present hybrid silicon pixel detectors is provided by micro-bump bonds with typical diameters of 25 μ m and pitches of as low as 50 μ m. Each bump bond connects one pixel cell on the sensor to the

corresponding pixel cell in the front-end ASIC. The current bump bonding technique is based on full wafer processing, which requires the use of handle and support wafers in case of thin wafers. It involves a series of processing steps: deposition of under bump metalisation layers, electroplating or evaporation of the actual bump material, photo-lithographic and etching steps, tacking and possible re-flowing of the bumps. Bump bonds used for hybrid pixel detectors installed in high energy and nuclear physics experiments or in medical imaging are based on Pb–Sn, Ag–Sn or indium bumps. ASICs are thinned to 150 μ m to minimise the material in tracking detectors, though prototype developments for future detectors already target ASIC thicknesses of less than 100 μ m. The thicknesses of present detectors are as low as 150–200 μ m.

For the LHC upgrades, bump bonding is still the interconnection technology of choice, since the pitch is not yet critical and the bonding can be performed by industry. For pixel pitches below 50 µm, industrial processes are available but not readily accessible for the research community and bump bonding is still one of the main cost factors for hybrid pixel detectors. Bump bonding is usually provided by small- to medium-size private and semiprivate companies which are ready to process small wafer quantities and are available to perform process development together with research customers. The development of cost-effective and readily accessible bump-bonding facilities, suitable for processing small numbers of prototype sensors would be a great advantage for the community. Such an initiative has been proposed, for example, in the UK national laboratories (CCLRC RAL/Daresbury), and this or similar projects, would have the support of the experimental collaborations. Extending the use of hybrid pixel detectors to larger radii will require lowering of the cost of finepitch bump bonding. Industrial scale solutions at potentially lower cost are already available for larger pitches, from about 100–200 µm or larger. A further cost reduction can be achieved by using chip-to-wafer or wafer-to-wafer bonding by thus reducing the number of processing steps and manual handling, but yields of wafer-to-wafer bonding may be a concern.

Novel techniques, which will also allow reducing the pitch to less than 20 μ m, are under study for future pixel detectors. Direct metallic connections, e.g. using Cu pillar bumps and SLID structures [120,121], will allow us to achieve fine pitch connections, while requiring a very high planarity of the components and limited possibility of rework. The direct bond interconnect (DBI) technology of Ziptronix Inc.⁷ uses direct oxide bonding and electrical connection integrated in the bonds to achieves a 3 μ m interconnect pitch. Its applicability to the integration of sensors and readout chips has been demonstrated using FPIX2 chips [122].

Technologies such as through silicon vias (TSV) are being studied to fan out the contacts for a chip to the back side of the ASIC instead of routing them to the wire bonding pads located on the edges of the chip [121,40]. TSVs have been successfully applied to FE-I3 chips which have been operated from the backside [123]. A redistribution laver on the ASIC back side can be used to bring the electrical contacts to a matrix sufficiently large to use standard Ball Grid Array (BGA) type connections. This will allow forming very compact modules by omitting the space required for the wire bonding connections. This will allow to form four-side buttable assemblies thus reducing the insensitive area between adjacent chips. The need of future pixel detectors to further reduce the material budget and thus use thinner wafers is fully in line with the requirements for making TSVs by considering that the limitations are given by the aspect ratios of the technologies used to generate the holes. BGA type connections can also be used for monolithic silicon pixel detectors without the requirement to form a TSV. The pads for

⁵ Gatan Inc., Pleasanton, CA, USA.

⁶ Schick Technologies Inc., Long Island City, NY, USA.

⁷ Ziptronix Inc. Morrisville, NC, USA.

the connections can be integrated on the front-side of the chip. However, in conjunction with using very thin silicon components, which are connected via standard BGA soldering techniques the effects of thermal stress, will be more pronounced.

3D integration technologies promise to provide a very elegant way of implementing advanced readout architectures of a pixel matrix [67]. It offers a solution to the conflict between high pixel granularity and fast readout requirements, where one tier is dedicated to charge collection while the others are devoted to signal processing through dedicated architectures. Digital electronics can be removed from the silicon layer where the sensing electrodes and the analog front-end circuits are located, eliminating interference due to substrate coupling. In a purely digital layer, the designer is allowed to integrate various advanced readout concepts, such as time-ordered readout of hit pixels, in a "data push" or triggered way, enabling a pixel matrix to deal with a hit rate of 100 MHz $\rm cm^{-2}$ with a readout efficiency close to 100% [124]. There are several approaches to 3D integration, which differ in terms of the minimum allowed pitch of bonding pads between different layers and of vertical TSVs across the silicon substrate. The HEP community focused a large effort on the design of 3D integrated circuits with the "via first" technology, where the TSVs are etched in the silicon wafers in the early stages of CMOS fabrication [67], provided by Tezzaron/GlobalFoundries.⁸ Even though this has only led to a fully functional device after several cycles, it remains a very promising approach. However, even with less aggressive 3D technologies, such as the so-called "via last" processes where TSVs are fabricated on fully processed CMOS wafers, a significant advantage can be gained in most cases, as only one or two connections are needed between the analog and digital blocks of a single pixel cell, and the digital layer can use lowdensity peripheral TSVs to reach backside bonding pads for external connection. Devices based on the "via last" technique are being studied within the AIDA EU project [125].

Sensor stitching opens up a promising path to progress towards thinner modules, with clock and signals routed on metal lines in the chips and larger area sensor arrays. Stitching is an industrial standard offered for several processes of interest for monolithic CMOS pixels. Experience with sensor stitching is currently limited to relatively large feature size processes [126] and more work is needed.

The development of interconnection technologies will have to address several key issues for new generations of pixel detectors. New technology and process options for the typical volumes used in experiments might reduce the cost for bump bonding of pixel detectors and thus would allow to construct larger area detectors. At the same time a further reduction of the overall material is the focus of most projects. The complexity in the handling and processing of thin wafers increases. The access and exploitation of 3D technologies will enable building even more compact pixel modules and will go hand in hand with new packaging technologies. However, research applications will be dependent on industrial developments for access to the via-first or via-middle processes involving steps which must take place within the CMOS foundries.

3.5. Alternative semiconductor materials

The introduction of new materials for pixel sensors is motivated by two main reasons: increased radiation tolerance for HEP and increased attenuation coefficient for photon imaging.

Diamond has excellent radiation tolerance and its larger bandgap compared to Si reduces the leakage current. This comes to the price of a \sim 0.5 smaller number of charge carriers generated in the same equivalent thickness expressed in radiation length units. Diamond detectors have been extensively used in beam monitors exposed to the most severe background conditions at colliders. The steady luminosity increase at colliders, in particular at the LHC, justify their consideration as a replacement of Si in the innermost layer(s) of the vertex trackers [127]. The RD42 collaboration promotes the development of diamond pixels for vertex tracking applications. A single crystal CVD diamond pixel sensor bump-bonded to an ATLAS pixel chip has demonstrated efficiency in excess to 99.9% and single point resolution of $(8.9 \pm 0.1) \mu m$ on a 50 μm pitch, in a beam test [128]. Diamond detectors are being considered by CMS and LHCb for their vertex tracker upgrades.

SiC has been considered for its attractive properties which include low leakage, seven times higher breakdown field compared to Si, two times higher carrier saturation velocity and radiation tolerance. In addition, it is blind to visible light, which is advantageous for several applications. Thanks to the recent progress in wafer manufacturing, very-low noise SiC pixel sensors can be manufactured [63]. The results are interesting in terms of the achievable energy resolution and the broad range of operating temperature.

At energies above about 15–20 keV, Si sensors, of the few hundred micron thickness generally used, begin to become nearly transparent. For harder X-rays, developing hybrid sensors with higher Z materials will be important. Hybrid pixels matching high-Z materials (GaAs, CdTe, CdZnTe) as sensitive layer with readout chips derived from HEP technology are well established in imaging applications based on single photon counting, such as medical radiology [64] and crystallography at light sources. This is especially important for FEL applications since these are planning to use higher harmonics, up 35 keV, and Si would result in poor quantum efficiency as well as increased radiation doses in the underlying ASICs. While these materials may not be necessarily relevant for HEP applications, they make possible the porting of readout chips derived from the HEP R&D to spectroscopic applications requiring high energy resolution and photon energy sensitivity beyond 10 keV.

4. Electronics, services and system issues

4.1. Readout electronics

Pixellated high-resolution semiconductor detectors and the revolution they have enabled in particle tracking have been made possible primarily through the parallel development of new detectors and readout electronics through high-density microelectronics technologies. The present trend in the pixels deployed in the LHC experiments is to include a significant amount of electronics with transistor counts well beyond 1000 per pixel, and a power consumption of several 100 mW per cm² of active area. The presently installed LHC readout chips are manufactured in 250 nm CMOS technologies using special layout and design techniques to increase the radiation tolerance both in terms of total dose and single event effects [129,130]. More advanced CMOS technologies offer reduced feature size and increased robustness to total dose often eliminating the need for enclosed layout transistors. Pixel sizes are therefore likely to be less limited by circuit density than by interconnection technology. Power consumption, material budget and cost will therefore be more significant constraints as technology for smaller pixel pitches is likely to be available.

4.1.1. Power consumption

The various future projects have a variety of requirements in terms of readout, which can be met with the use of new technologies. The upgrade of the ALICE inner tracker system, the STAR HFT at RHIC and the vertex trackers at lepton colliders, which have all to reduce the material to new levels and therefore limit

⁸ Tezzaron Semiconductor, Naperville, IL, USA; GlobalFoundries Inc. Milpitas, CA, USA.

the sensor thickness, will have to deal with less signal charge and hence more analog power consumption. This has to be carefully traded against the need of the envisaged low mass system to have as little material as possible for the power and signal distribution, cooling and mechanical structure and therefore require low power consumption [131]. For the SuperB project the main requirement for the FEE is to get in-pixel sparsification and fast time stamping to better than 1 µs in order to cope with the high hit rate of 100 MHz cm⁻², including a safety factor of five, and keep the bandwidth per module below 5 Gbit s^{-1} [132], with a light ladder. Several projects envisage powerful integrated cooling solutions, such as micro channel cooling, as discussed in Section 4.2, and may therefore tolerate power consumptions above several hundreds mW cm⁻². Lepton colliders, with the most extreme material budget requirements ($\leq 0.2\% X_0$ per layer), foresee air cooling within a power budget of less than 100 mW cm^{-2} (see Section 4.2). Power pulsing is proposed, given the favourable beam structure at a linear collider, with specific electronics blocks of the front-end ASIC being switched off in the time between bunch trains. This is not trivial to implement at component and system level and will require extensive study. Power pulsing cannot be applied at the LHC due to the continuous bunch structure.

In addition to performance parameters like data rate, time resolution and required on-chip data processing, the pixel size and material budget are also ultimately constrained mostly by power consumption. The analog power consumption for a given readout speed and S/N ratio is strongly dependent on the Q/C ratio, i.e. the collected signal charge Q divided by the capacitance C of the collection electrode. This ratio represents the signal strength at the input, and has to be compared to the noise of the input transistor to obtain the *S*/*N* value. Typically, the thermal noise is dominant in HEP pixel systems. Since the thermal noise is only weakly dependent on the current, I. (from \sqrt{I} in weak inversion to $\sqrt[4]{I}$) in strong inversion), this and hence the power needed for a given S/Nvalue will vary strongly with the Q/C ratio and be inverse proportional to $(Q/C)^n$, with $2 \le n \le 4$. It is therefore important to compare different technologies in terms of their Q/C ratio as this is key to lower analog power.

For monolithic pixel sensors collecting charge from just 10–15 μ m thick epitaxial layer, the Q/C ratio and power consumption might not be better compared to hybrid pixel detectors. The reduction in power consumption and Q/C improvement can be achieved by minimising *C* decreasing the size of the collection electrode and by increasing the charge collection and depletion depth by applying reverse bias voltage with a moderate- to highresistivity substrate. Operating them in depleted mode will also significantly increase radiation tolerance as charge is collected mainly by drift and not by diffusion. Analog and digital power consumption typically differ by less than an order of magnitude in pixel detectors in high energy physics. Analog power reduction by an improved Q/C or by power pulsing has therefore to be matched by a similar reduction in digital power. Power pulsing schemes also for the digital readout are considered. However also architectures limiting the off-chip data rate and minimising the number of operations are under study. As an example, in the LePix project [65], the in-pixel circuitry is reduced to minimise C, with data from different pixels combined in different projections and immediately transmitted to the periphery. The different projections are chosen carefully to minimise ambiguities and for a practical example with 4 projections, simulations indicate that occupancies of 50 hits/ cm^2 can be handled while only 4N signals need to be treated at the periphery for an $N \times N$ pixel matrix. An important component of the power consumption is the off-detector data transmission, and any progress to optimise power/data rate in this area will be beneficial to almost all new applications.

4.1.2. Time stamping

The choice of simple versus complex pixel architecture appears also in the design of pixels with a time resolution beyond that required by the LHC 25 ns bunch crossing and its upgrades. The LHCb upgrade is contemplating proton taggers situated a few 100 m up and downstream of the experiment with $\mathcal{O}(1 \text{ ns})$ time tagging within the pixel. Examples featuring a time resolution in the few ns range are TimePix [133,134], ToPix [135], Chronopix [136] and the TDCpix [137]. Distributing a time counter value over the pixel matrix and attaching its value to the hit information is an excellent way to produce time information at the few ns level, but the time reference distribution introduces higher power consumption and additional digital noise in the analog front-end. This was avoided in an alternative approach by replacing the digital time bus with a local oscillator [134]. For the lepton colliders a time binning of several ns range might be required to reduce the occupancy due to beam-induced backgrounds. For sub-ns time resolution, varying signal amplitude produced by the sensor and resulting discriminator time walk need to be compensated. An approach recently employed uses a constant fraction discriminator (CFD) and TDC in each pixel of the matrix with data sent out on a digital bus [139]. Another approach employed pixels with a single threshold discriminator sending the discriminated signal to the periphery of the readout ASIC to register the arrival time and timeover-threshold information to compensate for time walk [137]. The first approach has more complex pixels with higher analog power consumption due to CFD and TDC. The second consumes more in the digital part at the chip periphery, offering lower consumption in the pixel matrix and avoiding clock distribution over the sensitive pixel matrix. Time resolution of less than 200 ps has been demonstrated with a particle beam [137], and recently shown to be limited by the sensor. Investigations on the sensor are needed to assess whether this time resolution can be improved.

4.1.3. Trigger capabilities

New challenges provided by future applications are due to the addition of trigger capabilities. Significant physics improvements can be achieved by building track elements and reconstructing vertices from the pixel tracker information at level-2, or even level-1. Difficulties are related to the complexity of the interconnections between different layers, required by the trigger functionality, together with power and material budget issues. This is being investigated by several experiments. In particular, in the LHCb upgrade triggering would be performed in a fully-flexible software trigger, which can thus utilise displaced vertex triggering at the first level. This requires a high output rate from the FEE, and the output rate is a limiting factor in the instantaneous luminosity and proximity of the sensors to the beam. The output rate of the chip is currently limited by the number and speed of output stages which can be installed, together with their power consumption, which is currently 50% of the pixel chip budget. However, greater data output speeds would provide flexibility to go to higher luminosities and closer to the beam lines and would be a great advantage. The pixel chips closest to the beam will see rates of approximately 500 MHz pixel hits and will output $\simeq 12$ Gbit s⁻¹. The total data rate is approximately 2.8 Tbits s⁻¹. Achieving this output rate requires the implementation of on-chip zero suppression and the construction of 4×4 super-pixels in the pixel chip. Similar challenges are common to the CMS Phase 2 track trigger project [138].

4.1.4. Applications beyond HEP

The recent development of FEL facilities, producing ultra-intense, ultra-short pulses with a peak brilliance increase over conventional third generation synchrotron radiation machines by nine orders of magnitude make at the same time possible and necessary to perform single shot imaging experiments. These prevent photon counting architectures, and require detectors integrating the photons received in a single pulse. Still they must keep the total noise well below a single photon and operate with a very large dynamic range, up to 10⁶. Currently operating hard X-ray FELs operate at ~100 Hz frame rates. Future FELs, based on superconducting accelerators, will operate at orders of magnitude higher pulse repetition rate, requiring much faster readout together with more sophisticated data handling. Contrary to particle physics experiments where the occupancy is low and sparsification is possible, these applications typically require full frame readout. Various architectures are presently being developed, including dynamic gain switching (AGIPD) [140.141], multiple parallel gains (LPD), or non-linear gains (DSSC) [142]. Full frame applications, such as tomography, dynamic imaging and scattering experiments are able to take advantage of higher frame rates as brightness increases. Photon correlation spectroscopy will have increasing data rates and will require a more precise time resolution.

4.2. Cooling

The cooling system required to remove the heat dissipated by the readout electronics and heavily irradiated Si sensors represents a major contribution to the overall material budget and defines an important constraint on the FEE design and functionalities. In order to minimise the material budget new approaches to cooling are being pursued. The phase-1 CMS pixel upgrade adopts CO₂ cooling based on ultra light mechanics and thermal pyrolytic graphite (TPG), a very light material with excellent inplane thermal conductivity (> 1400 W/m–K), for the substrate [143]. The contribution of coolant and pipes to the material budget will decrease from 2% X_0 of the current detector to ~0.1% X_0 for the forward pixel modules.

Designs aiming to ultra-light ladders have so far relied on passive cooling. The HFT project at STAR has pioneered the study of thin CMOS monolithic pixel ladders where heat is extracted by air-flow. Tests showed that a flow speed of 10 m s⁻¹ removes up to 0.2 W cm⁻² with an acceptable temperature rise above ambient and displacements due to vibrations below 6 µm r.m.s. on a 200 mmlong ladder [42]. Air cooling is also adopted by BELLE-II using $\leq 1 \text{ m s}^{-1}$ flow. The power dissipation constraint for passive airflow cooling has major implications on the FEE design. In order to overcome this limitation more innovative approaches are needed such as the integration of the cooling system into the CF support structure or the Si wafer itself using micro-channel evaporator. The first approach is developed for the SuperB project, to absorb the 1.5 W cm^{-2} dissipated by the pixel front-end electronics and by ALICE for 0.5 W cm⁻². In these design, the support with integrated cooling is built with carbon fiber micro-tubes, with an hydraulic diameter of about 200 μ m obtained with poltrusion manufacturing process and polyimide tubes with CF filaments, respectively. Measurements on the SuperB support prototypes, with a total material budget as low as 0.11% X₀, indicate that it can remove $O(1 \text{ W cm}^{-2})$ over a length of tens of cm [144]. The integration of micro-channels in the Si wafer itself was originally developed for cooling microprocessor chips, where it can remove $O(100 \text{ W cm}^{-2})$ on small surfaces [145]. It allows the integration of the cooling system within the detector structure itself, with obvious advantages on the optimisation of thermal bridges and transparency to incident particles [146]. Micro-channel cooling is currently being evaluated also by the LHC collaborations and NA62 [147]

4.3. Power distribution and data transmission

Power distribution and data transmission are becoming important system aspects in the design and optimisation of vertex trackers. Due to the low voltage required by deep sub-micron microelectronics the voltage drop along the low-mass cables is significant. Power distribution for the next generation of detectors is thus considering using low currents and high voltages through serial powering [148] or DC-DC converters [149]. The former appears advantageous in terms of material budget [40].

The transmission of data from the on-detector front-end electronics to the data processing off-detector is becoming a major challenge. The bottleneck in bandwidth is in the transit region from around 10 cm up to a meter. In the front-end electronics the high bandwidth is achieved with parallel transmission of data and transmission and over long distances is made with optical serial links. Today the large amount of services required to power, cool and readout modern semiconductor trackers compromises their performance. Wireless data transmission is today the dominating technology for local data communication. A growing interest in 60 GHz technology worldwide is driven by the large unlicensed bandwidth offered by the technology [150]. An increasing number of components are being developed and are already commercially available. Due to the short wavelength, their dimensions are compatible with the sizes of detector components. The 60 GHz electronics can be processed with the same CMOS technology used for front-end electronics for pixel trackers [151]. One of the main advantages is that the data path is not fixed to the routing of wires. This opens for topological readout of the vertex tracker [152]. However, the bandwidth of a single wireless network at 60 GHz is far too low and a large number of wireless links is required. Both bandwidth and power consumption per bit transmitted need to be considerably improved for this to be a viable candidate and the operation of densely packed wireless links with minimal interference represents a major challenge to the usage of the technology in future detectors. Developments are required in areas of very directional antennas, data modulation technology and in confinement of power and networks. To make full profit of the technology, methods to cross boundaries not transparent to millimetre waves need to be developed.

5. R&D cycle from HEP to spin-offs back to HEP

The interplay between HEP and imaging applications can be understood as a two-way process by following the development of one of the first project to successfully transferring architectures originally developed for particle physics detectors to medical imaging and now back to LHC upgrade applications. The Medipix collaborations, which consist of a large number of institutes, are dedicated to the development of general purpose pixel detector readout chips mainly used for noise free particle detection and counting. This activity originated from the LHC-1 readout chip [153], which was successfully applied in the WA97 [154] and NA57 [155] experiments and became the precursor of the readout chips for the Delphi VFT [156] and then the ATLAS and ALICE pixel FEE chips. The Medipix2 focused on developing chips at the 250 nm CMOS technology node, used by the current LHC pixel readout chips, [157] and the Medipix3 develops chips in 130 nm CMOS. The Medipix2 chip [158] was initially foreseen for applications in X-ray imaging and, indeed, it has been used successfully for many experiments in the field of X-ray radiography successfully transferred to industry,⁹ marketing the chip for commercial X-ray diffraction cameras. Other applications include science at FEL facilities [159], neutron detection and radiography, electron microscopy, wavefront sensing in adaptive optics for astronomy, and radiation monitoring and dosimetry. It has also been used extensively to study and characterise new semiconductor sensor materials and structures. Particle and nuclear physics applications of the chips

⁹ PANalytical B.V., Almelo, The Netherlands.

include nTOF, ISOLDE, UA9 and, more recently in the ATLAS-MPX system [160] providing independent, real-time information about the radiation environment in the experimental cavern. The Timepix chip [133] was developed from the Medipix2 design at the request of and with funding from the EUdet consortium. The readout electronics was modified to measure the particle arrival time with respect to an externally applied shutter signal and Time-over-Threshold (ToT) information. These modifications made it an extremely versatile solution for the development of new detector technologies and for beam hodoscopes such as that assembled by LHCb [161].

The Medipix3 is a new chip [162], which uses inter-pixel eventby-event charge summing and hit allocation to extract energy sensitive images from an otherwise dispersive semiconductor detector medium. The collaboration has been so far successful in attracting new members and in technology transfer. The Timepix3 chip has a data driven readout architecture, which makes it an ideal prototype for the LHCb VELOpix upgrade. Its architecture is also being evaluated for the ALICE SPD upgrade. It can be expected that slightly modified versions of this chip could be developed for either experiments. Further developments will explore smaller pixel pitches and a larger pixel matrix, incorporate a new architecture to support power pulsing to provide a valuable test vehicle for linear collider detector engineering studies. Through the pooling of resources, it has been possible to make significant strides forward in the development of pixel readout electronics during the time when the LHC detectors were under construction and commissioning. The involvement of European industries has made possible to maintain the support of the community requests. Key sensor and interconnect technologies needed by the HEP community could be sustained during the 'trough' between the procurement phases of the LHC experiments. In this respect, it is interesting to consider a 'generic' pixel detector for an LHC experiment and compare its hit rate and readout requirements with other applications. In a pixel barrel of 1 m length with a radius of 50 mm and 10⁴ hits per 25 ns BCO, the rate of hits per mm^2 is ~1 MHz. This number is comparable to the track hit rate foreseen on the innermost chips of the LHCb VELOPix. However, given the geometry and size of the barrel it is unlikely that all hits will be readout without some form of data selection. For comparison, in a medical CT system the hit rate of the direct beam (which does not cross the body of the patient) is about \times 1000 higher. Of course, there is no readout system available at present for such a data rate but one can see that the requirements of HEP and medical imaging are at least comparable. The evolution of the Medipix programs clearly demonstrates how the collaboration with scientists from outside of HEP can be mutually beneficial. Access to deeper sub-micron CMOS will involve engineering runs at increasing costs making it very difficult, if not impossible, for individual experiments to have 'bespoke' chip designs. Collaboration and compromise on specifications may become mandatory and the experience of the MediPix collaborations may provide an important template for such future efforts.

6. Test facilities

The large number of R&D pixel projects currently under development for applications from imaging detectors for photon science applications to highly granular thin pixels for future colliders, require adequate test facilities. Special needs are set for high occupancy studies for HL-LHC pixel detectors and special beam structures for LC pixel detectors. The characterisation of pixel sensors typically entail the study of a number of properties, including charge-collection efficiency, spatial resolution and detection efficiency before and after irradiation, which require a test beam facility. High momentum particles are preferred since they minimise the effects of multiple scattering. Most R&D groups carry out regular

beam tests at FNAL, DESY or CERN accelerators since high energies beams are of major interest. In recent years, the availability of beam time has been limited but sufficient. In 2013 this situation will change with the CERN accelerator long shut down for the upgrade work. Only facilities at DESY, FNAL and SLAC will be available. FNAL will commission a second test beam line to be able to accommodate a larger number of users. In the years after the SPS long shutdown the number of requested weeks at test beam facilities will not be reduced compared to the current numbers. The extensive test beam program for HL-LHC detectors to test new sensors and later full prototypes, will continue with an increasing demand and urgency. Also LC-related tests will continue their multiple efforts, in the next several years, implying that an increase of requested beam time is probable as ILC detectors will focus on more system tests with combined detectors and CLIC-specific activity will ramp up. The pixel groups of the bfactory experiments, of PANDA [163] and CBM [164] at FAIR will also need test beam time. It is essential that the number of test beam facilities world-wide will not be reduced.

For HL-LHC pixel detectors, high rate tests, possibly with beam particles, are needed with intensities of the order of 2×10^8 particles cm⁻². Currently the only facility providing rates reaching this level is the H4irrad facility at the SPS, which is heavily subscribed. DESY and FNAL are studying the possibility to provide high rate test facilities emulating occupancies comparable to the HL-LHC conditions. Since more facilities are needed to accommodate the demands of the community, these new high rate facilities are highly desirable. Lowering the power consumption is one of the key challenges for pixel developments towards LC detectors. The baseline approach to control the power consumption of LC detectors is power pulsing, A LC-like spill structure would be useful to study power pulsing schemes. For HL-LHC bunch-crossing frequencies of 20-40 MHz are currently under discussion. To enable the study of efficiency versus the phase between on-detector and bunch-crossing clocks for future HL-LHC detectors, beams with a 25 ns bunch structure are needed to determine the necessary timing precision for the readout electronics and optimise timing through the entire readout chain.

Technical infrastructures already available at the beam areas such as beam telescope, magnets and standardised CO₂ cooling systems reduce the user set up time and increase the number of groups per test beam period. With the EU funded efforts (EUDET and AIDA), and the strong support of the hosting labs, the overall infrastructure at the test beams at CERN and DESY were significantly improved in recent years. The test beam line at FNAL had useful infrastructure implemented. Additionally the collaborations added "private" infrastructure to different beam lines. As a result, good beam telescopes are now available (Timepix, AIDA telescope and its copies) but more would be appreciated by the community. Besides high spatial resolution, good time resolution is desirable. Some groups have expressed interest for more generalised data acquisition systems for all the different beam telescope (as in the EUDAQ project). HL-LHC pixel sensors need to be cooled to temperatures as low as -35 °C during the tests, especially after high irradiation. Significant effort is put into providing adequate cooling systems. The adoption of standardised CO₂ cooling plants, similar to those already available for the Timepix telescope and planned for the AIDA infrastructure, appear to be helpful. Magnets for the study of detector performance in strong magnetic fields are also required. Different magnets are available but typically their field does not exceed 3 Tesla or the bore is not large enough to accommodate the systems under test.

7. Conclusions

Semiconductor detectors for vertex tracking have provided the much needed technological breakthrough to ensure the LHC detectors enjoy the same accuracy in track extrapolation as the last generation of e⁺e⁻ collider experiments, in a much harsher and demanding environment. Driven by track density and single point resolution requirements, the future of sensors for vertex tracking seems to belong entirely to pixellated sensors with point resolution $\leq 10 \,\mu$ m, time resolution of the order of few to 25 ns and tolerant to ever increasing radiation levels. The fast pace of development of industrial semiconductor processes provides us with opportunities and challenges for the ongoing R&D towards LHC upgrades and future collider projects. Advanced CMOS processes offer reduced feature size and increased robustness making pixel pitch less limited by circuit density than by interconnection technology. 3D layout, charge multiplication, very slim edges and monolithic technologies are pushing the R&D into new domains in terms of radiation tolerance, pixel pitch and material budget. The turn around times and costs for bump bonding of hybrid pixel sensors at decreasing pixel pitch can be a limiting factor. New interconnection techniques promise to provide ways for implementing advanced readout of the pixel matrix. However, HEP instrumentation is not in the position of fully exploiting cutting edge commercial technologies. Unlike other technologies, microelectronics is not primarily driven by HEP and industry shows that at each technology generation a correspondingly larger investment effort is necessary to fully exploit its potential benefits. Even within a resource-limited general scenario, significant investments are therefore necessary to allow the HEP community to explore new technologies, developing real systems based on them. The R&D is presently evaluating technologies which are several generations behind state of the art microelectronics and the gap is likely to increase, in the absence of adequate R&D resources. The length of the development and construction cvcle brings the need to match the technology lifetime and identify suitable established technologies. Mask costs for modern CMOS processes grow dramatically as feature sizes shrink, 3D multitier interconnection requires a long and expensive learning phase, making prototype development a more challenging and concentrated activity. New schemes must be developed to enable HEP R&D, performed typically by small research groups with limited budgets, to be aggregated and organised in larger coherent teams. New collaborative structures are mandatory to increase the capital investments, strengthen engineering competences and minimise risks with collegial reviews, compensating for the higher investment costs required to access advanced technologies. The characteristics of the R&D cycle dominating particle physics with long development times alternating with experiment construction present challenges and require experiments and R&D collaborations to support the diversification of applications between particle physics and other domains of science. Several of these applications share much of the requirements and challenges of particle physics. Also smaller scale applications, such as b-factories and nuclear science experiments, boost R&D towards performances essential for use at future larger colliders. Coming into operation in the next few years, they will add much needed experience with new technologies and system aspects. In order to keep the pace of the evolving requirements new concepts have to be constantly introduced, not only in the development of sensors, but also in readout electronics and services, in particular support structures, power distribution, power dissipation and cooling systems. The technology transfer process between particle physics and other applications works both ways and we have examples of returns from imaging to collider applications. To maintain the momentum in the development of pixel systems that will enable an even larger science area to be explored, the following action lines appear essential:

- the concurrent development of hybrid sensors able to sustain high radiation doses and thin monolithic pixels with small cell size is essential;
- microelectronics is key to the success of pixel detectors and investments are necessary to continue the exploration of the benefits from cutting edge processes;
- advanced interconnection technologies, including 3D multitier, should be strongly supported;
- system issues are becoming increasingly important and new approaches to integrated detector cooling, such as microchannels, need to be actively pursued;
- dedicated high rate test facilities are limited and the community should invest in new beam test infrastructure;
- collaboration with imaging instrumentation development in other field of science, e.g. light sources, needs to be encouraged also to compensate for the higher investment costs required to access advanced technologies and guarantee broad participation to benefits of the R&D.

Acknowledgments

We are indebted to G. Bolla, G. Casse, I Dawson, B. Di Girolamo, M. Mikuz, C. Rembser, H. Sadrozinski, M. Swartz, N. Unno and M. Vos for their contribution. M. Caccia, C. Damerell, E. Heijne, R. Horisberger, A. Marchioro, H.G. Möser and A. Seiden have reviewed the document and provided us with many precious inputs and suggestions. We are grateful to A. Cattai and the ICFA Instrumentation Panel for strongly supporting the preparation of this document.

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