



A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance



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ABSTRACT

For the upgrade of its Inner Tracking System, the ALICE experiment plans to install a new tracker fully constructed with monolithic active pixel sensors implemented in a standard 180 nm CMOS imaging sensor process, with a deep pwell allowing full CMOS within the pixel. Reverse substrate bias increases the tolerance to non-ionizing energy loss (NIEL) well beyond 10^{13} 1 MeV n_{eq}/cm^2 , but does not allow full depletion of the sensitive layer and hence full charge collection by drift, mandatory for more extreme radiation tolerance. This paper describes a process modification to fully deplete the epitaxial layer even with a small charge collection electrode. It uses a low dose blanket deep high energy n-type implant in the pixel array and does not require significant circuit or layout changes so that the same design can be fabricated both in the standard and modified process. When exposed to a ^{55}Fe source at a reverse substrate bias of -6 V, pixels implemented in the standard and the modified process in a low and high dose variant for the deep n-type implant respectively yield a signal of about 115 mV, 110 mV and 90 mV at the output of a follower circuit. Signal rise times heavily affected by the speed of this circuit are 27.8 ± 5 ns, 23.2 ± 4.2 ns, and 22.2 ± 3.7 ns rms, respectively. In a different setup, the single pixel signal from a ^{90}Sr source only degrades by less than 20% for the modified process after a 10^{15} 1 MeV n_{eq}/cm^2 irradiation, while the signal rise time only degrades by about 16 ± 2 ns to 19 ± 2.8 ns rms. From sensors implemented in the standard process no useful signal could be extracted after the same exposure. These first results indicate the process modification maintains low sensor capacitance, improves timing performance and increases NIEL tolerance by at least an order of magnitude.

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1. The standard process for the ALPIDE sensor in the ITS upgrade

Monolithic active pixel sensors (MAPS) integrating sensor matrix and readout in one piece of silicon revolutionized imaging for consumer applications, and now start making their way into high energy physics. For its upgrade of the Inner Tracking System (ITS), the ALICE experiment plans to install a new tracker [1] (Fig. 1) consisting of 7 barrel layers fully constructed with MAPS, covering a 10 m² area with about 12.5 billion pixels. This new detector should reduce the material budget or the radiation length per layer X/X_0 from 1.14% to 0.3% for the inner layers, the pixel size from 425×50 to about 28×28 μm^2 , and the radius of the first layer from 39 to 22 mm. This has led to a significant effort to develop the ALPIDE monolithic active pixel sensor [2], of which now the final prototype has returned from foundry [3].

The TowerJazz 180 nm CMOS imaging sensor process [4] has been chosen for the ALPIDE sensor due to the offering of a deep pwell (Fig. 2) and the possibility to use different starting materials. Only the nwell collection electrode is not shielded from the epitaxial layer by the deep pwell and is allowed to collect signal charge from the epitaxial layer. The deep pwell prevents all other nwells, which contain circuitry (PMOS transistors), from collecting signal charge from the epitaxial layer and therefore allows the use of full CMOS and therefore more complex readout circuitry in the pixel. ALICE is the first experiment where this has been used to implement a Monolithic Active Pixel Sensor (MAPS) with pixel front end (amplifier and discriminator) and a sparsified readout within the pixel matrix similar to hybrid sensors. The low capacitance of the small collection electrode (about 2×2 μm^2) made it possible to only consume 40 nW in the front end which was then combined with a zero suppressed readout for low overall power

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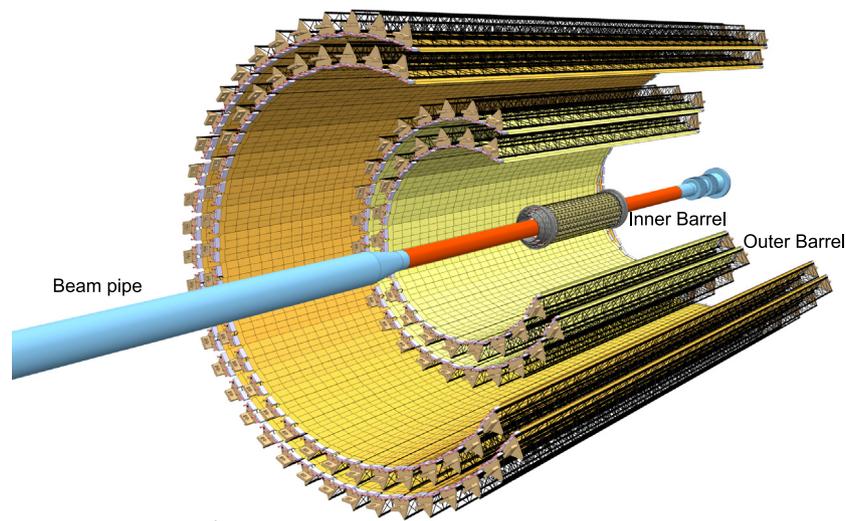


Fig. 1. Layout of the new ALICE ITS with 3 inner, 2 middle and 2 outer layers spanning a range in radius of 22 to 400 mm [1].

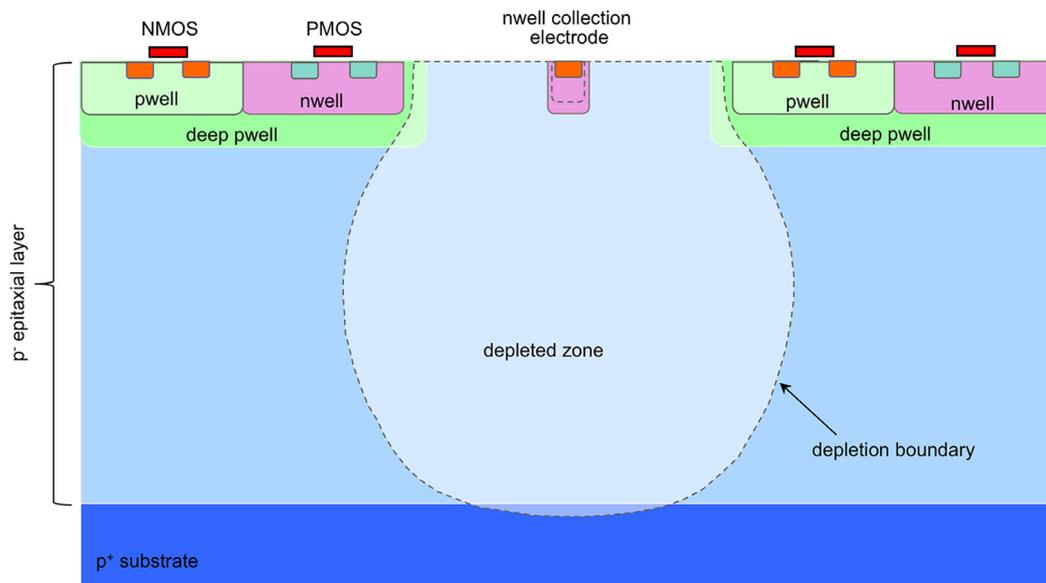


Fig. 2. A deep pwell shields the nwells with circuitry from the sensor and allows full CMOS in the pixel. In the standard process it is difficult to deplete the epitaxial layer over its full width.

consumption. The deep pwell also helps to shield the sensor from activity in the readout circuitry. Outside of the pixel matrix it is also possible to use a deep nwell to obtain a standard triple well structure.

This technology follows the general trend observed in many deep submicron CMOS technologies for increased total ionizing dose tolerance with decreasing gate oxide thicknesses [5–7]. Concerning tolerance to non-ionizing energy loss (NIEL), traditional MAPS collect charge primarily by diffusion, and often already show significant performance degradation after fluences in excess of 10^{12} – 10^{13} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$. MAPS devices with a higher radiation tolerance have been reported with a higher resistivity epitaxial layer for which the drift component in the charge collection is more important [8]. Also the ALPIDE sensor uses a higher resistivity epitaxial layer. Applying reverse substrate bias to the ALPIDE sensor increases the tolerance to non-ionizing energy loss to well beyond 10^{13} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$, sufficient for the modest ALICE requirements. However, depletion in the sensor is limited to the region around the collection electrode and signal charge generated outside the depleted area is still collected primarily by diffusion. To improve NIEL tolerance up to 10^{15} $1 \text{ MeV } n_{\text{eq}}/\text{cm}^2$ and beyond for more demanding applications, a drift field and hence depletion is required over the full

sensitive layer to push the charge carriers to their destination and strongly reduce their collection time and hence the probability for them to be captured by radiation-induced defects or traps and be lost for readout. This is further discussed below.

2. Towards full depletion of the sensitive layer

In the standard process (Fig. 2), depletion starts at the junction of the collection electrode and expands with increasing reverse bias, but it is difficult to laterally extend the depletion region far into the epitaxial layer in between the low resistivity substrate and the deep pwell, as this requires a potential gradient or an electric field in between two equipotentials. Increasing the size of the collection electrode and hence of the junction would facilitate the depletion over the full pixel area but would lead to a very significant penalty on the input capacitance and power consumption [9]. Reducing the area of the deep pwell would also help but would reduce the area available for circuitry and limit the complexity of the in-pixel circuitry. Another possibility is to place the readout circuitry in the pixel in the well implementing the collection electrode [10–13], but also this limits the complexity of the in-pixel

circuitry as otherwise the capacitance penalty is high. In addition, care has to be taken not to couple signals in the circuitry into the collection electrode [14]. Silicon-on-Insulator (SOI) technology also has been proposed [15] to implement a pixel sensor with a fully depleted sensitive layer, and significant progress was made, but the sensitivity of the buried oxide to ionizing radiation so far has prevented this technology from being adopted in the most aggressive radiation environments. SOI with a thick film of silicon over oxide combined with only partially depleted wells has recently been used to prevent transistors being affected by back gating and charge accumulation in the buried oxide [16]: signals could be collected after 10^{14} 1 MeV $n_{\text{eq}}/\text{cm}^2$, but not after 5×10^{14} 1 MeV $n_{\text{eq}}/\text{cm}^2$, attributed to trapping and large spacing between collection electrodes.

A possible solution to achieve full depletion of the sensitive layer combined with a low capacitance collection electrode is to implement a large or even planar junction separate from the collection electrode. The depletion will start from the junction and hence immediately extend over the full pixel area. Increasing reverse bias will then further extend the depletion towards the collection electrode, which can be kept small to maintain a low capacitance. In [17] a planar junction in a monolithic sensor was implemented on the back side of a 300 μm thick high resistivity p -type (12 $\text{k}\Omega\text{ cm}$) wafer. On the front side, an array of p -type collection electrodes contact the substrate through holes in an nwell which contains the readout circuitry. Increasing reverse bias on the back side junction gradually extends the depletion from near the back of the wafer to the front until full substrate depletion is reached and all collection electrodes are mutually isolated. Prototypes were fully functional and the small low capacitance collection electrodes resulted in a signal-to-single-channel noise of 150–1 and a 1.8 μm spatial resolution in the direction of smallest pixel pitch (34 μm). However, the devices required processing both sides of the wafer, typically not compatible with standard foundry CMOS processes. An approach to create a planar junction which requires processing of the wafer only on one side is to use an epitaxial layer of the opposite type as the substrate and this was recently further pursued [18].

In this work a low dose deep n -type implant has been used to implement a planar junction in the epitaxial layer within the pixel matrix below the wells containing circuitry (Fig. 3). The implant is sufficiently low dose to fully deplete it up to the nwell collection electrode implant for reverse bias voltages of a few Volts and obtain a sensor capacitance of only a few fF. Since the pwell in the pixel matrix and the substrate are now separated by a depletion layer and hence isolated, they can be biased independently, provided a sufficiently large potential barrier prevents the holes in the pwell from entering the epitaxial layer and hence avoids punchthrough.

Initial device simulations were carried out for epitaxial layer thicknesses between 15 and 30 μm and resistivities of 0.5–2 $\text{k}\Omega\text{ cm}$. When for 18 and 30 μm doping profiles obtained from Spreading Resistance Profiling (SRP) measurements became available, these were used for the optimization. These measured SRP profiles are far from constant over the thickness of the epitaxial layer as they include the out-diffusion from the low-resistivity substrate into the high resistivity epitaxial layer, drastically increasing the doping over several microns. Depth and doping level of pwell and deep pwell were varied by tens of percent, significantly changing the doping level near the deep low dose implant to verify tolerance to process variations. Pixel pitch was varied between 20 and 40 μm and the opening of pwell and deep pwell around the collection electrode between 6 and 10 μm to verify tolerance to geometry variations. The critical parameter is the dose of the deep n -type implant. It should be sufficiently low to fully deplete the implant at reasonable voltages, and sufficiently high to prevent punchthrough between pwell and substrate. After optimization it dominates the epitaxial layer doping by several orders of magnitude, and in simulation the implant dose could be varied by several tens of percent while maintaining correct operation. The nwell and deep n -type implant profiles overlap sufficiently to locally dominate the p -type doping of the epitaxial layer underneath the nwell

collection electrode and form a continuous n -type layer down to the planar junction. The simulations show that as expected for a planar junction, the epitaxial layer depletes over the full pixel area at 0 V. To deplete the low dose n -type implant up to the nwell implant defining the collection electrode and the epitaxial region between the collection electrode and the surrounding pwell and deep pwell, a moderate reverse bias of the collection electrode (up to 5 V) is required. At this moderate reverse bias the depletion extends into the region near the interface between the lowly doped p -epi-layer and the highly p + doped substrate where the doping from the substrate has out-diffused into the epitaxial layer. However, as this out-diffusion locally increased the epitaxial doping by orders of magnitude, the depletion ends several microns away from the epi-substrate interface itself. Punchthrough only sets in at around -20 V for an epitaxial layer thickness of 18 μm and above -30 V for 30 μm offering sufficient operating margin. Fig. 4 shows for the 18 μm thick epitaxial layer and different nwell collection electrode biases how substrate current and deep pwell current (respectively I_{sub} and $I_{\text{deep-pwell}}$ in the figure, measured in the simulation at their respective bias contacts) remain very low until they exponentially increase for reverse substrate biases beyond -20 V as punchthrough sets in. The pwell was grounded. The figure illustrates that the onset of punchthrough does practically not change with nwell collection electrode bias.

Fig. 5 illustrates as an example the depletion of the sensitive layer and in particular the low dose n -type implant by plotting simulated electron and hole densities. To save grid points and computation time and using the symmetry in a square $28 \times 28 \mu\text{m}^2$ pixel only one eighth of the pixel was simulated, hence yielding the pie shape in the figure. The red lines indicate the junctions, the white lines the depletion boundary. The pwell was grounded, the collection electrode and substrate are biased at +5 V and -15 V respectively, but similar depletion is already reached near zero substrate bias.

An important advantage of this approach is that apart from defining the region of the implant over the pixel matrix, the process modification does not require any layout changes in the design of the sensor, hence allowing the same designs to be processed in the standard and the modified process. This was done for one of the pALPIDE prototype mask sets (ITS3), allowing comparison on identical designs.

3. First experimental results

Comparison with the standard process.

The ITS3 mask set contains the pALPIDE-2 full-scale prototype for the ALICE ITS upgrade, but also many other test chips, including the Investigator [19], a chip containing a large number of mini pixel matrices with various pixel pitches, collection electrode geometries and collection electrode to deep pwell spacings. Each mini-matrix contains an 8×8 pixel array surrounded by one column/row of dummy pixels effectively occupying an area corresponding to 10×10 pixels. Any mini-matrix on the chip can be selected, of which then all the 64 pixel outputs are individually connected to a source–follower buffer circuit (shown in Fig. 6) driving the analog signal observed in the pixel off-chip allowing direct real-time observation of all pixel signals in parallel. Each of the channels consists of four source followers in series, so that the output follows the pixel input corresponding to that channel. The switches in the signal path are used to select the pixels from a particular mini-matrix. In addition, the signal is further buffered off-chip. One limitation is the moderate speed of the readout circuit (rise time constant ~ 10 ns). Therefore, the signal rise time is not only related to the development of the signal at the pixel input, so to the collection time of the signal charge, but also severely affected by the speed of the circuit. In all plots related to timing, the 10%–90% signal rise time has been plotted. For the measurements with ^{90}Sr , a different off-chip amplifier has been used with a somewhat smaller rise time. So far the circuit has been measured primarily on wafers with 25 μm epitaxial layer thickness.

Fig. 7 shows distributions for seed, cluster and single pixel cluster signal, and cluster size for a test exposing the chip to a ^{55}Fe radioactive

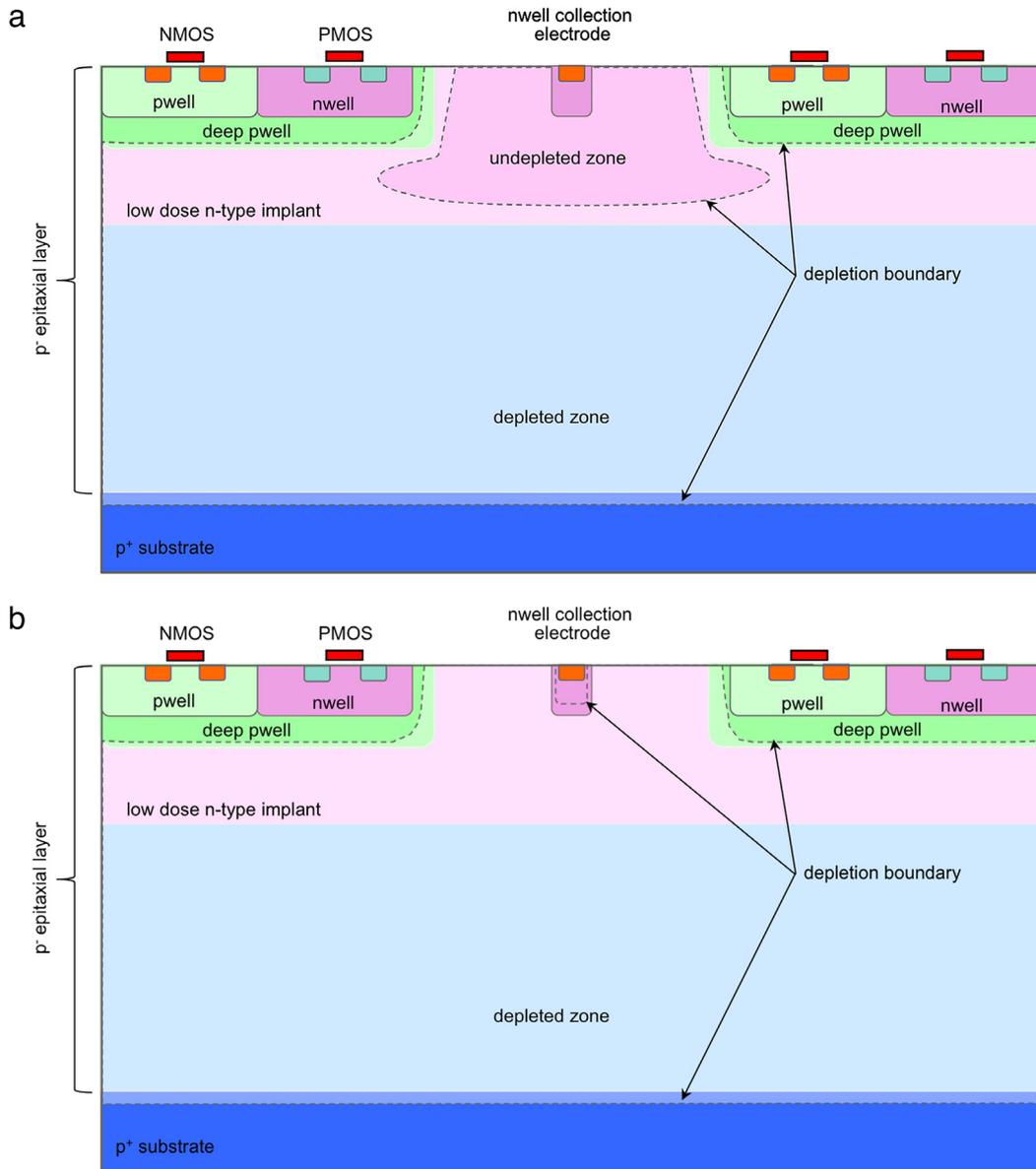


Fig. 3. Schematic cross-section of a pixel in the modified process: at very low reverse collection electrode bias the depletion of the low dose *n*-type implant is only partial around the collection electrode (a). For higher reverse biases the depletion reaches the nwell implant for the collection electrode (b) yielding a low sensor capacitance.

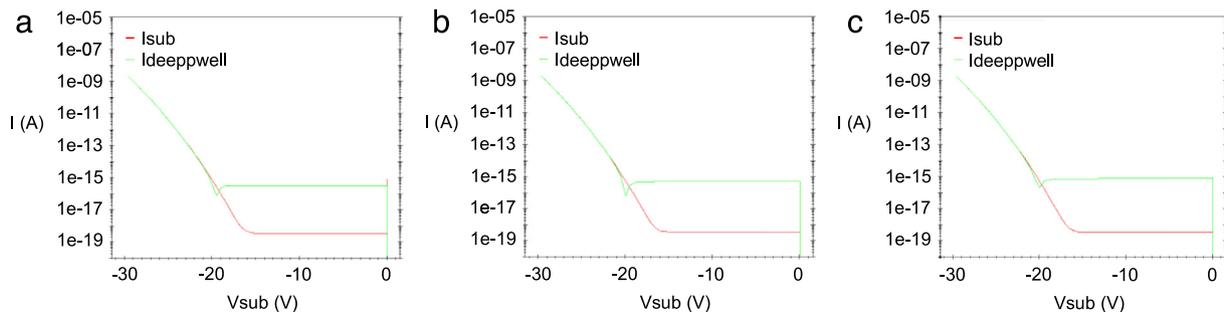


Fig. 4. Onset of punchthrough between deep pwell and substrate at around -20 V reverse substrate bias for various collection electrode biases ($V_{CE} = 1$ V (a), 3 V (b) and 5 V (c)), and as can be seen the onset is practically unaffected by V_{CE} . I_{sub} and $I_{deppwell}$ are the currents at the substrate and deep pwell terminals, respectively. In punchthrough the current between those two terminals severely increases and becomes dominant.

source [19,20]. The two characteristic X-ray peaks are clearly visible for both standard and modified process. The higher dose of the deep implant in the modified process is higher than the lower one by several tens of percent. The peak positions indicate that increasing the higher

implant dose yields a slightly higher sensor capacitance, for a lower dose there is no sensor capacitance penalty, indicating the depletion extends then to the nwell implant defining the collection electrode. The cluster size distributions indicate the full signal is collected on a single

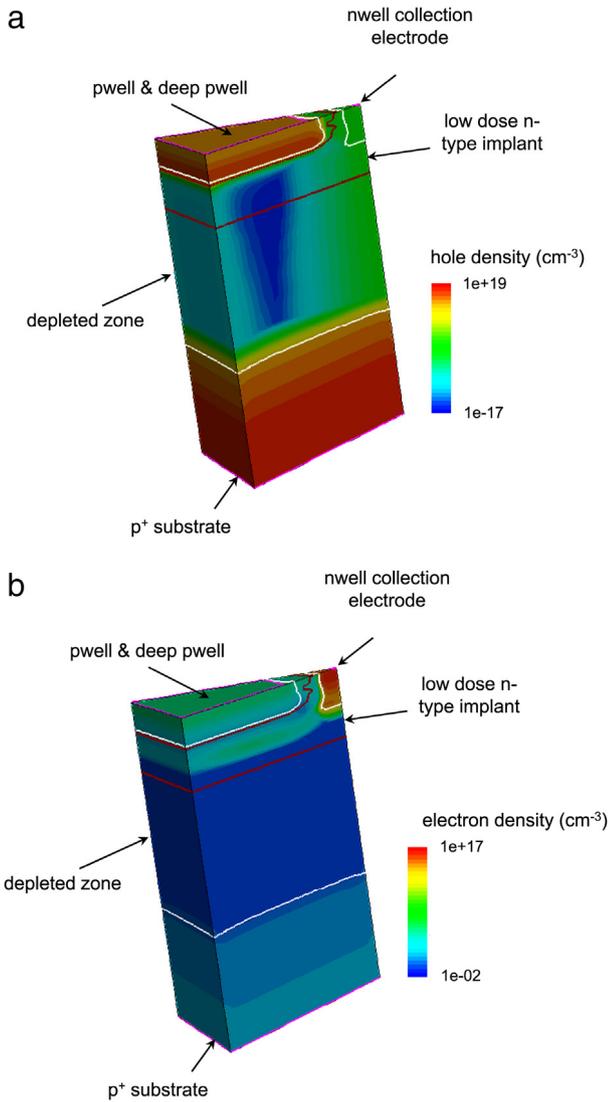


Fig. 5. Simulated hole (a) and electron (b) densities illustrate the depletion of the epitaxial layer and the low dose implant. The junctions are indicated with a red line and the edge of the depleted zone with white lines. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

pixel in a significantly larger fraction of the events for the modified process. This is clearly visible also in the distribution of the seed signal (the pixel with signal over threshold establishing there was a hit), where

the fraction of signals within the peak is much larger indicating much less charge sharing for the modified process. The cluster signal obtained by combining the signals from all pixels in the cluster, is very similar to that of single pixel clusters. The peak is somewhat wider as the noise of the different pixels is added, but there are only few clusters with signals outside of the peak illustrating little or no signal loss for both standard and modified process at this bias. In this example, the pixel size of the selected mini-matrix is $28 \times 28 \mu\text{m}^2$, the collection electrode is an octagon of $2 \times 2 \mu\text{m}^2$ centered in a $8 \mu\text{m} \times 8 \mu\text{m}$ square opening in the deep pwell, so that the minimum space between collection electrode and pwell equals $3 \mu\text{m}$. This geometry is also approximately the one used for the final ALPIDE chip. Pwell and substrate are biased at -6 V , the collection electrode at about 1 V .

In Fig. 8 signal rise time and amplitude were measured for a single pixel and plotted in a two-dimensional distribution for both standard and modified process. As already stated, for the standard process charge sharing between pixels occurs much more often and this typically happens for particles incident near the boundary between pixels. Since the epitaxial layer is not depleted there, and charge has to be collected by diffusion, this explains the increase of the average charge collection time with decreasing pixel signal. For the modified process charge sharing is much less frequent but also signal rise time is not dependent on the size of the signal or whether the signal is shared between pixels or not. Fig. 9 clearly illustrates the lower and more uniform signal rise time for the modified process. The signal rise time is comparable for the two dose splits of the low dose implant. The much larger fraction of single pixel hits and the lower and more uniform collection time all indicate a drastically increased depletion volume in the sensor for the modified process, confirming the device simulations. More extensive measurements are in progress and will be reported together with a more detailed description of the Investigator in [19].

The improved timing performance and the combination of the low capacitance collection electrode and the increased depletion volume and its potential for NIEL tolerance has raised interest in this modified process not only within ALICE but also in other experiments, with as a consequence significant measurement activity on the Investigator [21–23].

Post-irradiation performance.

To verify tolerance to non-ionizing energy loss, several Investigator chips were irradiated up to various neutron fluences, and performance before and after irradiation was compared using a ^{90}Sr radioactive source [22,23]. In this measurement, the output of a single $50 \mu\text{m} \times 50 \mu\text{m}$ pixel was connected to a very fast amplifier of which the output was digitized. The collection electrode is a $3 \times 3 \mu\text{m}^2$ octagon centered in a $40 \mu\text{m} \times 40 \mu\text{m}$ opening in the deep pwell. To reduce the radiation-induced leakage current, the irradiated devices were cooled to $-30 \text{ }^\circ\text{C}$, the unirradiated device was measured at room temperature. Fig. 10 shows the spectrum for the modified process with the higher implant

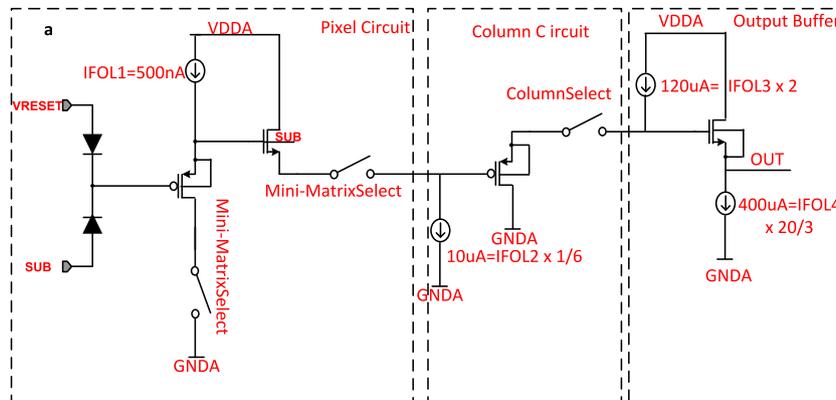


Fig. 6. Schematic of the readout channel of one pixel in the Investigator. A particular mini-matrix is selected using the switches, and all 64 pixels in the mini-matrix can then be read out in parallel.

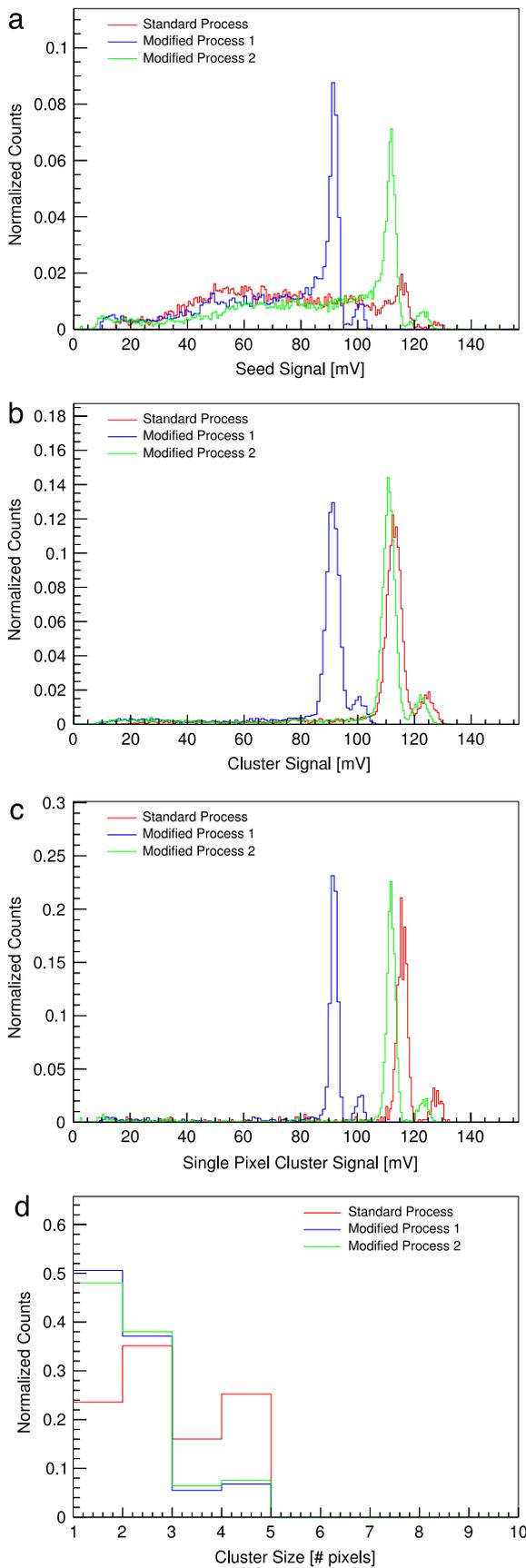


Fig. 7. Signal and cluster distribution from a ^{55}Fe radioactive source measured at room temperature for standard and modified process with higher (modified process 1) and lower (modified process 2) dose for the low dose implant [19,20]: (a) seed signal, (b) cluster signal, (c) single pixel cluster signal and (d) cluster size distribution.

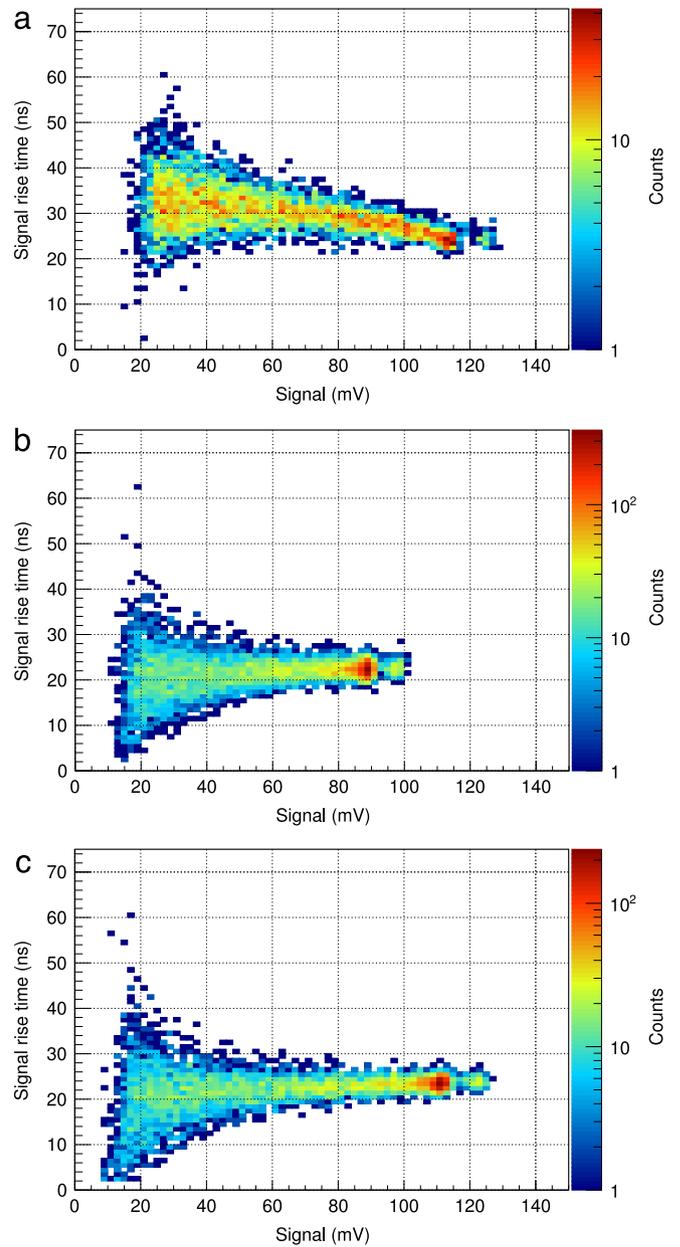


Fig. 8. (color online). Measured charge collection time at room temperature versus signal from a ^{55}Fe radioactive source for standard (a) and modified process with higher (b) and lower (c) dose for the low dose implant [19,20].

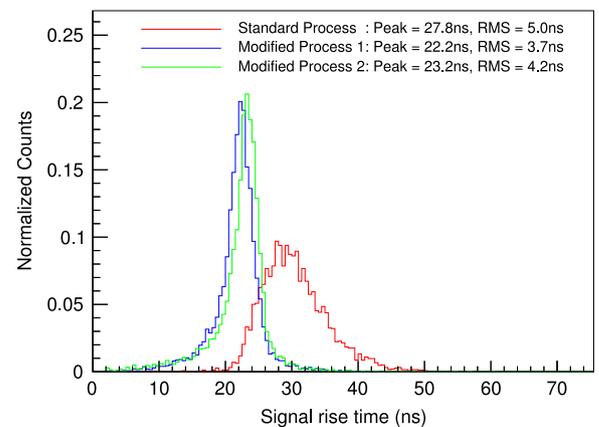


Fig. 9. Measured signal rise time at room temperature from a ^{55}Fe radioactive source for standard (a) and modified process with higher (modified process 1) and lower (modified process 2) dose for the low dose implant [19,20].

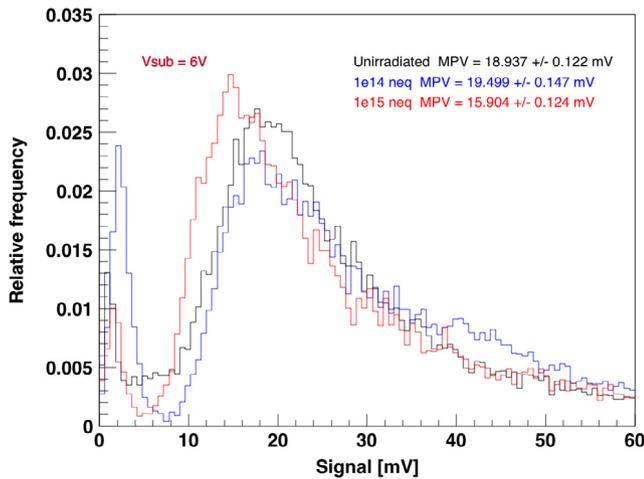


Fig. 10. (color on-line). ^{90}Sr spectrum for the modified process (higher dose) before and after neutron irradiation [22,23].

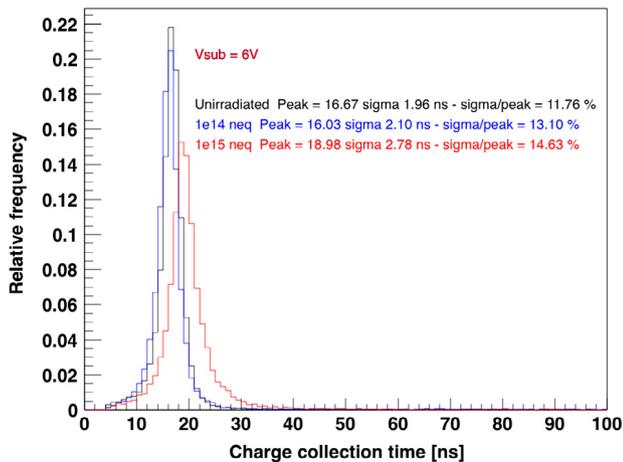


Fig. 11. (color on-line). Signal rise time from a ^{90}Sr source for the modified process (higher dose) before and after neutron irradiation [22,23]. The unirradiated device was measured at room temperature, the others at -30°C .

dose before and after neutron irradiation, and illustrates the only minor degradation after 10^{15} $1\text{ MeV } n_{\text{eq}}/\text{cm}^2$ with a mean probable signal value reducing from about 19 to about 16 mV.

Fig. 11 shows the distribution of the signal rise time extracted during the same measurement. The unirradiated device measured at room temperature and the one irradiated to 10^{14} $1\text{ MeV } n_{\text{eq}}/\text{cm}^2$ measured at -30°C show little difference. The degradation may partly be compensated by the lower temperature, but the additional degradation from 10^{14} to 10^{15} $1\text{ MeV } n_{\text{eq}}/\text{cm}^2$ remains minor with an increase in rms spread of the signal rise time from 2.1 ns to about 2.8 ns.

From Investigator chips implemented in the standard process irradiated up to 10^{15} $1\text{ MeV } n_{\text{eq}}/\text{cm}^2$, no useful signal could be extracted. First test beam results indicate efficiencies of above 97% for pixels with 25 and 30 μm pitch implemented in the modified process with higher dose implant after 10^{15} $1\text{ MeV } n_{\text{eq}}/\text{cm}^2$ [23], which is a substantial improvement. Chips tested so far were from the same batch and from two wafers/split. For each irradiation level usually three chips were irradiated and measured. The higher implant dose for the modified process is several tens of percent higher than the lower one. Despite a capacitance penalty for the higher dose, both yield functional devices indicating a relatively large tolerance to process variations confirming the device simulations. Work is in progress to compare the different splits and pixel geometries in more detail regarding performance and radiation tolerance also up to even larger fluences.

4. Conclusions

Monolithic active pixel sensors (MAPS) have been adopted for the ITS upgrade in the ALICE experiment, where a monolithic sensor has been implemented with front end (amplifier and discriminator) and sparsifying readout within the matrix. Radiation tolerance to more extreme levels and low power consumption impose depletion of the sensitive layer to obtain charge collection by drift, and a small collection electrode to optimize the collected signal charge over input capacitance ratio. The standard 180 nm TowerJazz CMOS imaging sensor process chosen for the ALPIDE sensor in the ALICE ITS upgrade does not allow full depletion of the epitaxial layer if the readout circuitry occupies a significant fraction of the pixel area. This paper describes a process modification to obtain full depletion of the epitaxial layer even with a small collection electrode. It uses a low dose blanket n -type implant in the pixel array and does not require significant circuit or layout changes so that the same design can be fabricated both in the standard and modified process. The implant was optimized using device simulations, indicating full depletion of the sensitive layer can be reached. Measurements are still in progress, but first results illustrate a significant improvement in timing performance and radiation tolerance for the modified process, essentially confirming the simulation results, with no sensor capacitance penalty for lower implant doses and only up to a 20%–30% for higher implant doses, motivating several groups in different experiments to participate in further measurements.

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