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Development of monolithic pixel detector with SOI technology for the ILC vertex detector

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Abstract: We have been developing a monolithic pixel sensor for the International Linear Collider (ILC) vertex detector with the 0.2 μm FD-SOI CMOS process by LAPIS Semiconductor Co., Ltd. We aim to achieve a 3 μm single-point resolution required for the ILC with a $20 \times 20\,\mu\text{m}^2$ pixel. Beam bunch crossing at the ILC occurs every 554 ns in 1-msec-long bunch trains with an interval of 200 ms. Each pixel must record the charge and time stamp of a hit to identify a collision bunch for event reconstruction. Necessary functions include the amplifier, comparator, shift register, analog memory and time stamp implementation in each pixel, and column ADC and Zero-suppression logic on the chip. We tested the first prototype sensor, SOFIST ver.1, with a 120 GeV proton beam at the Fermilab Test Beam Facility in January 2017. SOFIST ver.1 has a charge sensitive amplifier and two analog memories in each pixel, and an 8-bit Wilkinson-type ADC is implemented for each column on the chip. We measured the residual of the hit position to the reconstructed track. The standard deviation of the residual distribution fitted by a Gaussian is better than 3 μm.

Keywords: Particle tracking detectors; Particle tracking detectors (Solid-state detectors)

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1 Introduction

The International Linear Collider (ILC) experiment needs a vertex detector with satisfactory space and time resolutions to distinguish the decay of heavy flavor quarks, such as the charm and bottom quarks, and tau leptons for precise measurement of the properties of the Higgs boson and search for physics beyond the Standard Model. We have developed a monolithic pixel detector with silicon-on-insulator technology (SOIPIX) [1] as shown in figure 1 based on a 0.2 μm fully depleted SOI CMOS process developed by LAPIS Semiconductor Co., Ltd. [2].

Hybrid type pixel detectors are currently used for high-energy accelerator physics experiments. The sensor and signal readout ASIC are mechanically connected through bump bonding [3]. SOIPIX has a greater potential for decreasing pixel size and sense node capacitance compared to a hybrid type pixel detector because it does not comprise mechanical bump bonding. A smaller parasitic capacitance results in higher speed and lower noise. In an SOI CMOS process the electronics is isolated from the bulk silicon so that they are less sensitive to single event effects. Additionally, SOI CMOS is advantageous in circuit integration because there is no well structure for a MOSFET. Therefore, SOIPIX enables us to implement a complex circuit in a small size pixel and to fulfill the requirements of space and time resolution for the ILC.

We designed and evaluated a prototype pixel sensor for the ILC, named as SOI sensor for FIne measurement of Space and Time (SOFIST) to optimize pixel size and signal readout circuit. Currently, we aim to develop a pixel size less than 25 μm. Requirements for the ILC are as follows [4]

- Single point resolution of better than 3 μm.
- Time resolution to identify a single bunch crossing every 554 ns for 1300 bunches.

- Low detector occupancy of less than 2%.
- Low material budget of less than 0.1–0.2% of radiation length X_0.

At the ILC, beam bunch crossings occur every 554 ns during 1-msec-long bunch trains at intervals of 200 ms. To identify a collision bunch for event reconstruction, each pixel must record the time stamp of a hit. To maintain a low detector occupancy, existing groups utilize a rolling-shutter readout or a small size pixel detector [5, 6]. However, SOIPIX can implement complex circuitry in the pixel, so we aim to recognize the collision bunch of a hit using time stamping.

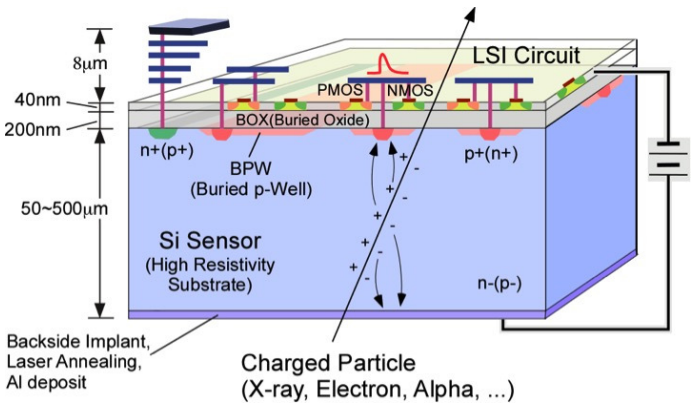

Figure 1. Cross section of the SOI monolithic pixel detector. The signal readout circuit is processed on the SOI layer. The buried oxide layer (BOX) isolates the readout circuit from the silicon sensor. The buried *p*-well (BPW) is created under the BOX to suppress the back-gate effect. The BPW is also utilized as a sense node to collect charges in the sensor. Thickness of the silicon sensor can be reduced from 500 μm to 50 μm according to application.

Figure 2 shows the conceptual design of the SOFIST and signal readout circuit for a single pixel. The pixel size is $20 \times 20\ \mu\text{m}^2$. The active area that corresponds to a $3,125 \times 500$ pixel array is $62.5 \times 10\ \text{mm}^2$. To achieve a single point resolution better than 3 μm, a weighted center of charges is calculated. The charge distribution in the cluster is used to improve the spatial resolution much better than pixel size$/\sqrt{12}$. The analog signal is amplified and recorded in an analog memory if the signal exceeds the threshold of a comparator, as shown in figure 2(b). In addition, a function that records the time stamp of a hit is implemented. The ramp voltage of the timing of a hit is recorded to the memory as a time stamp, and is then digitized by on-chip column ADC ($>$ 11 bits) to identify the beam bunch collision. These digital data have to be sent to the backend circuit before the next beam train injection. Zero-suppression logic extracts hit pixels and reduces the data to transfer. Multiple memories (at least four) are implemented for both the analog signal and the time stamp so that we can maintain a low detector occupancy during 1 beam-bunch train. The shift register (figure 2(b)) is used as a latch to change the memory to hold the information of hits. The sensor thickness is reduced to 50 μm to maintain a low material budget. Radiation hardness of the SOIPIX, especially tolerance to total ionizing dose effect up to 500 kGy is achieved [7]. This is enough for the ILC since the radiation level is less than 1 kGy/year. We are still designing and evaluating the prototype to optimize pixel size and signal readout circuit.

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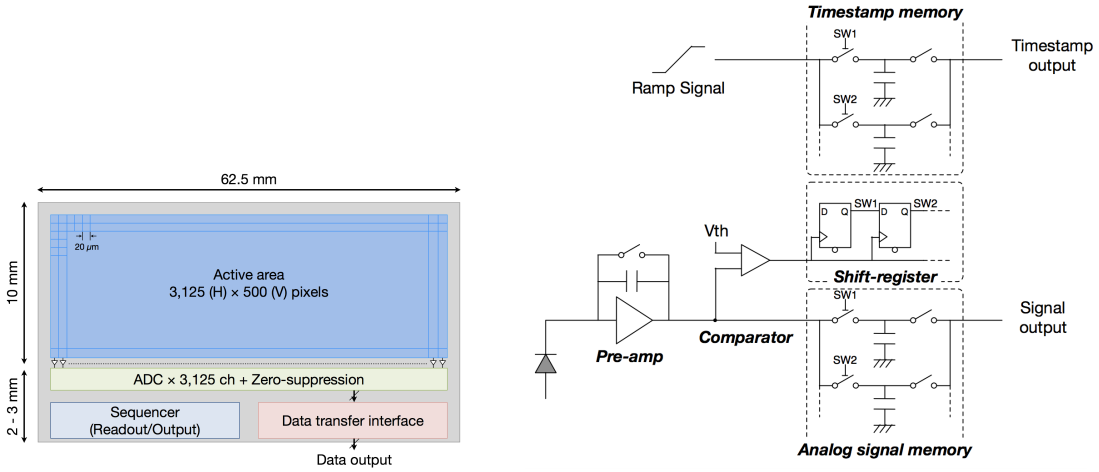

(a) SOFIST.

(b) Signal readout circuit.

Figure 2. (a) SOFIST overview. Pixel size is $20 \times 20\,\mu\text{m}^2$. Active area corresponding to $3,125 \times 500$ pixel array is $62.5 \times 10\,\text{mm}^2$. (b) Signal readout circuit in a single pixel. It has an amplifier, comparator, shift register, analog signal memories, and time stamp memories. A column ADC and Zero suppression logic are on the chip.

2 Beam test setup

We tested the first prototype SOFIST ver.1 chip by using a 120 GeV proton beam at the Fermilab Test Beam Facility for evaluating the signal-to-noise ratio and spatial resolution. Another SOI pixel detector FPIX2 dedicated to fine spatial resolution was used as a telescope.

2.1 SOFIST ver.1

Our first prototype sensor, SOFIST ver.1, has a charge sensitive amplifier (CSA) and two analog memories for storing signal charges up to two hits in a $20 \times 20\,\mu\text{m}^2$ pixel, as shown in figure 3. The CSA consists of a common-source stage with a feedback capacitance C_f. Two feedback capacitances $C_\text{f} = 5$ and 20 fF are prepared for the CSA. These assume the thickness of the sensor as 50 and 500 μm, respectively. A pixel array of 50×50 is constructed using 10 columns of high-gain CSA pixel ($C_\text{f} = 5$ fF) and 40 columns of low-gain CSA pixel ($C_\text{f} = 20$ fF). The conversion gain of high and low-gain CSA are 37 and 9.4 $\mu\text{V}/e^-$, and the outputs are approximately 0.135 (high-gain) and 0.349 V (low-gain) for 3,700 and 37,000 electrons respectively for one minimum ionizing particle passing through a 50 or 500 μm thick silicon sensor. In this paper, we tested a sensor of 500 μm thickness. The output amplifier is constructed using a PMOS source follower and signal readout switch. An 8-bit Wilkinson-type ADC is implemented for each column on the chip [8]. The range of input is 1 V, and this ADC operates at 100 MHz with 10 μs of conversion time for a single row. The sensor wafer is an n-type float zone with a resistivity of more than 2 k$\Omega\cdot$ cm. The size of the BPW for the sense node in the low gain pixels are to evaluate the noise and optimize the BPW size, as shown in figure 3(a). The SOFIST ver.1 was delivered in December 2015.

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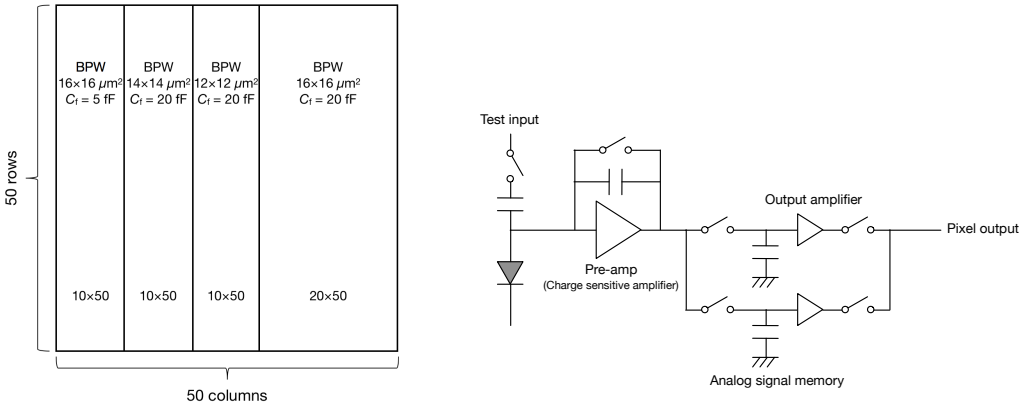

(a) Pixel layout

(b) Signal readout circuit

Figure 3. (a) Pixel array of SOFIST ver.1 with pixel size is $20 \times 20\ \mu\text{m}^2$. Left 10 columns are for high-gain pixel, and right 40 columns are for low-gain pixel. BPW size in low-gain pixel are different for evaluating a noise. (b)Signal readout circuit in a single pixel of SOFIST ver.1. Capacitances for the analog memories are 100 fF of MIM capacitance.

2.2 Telescope

FPIX2 is also a SOI pixel detector, and it has an $8 \times 8\ \mu\text{m}^2$ pixel dedicated to fine position resolution better than 1 μm. A 128 pixel array consists of $1 \times 1\ \text{mm}^2$ of active area. The pixel circuit is constructed by six MOSFETs that correspond to two for a protection diode, two for a CMOS reset switch, PMOS source follower and signal readout switch. The analog signal is extracted by a rolling-shutter readout architecture. The pixel array is divided in eight blocks for the parallel readout of the rolling shutter. The eight outputs are then digitized by an eight channel 12-bit ADC on the DAQ board, SEABAS2 [9]. Scan time for a single pixel is 280 ns, and the frame rate is 1 kHz including the ADC conversion time. The sensor wafer is a $p-$type float zone (500 μm thickness), and its resistivity is more than 25 k$\Omega\cdot$ cm.

2.3 Setup and DAQ system

The setup for the beam test is shown in figure 4. Four layers of FPIX2 are used as the telescope for SOFIST ver.1. An event is triggered by coincidence of the scintillation counter of $3 \times 3\ \text{mm}^2$ and the ATLAS upgrade pixel detector, FE-I4 [10]. FE-I4 provides a region-of-interest trigger signal with an area of $2 \times 1.7\ \text{mm}^2$ covering the FPIX2 and SOFIST ver.1 active area. An event trigger decision is sent from the master DAQ board to each sensor. During data acquisition, a slave DAQ board for each sensor outputs a busy signal to the master board. In addition, the time stamp clock (1 kHz) enables synchronization of the event among the sensors to reconstruct a track sent from the master board. A cycle reset pulse of 200 ns width and 10 μs interval, for the SOFIST ver.1 pre-amplifier is also sent from the master board. A maximum data rate of 500 Hz is achieved.

3 Experimental procedure and results

We collected a total of 4 M events in a 148-hours beam time. Statistics for the tracking was limited due to its small overlap area among all sensors. In addition, a size difference among the BPW has

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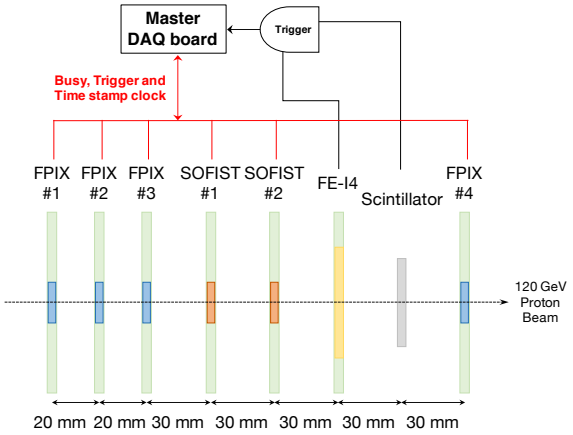

Figure 4. Setup (not to scale)

an effect on the charge shared between boundary pixels. The hit on the boundary is removed from the analysis for the spatial resolution. For each run we collected 30 k events, corresponding to 1 k tracks reconstructed by FPIX2 for the DUT, SOFIST ver.1.

3.1 Clustering and signal to noise ratio

The sensor bias voltage of SOFIST ver.1 for the test is 130 V which corresponds to the full depletion of the 500 μm thickness sensor. The analog signal readout is performed using an external 12-bit ADC to evaluate the amount of the signal and noise more precisely than using the on-chip 8-bit column ADC. To obtain pedestal distributions from off-beam data, some runs were taken using a pulse as trigger. Noise of one pixel is extracted by fitting a Gaussian to the pedestal distribution. We define the mean of the Gaussian sigma of all pixels as the noise of the sensor. The noise of the high-gain pixel was 2.21 ± 0.04 ADU, and that of the low-gain pixels were 1.44 ± 0.03 (BPW = 12×12 μm^2), 1.45 ± 0.03 (BPW = 14×14 μm^2) and 1.48 ± 0.03 (BPW = 16×16 μm^2) ADU, as shown in figure 5.

The criteria for the signal clustering are as follows: 1) calculate S/N for each pixel; 2) extract a pixel with S/N $>$ 64 (128 for high-gain) as a seed; 3) extract a pixel with S/N $>$ 16 (32 for

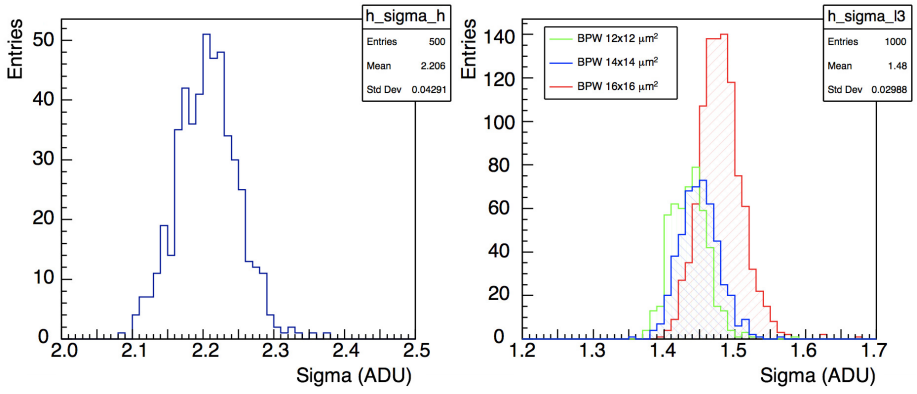

Figure 5. Pixel noise distribution. Left shows high-gain pixels and right shows low-gain pixels. The signal readout was done with an external 12-bit ADC.

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high-gain) from 5×5 pixels around the seed pixel, and then add a pixel to the cluster. Figure 6 shows the extracted cluster charge spectrum. The Red lines shows a Landau fit result. The most probable value of the Landau of the high gain pixel was 899 ± 1.8 and those for the low gain pixels were 451.8 ± 0.9 (BPW $= 12 \times 12\,\mu\text{m}^2$), 429.9 ± 0.8 (BPW $= 14 \times 14\,\mu\text{m}^2$) and 421.4 ± 0.6 (BPW $= 16 \times 16\,\mu\text{m}^2$). We obtained signal-to-noise ratios of high and low-gain pixels where the noise is of a single pixel, as shown in table 1. If we assume the charge to be shared over approximately 10 pixels, the necessary S/N is more than 17 to achieve 3 μm of spatial resolution. We can estimate the S/N of 50 μm thick sensors to be 41 (high-gain), which is enough to satisfy the requirement. We will evaluate the S/N and charge sharing of the sensor thinned to 75 μm during the next beam test.

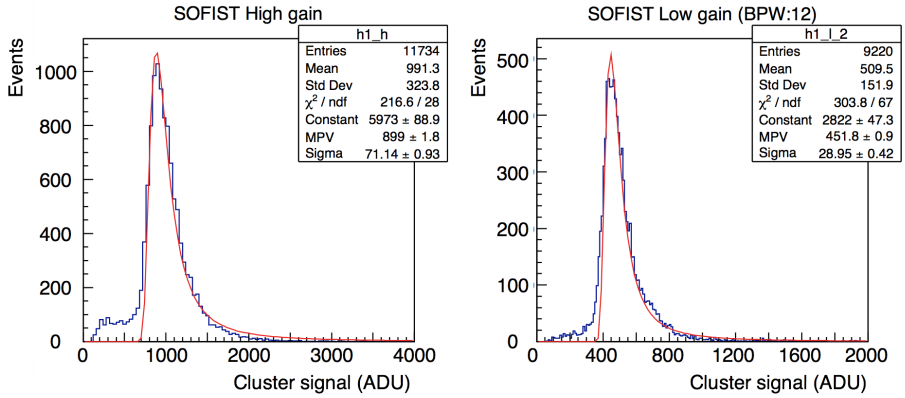

Figure 6. Cluster signal distributions. Left shows high-gain pixels and right shows low-gain pixels (BPW = $12 \times 12\,\mu\text{m}^2$). The signal readout was external 12-bit ADC.

Table 1. Summary of signal-to-noise ratio.

	High-gain $16 \times 16\,\mu\text{m}^2$	low-gain $12 \times 12\,\mu\text{m}^2$	low-gain $14 \times 14\,\mu\text{m}^2$	low-gain $16 \times 16\,\mu\text{m}^2$
S/N	409 ± 45	315 ± 30	296 ± 27	285 ± 20

3.2 Alignment and tracking

The hit position is reconstructed by calculating the weighted center of charges of the pixels belonging to the cluster. As a relative alignment among the sensors, we estimated the parallel shifts for x, y directions and rotation around the z-axis. The parallel shifts for x and y directions, Δx and Δy, that minimize the differences of the hit position on each sensor were calculated by utilizing a least square method. After applying these offsets to the x, y directions, the tracking was performed with FPIX2 of four layers for SOFIST ver.1. For FPIX2, three layers without the device under test (DUT) are used for the tracking. Track candidates for each directions are extracted by fitting a linear function to the hits on FPIX2. The track that has the minimum chi square is chosen if the event has multiple track candidates. The event is removed if the tracks for x, y directions are not constructed by the same hit combination. The rotation angle is extracted by the correlation between the residual and

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orthogonal hit position. The residual X_{res} is expressed as

$$\begin{aligned} X_{\mathrm{res}} &= X'(1-\cos\theta) + Y'\sin\theta \\ &\approx Y'\theta \quad (\theta \approx 0) \end{aligned} \tag{3.1}$$

where X' and Y' are the hit positions after applying Δx and Δy, and θ is the rotation angle around the z-axis. The rotation angle can be obtained as the slope of this equation if θ is sufficiently small. To evaluate the spatial resolution precisely, further alignment was applied to each sensor as follows: 1) calculate the mean of the residual, $|X_{\mathrm{res}}|$ and $|Y_{\mathrm{res}}|$; 2) subtract $|X_{\mathrm{res}}|$ and $|Y_{\mathrm{res}}|$ from Δx and Δy respectively; 3) calculate θ according to Equation 3.1; 4) repeat until Δx and Δy are less than 0.2 μm. FPIX2 #2 was used as the reference in this iterative alignment. The alignment was applied in the following order; FPIX2 #4, #1, #3, SOFIST ver.1 #1, #2.

3.3 Spatial resolution

Figure 7 shows the residual distribution between the track and hit position (y-direction) on SOFIST ver.1 #2 sensor according to section 3.2. The Red line shows a Gaussian. The nominal condition for measuring the residual is the 12-bit external ADC readout and a 500 μm depletion layer. We also measured the residual using an on-chip 8-bit column ADC readout with a 500 μm depletion layer and a 12-bit external ADC readout with a 200 μm depletion layer. The measured residual sigma for x and y-direction are summarized in table 2. The residual distribution is a convolution of SOFIST ver.1 resolution and FPIX2 resolution. The intrinsic spatial resolution of FPIX2 is approximately 0.7 μm [11], which leads SOFIST ver.1 resolution close to 1.2 μm. The effect of multiple scattering at the setup is very small due to the high energy beam.

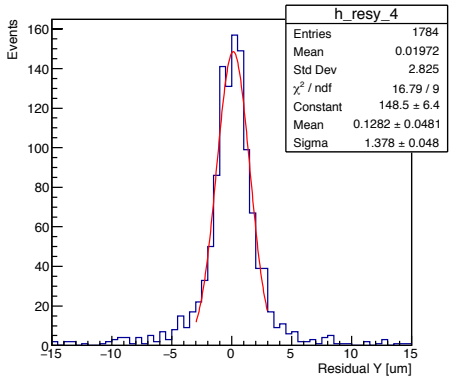

Figure 7. Residual distribution in y-direction to the track reconstructed by four layers of FPIX2.

Table 2. Measured residual to the track reconstructed by FPIX2.

	#1 x (μm)	#1 y (μm)	#2 x (μm)	#2 y (μm)
12-bit ADC, 500 μm depletion	1.37 ± 0.04	1.35 ± 0.04	1.50 ± 0.05	1.38 ± 0.05
8-bit ADC, 500 μm depletion	1.49 ± 0.06	1.38 ± 0.05	1.57 ± 0.08	1.55 ± 0.08
12-bit ADC, 200 μm depletion	1.33 ± 0.03	1.32 ± 0.03	1.58 ± 0.05	1.54 ± 0.04

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4 Conclusions and future prospect

We have been designing and developing a monolithic pixel detector using SOI technology for the ILC vertex detector. The first prototype sensor SOFIST ver.1 has an amplifier, two analog memories, and on-chip column ADCs. Its pixel size is $20 \times 20\,\mu\text{m}^2$. Using a 120 GeV proton beam at Fermilab Test Beam Facility, we obtained a residual resolution of approximately 1.5 μm. The effect of Coulomb multiple scattering is negligible. If we subtract the tracking resolution, the spatial resolution of SOFIST ver.1 is estimated to be close to 1.2 μm under the used readout and depletion conditions. The second prototype sensor SOFIST ver.2 ($25 \times 25\,\mu\text{m}^2$ pixel size) has a time stamp circuit and on-chip Zero-suppression logic. We plan to perform a beam test in January 2018 to study these functions. Our next challenge is implementing the full pixel circuit in the $20 \times 20\,\mu\text{m}^2$. The next prototype sensor SOFIST ver.4 is a 3D integrated SOI sensor. We will adopt the 3D integration technology of *Au* cone bump method by T-Micro [12] that allows connection between upper and lower chip with 5 μm $\times$ 5 μm spacing. The lower chip for the analog part has an amplifier and comparator, and the upper chip for the digital part has a shift register, and analog and time stamp memories up to three hits. SOFIST ver.4 was submitted in June 2017, and it will be delivered in December 2017.

Acknowledgments

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