From “Development of monolithic pixel detector with SOI technology for the ILC vertex detector”

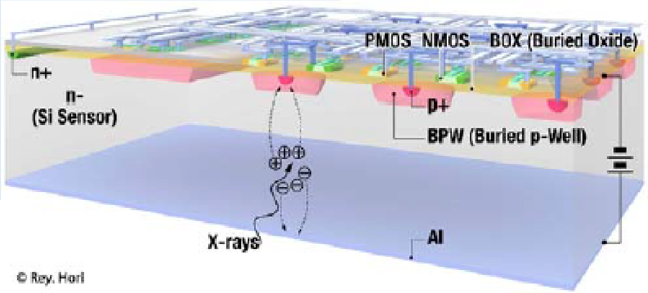
M. Yamada et. al., JINST, vol.13, 2018, C01037

JC64 paper 05.18.2018

Several Introduction slides about the SOI detector from Prof. Arai (@ OIST 2017Dec)

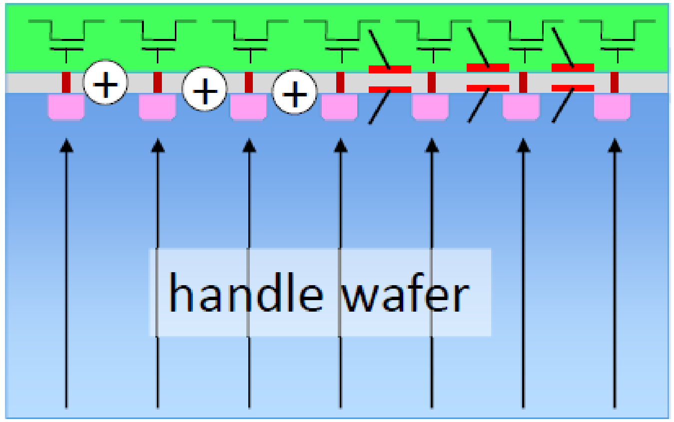
Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding. Small pixel size.
- Fabricated with semiconductor process only.
  → High reliability and Low Cost.
- High Resistive fully depleted sensor (50um~700um thick) with Low sense node capacitance. → Large S/N.
- On Pixel processing with CMOS circuits.
- No Latch up and very low Single Event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.



Charge affects the circuit (transistor) operation

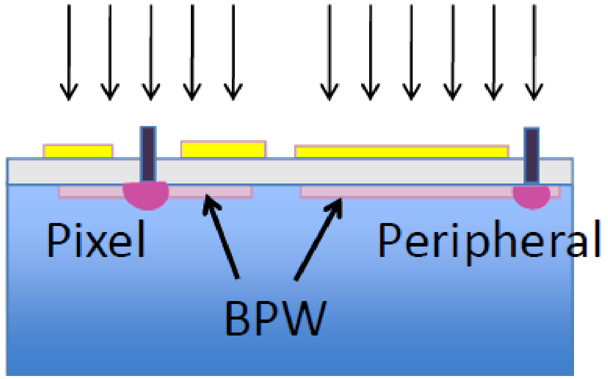
Main issues in SOI Pixel



- Transistors does not work when high-voltage is applied to handle wafer.
  (Back-Gate Effect)
- Circuit signal and sense node couples.
  (Signal Cross Talk)
- Oxide trapped hole induced by radiation will shift transistor threshold voltage.
  (Radiation Tolerance)

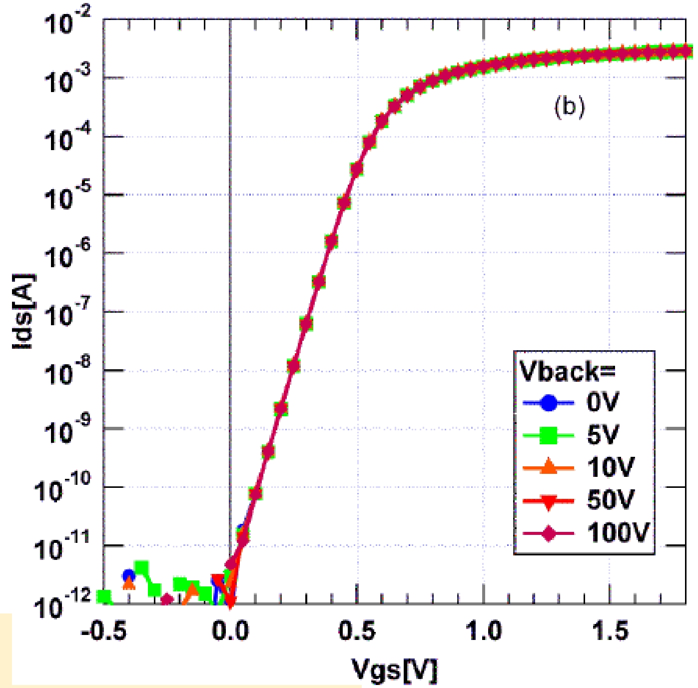
1st refinement: Buried p-Well (BPW)

keyword in the paper



- Keep Top Si not affected
- Low Dose

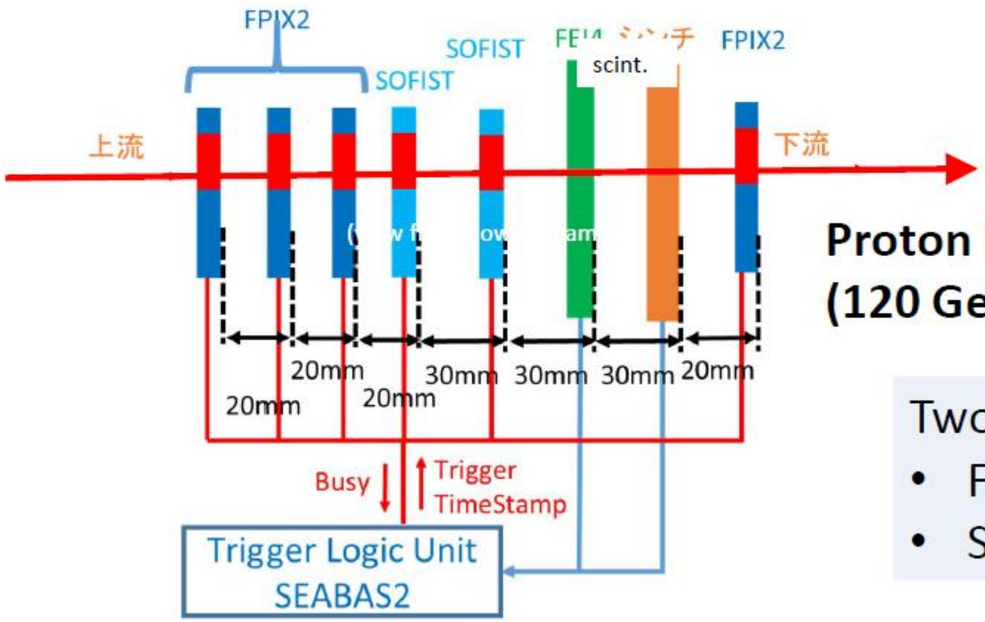
NMOS Ids – Vgs with BPW=0V

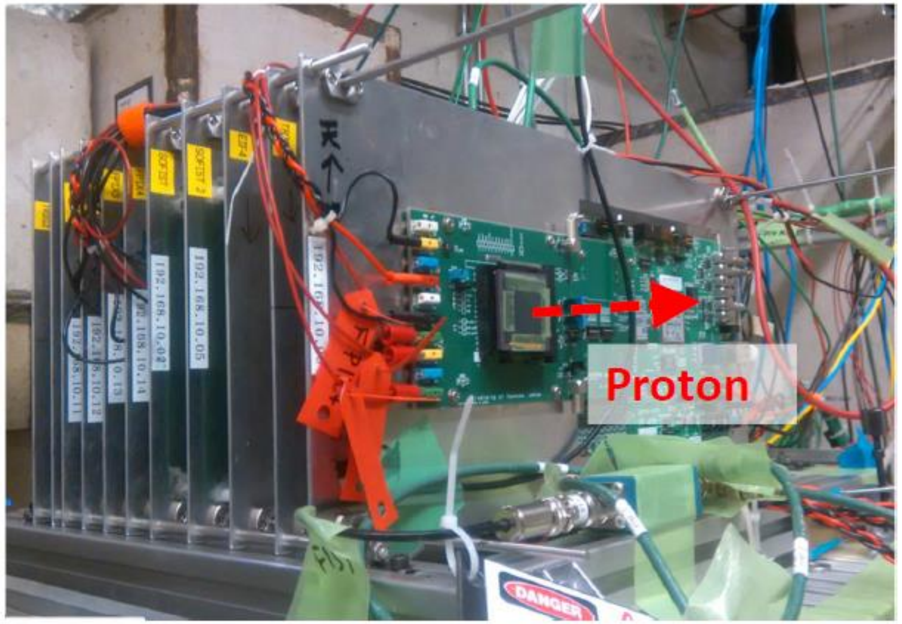


- Suppress the **Back Gate Effect**.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- With biasing middle Si layer, radiation hardness is improved.

“The BPW is a p+ layer implanted underneath the BOX layer, which reduces the electric field in the BOX layer by utilizing the p+-n junction. “ （from M. Kochiyama et al., NIMA (2010)）

Tracking Resolution:
High-Energy Beam test @Fermi National Accelerator Lab.





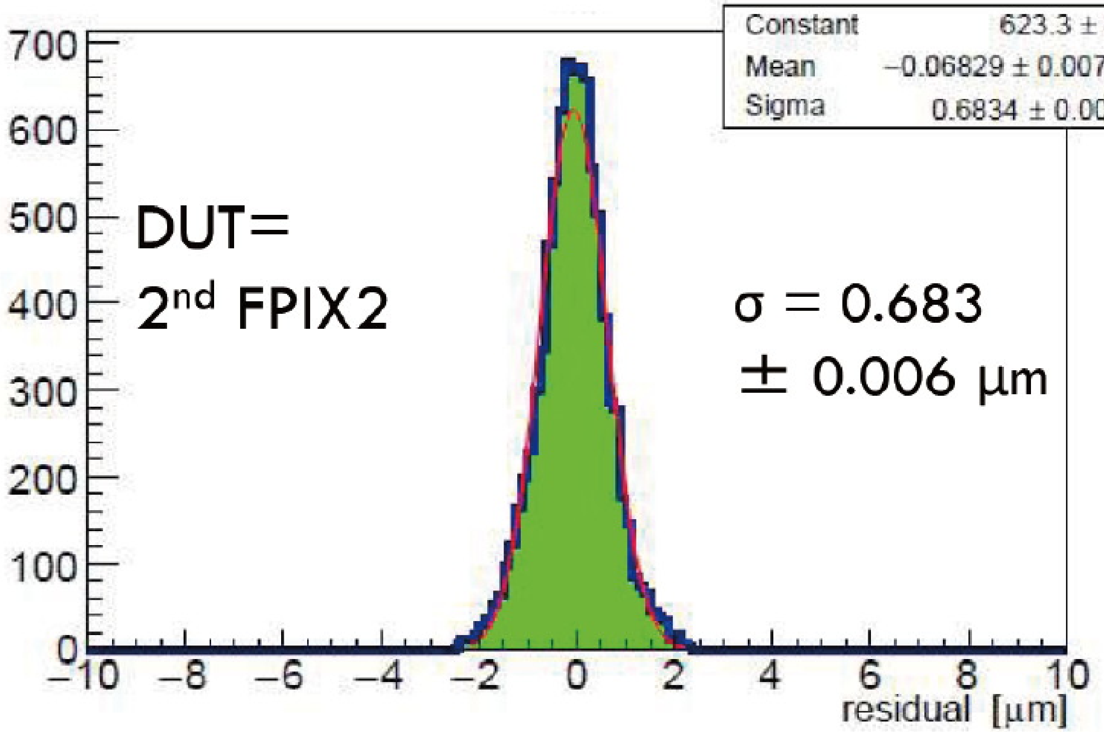
Proton Beam (120 GeV/c)

Two kinds of SOIPIX-DSOI detectors are used:

- FPIX2 x 4: 8 µm square pixel detector
- SOFIST1 x 2: 20 µm square pixel detector

I (Ryuta) have shortly introduced this page & next page in the past JC.

Tracking Resolution (cont.)



Less than 1 μm Position Resolution for high-energy charged particle is achieved first in the world .

(K. Hara et al., Development of Silicon-on-Insulator Pixel Detectors, Proceedings of Science, to be published)

Today’s paper is about the other (SOFIST) SOI pixel detector

Return to the paper ...

Requirements for the ILC vertex detector

-- from the paper --

・ Single point resolution of better than 3 μm

・Time resolution to identify a single bunch crossing every 554 ns for 1300 bunches.

→ one comment : FPCCD (for ILC vertex) has no timing information

・Low detector occupancy of less than 2%

・Low material budget of less than 0.1-0.2% of radiation length X_0 .

SOI sensor for Fine measurement of Space and Time (= SOFIST)

・ A prototype pixel sensor for the ILC

・ monolithic pixel sensor with silicon-on-insulator technology (SOIPIX), 0.2 μm fully depleted SOI CMOS process

・Pixel size : 20 x 20 μm^2

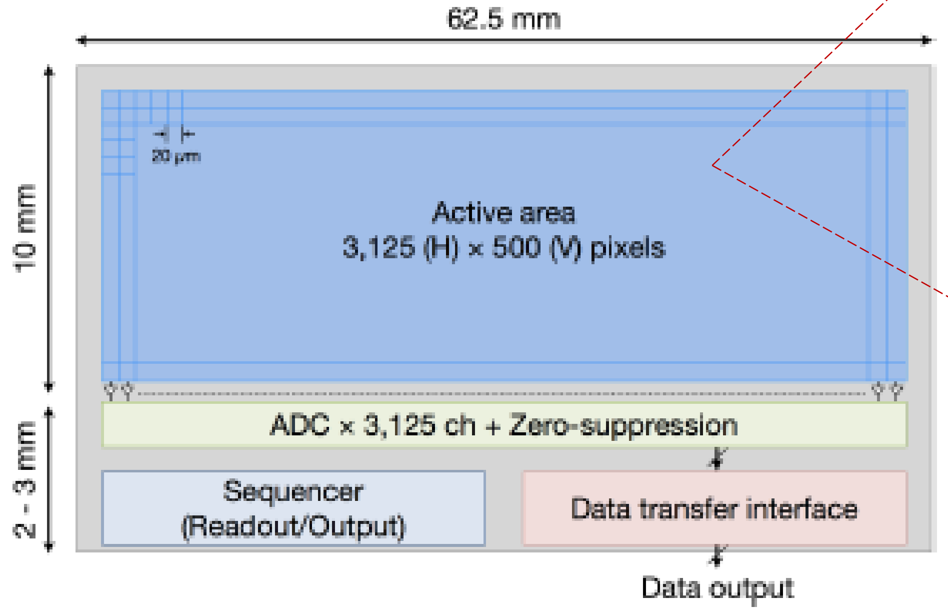
・Number of pixels : 3125 x 500 (⇔ 50 x 50 , proto ver.1)

・Sensor thickness: 50 μm (⇔ 500 μm proto ver.1)

Overview

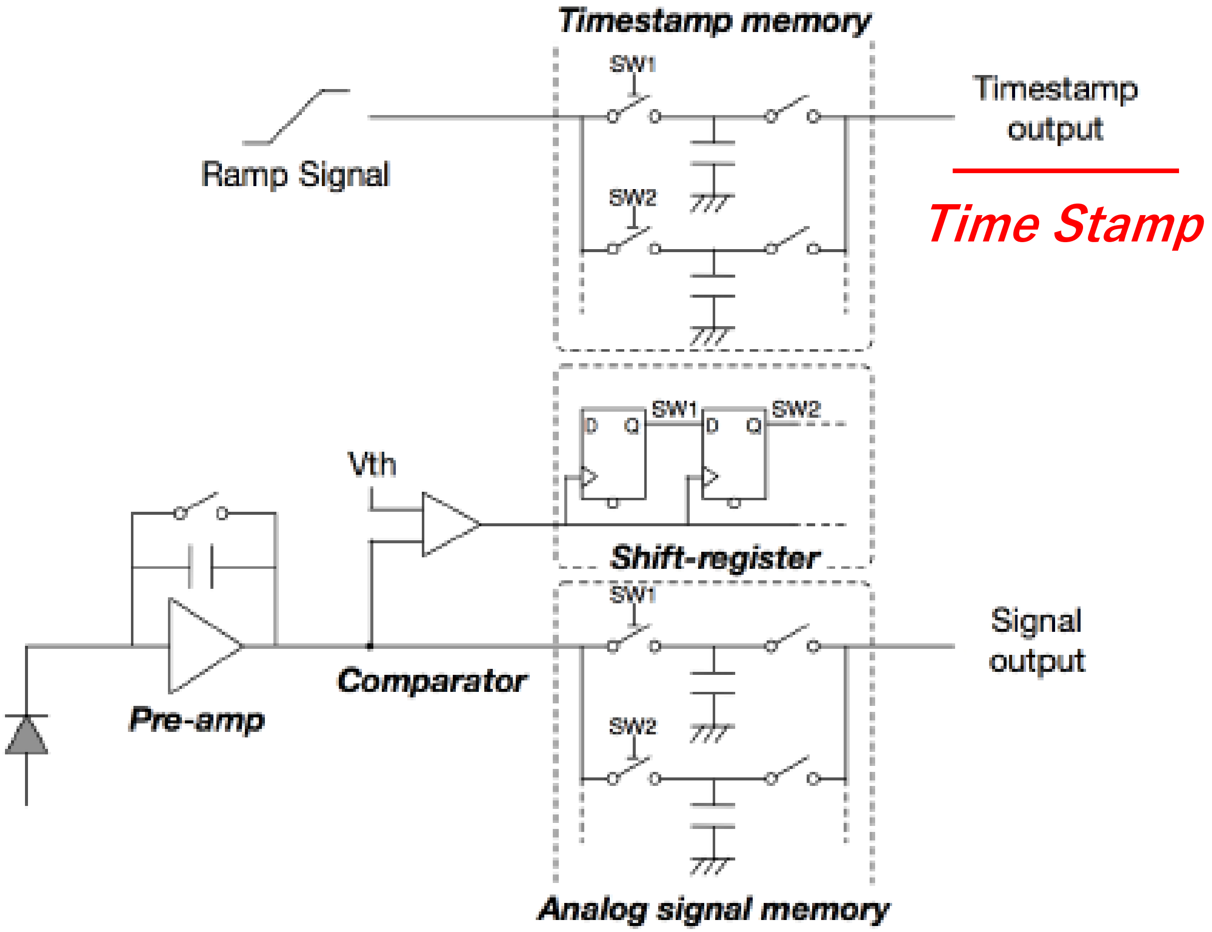
-- Amp/shift register/memory/time stamp in a pixel

-- column ADCs, zero-suppression, memories, outside of active area



(a) SOFIST.

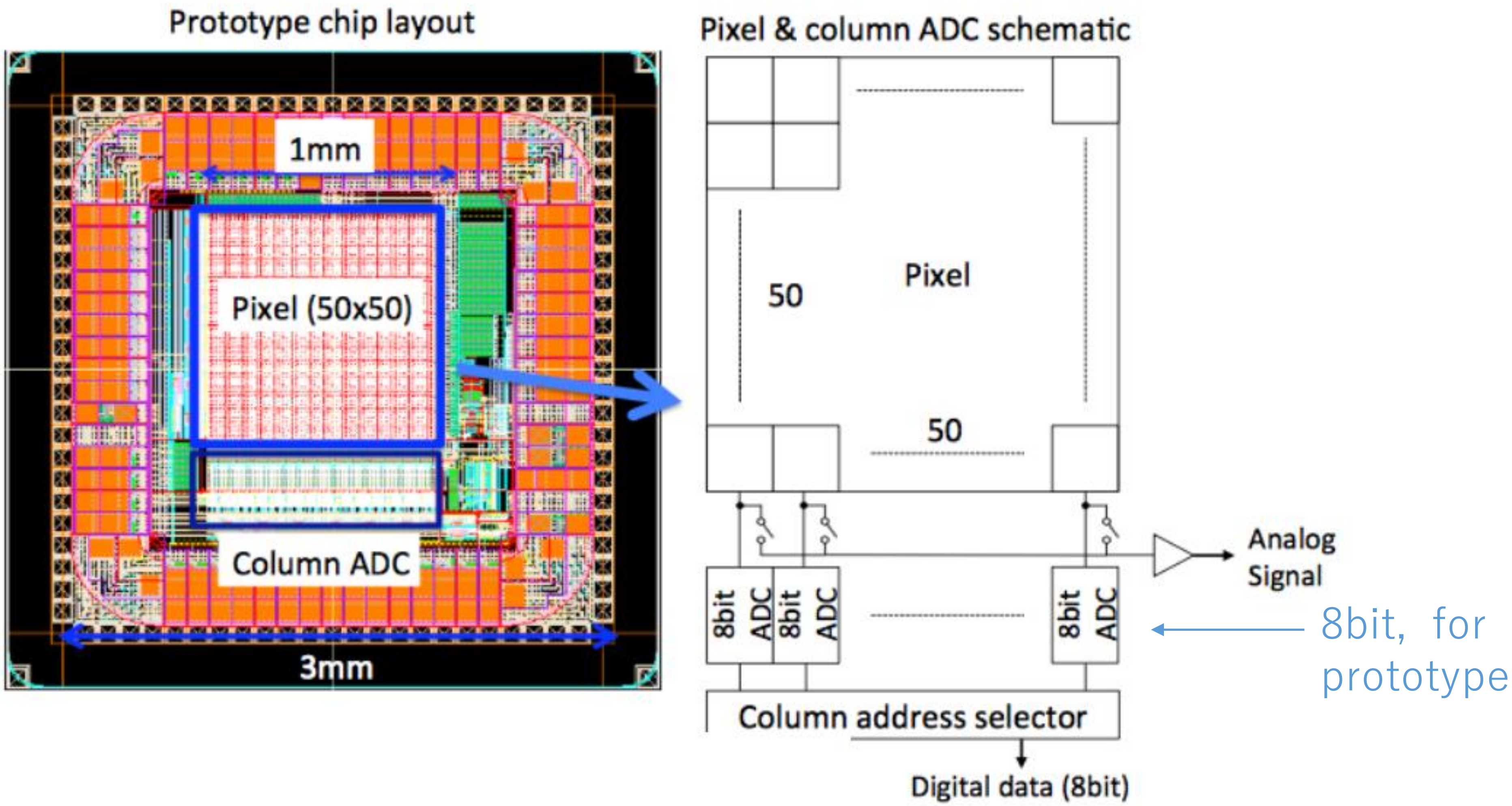
Circuit within a pixel



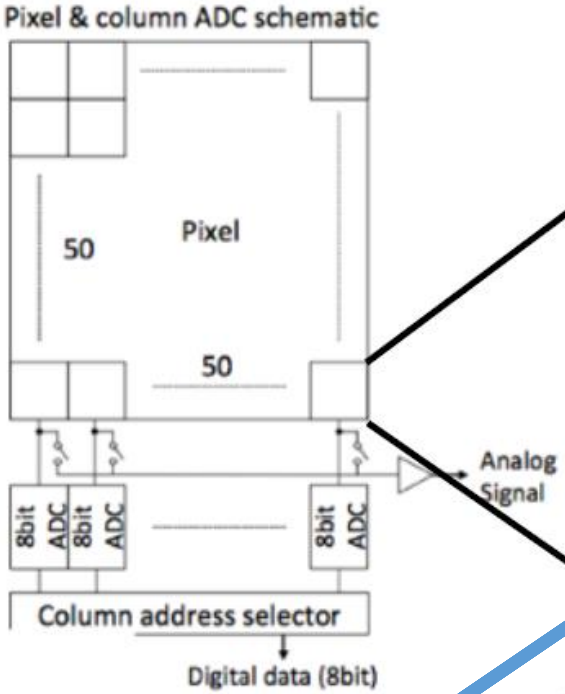
(b) Signal readout circuit.

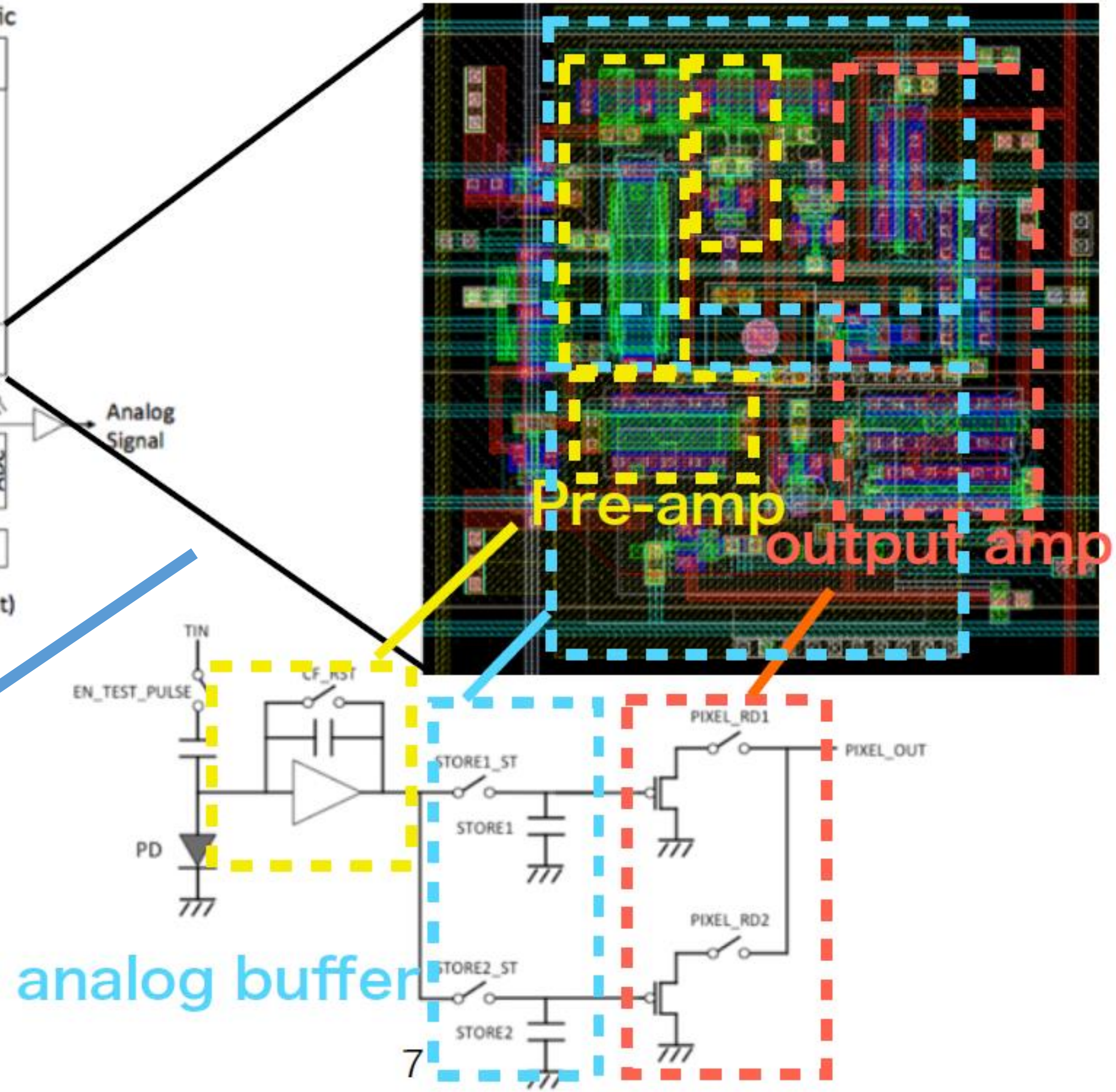
Figure 2

SOFIST prototype ver.1



taken from a slide by T. Mori "operation test of SOFIST:SOI sensor of ILC"





My(Ryuta) impression is that the surface is almost covered with the (CMOS) circuit, even at proto stage

taken from a slide by T. Mori "operation test of SOFIST:SOI sensor of ILC"

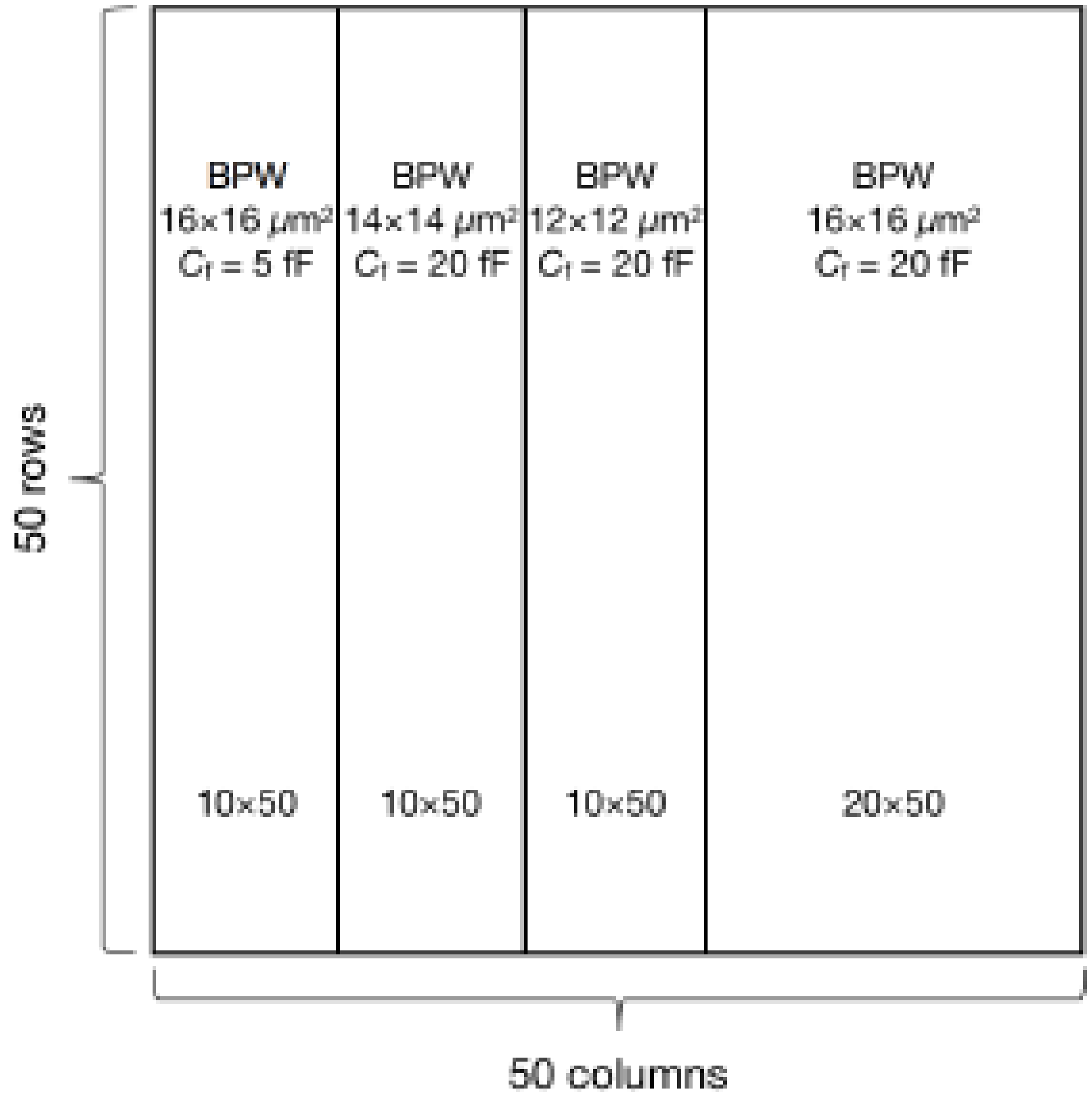
Pixel Layout

- Different BPW size

  16x16, 14x14, 12x12

- Different Gain

  Gain ~ 1/C



(a) Pixel layout

Beam Test

・ 120 GeV proton beam

・ Fermilab Test Beam Facility

・ FPIX(2) , another SOI pixel detector with 8x8 μm^2 -- fine position resolution

・trigger is made by coincidence of he scintillation counter and ATLAS pixel detector FE-I4

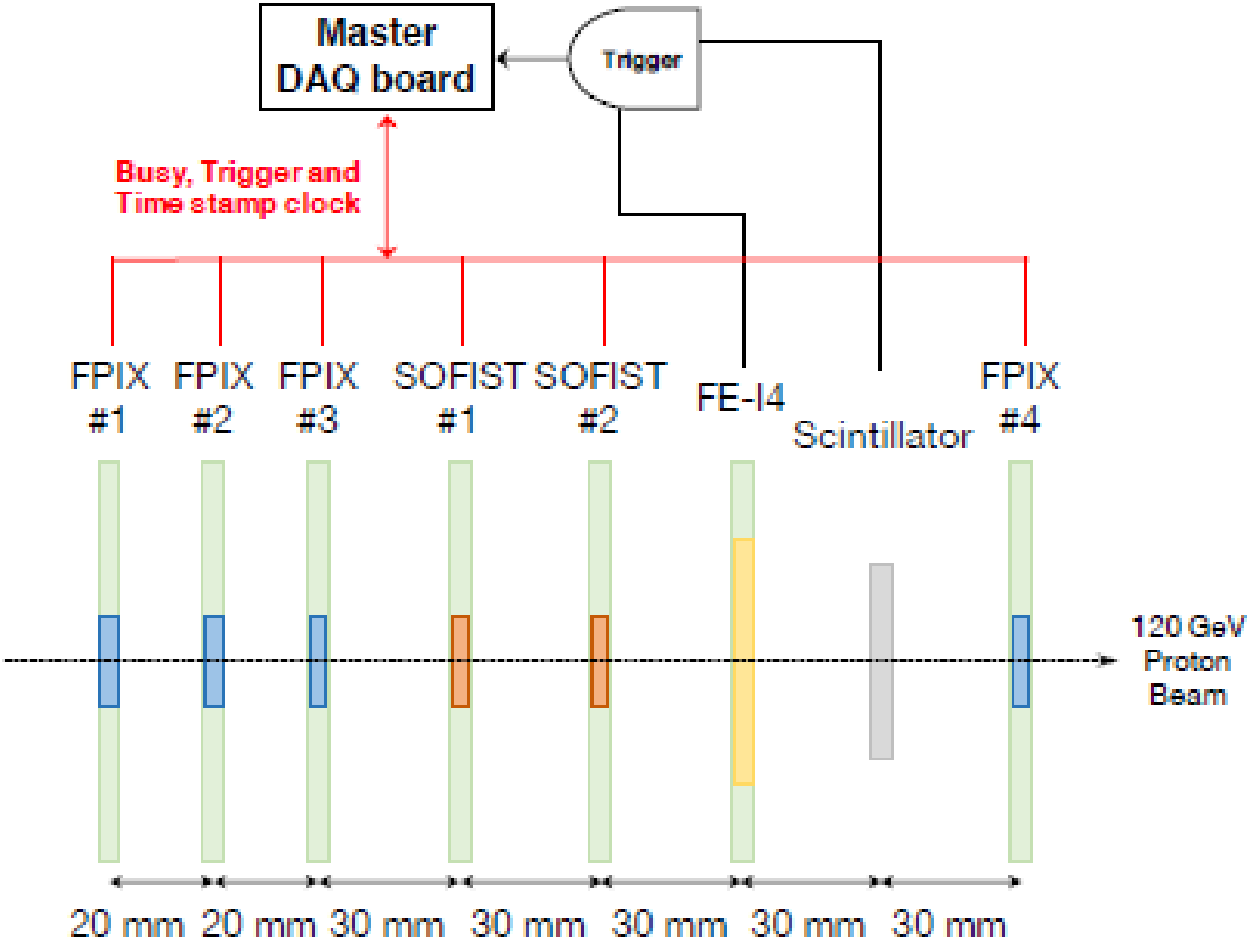


Figure 4. Setup (not to scale)

・148 hours beam time (but they claimed "low" statistics for tracking …)

Analysis I. Noise distribution

[Step]

1) noise of one pixel is extracted by fitting a Gaussian to the pedestal distribution

2) mean of Gaussian sigma of all pixels as the noise of the sensor

Gaussian sigma distribution

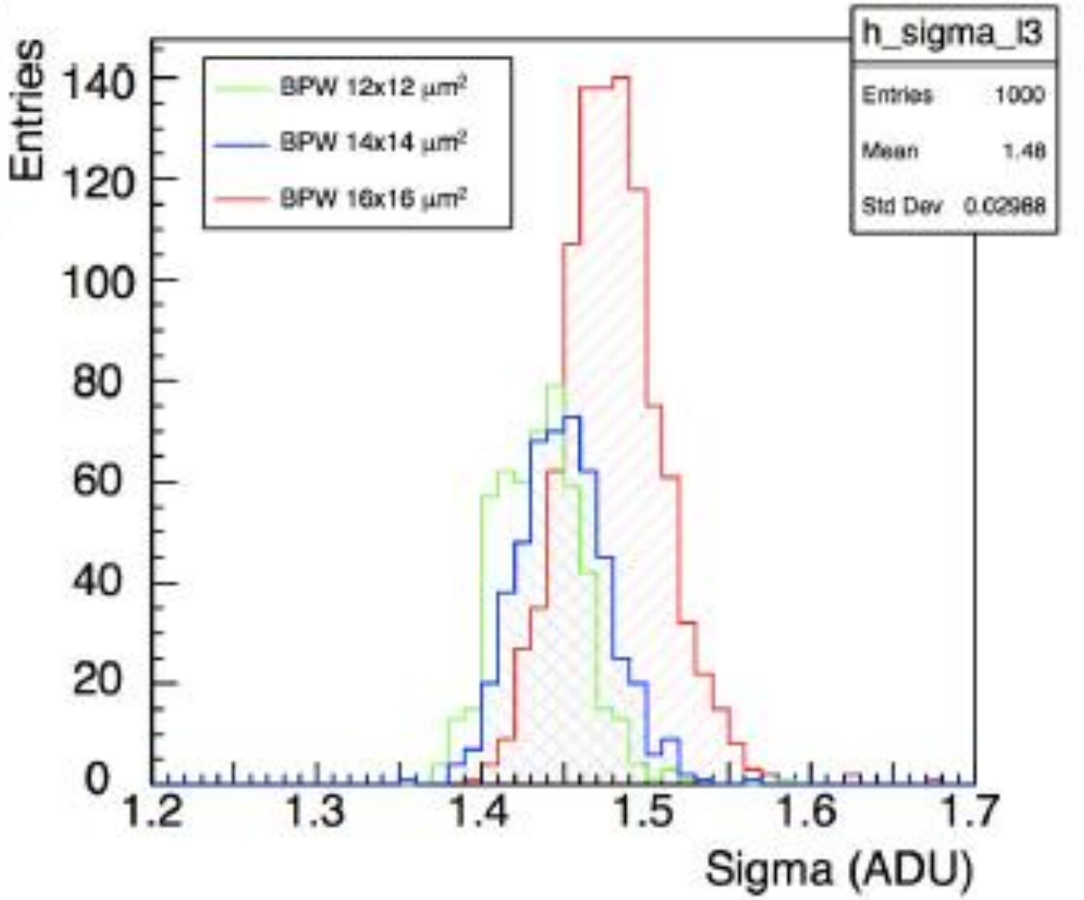


Figure 5. Pixel noise distribution. Left shows high-gain pixels and right shows low-gain pixels. The signal readout was done with an external 12-bit ADC.

Analysis II. Clustering

[Step]

1) calculate S/N for each pixel

2) extract a pixel with S/N>64 as a seed

3) extract a pixel with S/N>16 from 5x5 pixels around the seed, then add a pixel to the cluster

"N" would be the Gaussian sigma of the pixel or the "sensor" noise ?

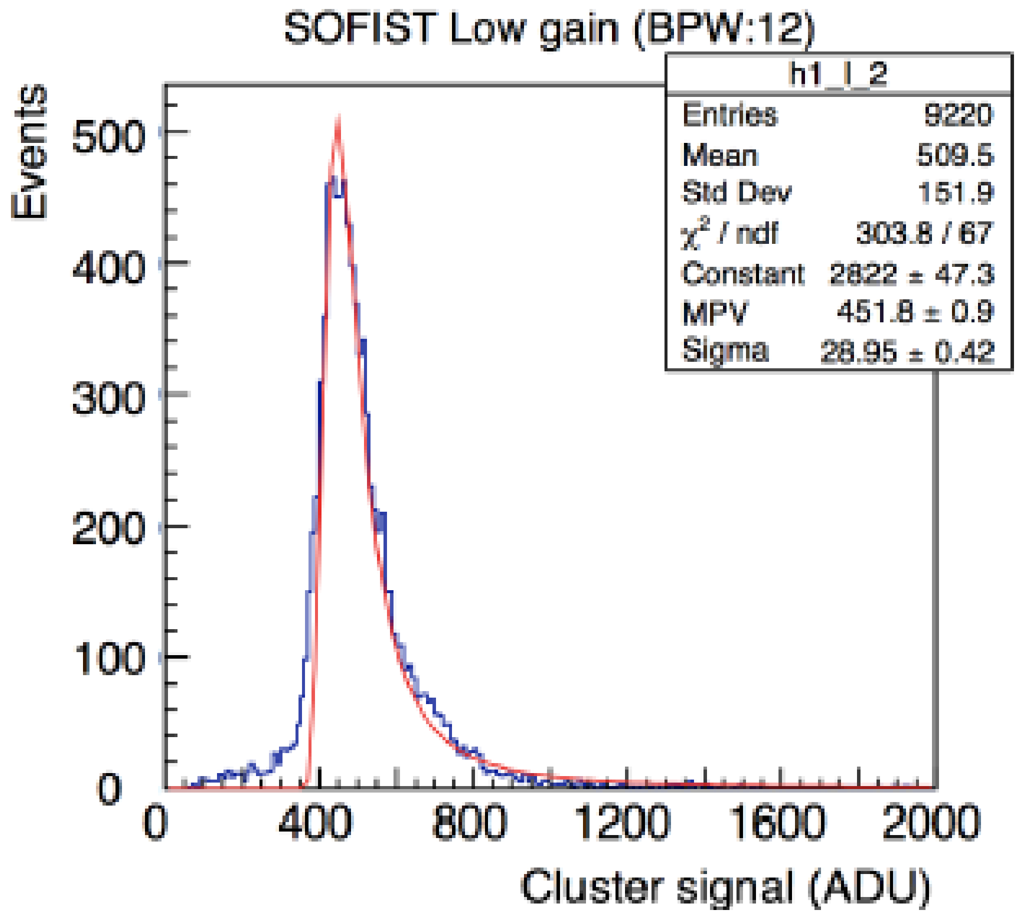


Figure 6. Cluster signal distributions. Left shows high-gain pixels and right shows low-gain pixels (BPW = $12 \times 12\ \mu m^2$). The signal readout was external 12-bit ADC.

Signal-to-Noise Ratio

Comments (question) from Tao about the definition of the S/N

Table 1. Summary of signal-to-noise ratio.

	High-gain $16 \times 16\ \mu m^2$	low-gain $12 \times 12\ \mu m^2$	low-gain $14 \times 14\ \mu m^2$	low-gain $16 \times 16\ \mu m^2$
S/N	409 ± 45	315 ± 30	296 ± 27	285 ± 20

S: Most Probable value of the fitted Landau function

N: Noise of a single pixel (“sensor” noise)

However, though it is not explicitly written, the cluster size might be close to 1 due to

-- full depletion with high bias voltage => charge will be collected mainly by drift not diffusion

-- it is possible that the beam track is almost perpendicular to the sensor

-- relatively high cut threshold, owing to the 500 μm thickness

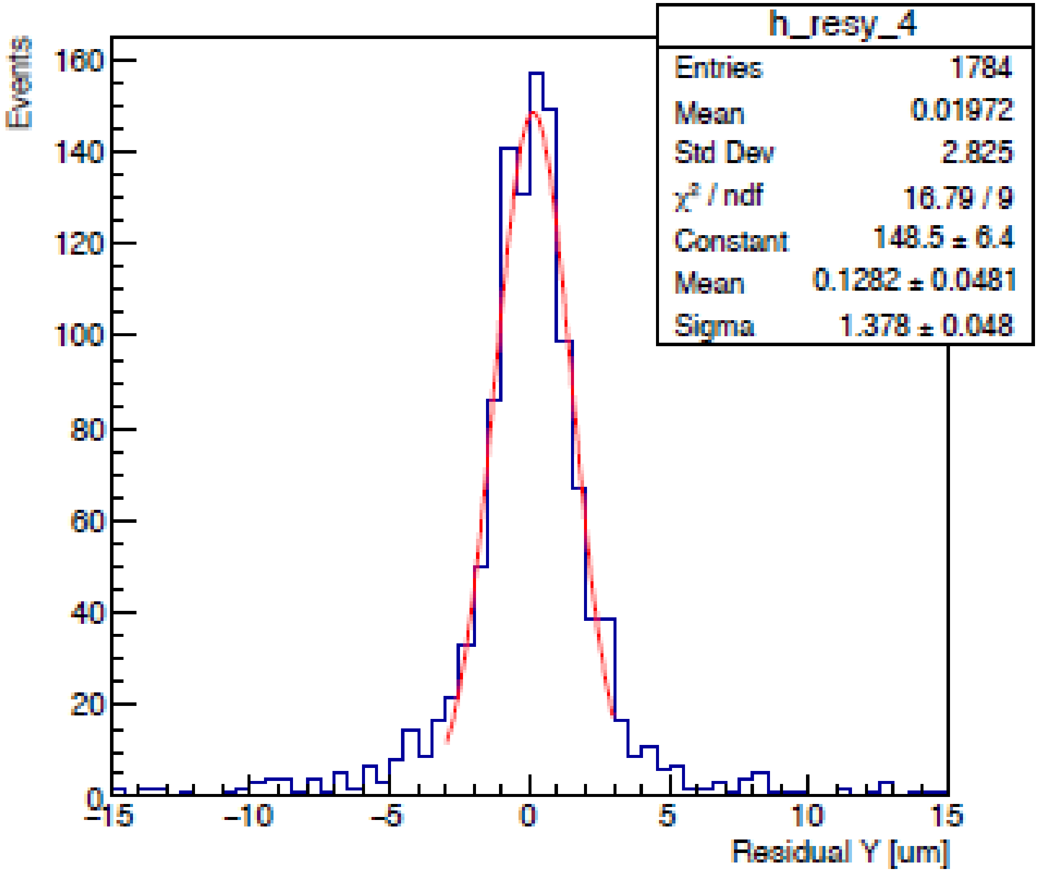
Analysis III. Spatial Resolution

-- (in offline) X, Y position adjustment between the sensors.

-- (in offline) rotation angle around z direction adjustment

Iterative alignment

obtain residual distribution after this fine-tuning



Subtracting the position resolution of the reference detector (FPIX2), the position resolution of SOFIST is ~1.2 μm.

Conclusion and future prospect

memories, and on-chip column ADCs. Its pixel size is $20 \times 20\,\mu m^2$. Using a 120 GeV proton beam at Fermilab Test Beam Facility, we obtained a residual resolution of approximately $1.5\,\mu m$. The effect of Coulomb multiple scattering is negligible. If we subtract the tracking resolution, the spatial resolution of SOFIST ver.1 is estimated to be close to $1.2\,\mu m$ under the used readout and depletion conditions. The second prototype sensor SOFIST ver.2 ($25 \times 25\,\mu m^2$ pixel size) has a time stamp circuit and on-chip Zero-suppression logic. We plan to perform a beam test in January 2018 to study these functions. Our next challenge is implementing the full pixel circuit in the $20 \times 20\,\mu m^2$. The next prototype sensor SOFIST ver.4 is a 3D integrated SOI sensor. We will adopt the 3D integration technology of *Au* cone bump method by T-Micro [12] that allows connection between upper and lower chip with $5\,\mu m \times 5\,\mu m$ spacing. The lower chip for the analog part has an amplifier and comparator, and the upper chip for the digital part has a shift register, and analog and time stamp memories up to three hits. SOFIST ver.4 was submitted in June 2017, and it will be delivered in December 2017.