Front-End Electronics for Timing Detectors

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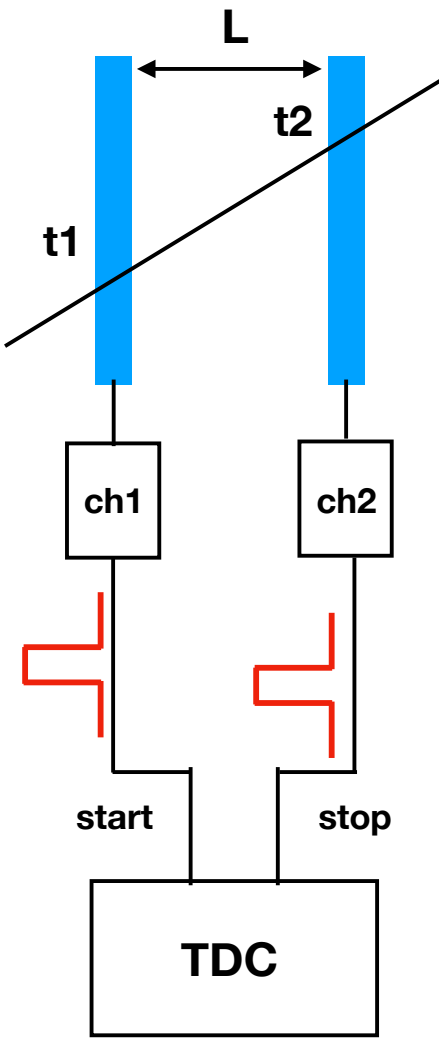
Outline

Application 1: PID in particle physics

- Traditionally, high resolution timing detectors are used in HEP to indentify particles



  - Measure the time to fly between two points to obtain velocity
  - Combine with momentum information to derive the mass

$$t = \frac{L}{v} = \frac{LE}{pc^2}$$

$$t = \frac{L\sqrt{(pc)^2 + (m_0c^2)^2}}{pc^2}$$

$$t = \frac{L}{c}\sqrt{1 + \frac{(m_0c^2)^2}{(pc^2)^2}}$$

How much resolution do we need for PID?

- Take two particles with same momentum

$$\Delta t = L\left(\frac{1}{v_1} - \frac{1}{v_2}\right) = \frac{L}{pc^2}\left(E_1 - E_2\right)$$

$$\Delta t = \frac{L}{pc^2}\left(\sqrt{p^2c^2 + m_{01}^2c^4} - \sqrt{p^2c^2 + m_{02}^2c^4}\right)$$

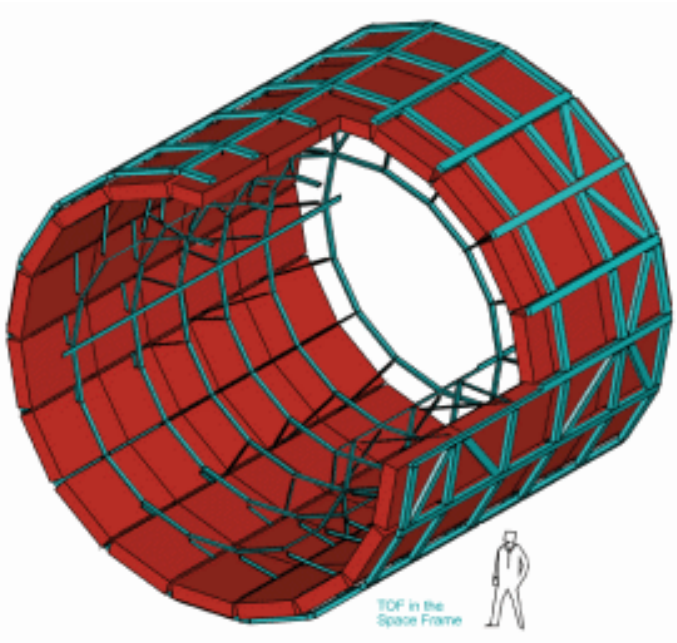
$$\sqrt{p^2c^2 + m_{01}^2c^4} = pc\sqrt{1 + \frac{m_{01}^2c^4}{p^2c^2}} \approx pc\left(1 + \frac{m_{01}^2c^4}{2p^2c^2}\right)$$

$$\Delta t \approx \frac{L}{pc^2}\left[\left(pc + \frac{m_{01}^2c^4}{2pc}\right) - \left(pc + \frac{m_{02}^2c^4}{2pc}\right)\right] = \frac{Lc}{2p^2}\left(m_{01}^2 - m_{02}^2\right)$$

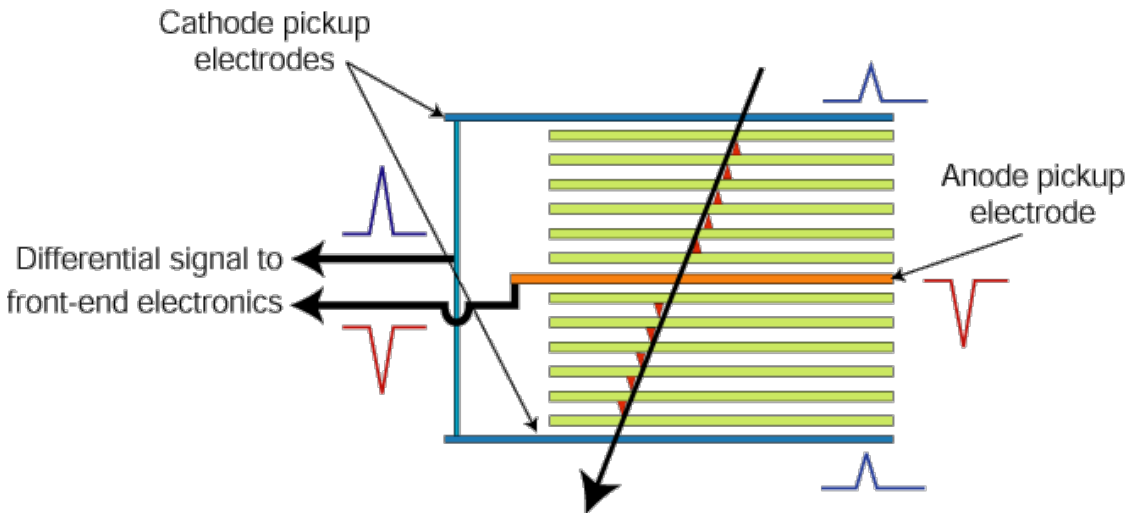
- For Kaon (500 MeV), pion (140 MeV) with p=1 GeV, L=2m, Δt= 800 ps

Example: the ALICE ToF detector at CERN

- Large area: 160 m^2
- Channel counts: about 160.000
- Time resolution: O(50 ps)



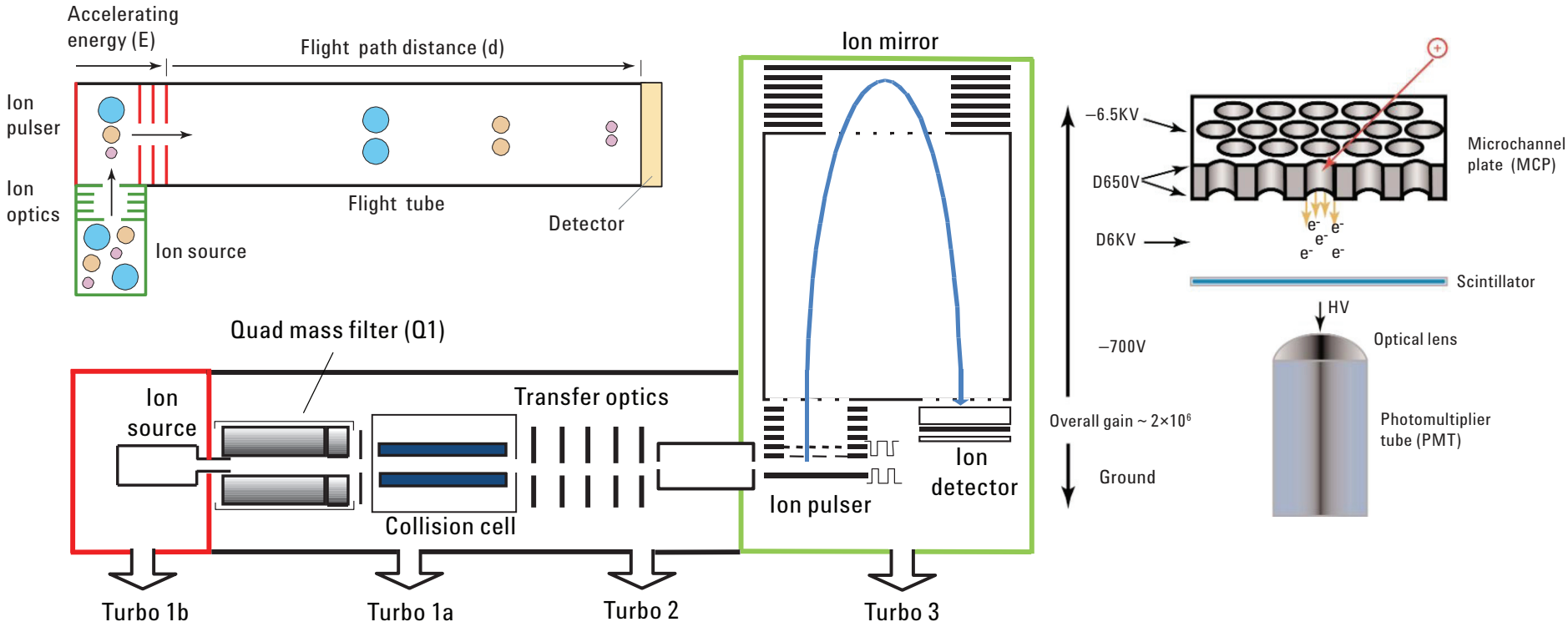
- Sensors: Multi-gap Resistive Plate Chambers (MRPC)



- For more info: http://aliceinfo.cern.ch/Public/en/Chapter2/Chap2_TOF.html

Application 2: Time of flight mass spectrometry

- Sorting chemical species on the basis of their mass-to-charge ratio
- Powerful analysis technique applicable both to pure samples and mixtures
- ToF is just one among many possible technique



ToF mass spectrometry

- Non-relativistic regime!

$$E = \frac{1}{2}mv^2 \rightarrow v^2 = \frac{2E}{m}$$

$$v = \frac{d}{t} \rightarrow m = \frac{2Et^2}{d^2}$$

$$m = A\left(t_m - t_0\right)^2$$

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- Fastest mass spectrometry analyzer
- Well suited for pulse ionization techniques
- Highest practical mass range

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- Fastest mass spectrometry analyzer
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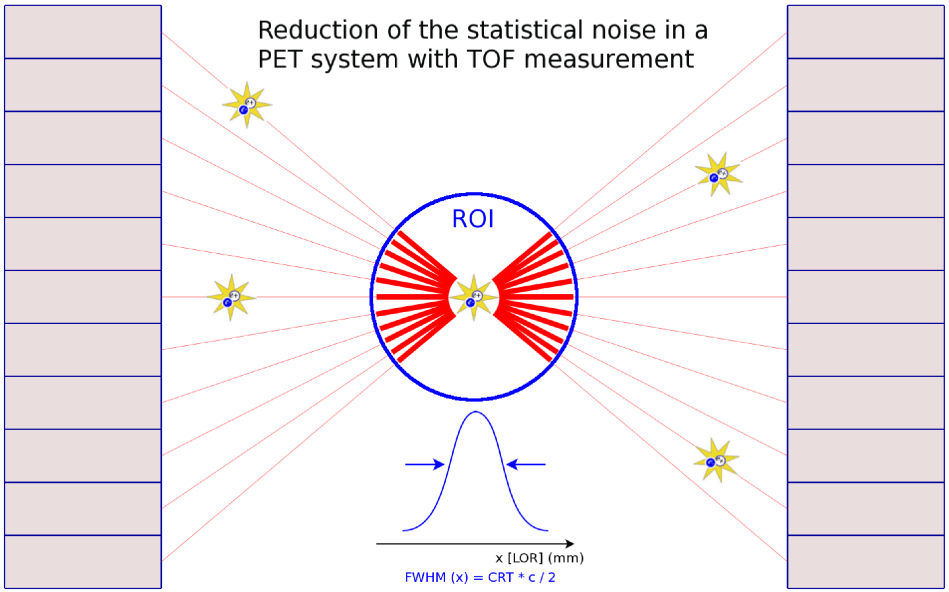
- Highest practical mass range
- Require pulse ionization methods
- Dynamic range of fast digitizers

Application 3: Positron Emission Tomography

- Anticipated 50 years ago, but still evolving

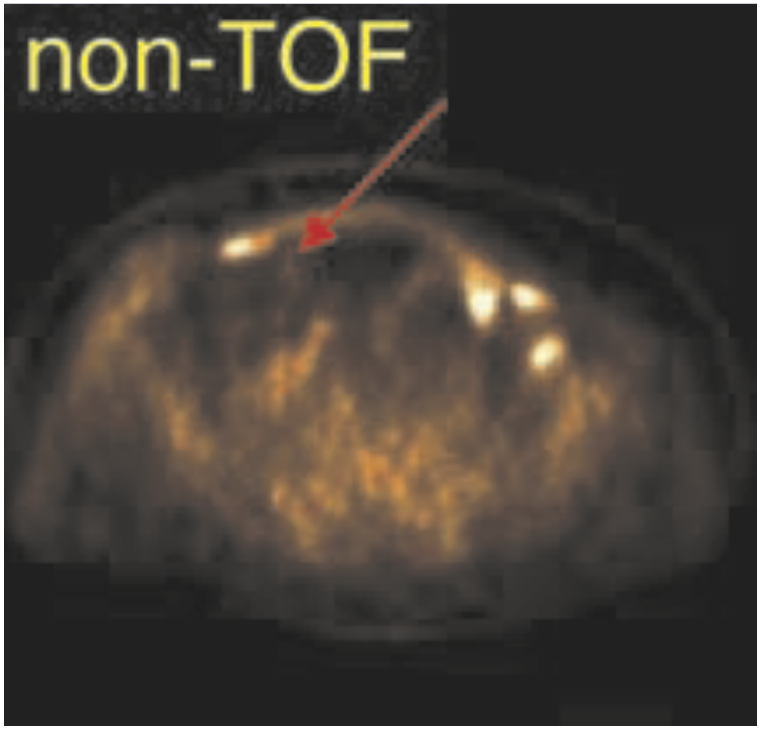


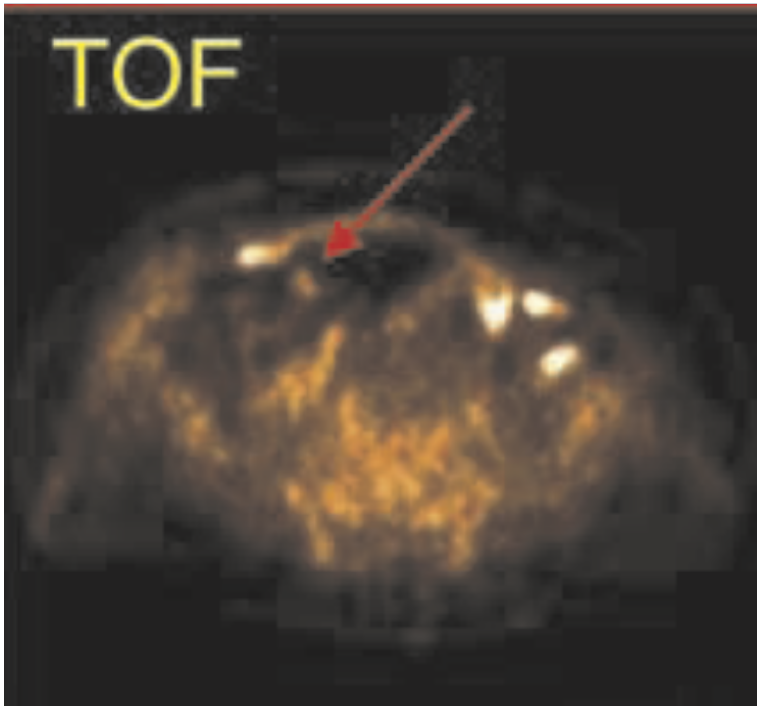
- More weight to photons coming from the ROI
- Stronger benefit on larger patients
- Commercial instruments offering better than 300 ps arriving on the market
- The holy Grail:
  10 ps→3 mm→direct imaging

S. Surti, *Journal of Nucl. Med.*

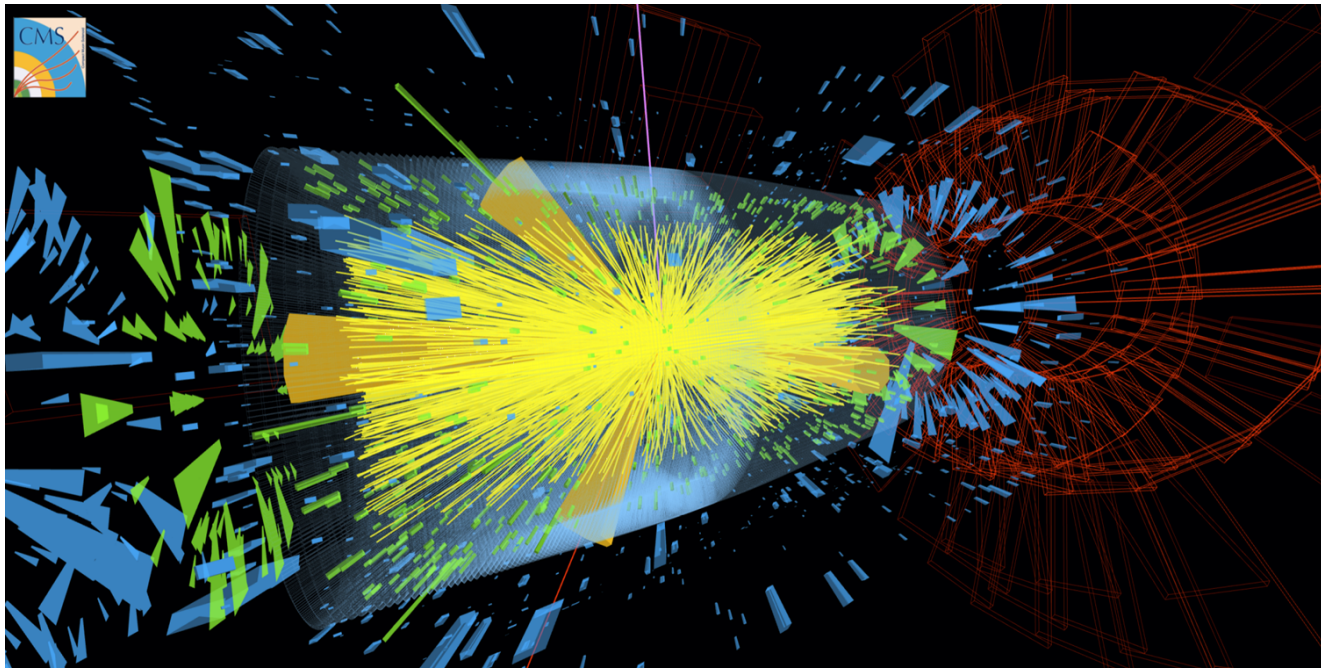
$$\Delta x = \Delta t \frac{c}{2}$$

ToF in PET





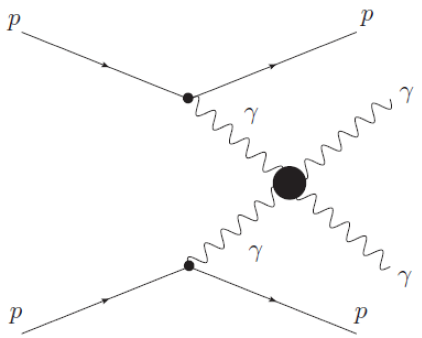
Applications 4: Pile-up rejection in HEP



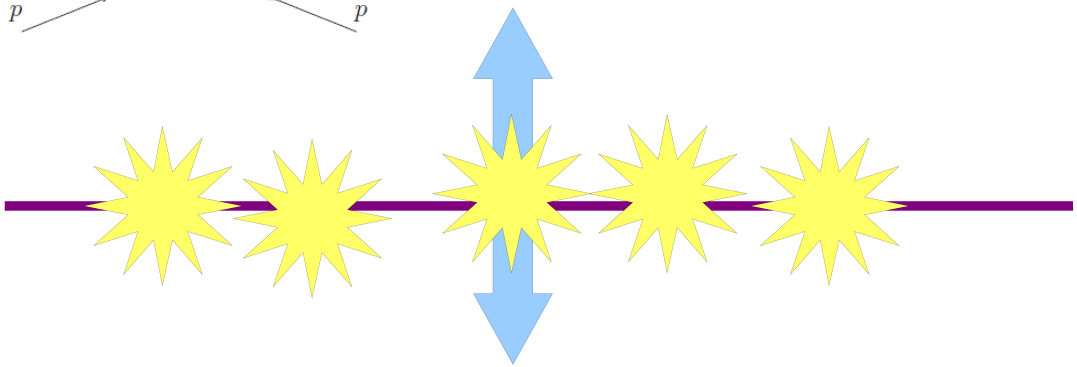
- The peak luminosity of the HL-LHC will increase up to $\approx 10^{35}$
- This will produce 140 to 200 collisions per bunch crossing
  - Disentangling interesting events from background only with tracking and vertexing becomes challenging
  - The average collision distance in time is $100 \div 170$ ps

Application 5: Forward physics at HL-LHC

- Collision survivors can be used to probe new physics



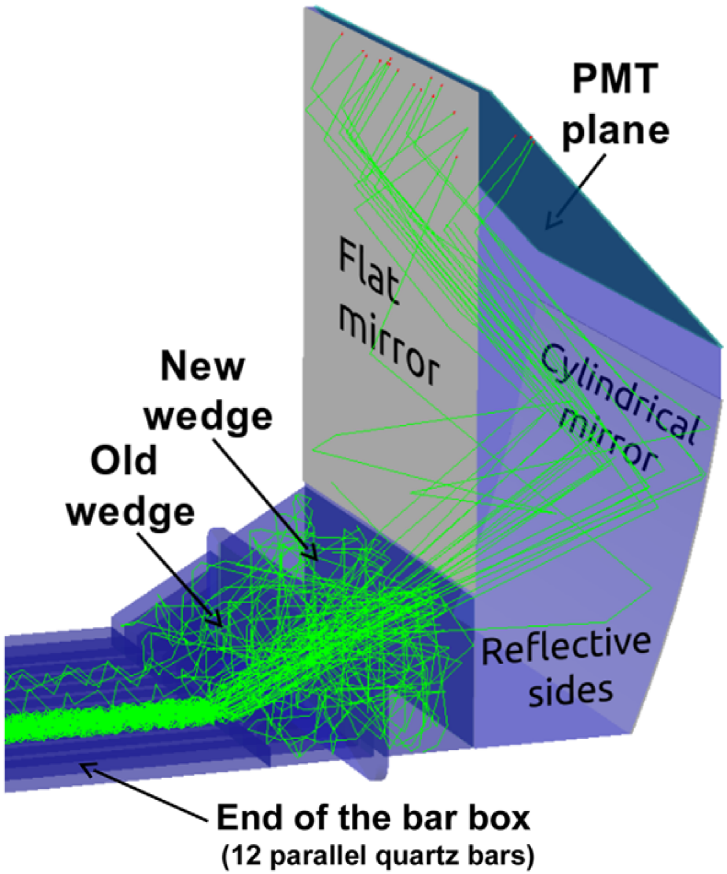
$$pp \rightarrow p\gamma\gamma p$$



- $pp \rightarrow p\gamma\gamma p$ sensitive to extra-dimensions
- Intact protons detected 250 m far from the collision point
- Need of 10 ps timing to suppress pile-up

Application 6: detector improvement

- Particle identification through Cherenkov radiation: $\cos\theta_c = \frac{1}{\beta n(\lambda)}$

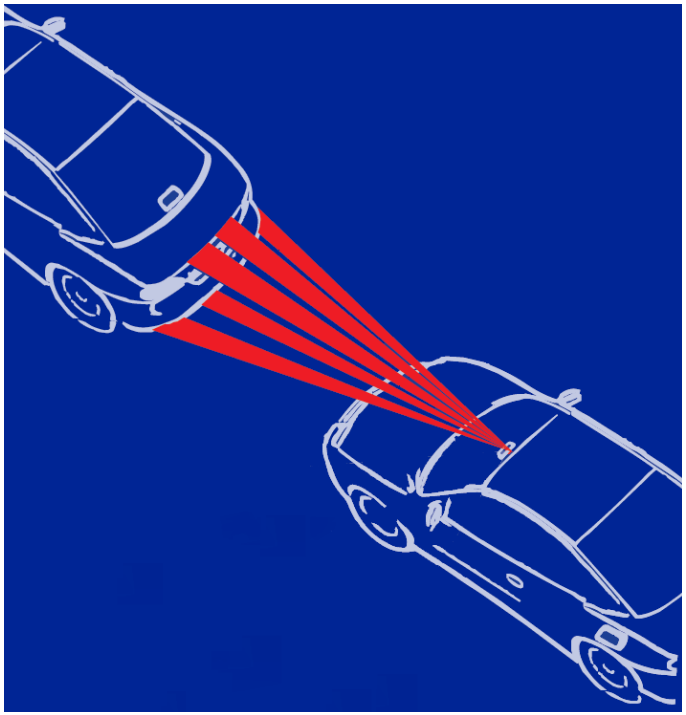


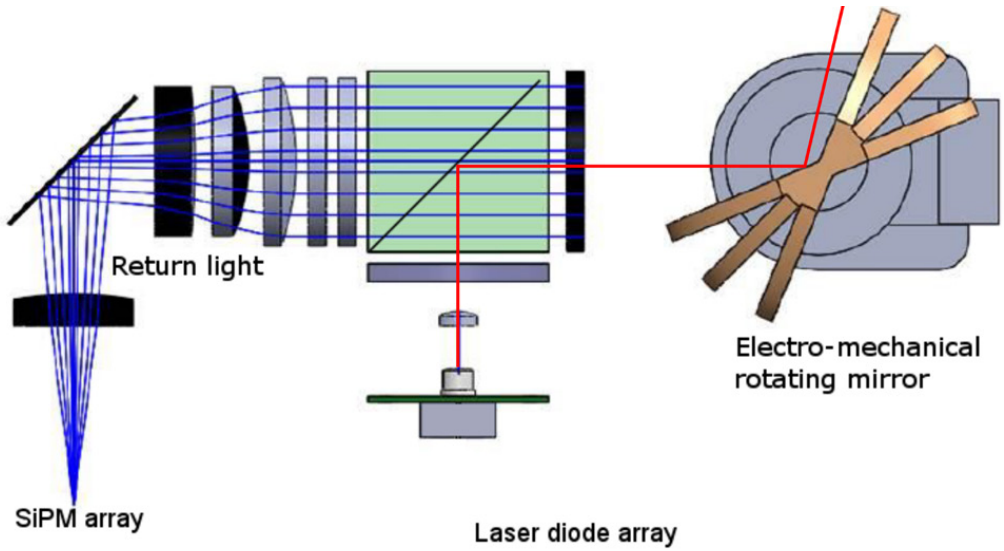
- Red photons give smaller angles than blue photons
- Red photons propagate faster in the medium
- Time of propagation used for chromatic corrections
- Improvement by 0.7 mrad reported
- Time resolution O(100 ps)

B. Dey et al., NIM A 775 (2015), pp. 112-131

Applications 7: LIDAR in ADAS systems

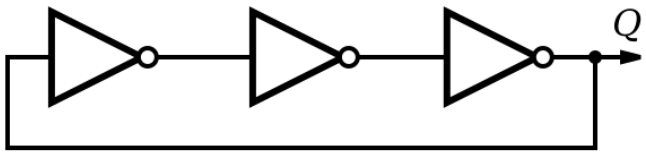
- LIDAR expected to become a key component in future cars

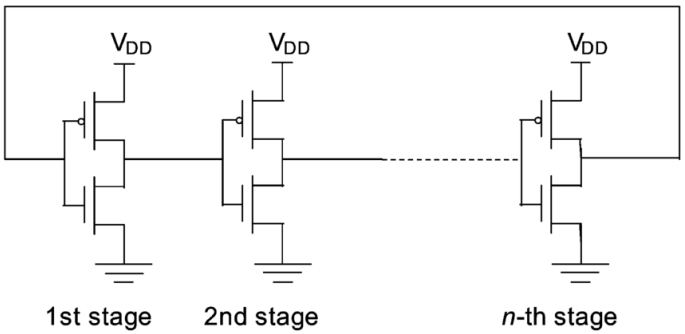




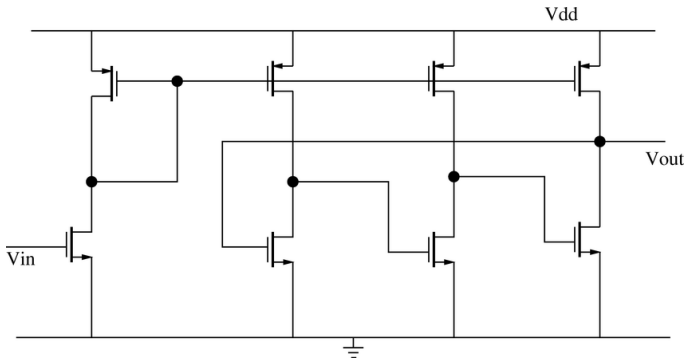
S. Gnecchi, C. Jackson, "A 1 16 SiPM Array for Automotive 3D Imaging LiDAR Systems" http://imagesensors.org/2017-papers/

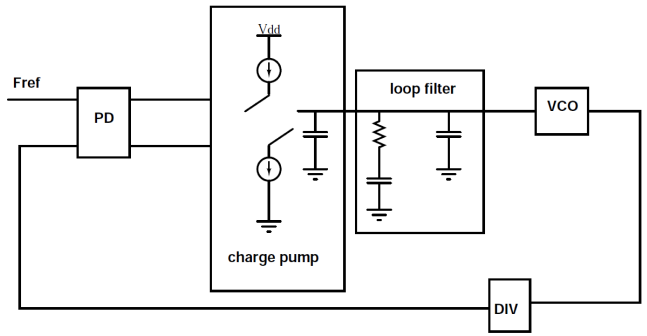
- Ring oscillators





- VCOs and (analogue) PLL

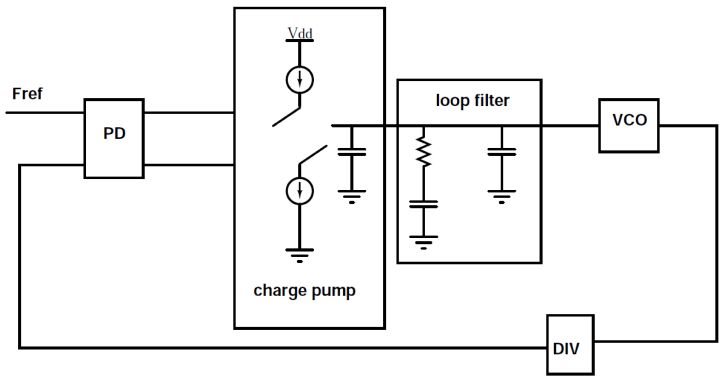




Application 8: Timing for everyone

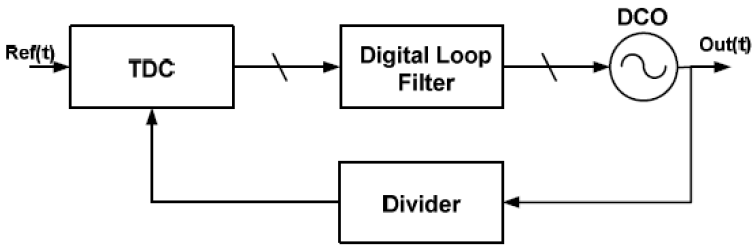
- A precise timing system is in (almost) every pocket...

Analog PLL



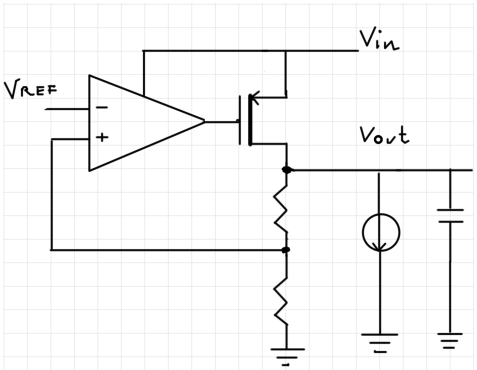
- Feedback signal generated by charge pump and filters
- VCO controlled by an analog voltage

All Digital PLL

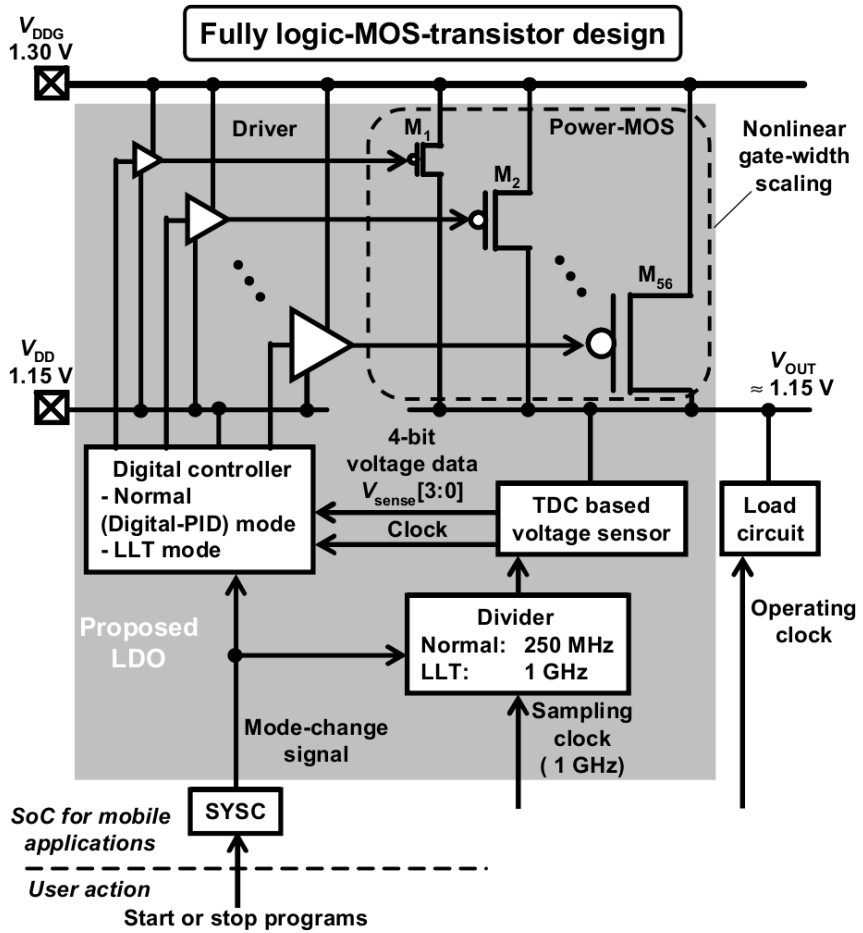


- Phase difference measured with a TDC
- VCO programmed by digital signals

Application n: Power supply control



- Low Dropout-Regulators (LDO)
- They usually use analog loops
- ...but the loop can also be digital
- A TDC measures a known time interval
- V_{out} reduced $\rightarrow$ less counts
- V_{out} increased $\rightarrow$ more counts
- The loop keeps counts constant counts



K. Otsuga et al,

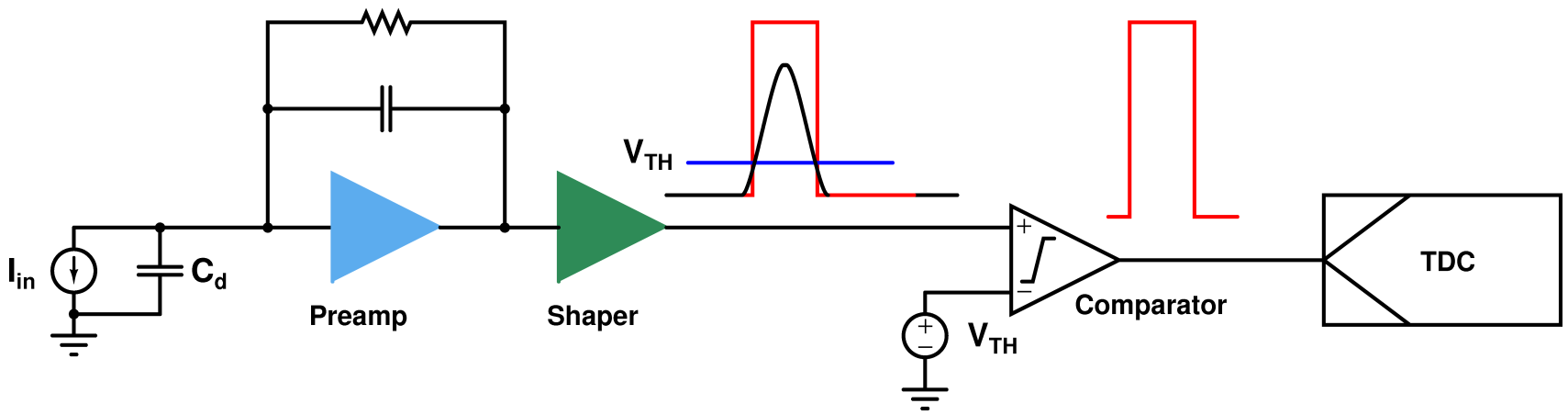
IEEE International SoC Conference, 2012

Trends in timing front-end electronics

- Time resolution of 100 ps or better already achieved in the sixties of last century
- Typical ToF systems have low channel density
- Electronics either discrete or based on front-end ASICs with few channels

- Improve time resolution well below 100 ps (target 10 ps)
- Extend timing to densely packed detector systems.
- Need of highly integrated ASICs for timing

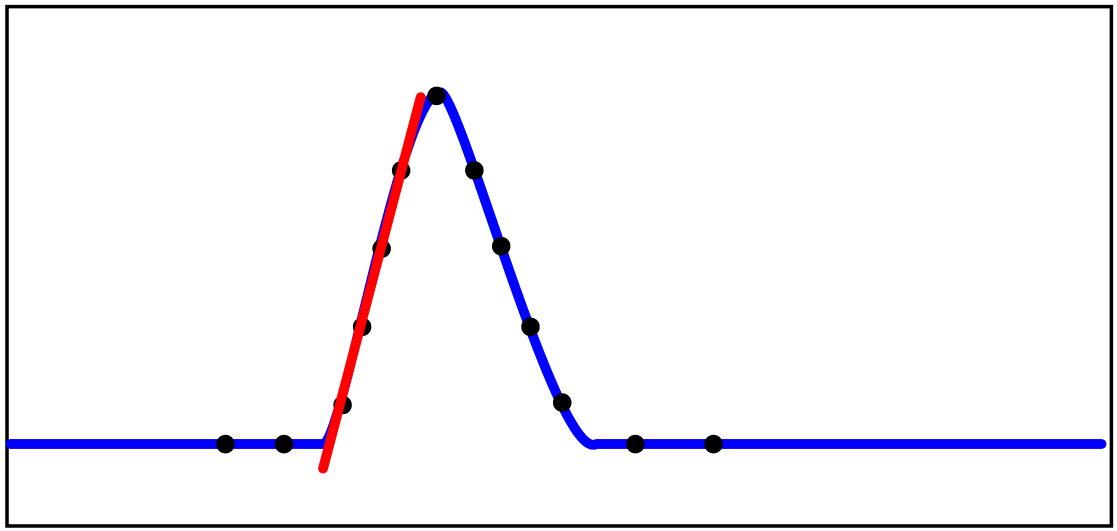
Timing systems: single sample



- The sensor signal is usually amplified and shaped
- A comparator generates a digital pulse
- The threshold crossing time is captured and digitized by a TDC
- TDC can be embedded on the front-end chip or external

- Timing is derived from a single sample

Timing systems: multiple samples



- The sensor signal is usually amplified and shaped
- The full waveform is sampled and digitized at high speed
- In many systems, sampling and digitization are decoupled
- Timing is extracted with DSP algorithms from the digitized waveform samples

- Timing is derived from multiple samples

Digital timing extraction

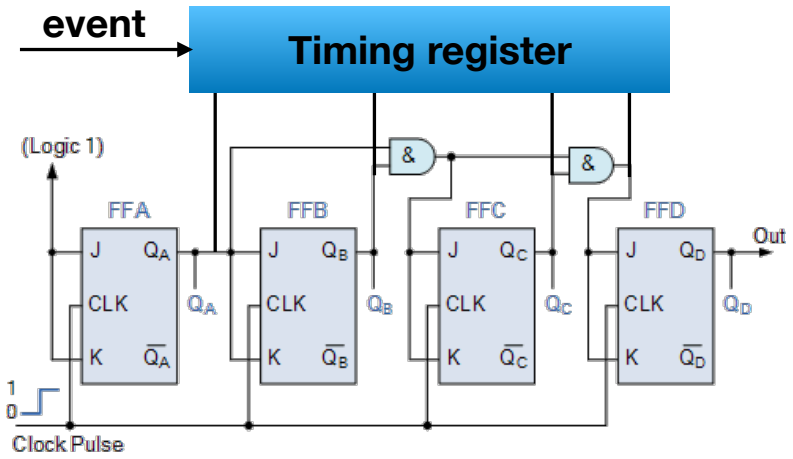
- Different algorithms are used to compute the timing from the digitized samples
- There is nothing such an optimal method
- Some techiques can be more suited that others for real time execution on FPGA

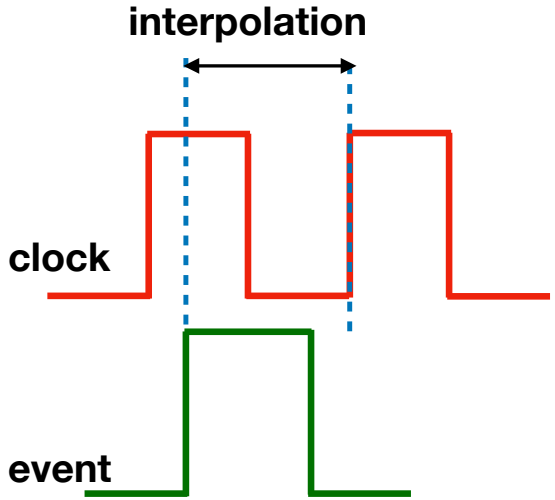
- Some examples of digital algorithm:
  - Digital leading edge
  - Digital constant fraction
  - Interpolation
  - Initial slope approximation
  - Reference pulse
  - ...

To learn more: E. Delagnes, Precise Pulse Timing based on Ultra-Fast Waveform Digitizers, Lecture given at the IEEE NSS Symposium, Valencia, 2011

Outline

TDC: the principle





- Count the transitions of a periodic signal (clock)

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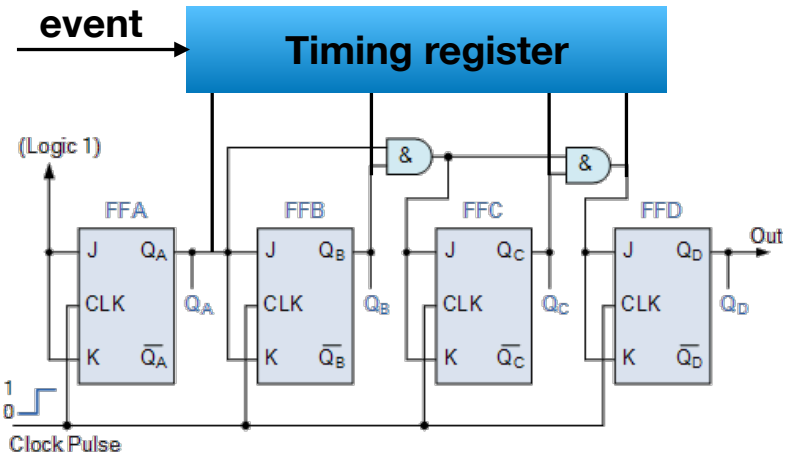

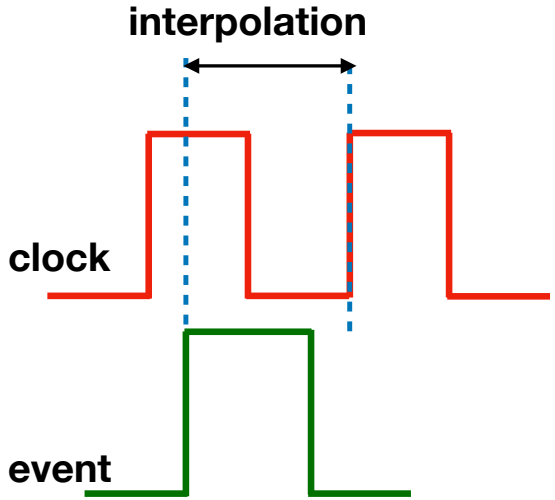

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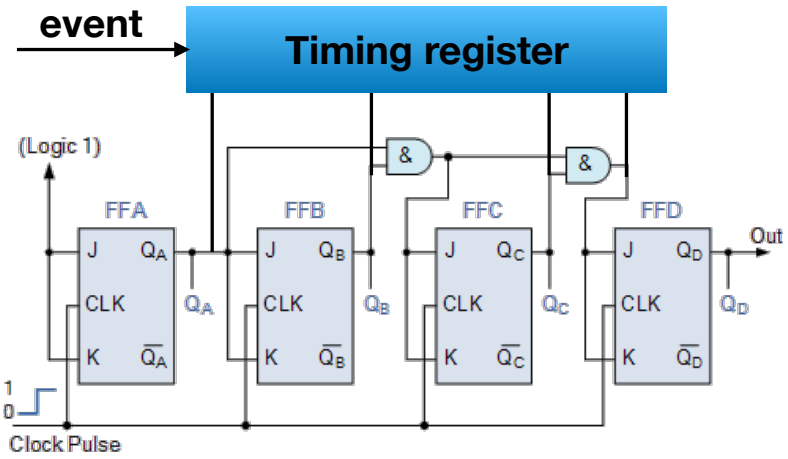

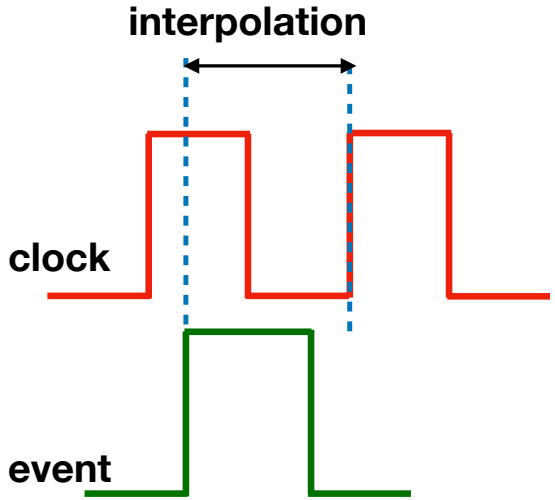

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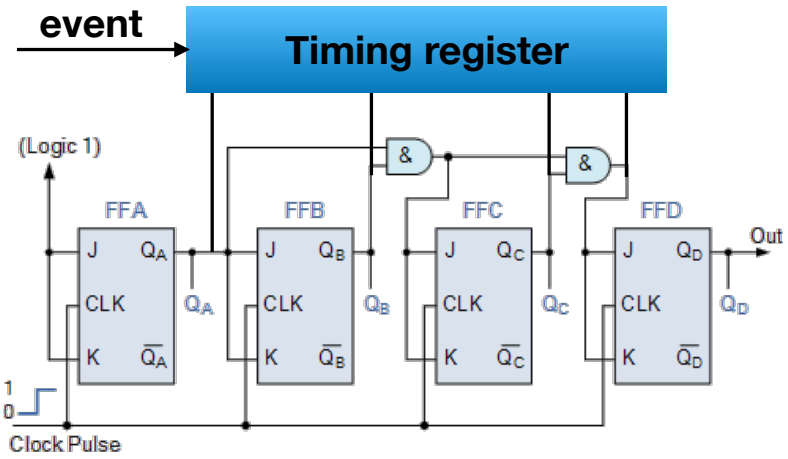

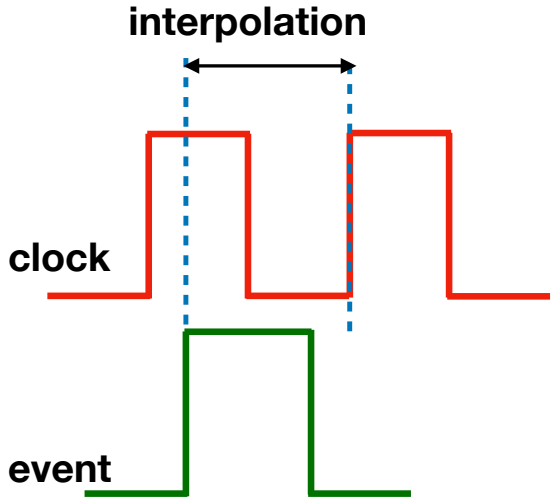

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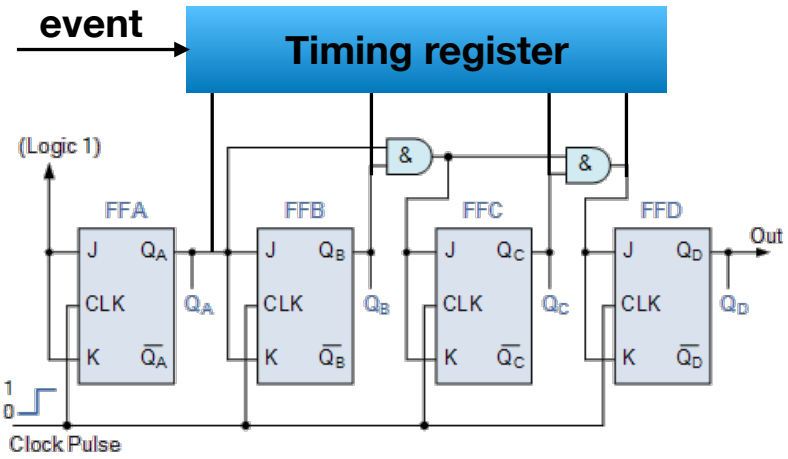

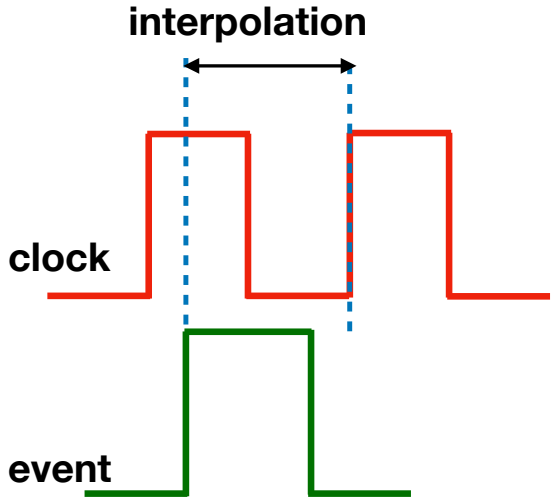

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- Interpolating= Measuring the time elapsing between the event and the next clock transition with an additional and dedicated circuit (interpolator)

What is a TDC

- **mixed-mode or fully-digital circuit**
  - input: trigger signals, typ CMOS
  - output is a **time stamp**: **N-bit** digital word corresponding to a time difference between two events
- Full scale range T_{ref}: maximum time difference that can be measured
- **Time Binning**: smallest time step (LSB): $T_{ref}/2^N$

Performance dictated by:

- Conversion Rate (samples/sec)
- Linearity - i.e. Proportionality of digital code to input time difference
- Quantization error: rms is $LSB/\sqrt{12}$
- Single-shot accuracy (precision in measuring an individual hit)
- Power

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  - **Digital delay line**
  - **Pulse shrinking**

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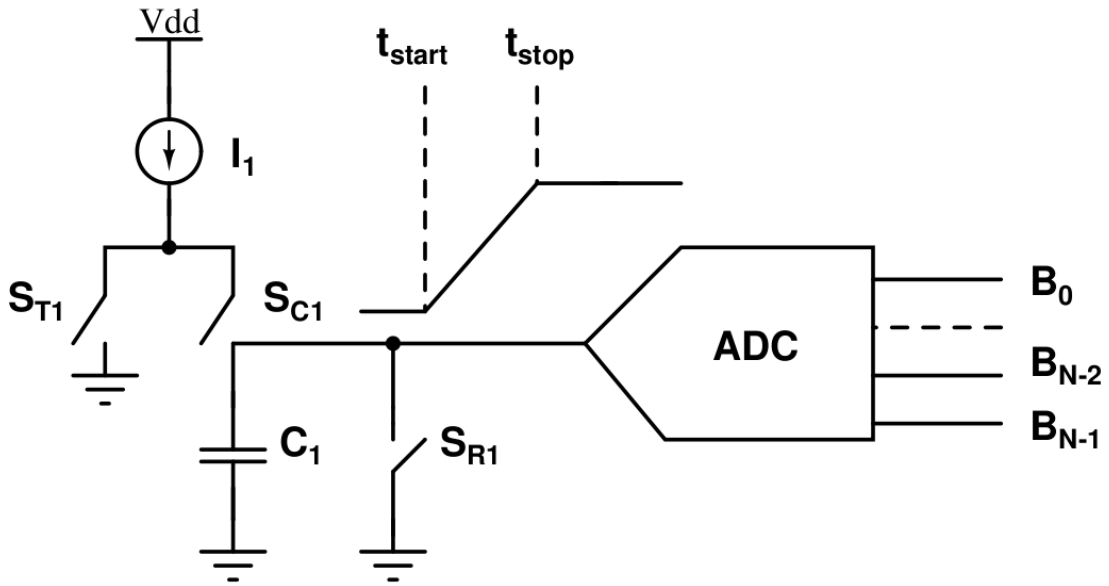
TDC with Analogue Interpolators



- Oldest method to measure time intervals: charge a capacitor with a constant current source and digitize the resulting voltage
  - $V_{out} = \frac{I1}{C1}(t_{start} - t_{stop})$

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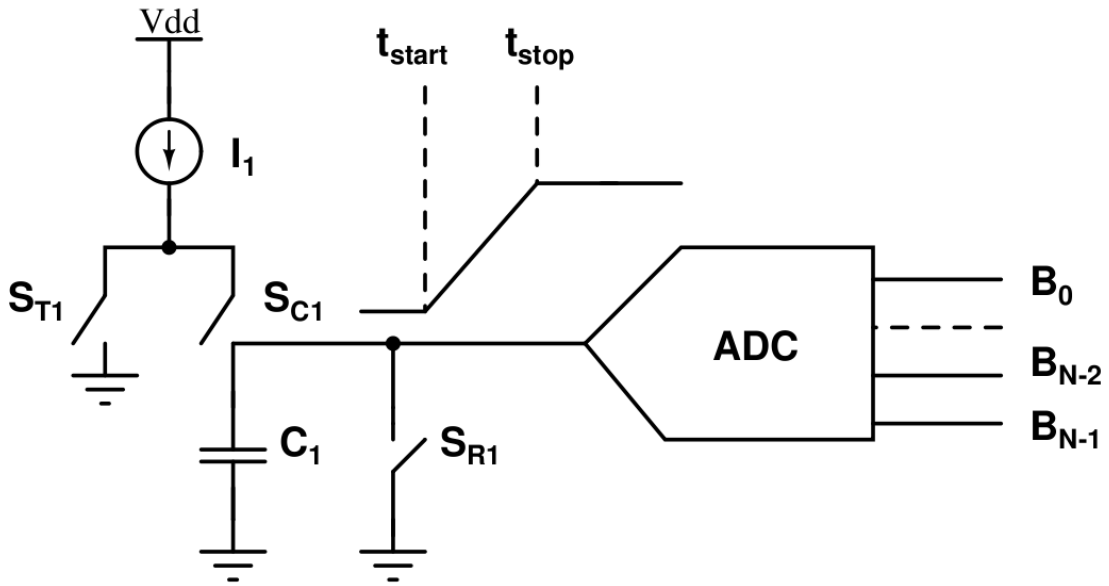

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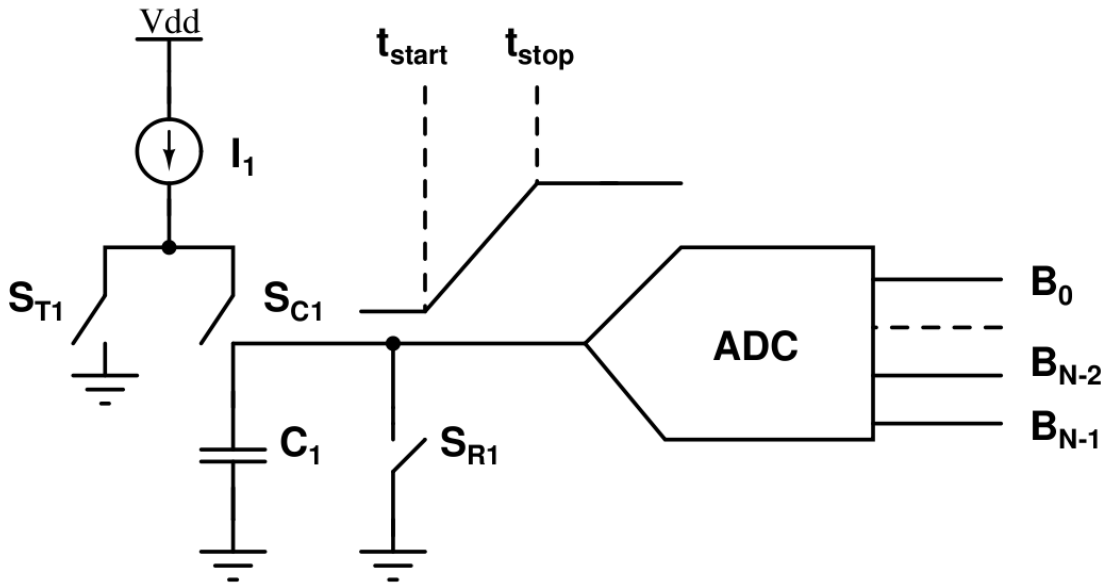

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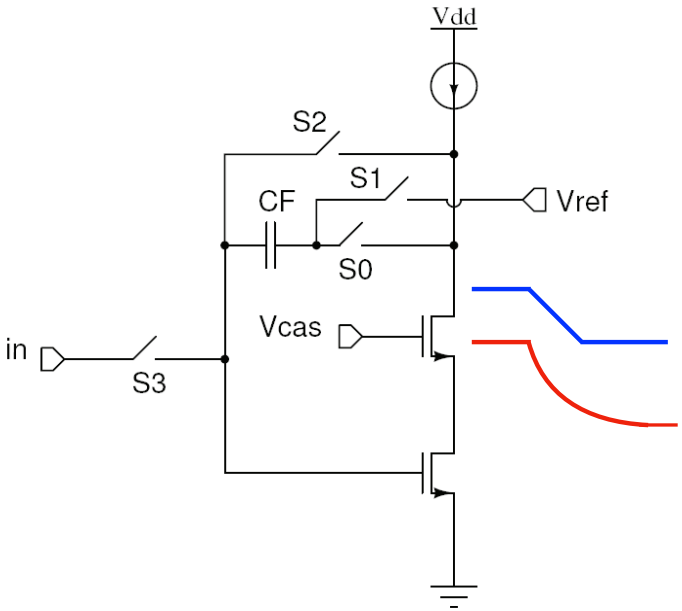
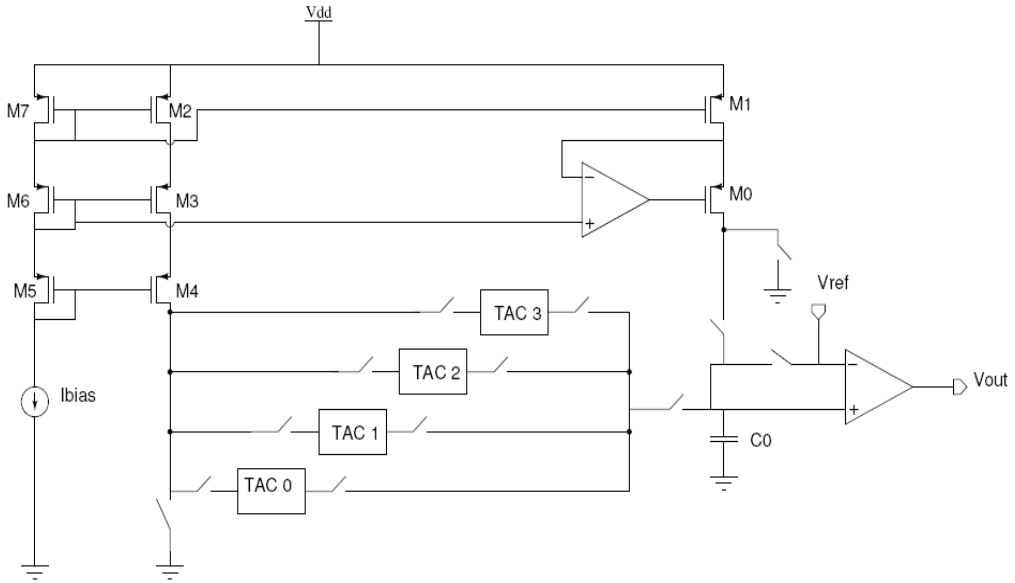
- If t_{stop} is the edge of a reference clock: becomes a Synchronous TDC
- ADC is frequently Wilkinson (determines the NBITs of the TDC)
  - little circuitry, simple to implement
  - low power, good linearity
  - Problem: conversion time!

Modern use of TACs-1





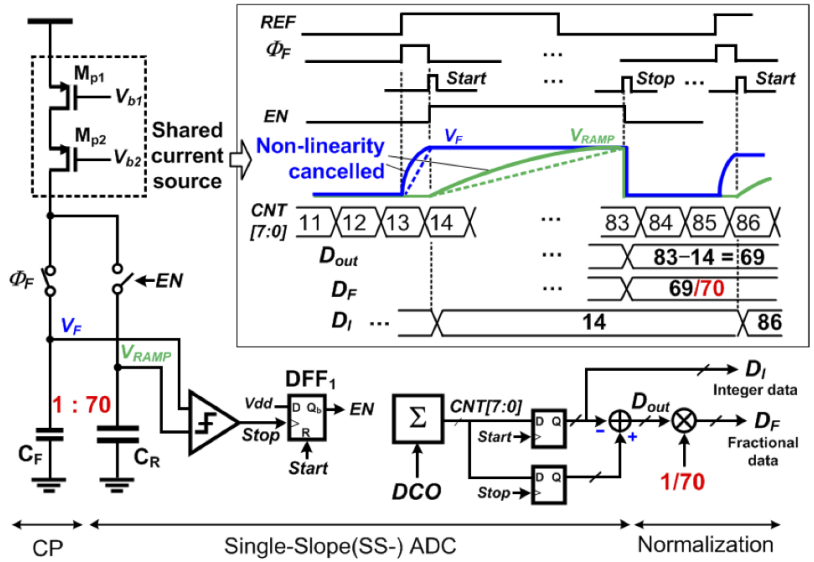
A. Rivetti et al, IEEE NSS-MIC Conference Records, 2009

ISSCC 2016 / SESSION 19 / DIGITAL PLLs / 19.7

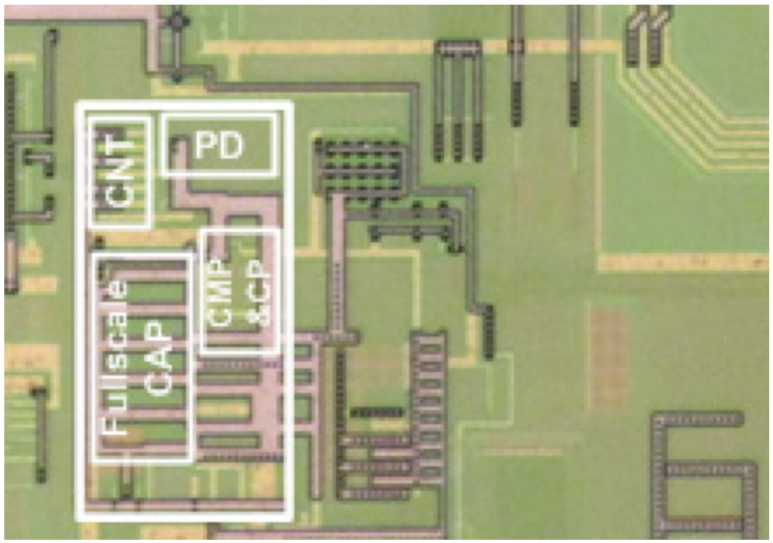
19.7 A 65nm CMOS ADPLL with 360μW 1.6ps-INL SS-ADC-Based Period-Detection-Free TDC

Akihide Sai, Satoshi Kondo, Tuan Thanh Ta, Hidenori Okuni, Masanori Furuta, Tetsuro Itakura

Toshiba, Kawasaki, Japan



		[3] ISSCC'10	[4] JSSC'15	[5] CICC'13	[6] ISSCC'15	This work
Architecture		VDL+DTC	TA+TDC	CP+SAR-ADC	Stochastic	CP+SS-ADC
Supply Voltage		1.2V	1.0V	1.0V	1.2V	1.2V
Technology		65 nm CMOS	65 nm CMOS	65 nm CMOS	14 nm FinFET	65 nm CMOS
Cal. Needed? (Time)		Yes (120ms)	Yes (38us)	Yes (-)	Yes (-)	No
Measurement Type		-	-	Static	Static	Dynamic
w/ ADPLL?		Yes	Yes	No	No	Yes
TDC	Sample Rate	35MS/s	50MS/s	40MS/s	100MS/s	40MS/s
	State Resolution	6.8ps 5.4bit	0.9ps 4bit	0.84ps 8bit	1.17ps 10bit	6.0ps 6.1bit
	Effective Resolution	-	-	-	-	8.9ps 5.5bit
	INL	-	1.25ps(sim)	2.3ps 2.7LSB	2.7ps 2.3LSB	1.6ps 0.27LSB
	Power	-	0.2mW (Except DTC)	2.7mW	0.78mW	0.36mW (Except CNT)
ADPLL	In-band Worst Frac. Spur	-52dBc @3kHz	-51.5dBc @392kHz	-	-	-52.6~-43dBc 2.4k~40MHz
	Ref. Spur	-	-69dBc	-	-	-66dBc
	In-band PN@2.24G	-105dBc/Hz	-112dBc/Hz	-	-	-106dBc/Hz



TDC with Digital Delay Lines

- Exploits the intrinsic delay of digital gates to measure time intervals

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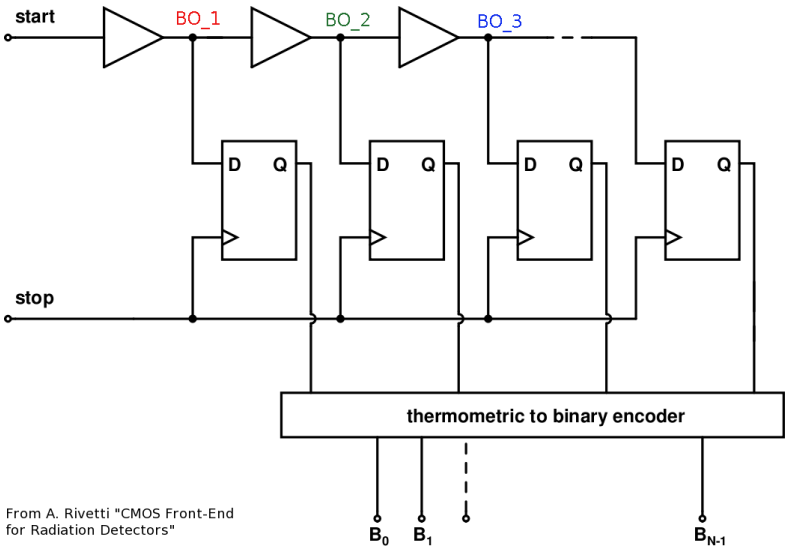
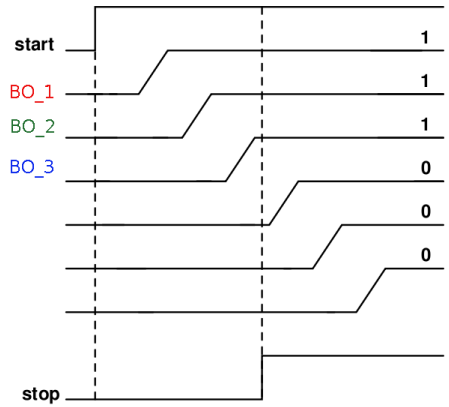


From A. Rivetti "CMOS Front-End for Radiation Detectors"



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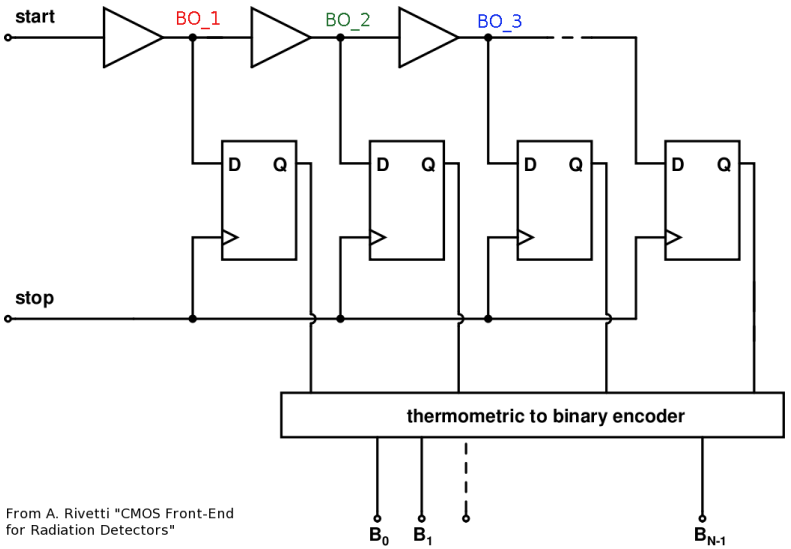

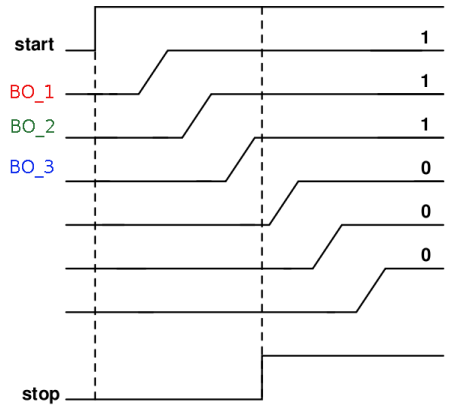

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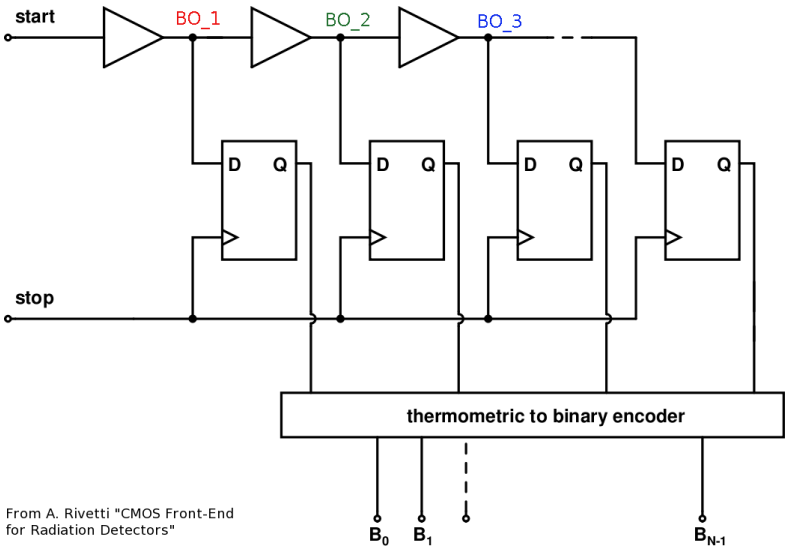

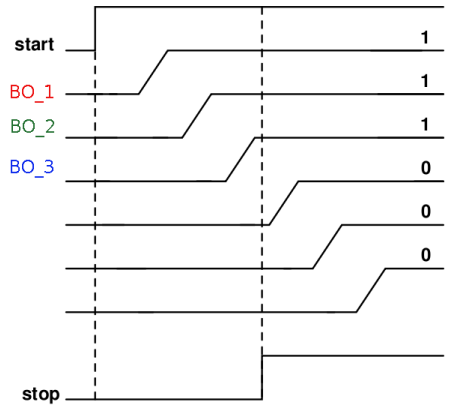

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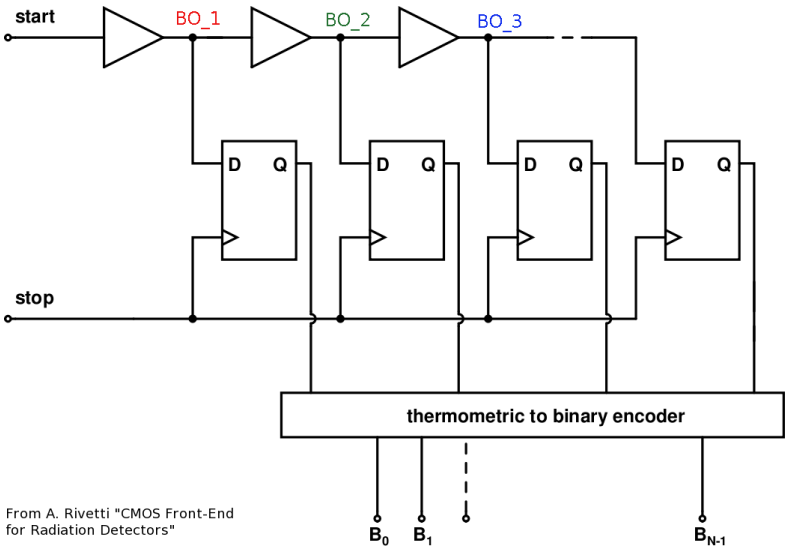

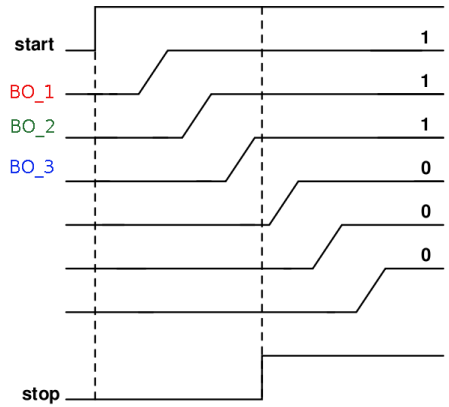

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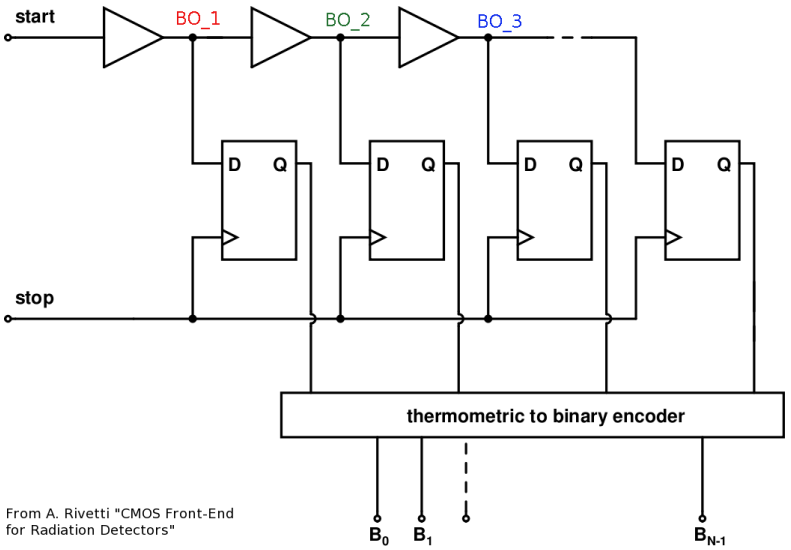

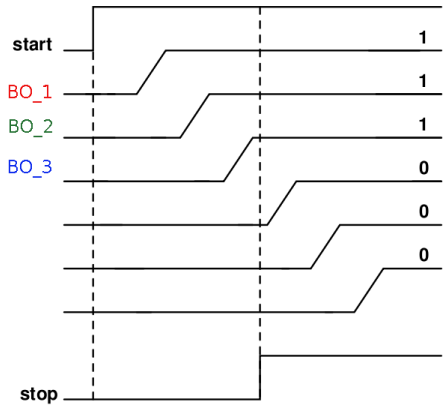

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- Maximum time interval measured: T
- Delay of single cell: $\tau 1$
- Required $N = \frac{T}{\tau 1}$ cells

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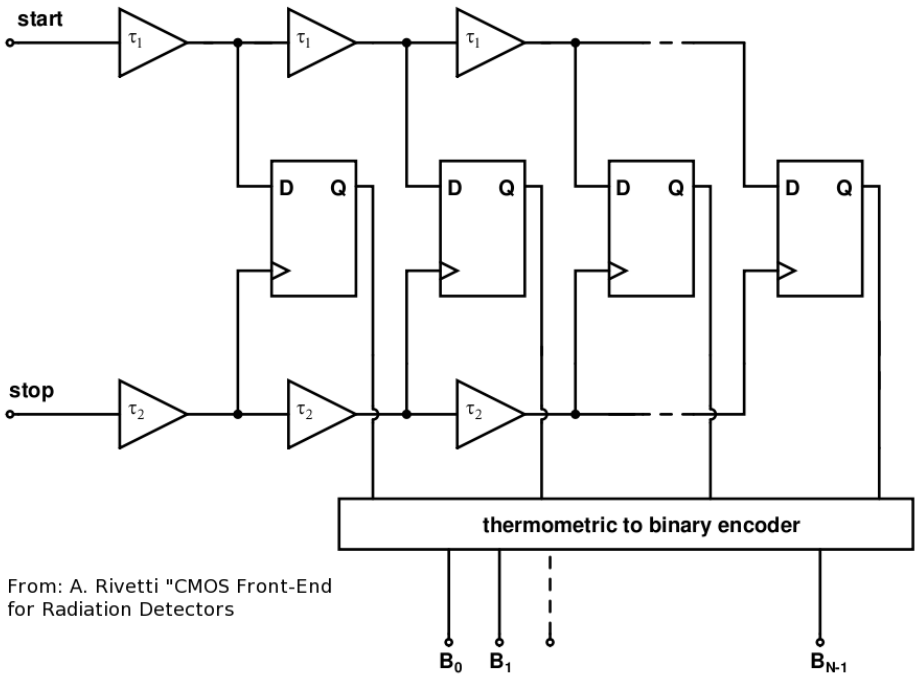

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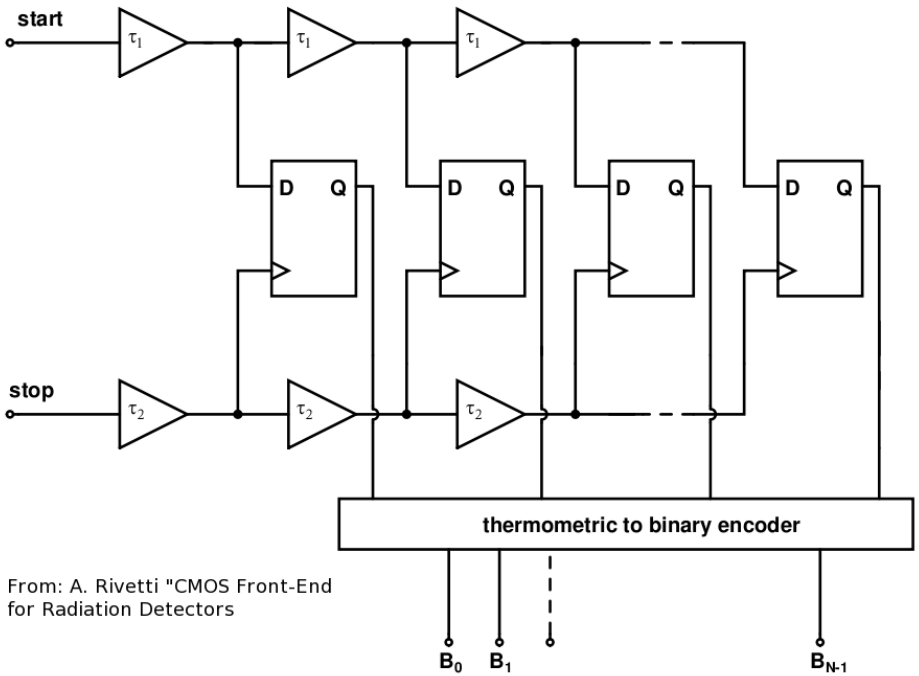

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- Start and Stop Signal propagate through delay lines with cell delay $\tau 1$ and $\tau 2$
- The LSB is given by $\tau 1 - \tau 2$
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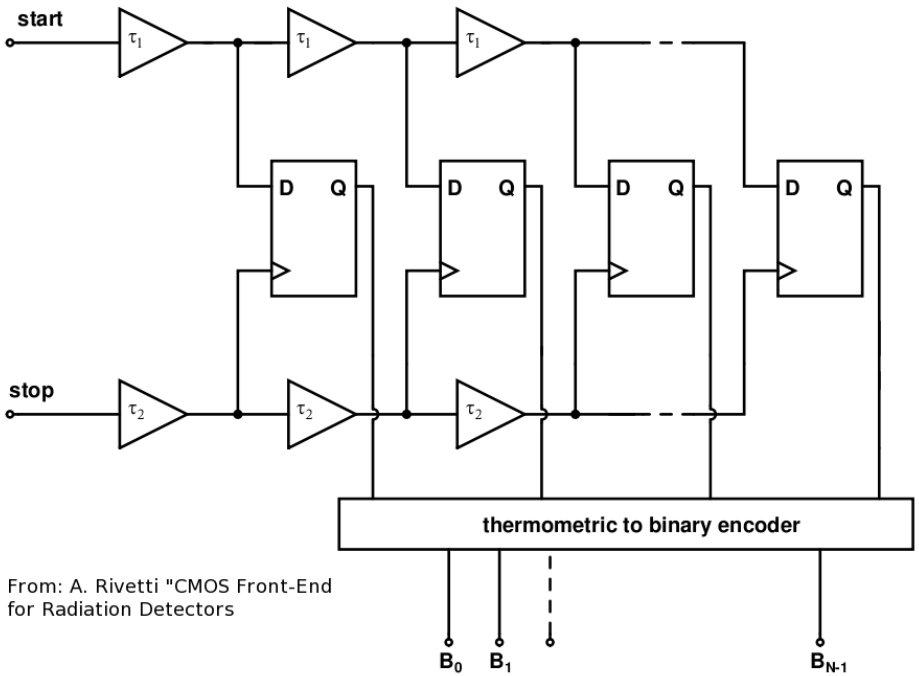

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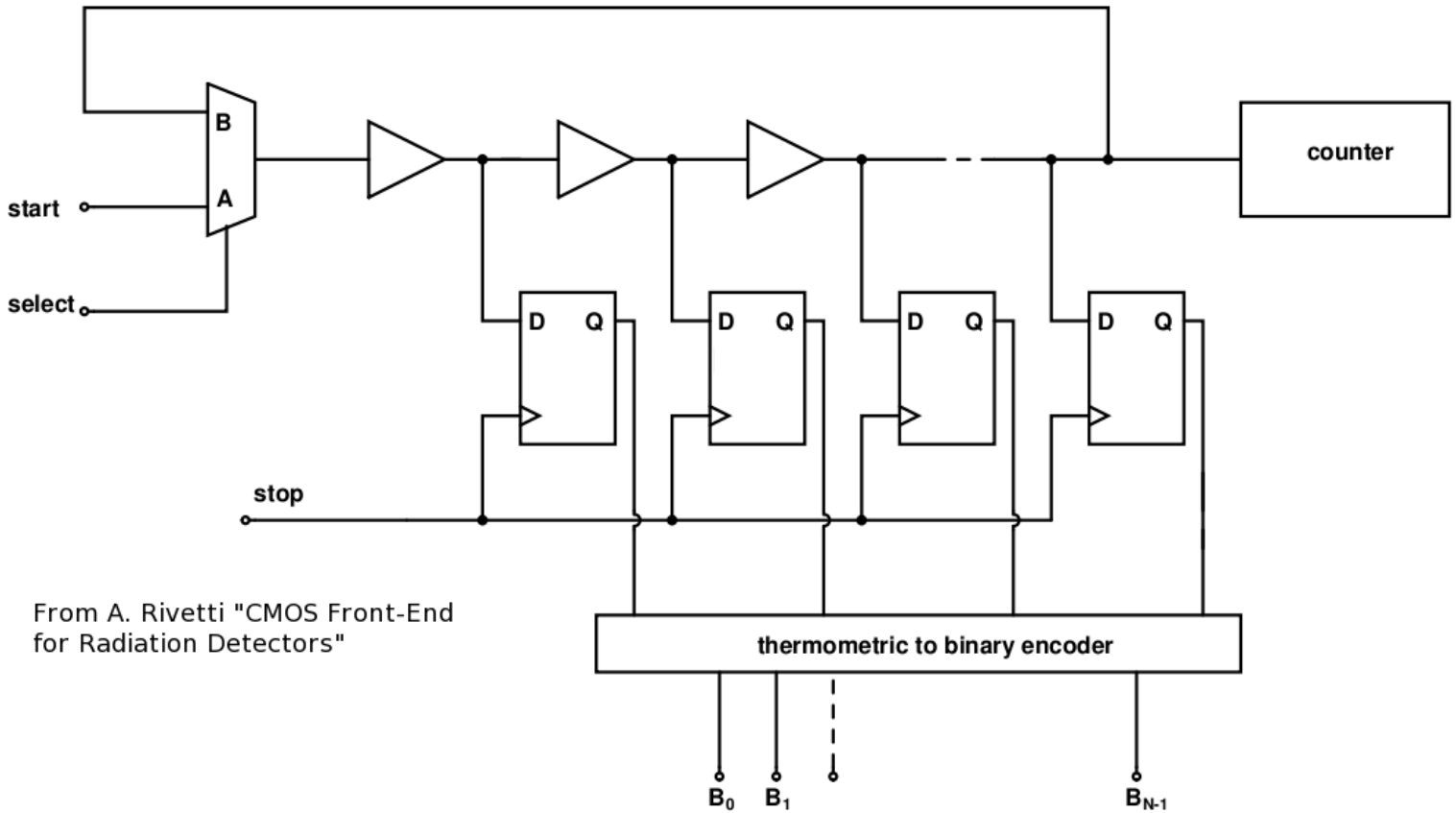
Large dynamic range are require many cells

$\hookrightarrow$ area becomes prohibitive!

Implementation example of a looped delay line:



- Re-use the same cells: pulse folded-back to the input of the delay line
- Count how many times the pulse edge has circulated:
  - ↪ Counter provides coarse time information

General aspects on digital TDCs

- The use of these techniques require good knowledge on the effects of process, voltage and temperature (PVT) variation

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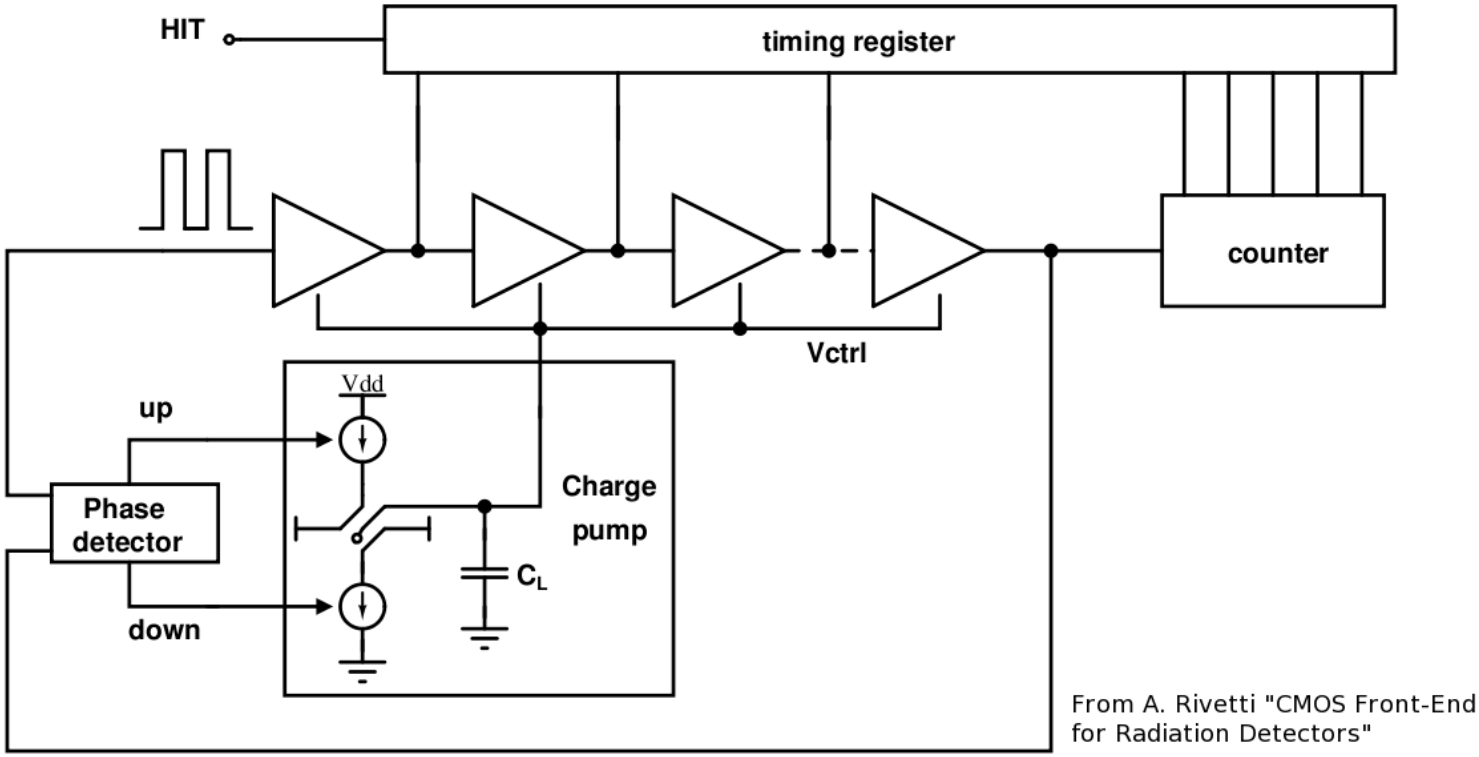
↪ **Good use of statistical simulation tools and proper layout is fundamental**

TDC Based on Delay-Locked-Loop



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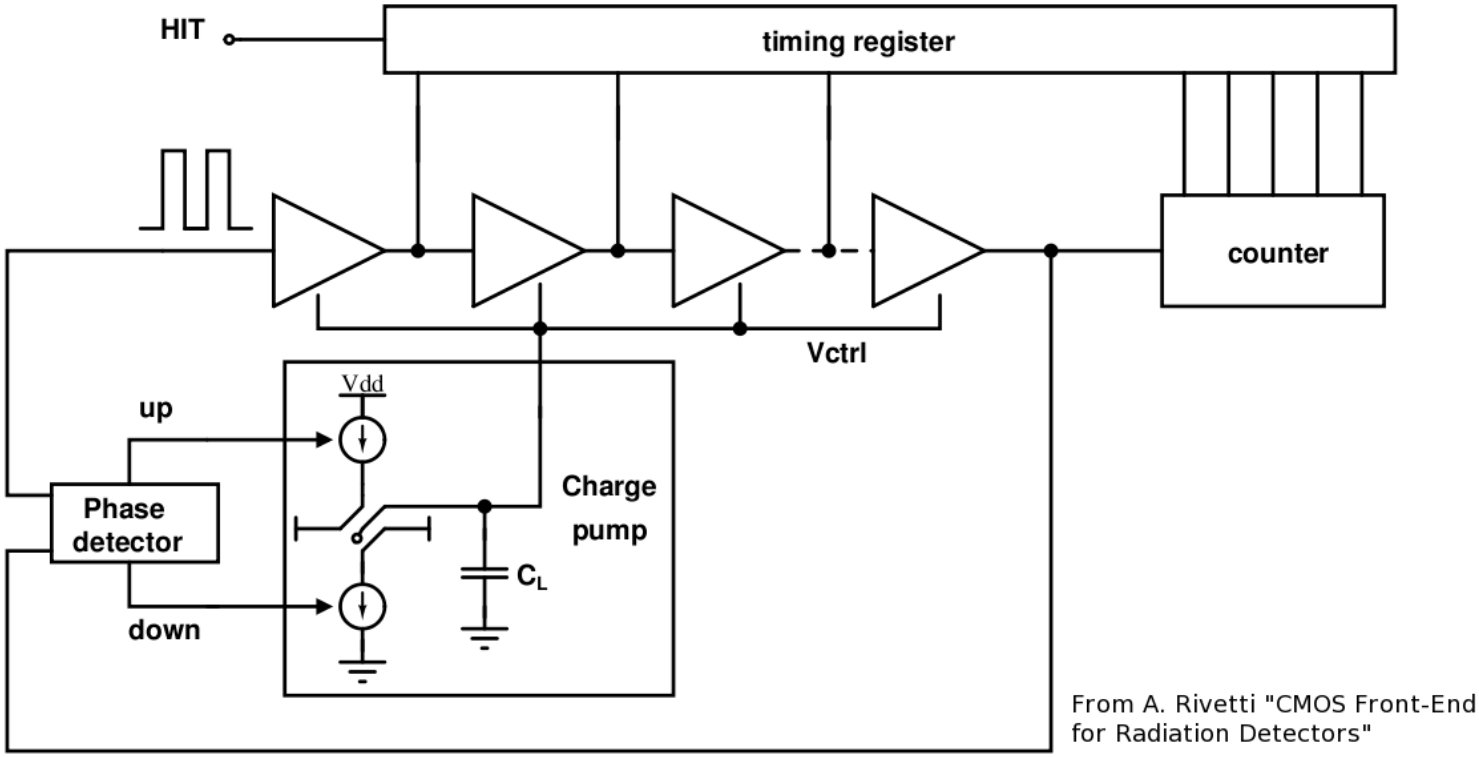

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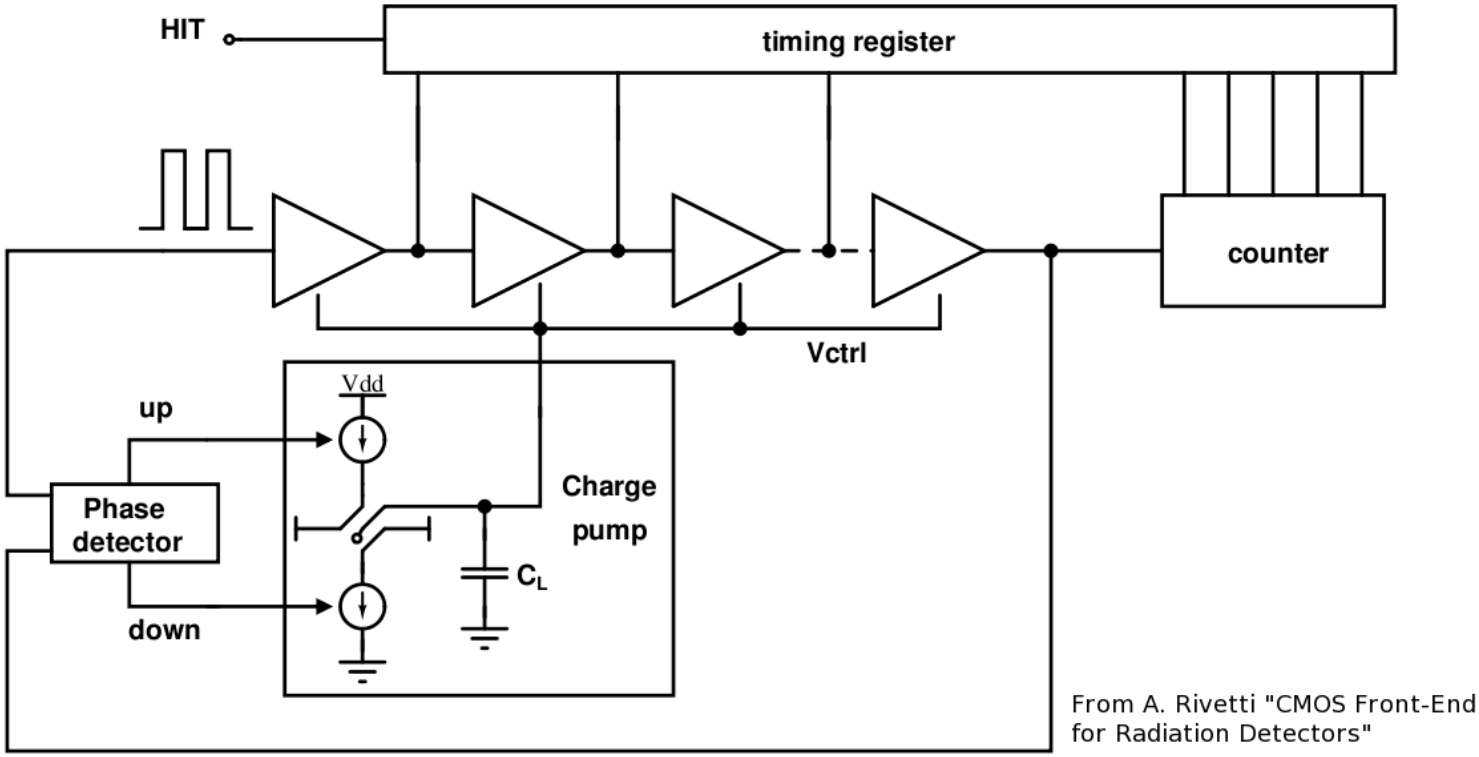

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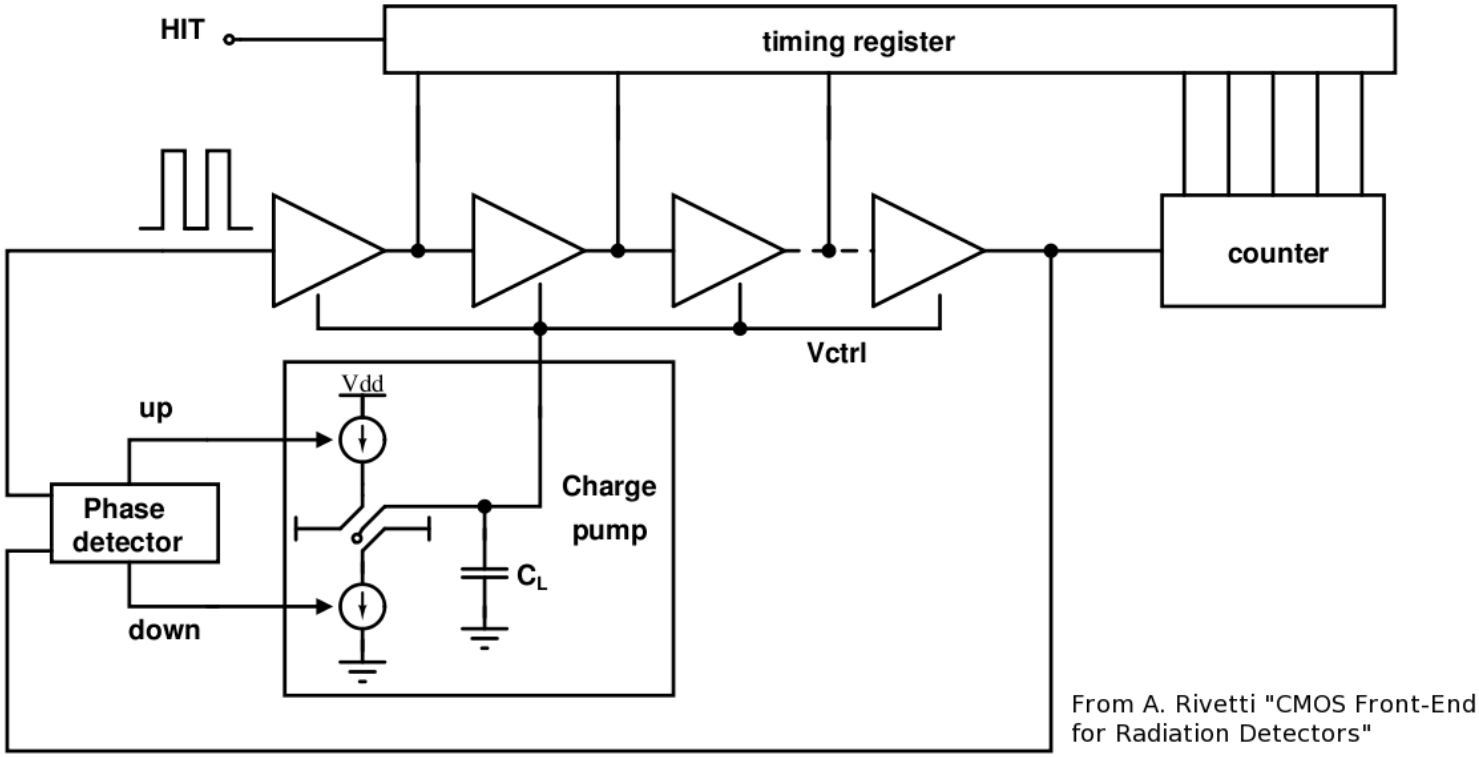

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- Output signal increments a counter and provides **coarse information**
- Status of DLL is latched to registers and allows **fine interpolation**

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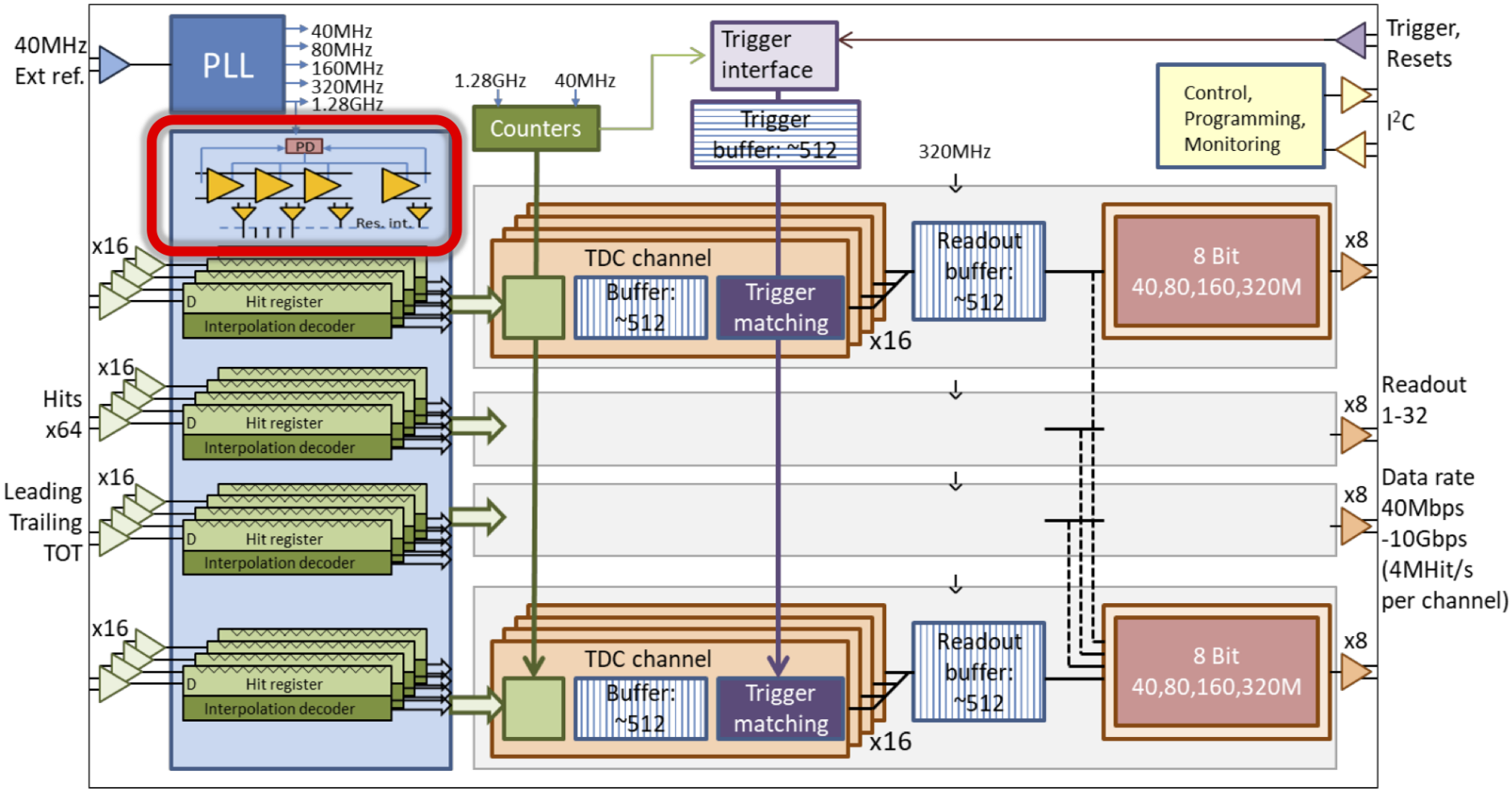
    ↪ $LSB = \frac{T_{clk}}{n\_cells} \Rightarrow$ **50 ps** with **640 MHz** and **32 delay cells**
- Tackle: share a global DLL among several channels - **robust buffer scheme to control skew**

DLL-based TDC: a practical example



- M. Horstmann (CERN): https://indico.cern.ch/event/688153/sessions/261017/#20180521

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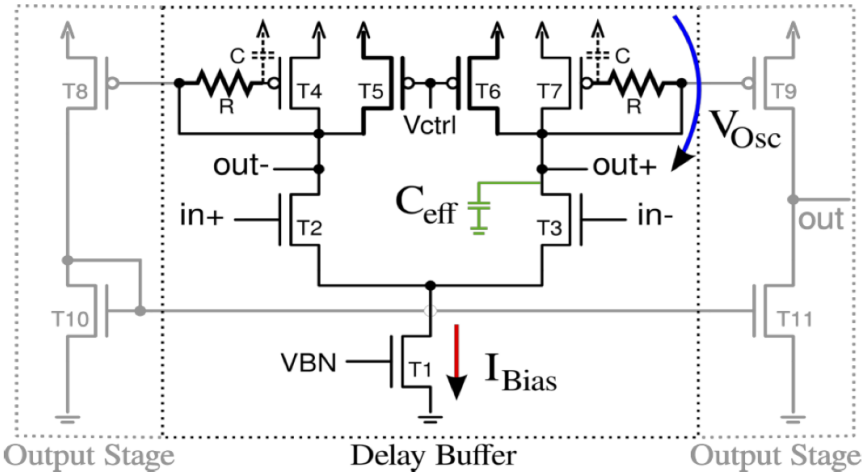
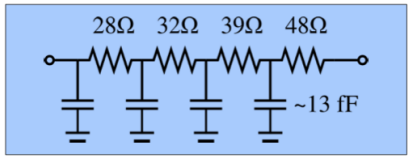
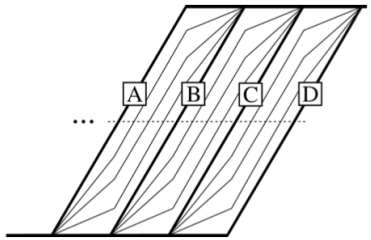
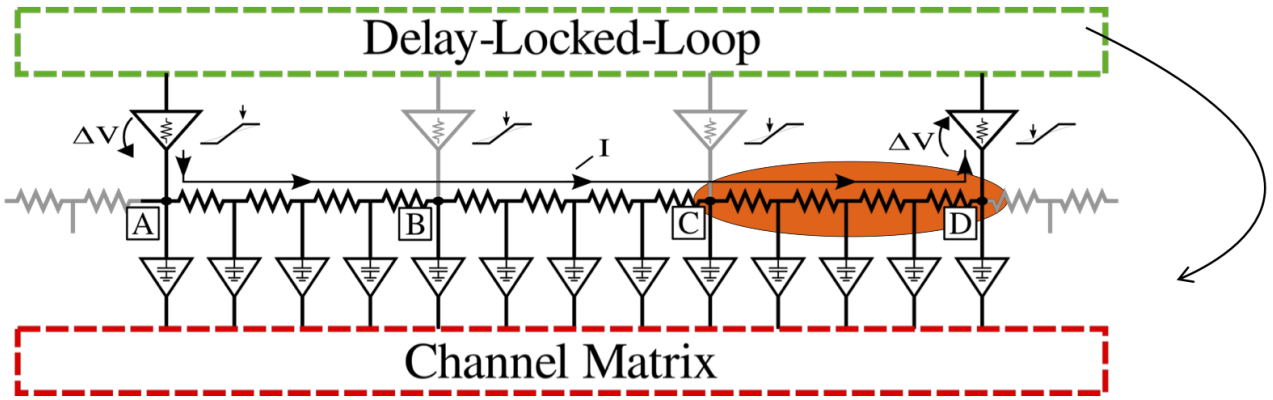
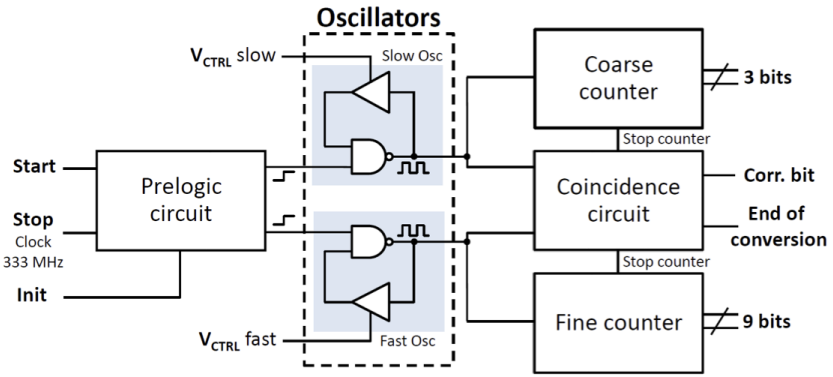


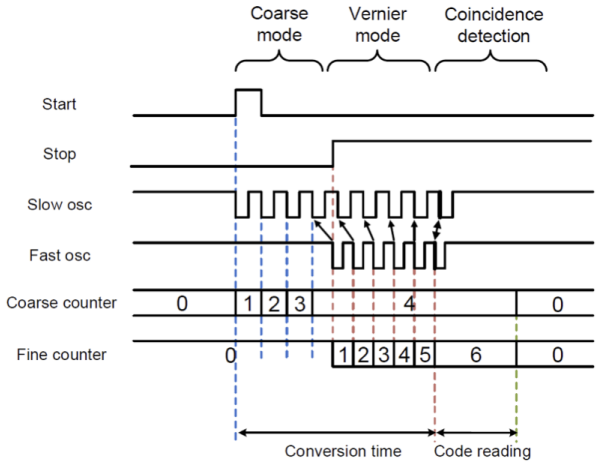


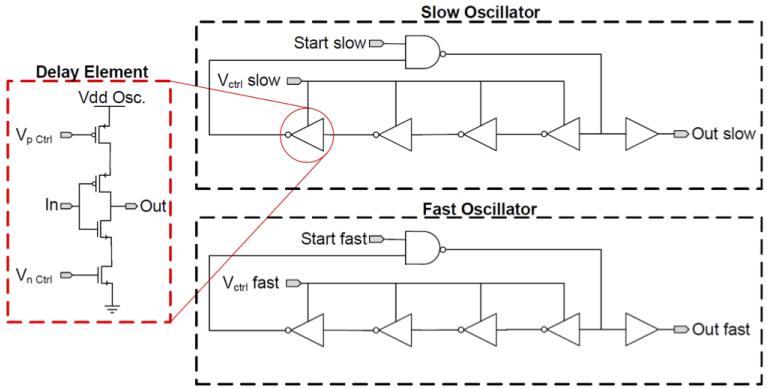


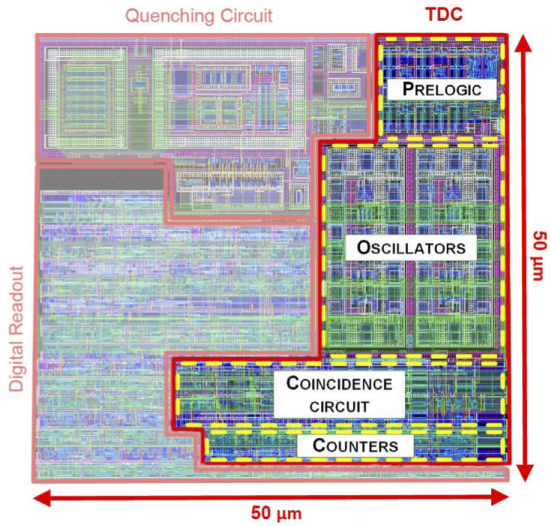


Ring Oscillator TDCs



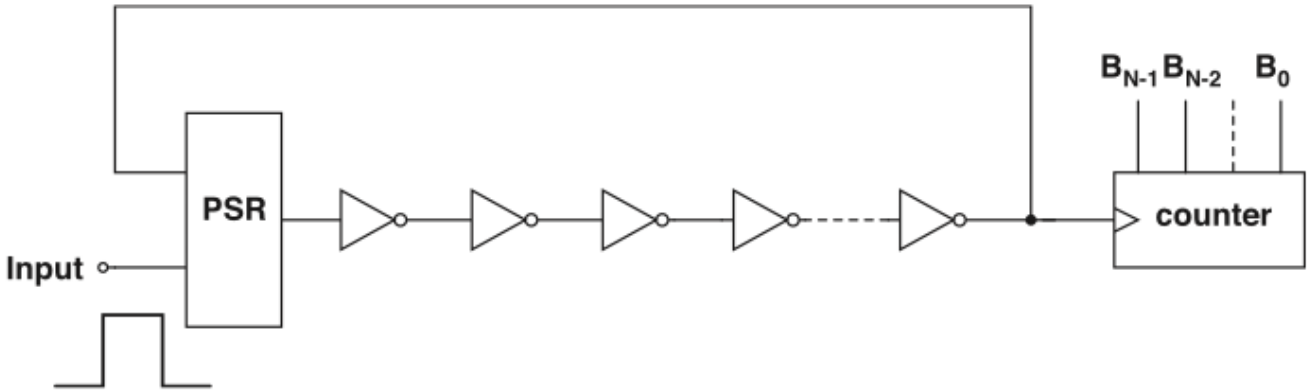


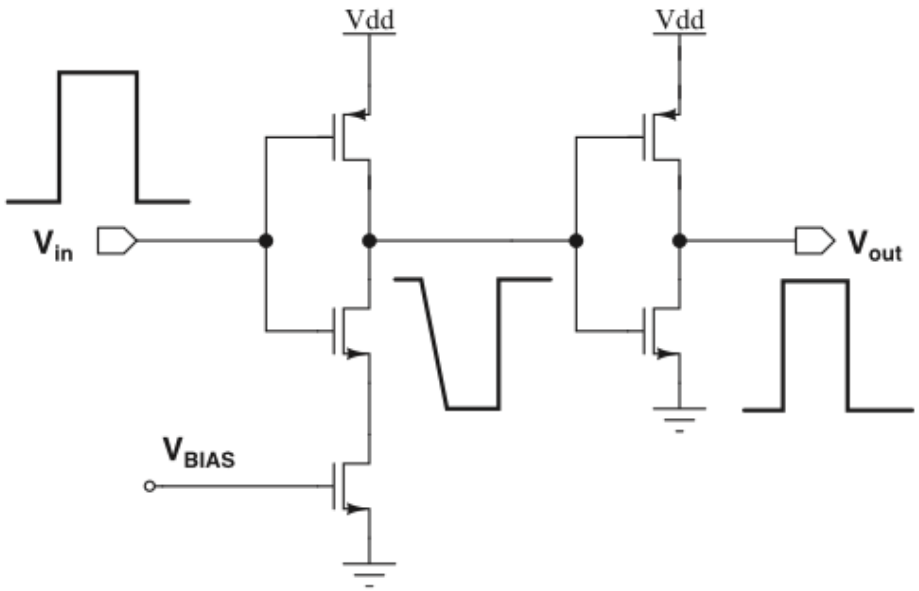




- N. Roy (Sherbrooke): https://indico.cern.ch/event/688153/sessions/261017/#20180521

Pulse Shrinking TDCs





A 14-Bit, 1-ps Resolution, Two-Step Ring and 2D Vernier TDC in 130nm CMOS Technology

Hechen Wang and Fa Foster Dai
Dept. of Electrical and Computer Eng., Auburn University, Auburn, AL 36849

TABLE I. TDCs PERFORMANCE COMPARISON

	VLSI 14 [7]	ISSCC 15 [8]	ISSCC 16 [9]	CICC 17 [2]	ISSCC 17 [1]	**This work**
Topology	Cyclic	Stochastic	SS-ADC	2D Vernier	SAR-ADC	**Ring+2D Vernier**
Process	28nm	14nm	65nm	45nm	14nm	**130nm**
NoB	12	10	6.1	8	7	**14**
ENoB (1)	9.74	8.28	5.76	7.58	3.68	**13.2**
Resolution	0.63ps	1.17ps	6ps	1.25ps	0.2ps	**1.0ps**
ER (2)	3.15ps	3.85ps	7.60ps	1.67ps	2ps (4)	**1.74ps**
Speed [MHz]	10	100	40	80	26	**10**
DNL [LSB]/[ps]	0.5/0.32	0.8/0.94	---/---	0.25/0.31	---/---	**0.41/0.41**
INL [LSB]/[ps]	3.8/2.39	2.3/2.7	0.27/1.6	0.34/0.4	9/1.8	**0.79/0.79**
Power [mW]	0.82	0.78	0.36	0.33	---	**2.4**
FoM (3)	0.02	0.01	0.13	0.02	---	**0.02**

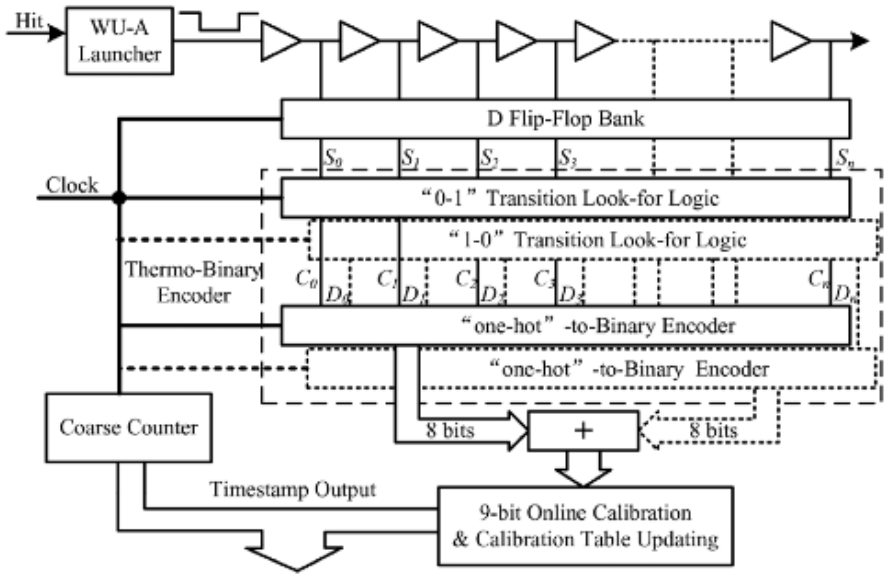
1. ENoB = NoB – $\log_2$ (INL+1).
2. Effective Resolution (ER) = Resolution × $2^{(NOB - ENOB)}$.
3. FoM = Power / ($2^{NOB} \times F_S$) [pJ / conv-step].
4. calculated based on in-band phase noise. PN = $10\log(N^2(2\pi f_r)^2 t_{res}^2/12/f_r)$.

High resolution TDCs: FPGA

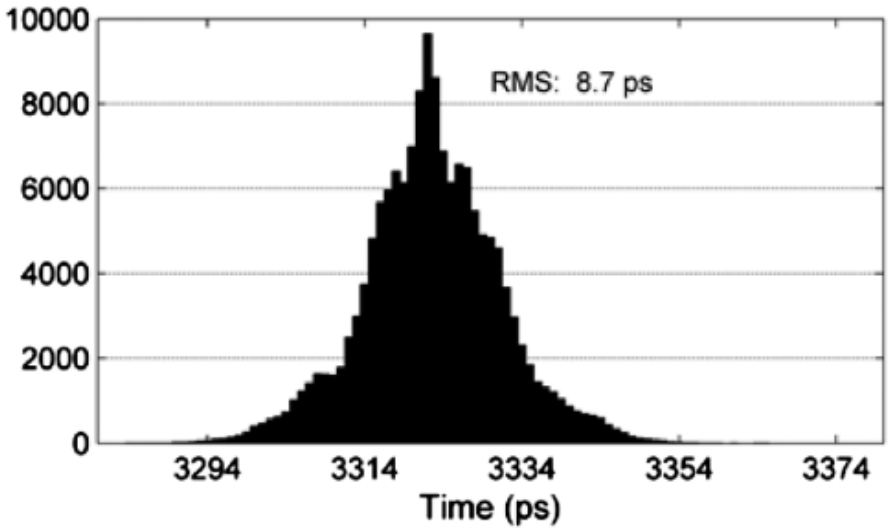
IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 62, NO. 3, JUNE 2015 773

A 128-Channel, 710 M Samples/Second, and Less Than 10 ps RMS Resolution Time-to-Digital Converter Implemented in a Kintex-7 FPGA

Chong Liu and Yonggang Wang



(a)



(c)

Outline

Timing: the (very front-end) issues

- Several factors challenge the timing accuracy of a system:
  - Random noise internal to the front-end electronics (can be traded with power)
  - Random noise from external sources (e.g. clock distribution system)
  - Signal integrity (substrate noise, PSSR, etc..)
  - Pulse amplitude variations
  - Pulse shape variations

- Timing below 100 ps rms is not trivial
- Research is now geared towards sub 10 ps system resolution

Timing jitter: single sample

$$\sigma_t = \frac{\sigma_v}{\frac{dV}{dt}} \qquad \frac{dV}{dt} \approx \frac{V}{t_r} \rightarrow \sigma_t = \frac{t_r}{SNR}$$

Checks:

$t_r = 1$ ns, $SNR = 10 \rightarrow \sigma_t = 100$ ps

$t_r = 40$ ns, $SNR = 500 \rightarrow \sigma_t = 80$ ps

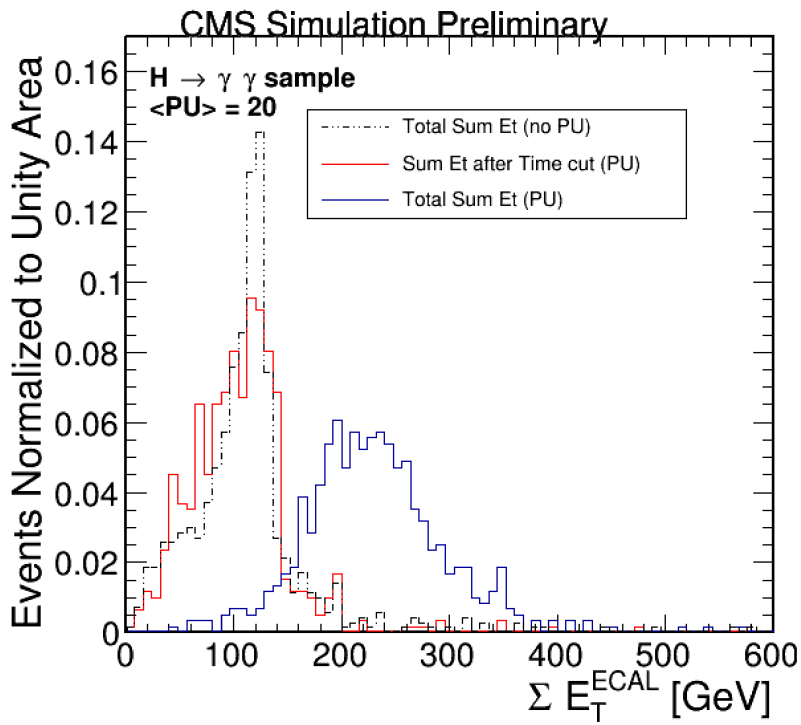
$$t_r \propto \frac{1}{BW} \qquad SNR \propto \frac{1}{\sqrt{BW}} \rightarrow \boxed{\sigma_t \propto \frac{1}{\sqrt{BW}}}$$

- Match the front-end rise time with the sensor rise/collection time

Timing with large SNR

- Calorimeters can profit from large signals to make timing is easier!

- Calorimeters already achieve quite good time resolution
- System resolution now saturates at around 100 ps
- Exact values depends on the situation considered
- Interaction region $\approx$ 6 cm
- With 30 ps resolution event origin confined to 1 cm.
- Need a 4-5x improvement with respect to today standard



From D. Del Re, J. of Physics: Conference Series 587 (2015), doi:10.1088/1742-6596/587/1/012003

Timing jitter: multiple sampling

- Sample the input signal beyond Nyquist
- Assume first-order system relationship

$$\sigma_t = \frac{t_r}{SNR}\frac{1}{\sqrt{N}} \qquad N = \frac{t_r}{t_s}$$

$$\sigma_t = \frac{1}{SNR}\sqrt{\frac{0.35}{BW \cdot f_s}} = \frac{1}{SNR}\frac{1}{\sqrt{3 f_{-3dB} f_s}}$$

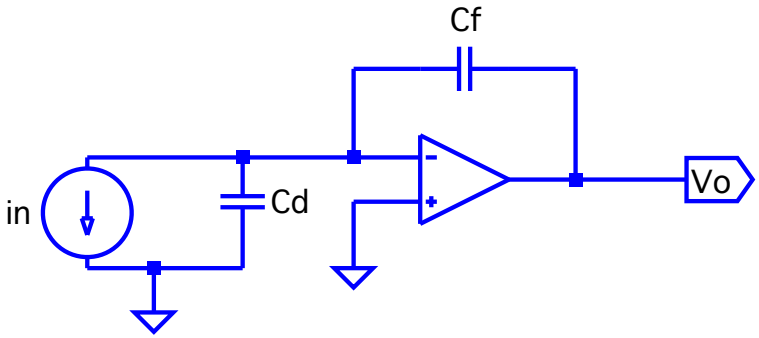
SNR	f_s	f_{-3db}	σ_t
10	1 Gs/s	150 MHz	150 ps
10	10 Gs/s	1.5 GHz	15 ps
100	1 Gs/s	150 MHz	15 ps
1000	10 Gs/s	1.5 GHz	0.15 ps

- Redundancy is advantageous only if noise in uncorrelated

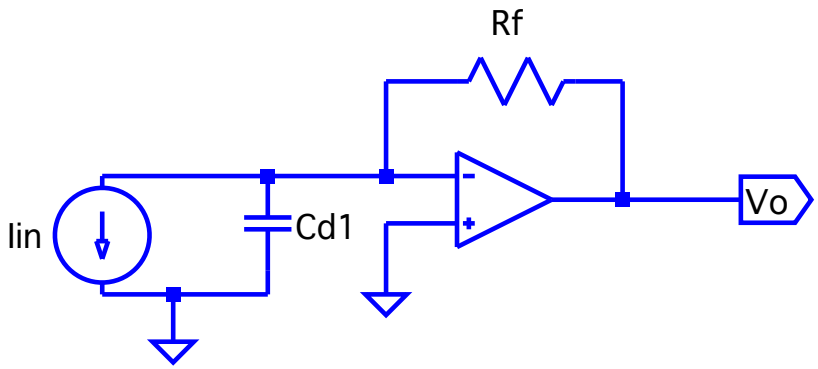
- Unfortunately, jitter is not the full story...

Outline

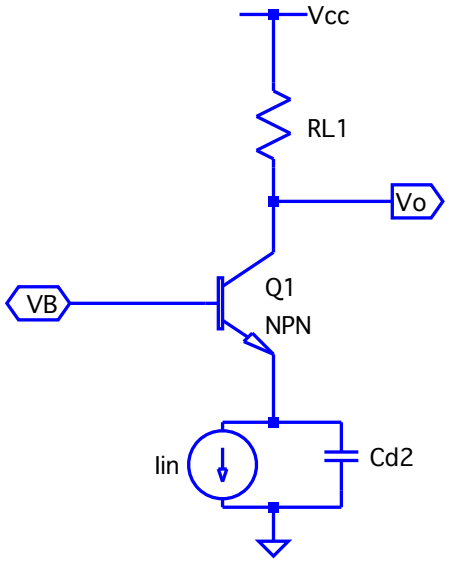
Input stage topologies



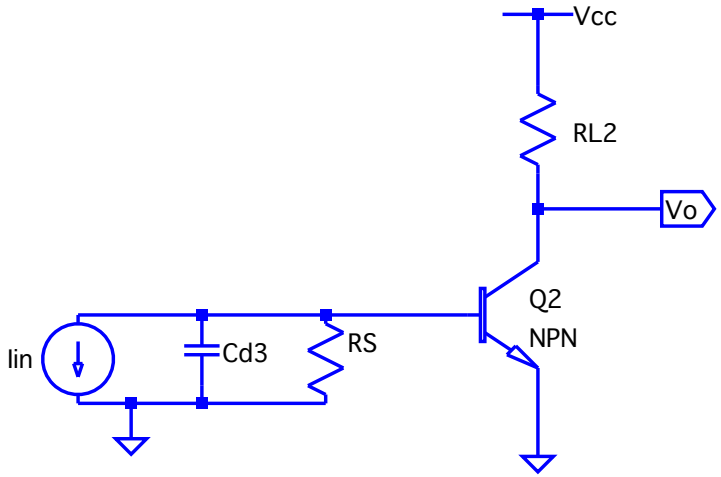
Charge sensitive



Transimpedance



Common base (gate)



Voltage amplifier

A simple example

- Take a simple voltage amplifier
- Step at the input is Q_{in}/C_d
- Assume single pole response with time constant $\tau = RC$
- Amplifier rise time is: $t_a = 2.2\tau$
- Amplifier cut-off frequency is $f_T = \frac{1}{2\pi\tau}$
- Total rise time at the output is $\sqrt{t_d^2 + t_a^2}$
- Output voltage squared is $v_n^2 \frac{\pi}{2} f_T$
- Now put everything together...

$$\sigma_t = \frac{\sigma_n}{\frac{dV}{dt}} \approx \frac{v_n}{\sqrt{2t_a}} \frac{C_d}{Q_{in}} \sqrt{t_a^2 + t_d^2} = \frac{v_n C_d}{Q_{in}} \sqrt{t_d}$$

See also C. de la Taille lecture

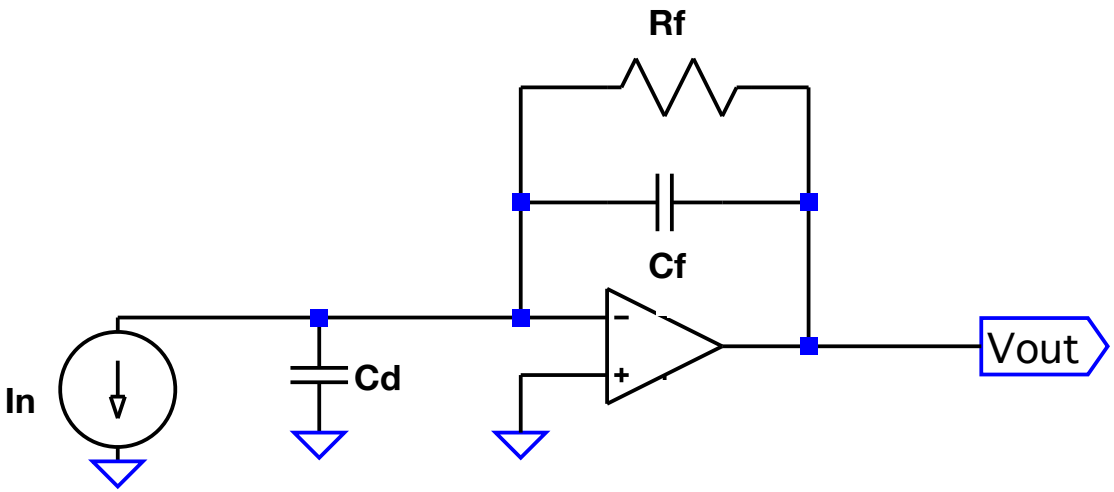
Reality check

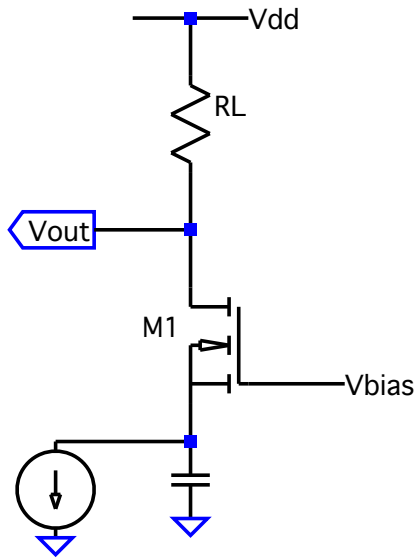
- Consider the following parameters: $t_d = 1$ ns, $C_d = 300$ pF, $Q_{in} = 1 \cdot 10^6$ e$^-$
- If we want $\sigma_t = 10$ ps, we need $v_n \approx 1.7 \cdot 10^{-10}\ V/\sqrt{Hz}$
- Assume MOS input transistor in weak inversion: $v_n = \sqrt{\frac{2\alpha kT}{g_m}}$
- Combining all parameters (take $\alpha = 1$), we get $g_m = 0.291$ S
- The transconductance in w.i. is $g_m = \frac{I_{DS}}{n\phi_T}$ $(n \approx 1.3, \phi_T = kT/q = 26mV)$
- The bias current needed in the input transistor is ≈ 10 mA

Most common input stages

TIA or CSA topology

- $f_{in} < 1/2\pi R_f C_f \rightarrow$ TIA
- $f_{in} > 1/2\pi R_f C_f \rightarrow$ CSA



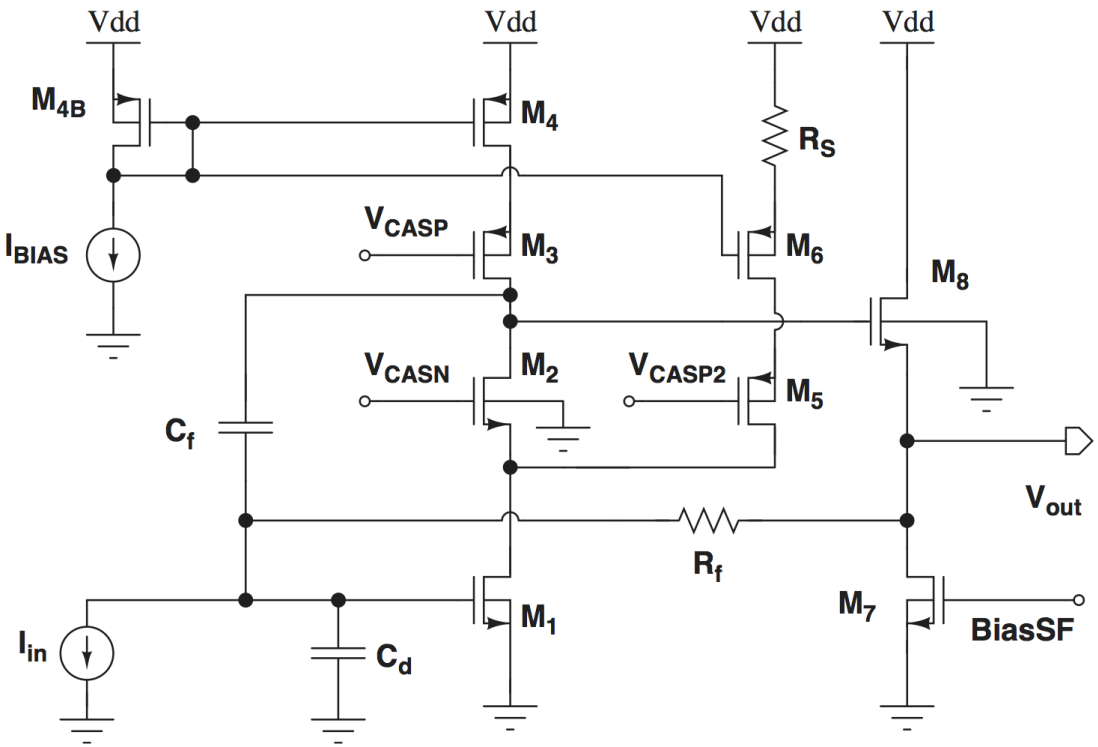


Rise time calculation

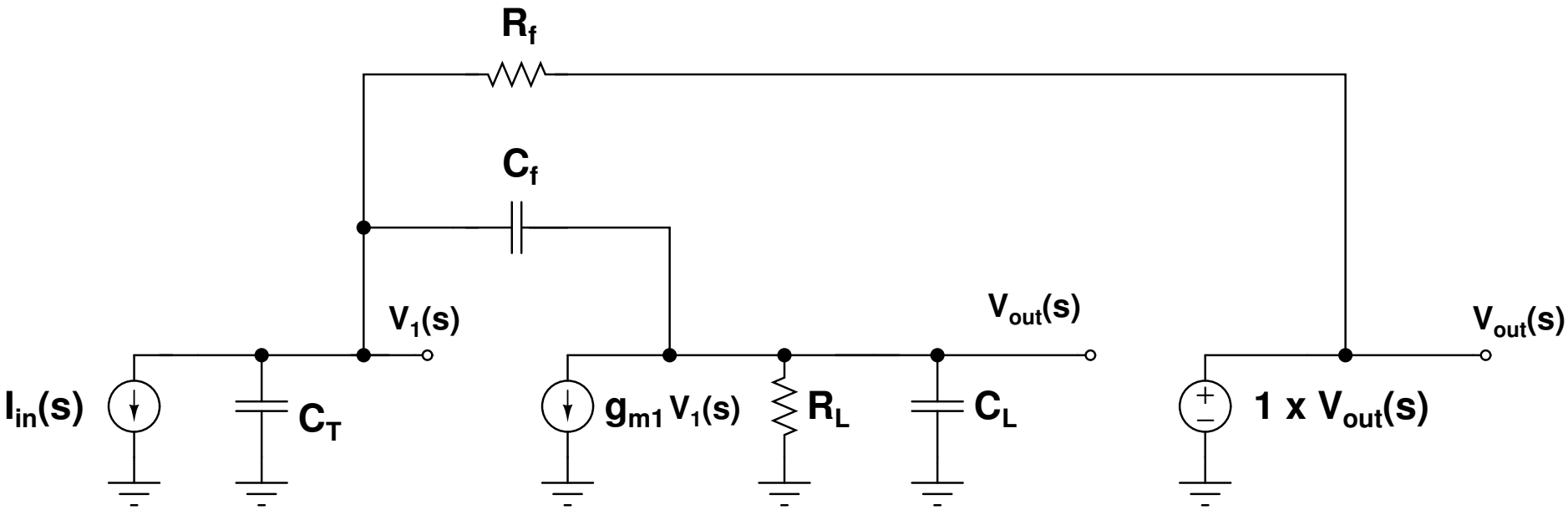
TIA or CSA topology

- $f_{in} < 1/2\pi R_f C_f \rightarrow$ TIA
- $f_{in} > 1/2\pi R_f C_f \rightarrow$ CSA

Equations and figures from A. Rivetti, CMOS Front-End for Radiation Sensors, CRC Press, 2015



Step1: small signal model



Step 2: solve the equations

$$T(s) = \frac{\left(g_{m1} - sC_f\right) R_f R_L}{s^2 \zeta R_f R_L + s\left[R_L C_L + R_f C_T + (1 + g_{m1} R_L) C_f R_f\right] + 1 + g_{m1} R_L}$$

$$R_f C_f > \frac{4\left(C_T C_L + C_T C_f + C_f C_L\right)}{g_{m1} C_f}$$

$$\tau_f = R_f C_f$$

$$\tau_r = \frac{C_T C_L + C_T C_f + C_L C_f}{g_{m1} C_f}$$

Output equation

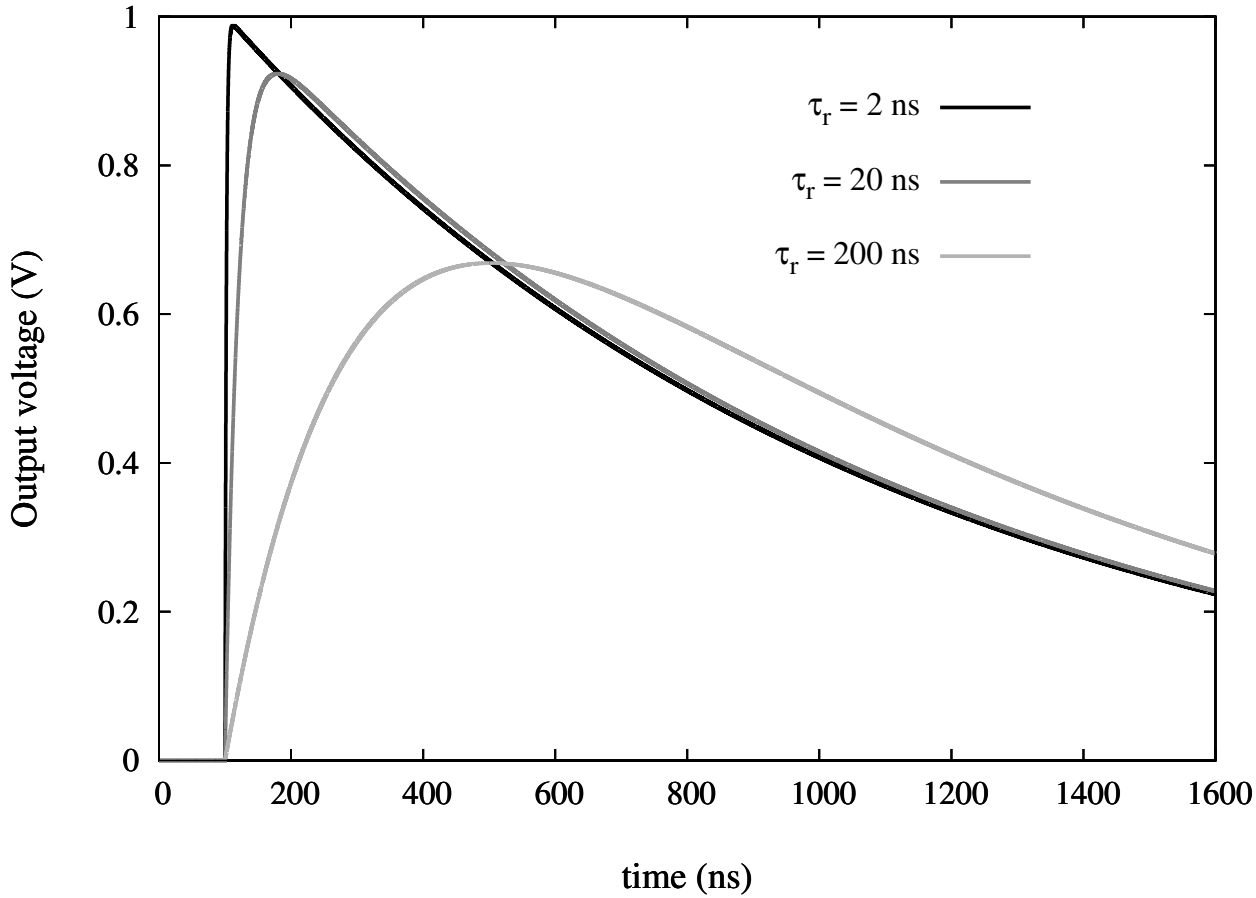
- Impulse response of a system with two real poles

$$V_{out}(t) = Q_{in}\frac{R_f}{\tau_r - \tau_f}\left(e^{-\frac{t}{\tau_r}} - e^{-\frac{t}{\tau_f}}\right) = \frac{Q_{in}}{C_f}\frac{\tau_f}{\tau_r - \tau_f}\left(e^{-\frac{t}{\tau_r}} - e^{-\frac{t}{\tau_f}}\right)$$

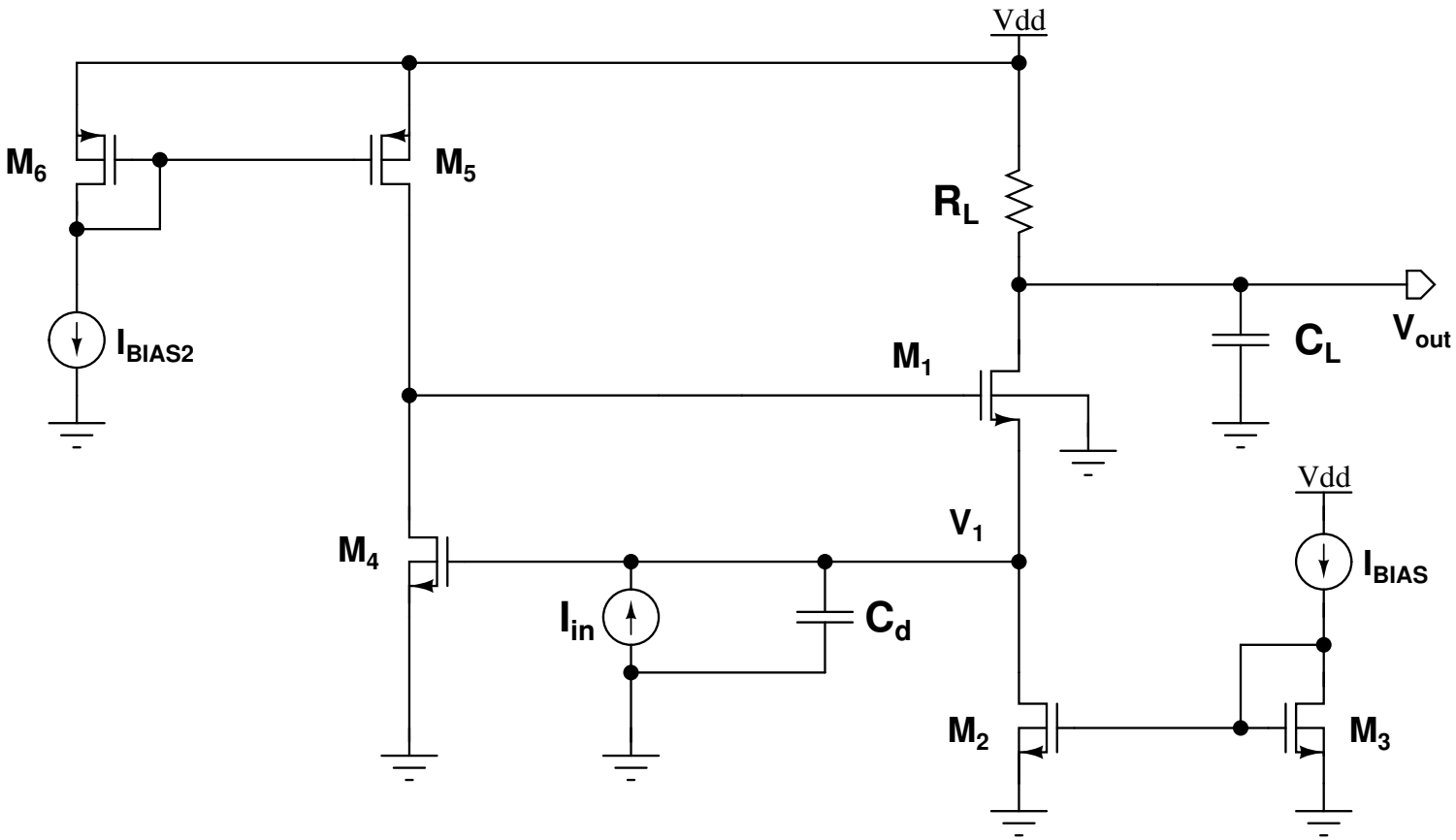
$$V_{out,peak} = \frac{Q_{in}}{C_f}\left(\frac{\tau_f}{\tau_r}\right)^{\frac{\tau_r}{\tau_r - \tau_f}}$$

Example of output waveforms

$$\tau_r \approx \frac{C_T\,(C_L + C_f)}{g_{m1}\,C_f}$$



Common gate topologies

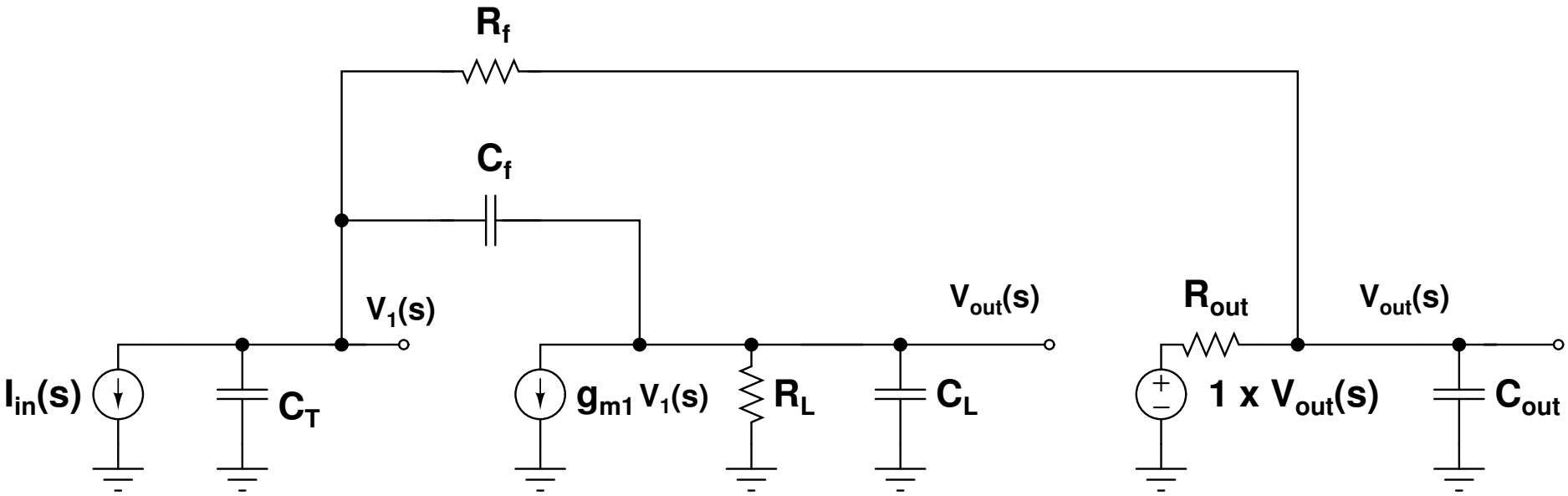


Cgate speed performance

$$\frac{V_{out}}{I_{in}} = \frac{R_L}{\left[1 + s\frac{\left(C_T + AC_{gs}\right)}{g_{m1}A}\right](1 + sR_LC_L)}$$

$$\frac{V_{out}}{I_{in}} = \frac{R_L}{\left(1 + s\frac{C_T}{g_{m1}A}\right)(1 + sC_LR_L)}$$

Complicating the picture...



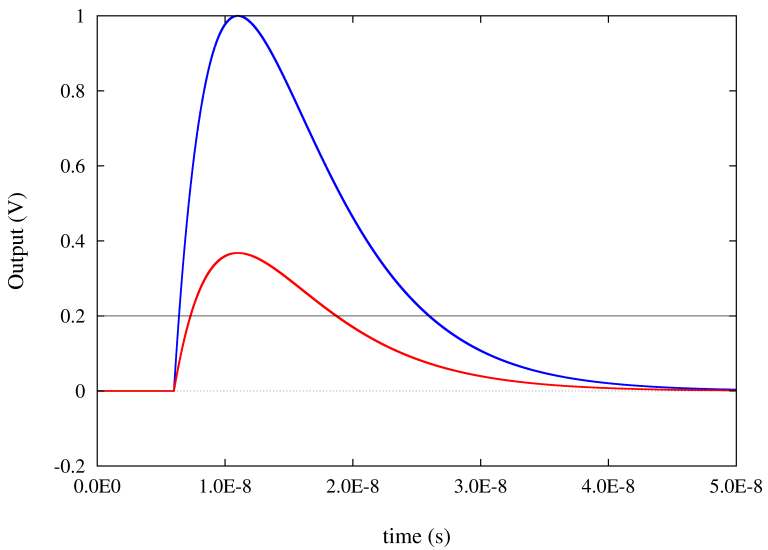
Optimizing rise-time performance

- Front-end transfer function analysis essential to gain intuition
- Unfortunately it needs many approximations to be manageable
- Transistors models in deep submicron technologies are very complex
- Mathematical modeling helpful for a first-cut design
- Costraint-driven CAD optimization

Outline

Time walk

- Pulses of same shape and different amplitude crosses the threshold at different times
- Even worse if also the shape changes
- This is a problem for accurate timing



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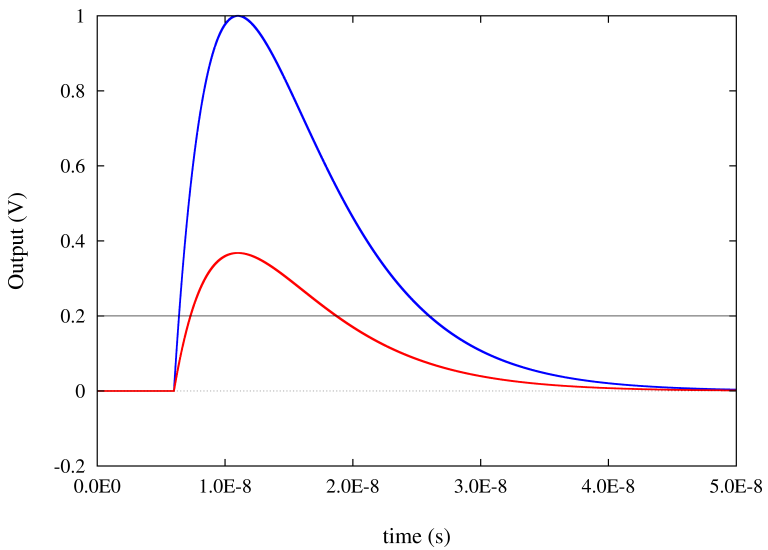

Common solutions

- Correct using the pulse amplitude
- Correction usually done off-line
- Time-over-threshold often used
- Zero-crossing timing
- Track in real-time the pulse with the threshold

Time walk

- Pulses of same shape and different amplitude crosses the threshold at different times
- Even worse if also the shape changes
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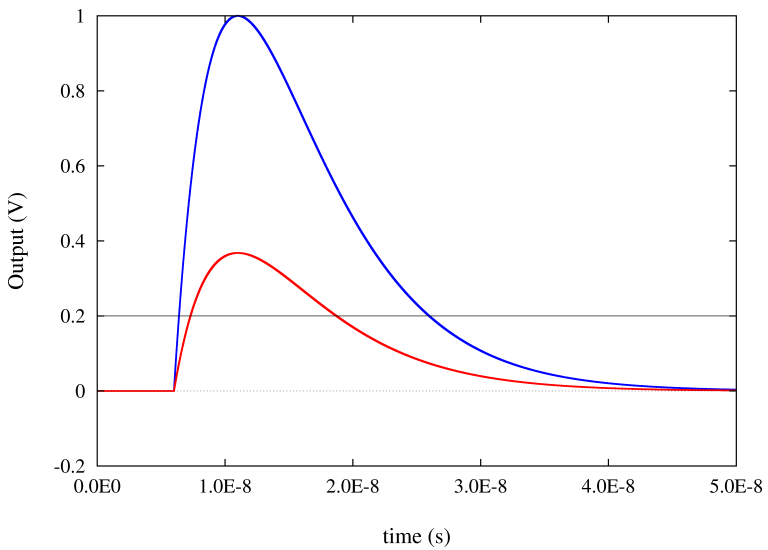


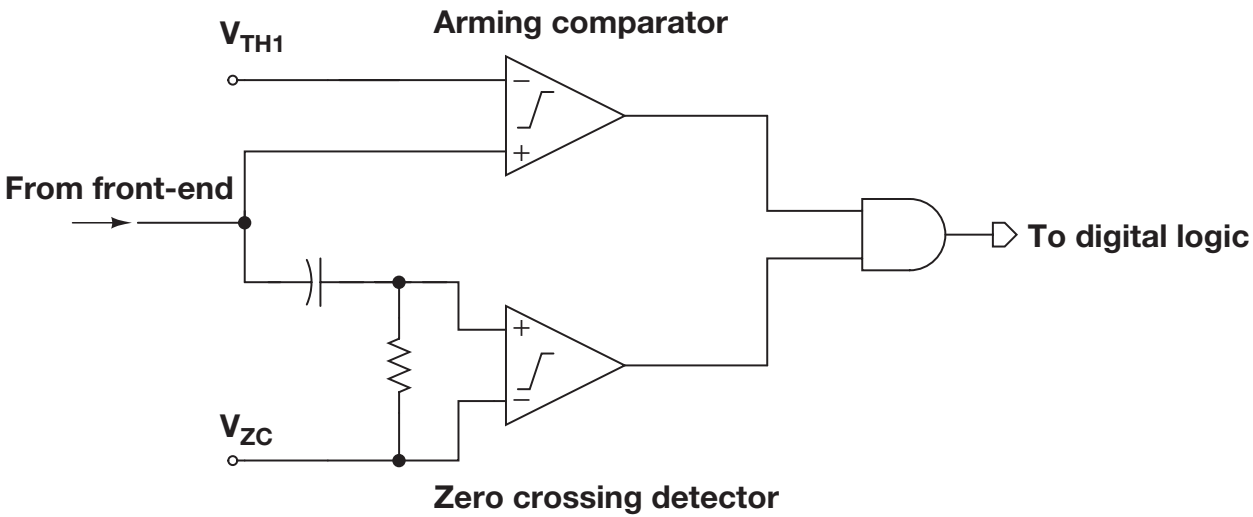
Common solutions

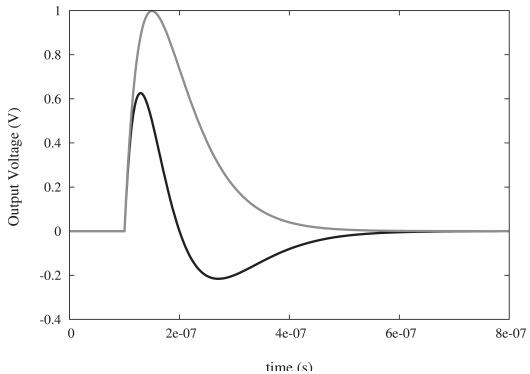
- Correct using the pulse amplitude
- Correction usually done off-line
- Time-over-threshold often used
- Zero-crossing timing
- Track in real-time the pulse with the threshold

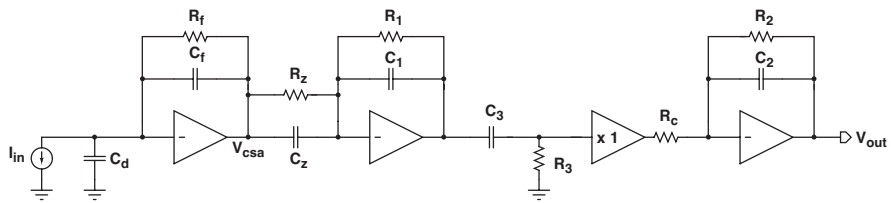
- Constant Fraction Timing

Zero-crossing timing

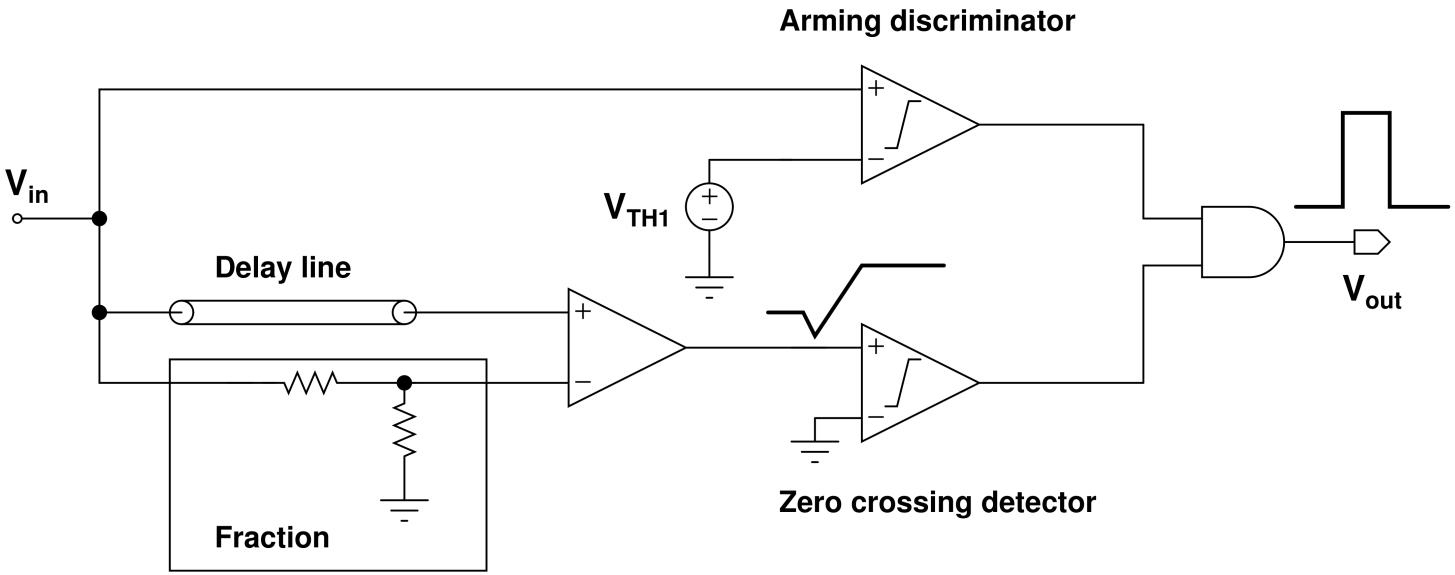
- All signals reach the peak at the same time
- Differentiate and take the zero crossing time
- Jitter is increased



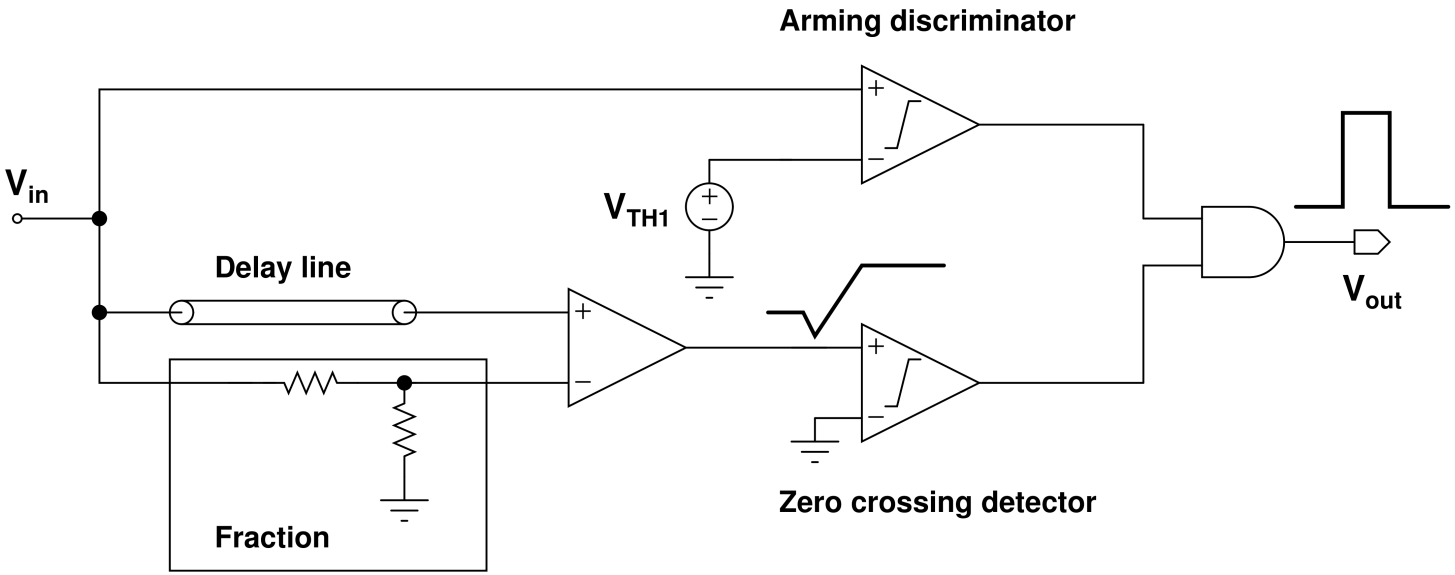




CFD: the principle

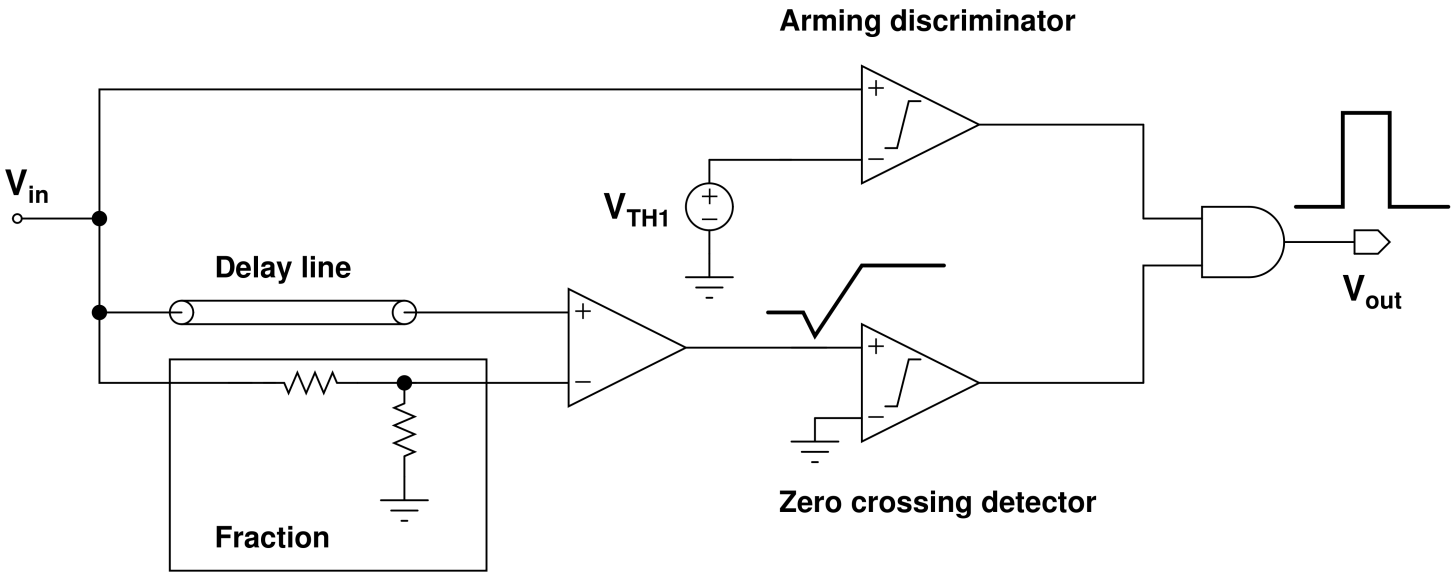


CFD: the principle



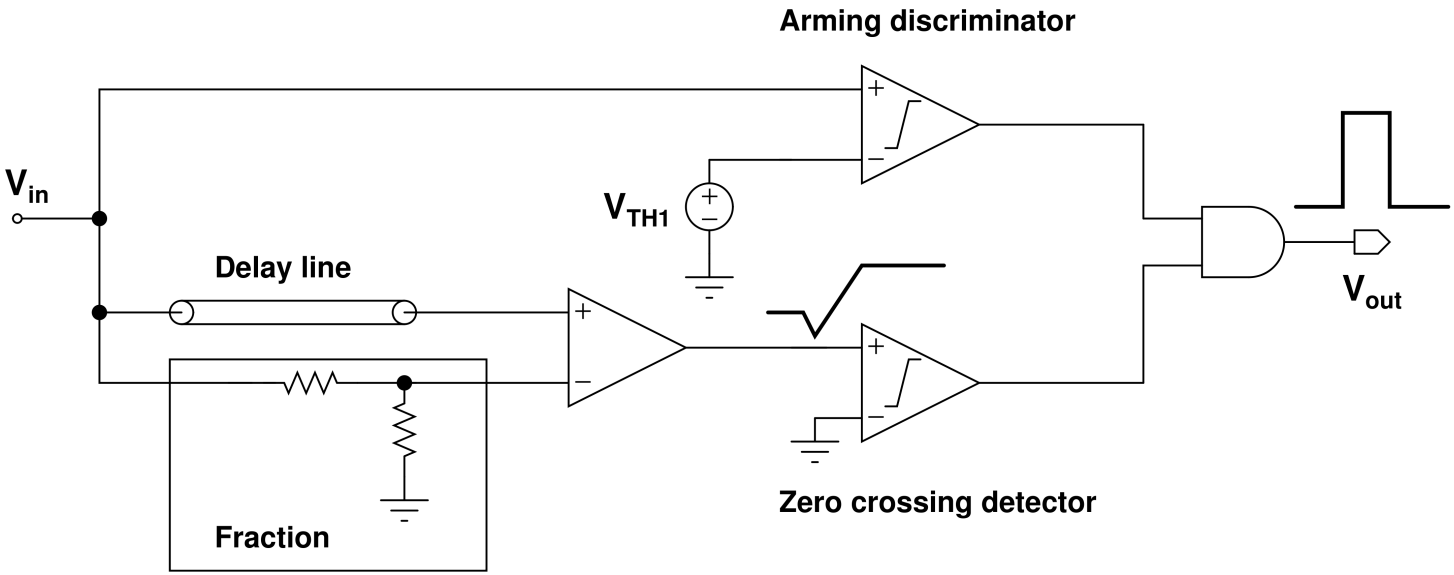
- The input signal is both delayed and attenuated

CFD: the principle



- The input signal is both delayed and attenuated
- The delayed and attenuated signals are combined to yield a bipolar waveform

CFD: the principle

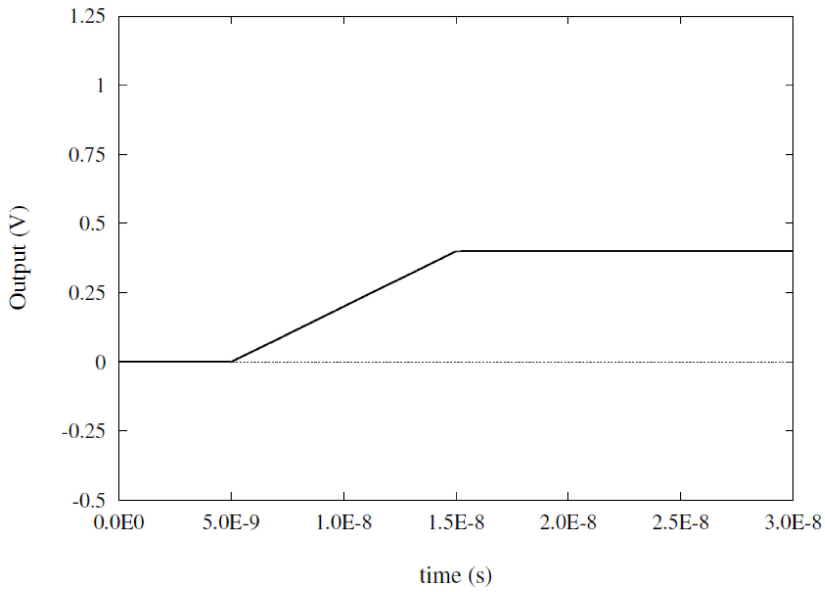


- The input signal is both delayed and attenuated
- The delayed and attenuated signals are combined to yield a bipolar waveform
- The zero crossing of the bipolar waveform is used for timing

CFD: the algorithm

Assume a step input signal:

$$V(t) = \begin{cases} 0 \text{ for } t < 0 \\ \frac{t}{t_r} V_0 \text{ for } 0 < t < t_r \\ V_0 \text{ for } t > t_r \end{cases}$$



$t_d > t_r$, amplitude compensation

$fV_0 = \frac{t-t_d}{t_r} V_0 \qquad t_{zc} = ft_r + t_d$

$t_d < t_r$, ARC compensation

$f \frac{t}{t_r} V_0 = \frac{t-t_d}{t_r} V_0 \qquad t_{zc} = \frac{t_d}{1-f}$

CFD: in practice

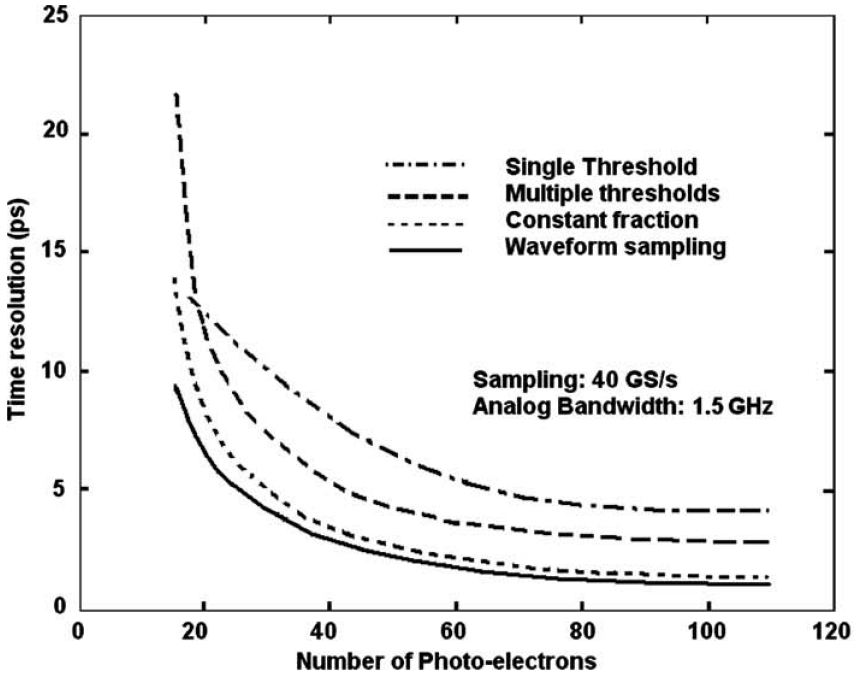
Take now simple $CR - RC$ shaping and an ideal delay line:

$$\frac{t - t_d}{\tau} e^{-\frac{t-t_d}{\tau}} - f \frac{t}{t_d} e^{-\frac{t}{\tau_d}} = 0 \rightarrow t_{zc} = \frac{t_d e^{\frac{t_d}{\tau}}}{e^{\frac{t_d}{\tau}} - f}$$

- Jitter optimization: $\tau = t_{coll} \rightarrow$ sensitivity to pulse shape fluctuations!
- Can be reduced by reducing t_d, f, or both...
- CFDs rely of fully linear signal processing
- Not trivial to implement in modern CMOS technologies due to the reduced voltage headroom, but it can be done.

Some comparison

J. F. Genat et al. Signal processing for picosecond resolution timing measurements, NIM A 607 (2009) 387-393



- Simulations based on MCP signal
- No sampling jitter added
- The barrier of 10 ps broken around 20 pe
- Practical equivalency between WS and CFD

Can we have better algorithms?

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Nuclear Instruments and Methods in Physics Research A 457 (2001) 347–355

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

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Timing of pulses of any shape with arbitrary constraints and noises: optimum filters synthesis method

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Received 9 June 2000; accepted 15 June 2000

Abstract

In this paper the optimum filtering for the precise measurement of the occurrence time of any kind of time-limited signal is dealt with. We find the time-limited optimum weighting function (WF) in the presence of any kind of uncorrelated, stationary, additional noises and we allow the introduction of arbitrary assigned time domain constraints in the WF. The method can be easily translated into computer programs and it can be used as a tool for optimising a digital signal processing spectroscopy set-up in its digital filter section. An application of the method to signals at the output of large volume HPGe γ-ray detectors is finally presented.

Can we have better algorithms?

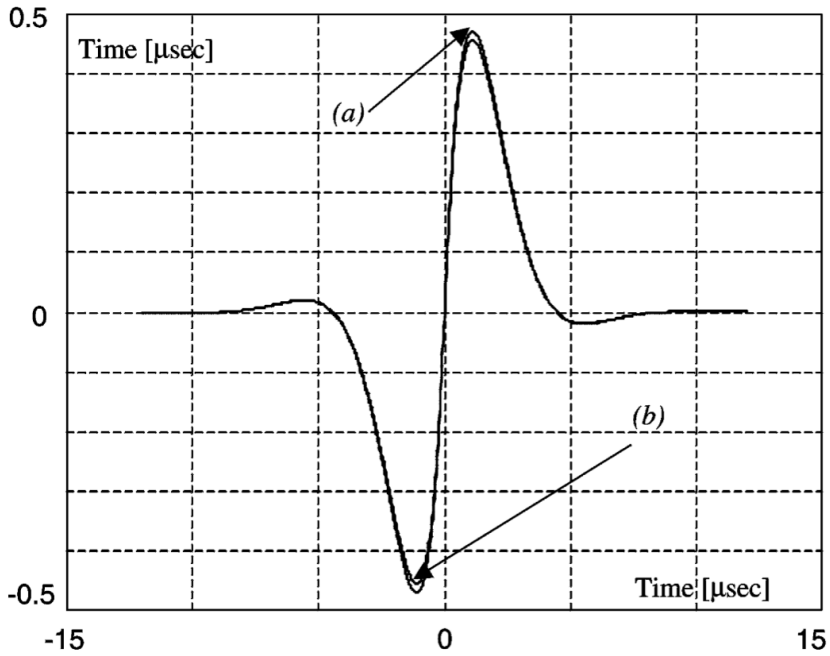


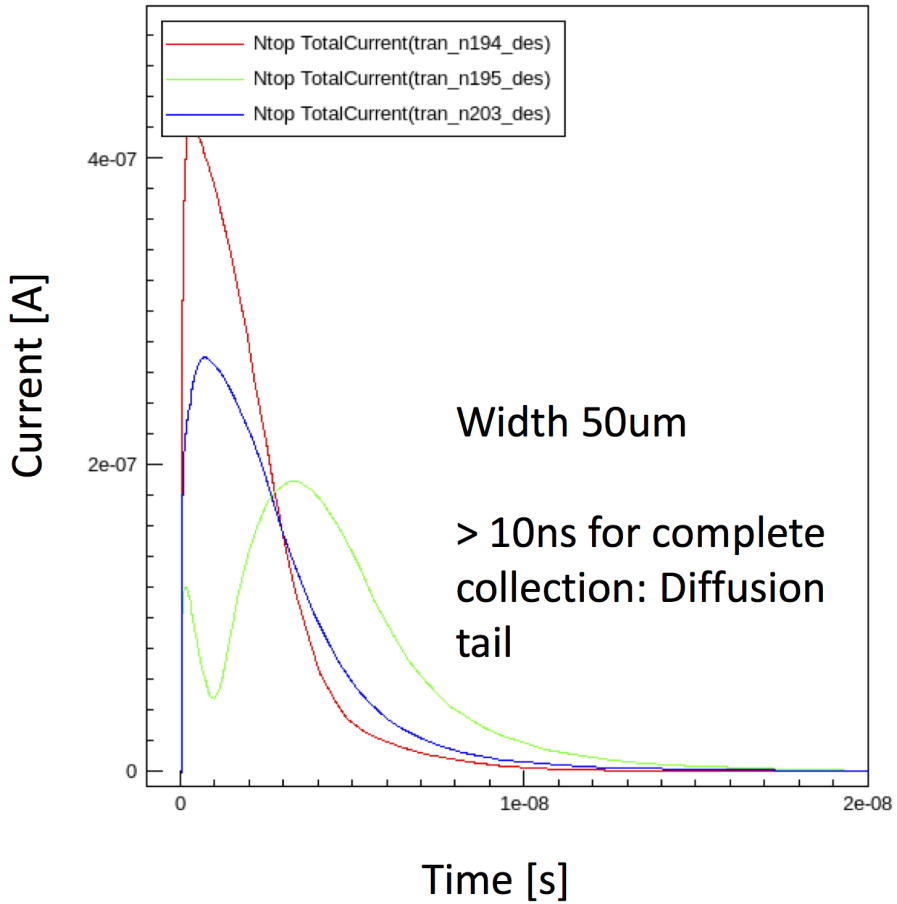
Fig. 1. Comparison between the approximated optimum synthesised WF $w(t)$ (a) and the analytical one (b)in the test case (see text): the two curves almost coincide and the maximum divergence is in correspondence with the cusp peak. This is to be expected, since our representation of $w(t)$ involves an analytical function expressed with a finite number of harmonics. The number of harmonics is 200. The difference in time resolution is just 2%.

Simulation methodology

- Generate a set of charges from the Landau distribution covering the dynamic range
- Send the charges in different part of the sensing element
- Collect the resulting current waveforms in the form of time-amplitude lis
- Input them in SPICE with the timing chain (transistor level)
- Important to consider also the discriminators
- Analyze the SPICE outputs and extract the timing
- A lot of scripting...

Signal example

Courtesy L. Pancheri, Trento



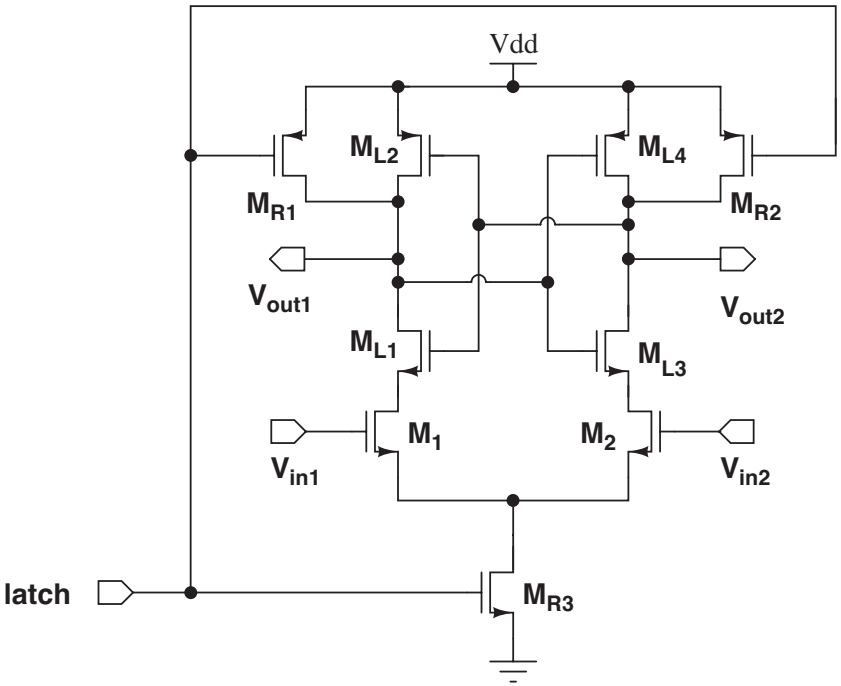
The ideal timing detector

- The ideal timing detector should provide:
  - very fast signals $\rightarrow$ short flight path of the charge carriers in the sensor
  - shape stability
  - low pulse amplitude spread
  - small capacitance
  - sustain high counting rates
  - be radiation tolerant
  - be easily scalable to large large areas
  - cheap

- No sensor fulfills all the above specs

Outline

Latched comparators

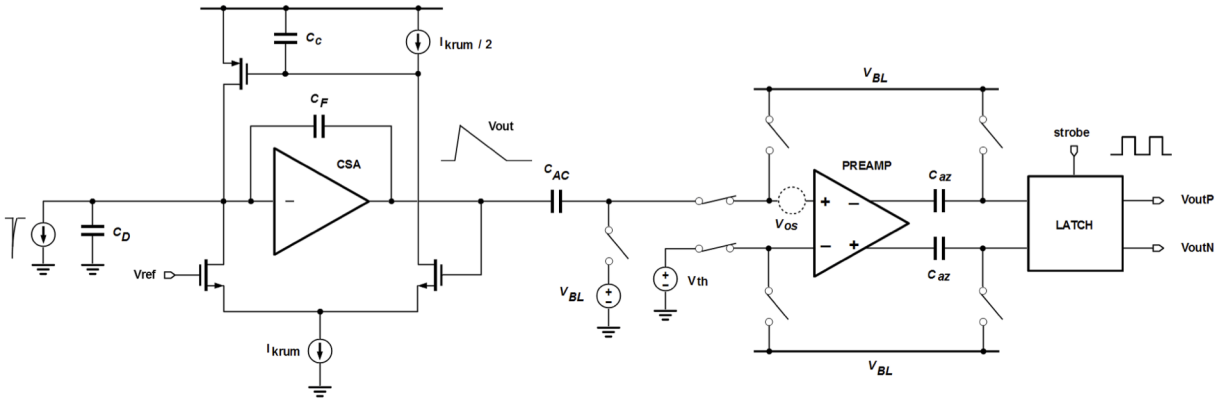


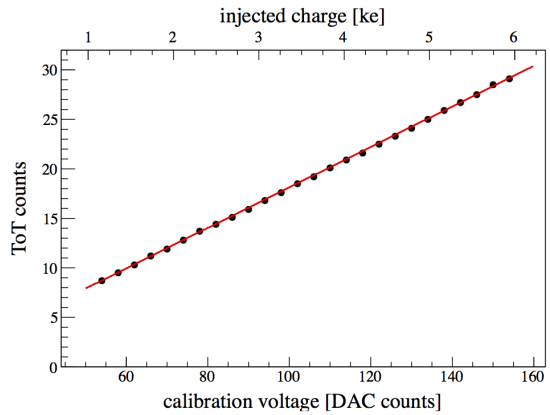
- Latched (synchronous comparators) have many advantages
- Only dynamic power
- Very fast thanks to positive feedback
- Are they good as timing discriminator?

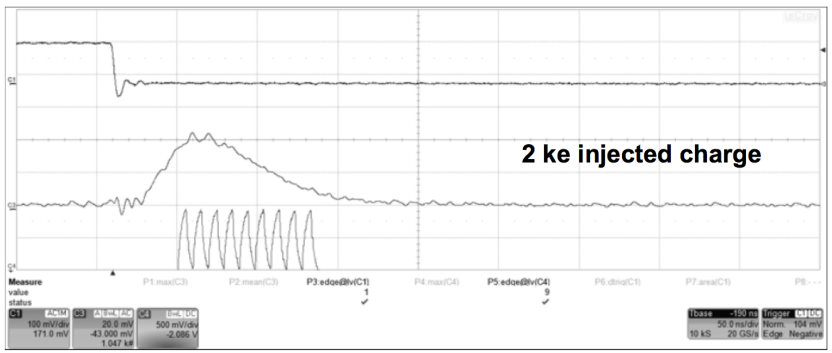
Synchronous discriminator in front-end

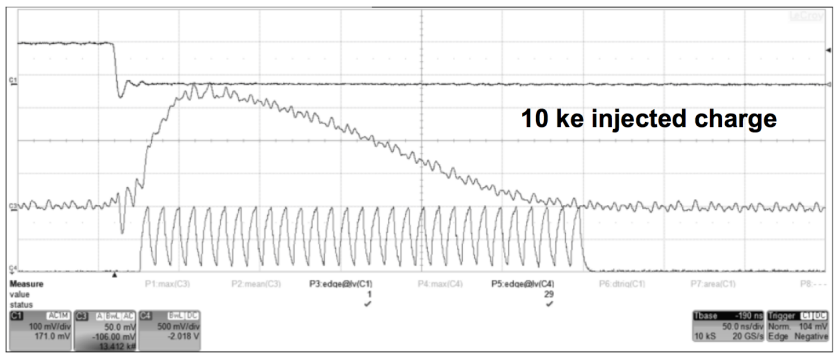
- Dynamic comparator with offset compensation
- Fast ToT with local oscillator

E Monteil et al, "A synchronous analog very front-end in 65 nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC", JINST 2017

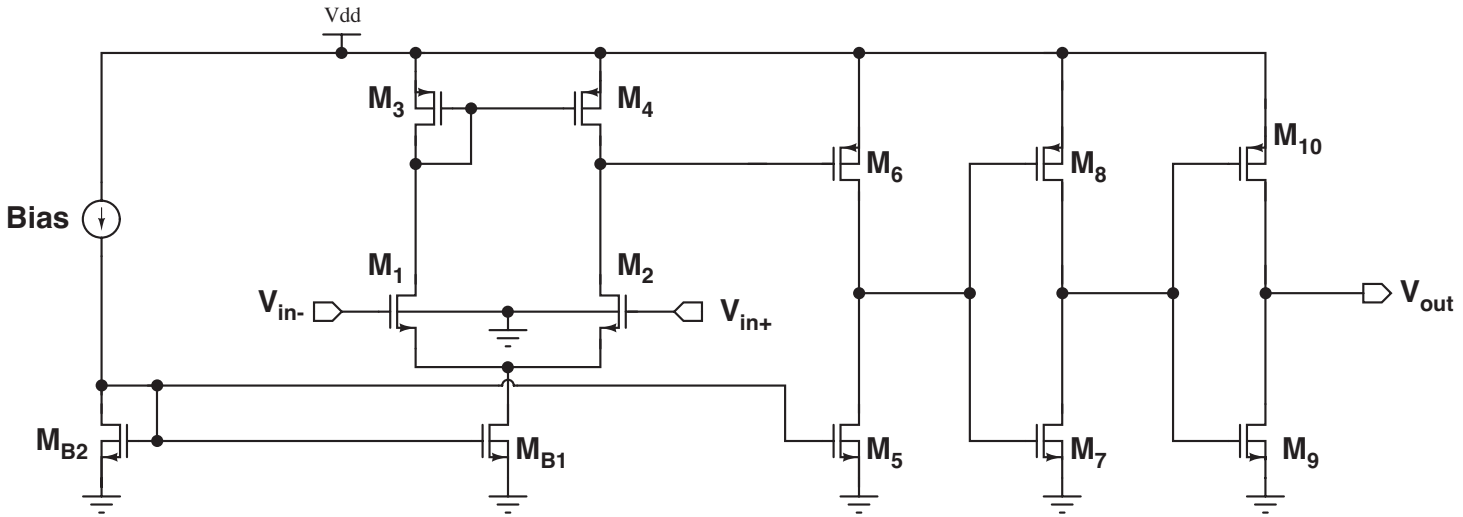


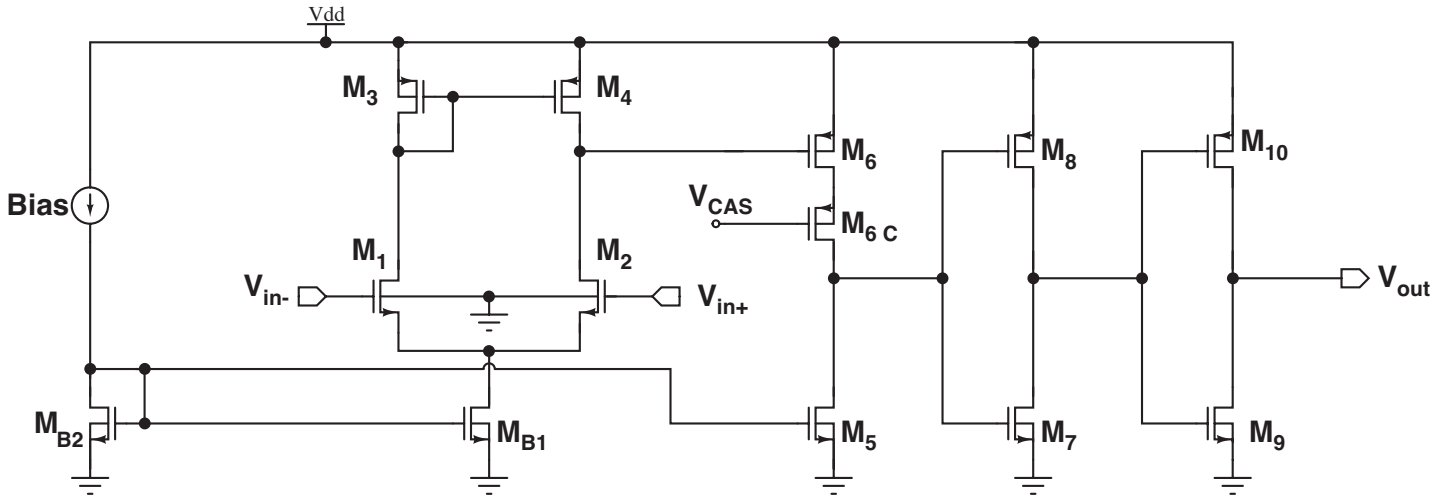






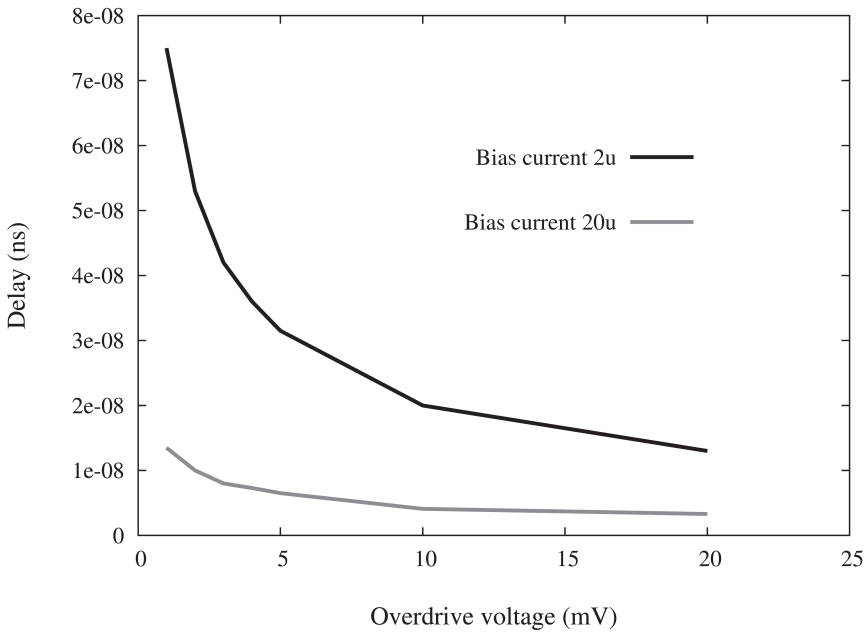
Simple comparators

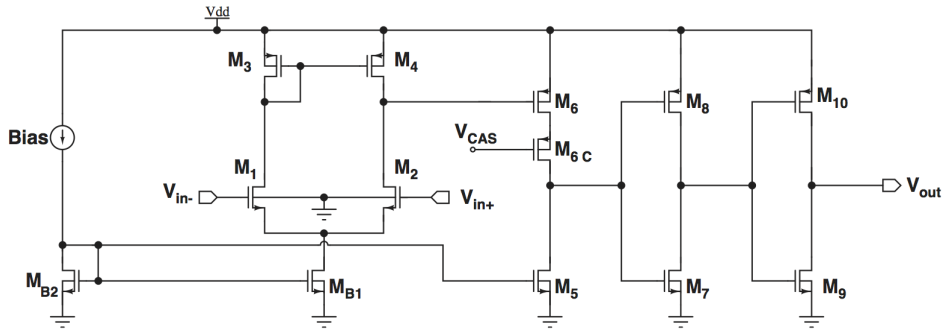




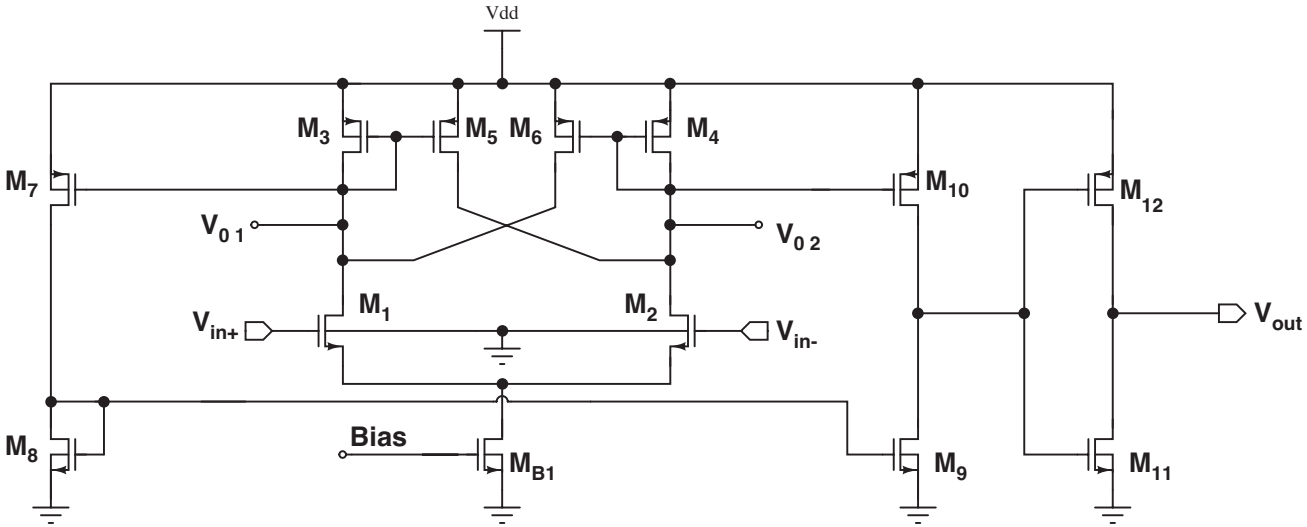
Time delay

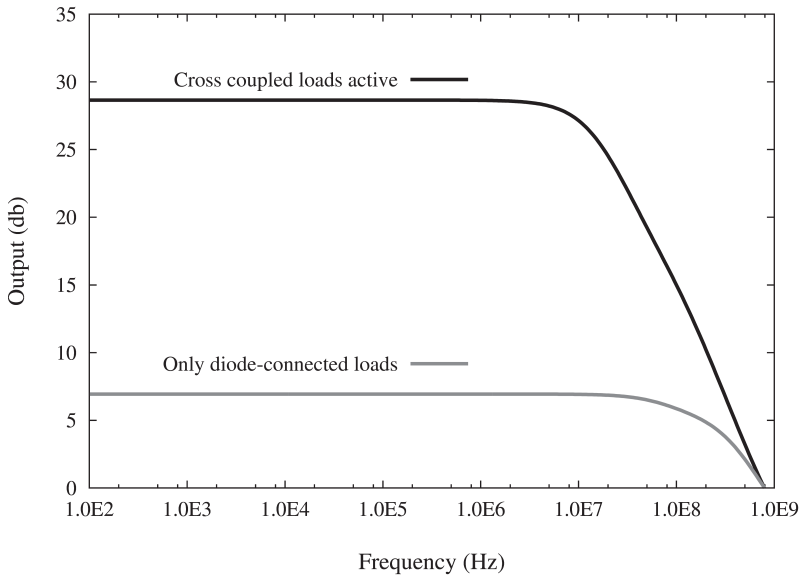
- Comparator can contribute significantly to time-walk
- Fast comparators means power





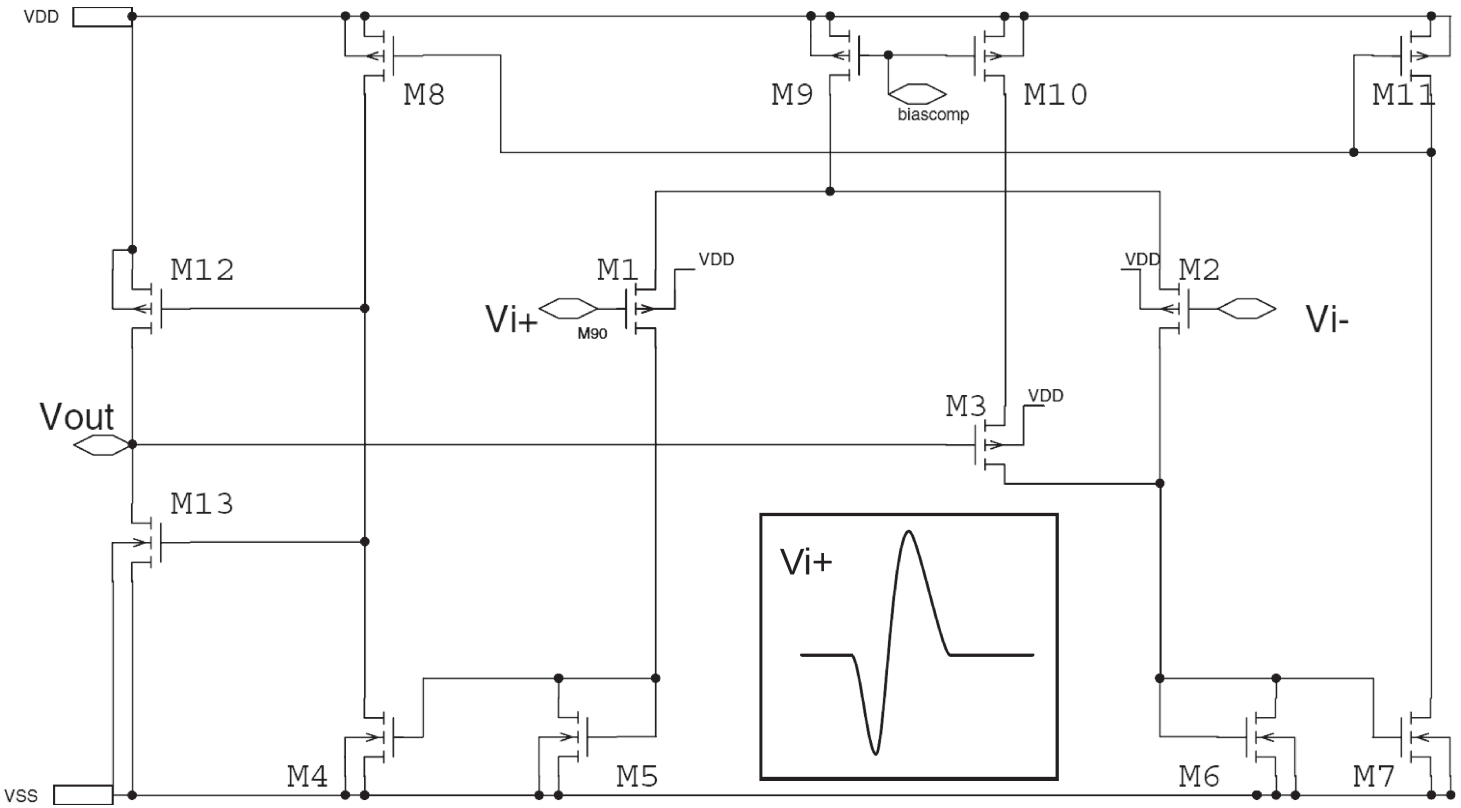
More advanced comparators



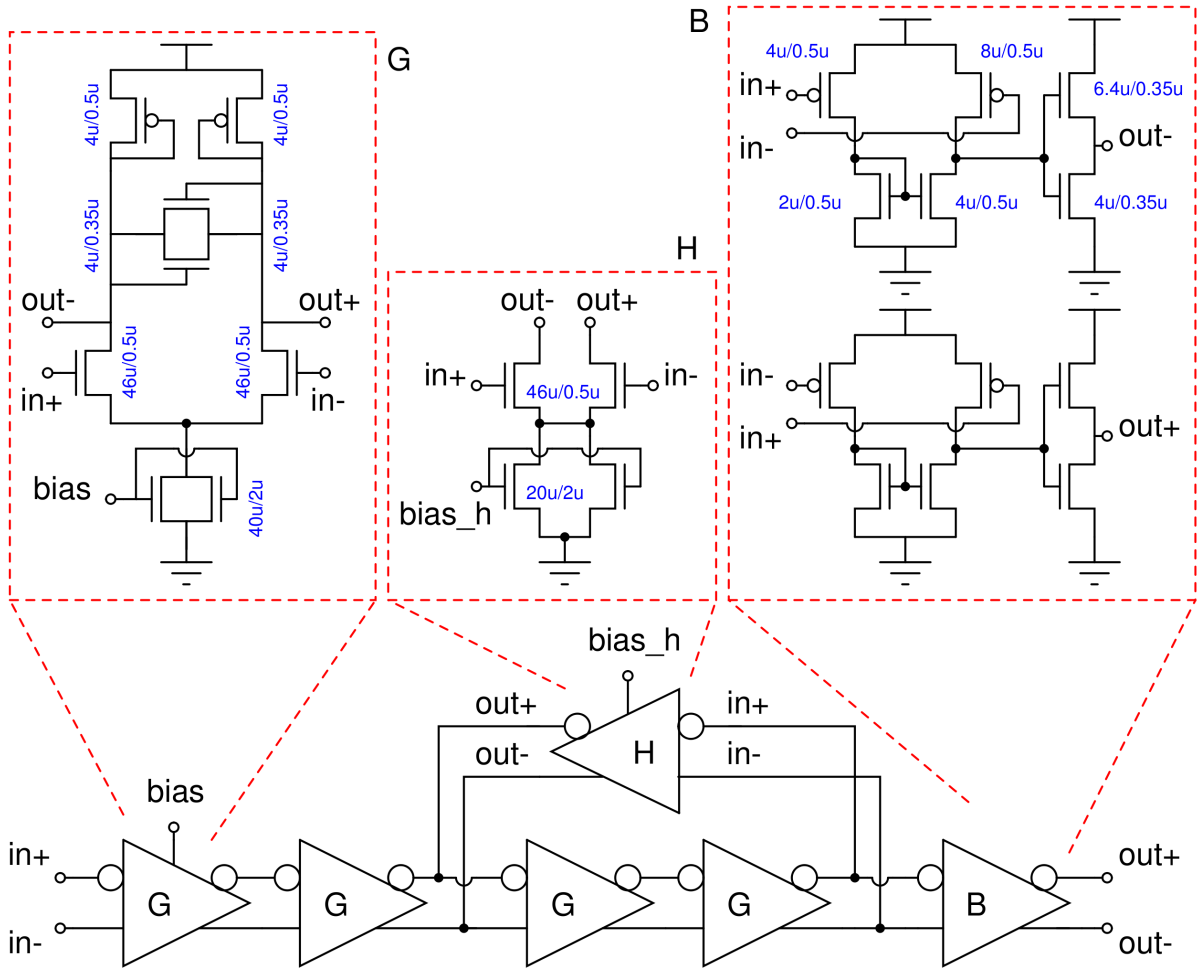


- Assume $g_{m1} = g_{m2}$, $g_{m3} = g_{m6}$
- Differential gain dominated by transistor output conductance
- Common mode gain dominated by diode-connected transistors

Zero crossing detectors



Fast comparators



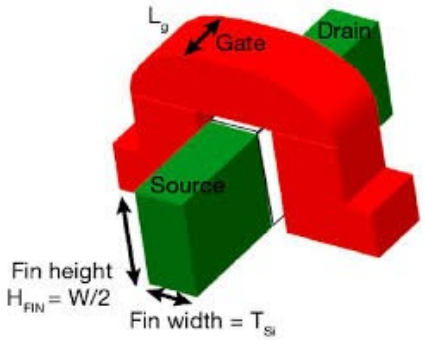
Outline

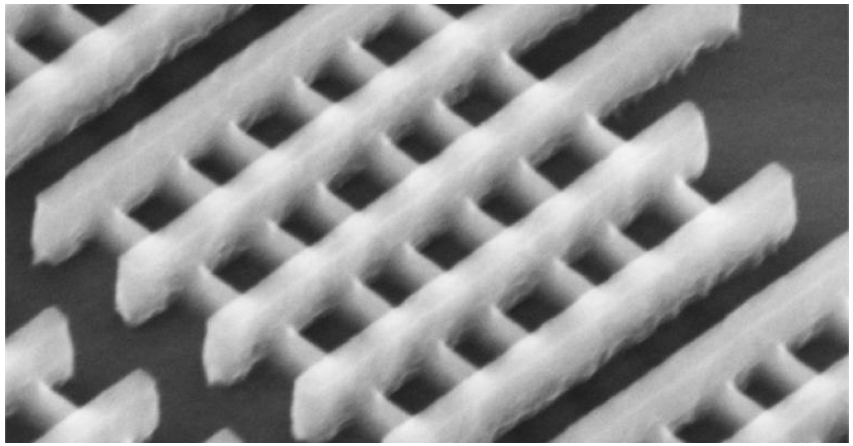
About very fast circuits

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. 12, DECEMBER 2017

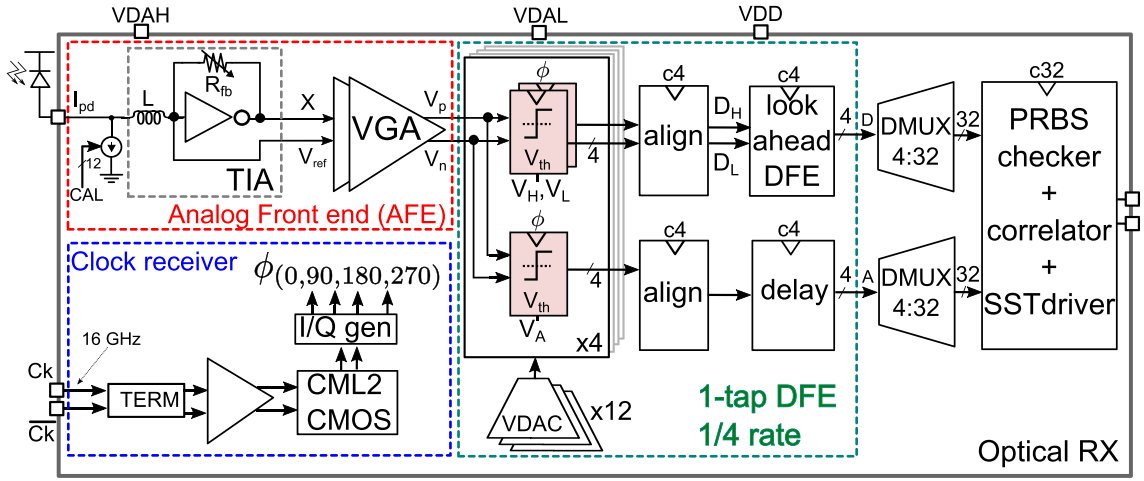
A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET

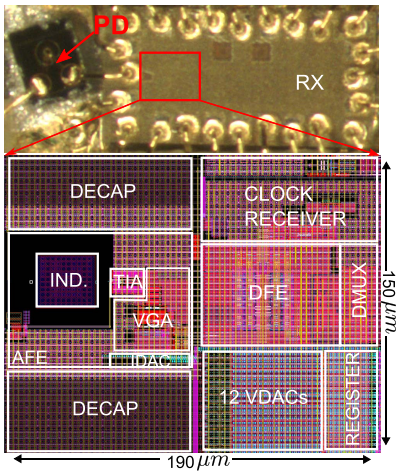
Ilter Ozkaya, *Student Member, IEEE*, Alessandro Cevrero, *Member, IEEE*,
Pier Andrea Francese, *Senior Member, IEEE*, Christian Menolfi, *Member, IEEE*,
Thomas Morf, *Senior Member, IEEE*, Matthias Brändli, Daniel M. Kuchta, *Senior Member, IEEE*,
Lukas Kull, *Senior Member, IEEE*, Christian W. Baks, Jonathan E. Proesel, *Senior Member, IEEE*,
Marcel Kossel, *Senior Member, IEEE*, Danny Luu, *Student Member, IEEE*,
Benjamin G. Lee, *Senior Member, IEEE*, Fuad E. Doany, Mounir Meghelli, *Member, IEEE*,
Yusuf Leblebici, *Fellow, IEEE*, and Thomas Toifl, *Senior Member, IEEE*



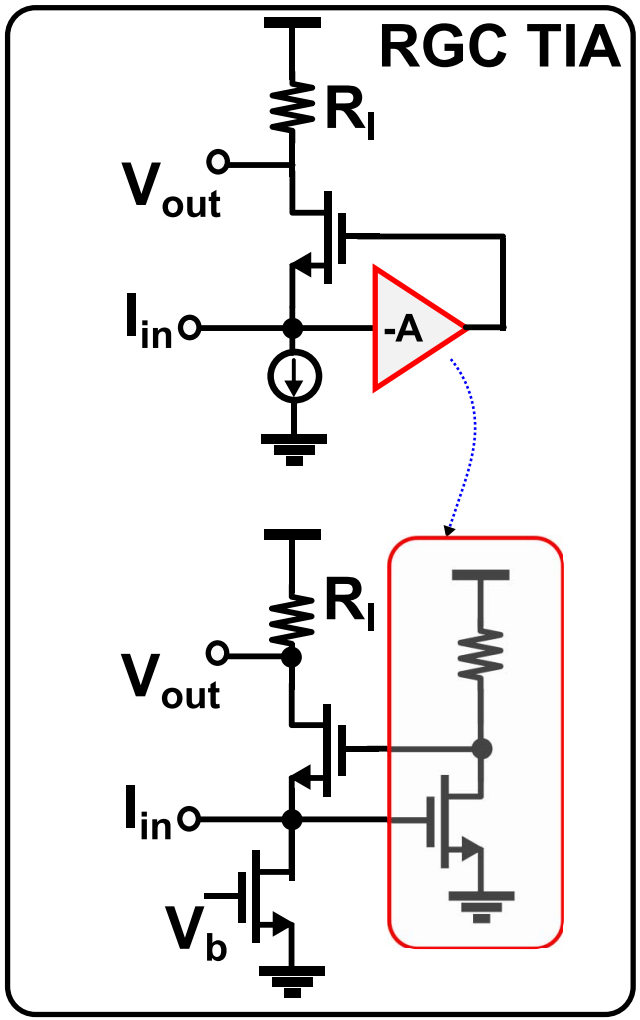


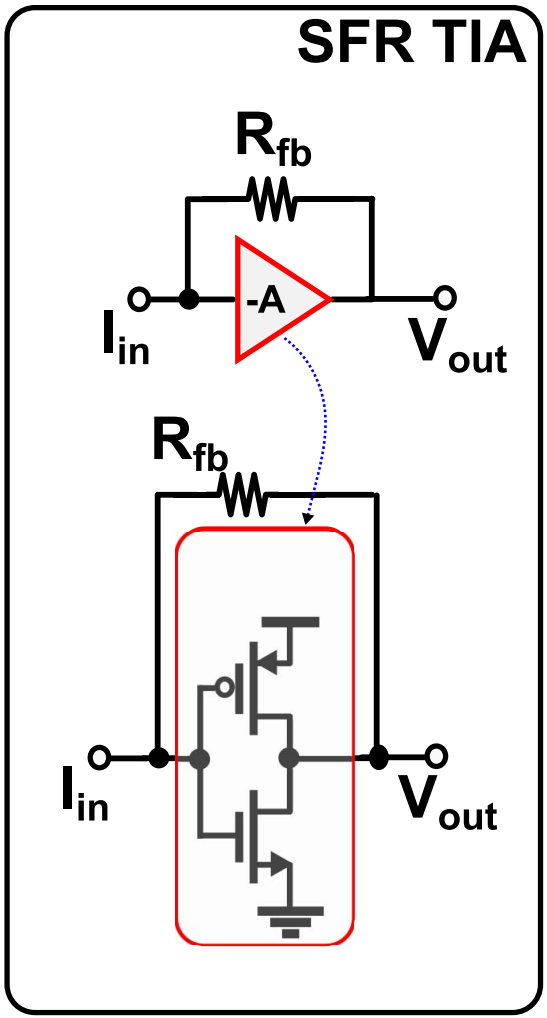
System overview





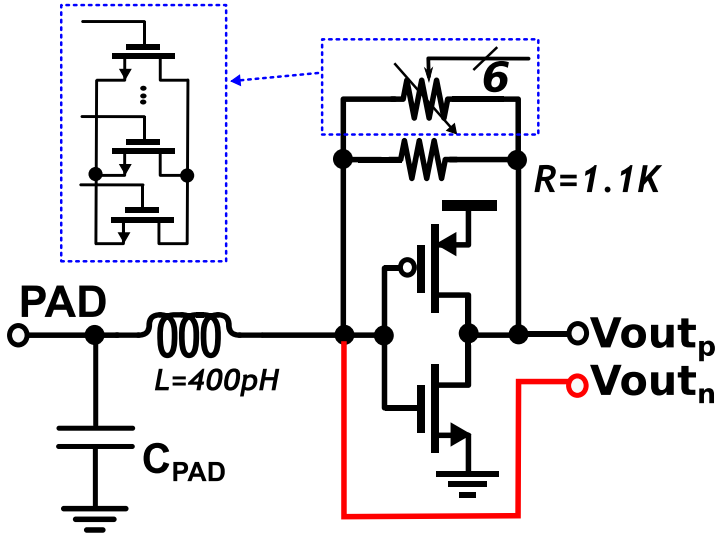
Input topology choice

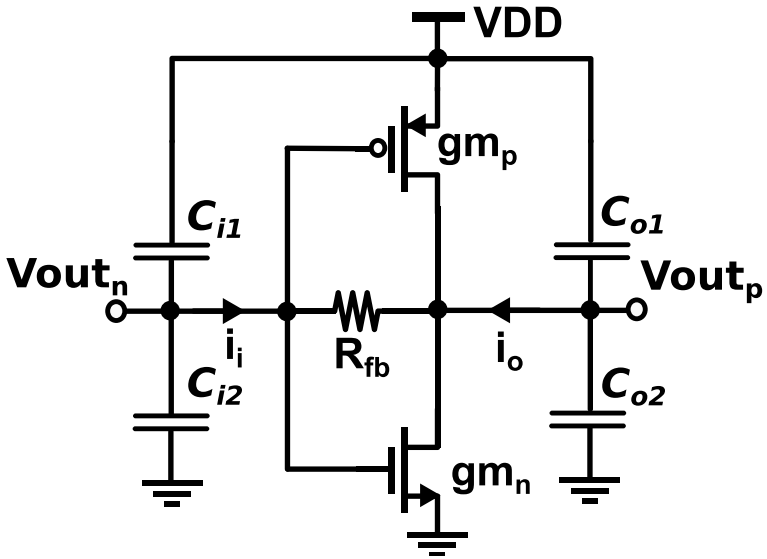




Transimpedance amplifier

…or “how many things you can do with an inverter”!



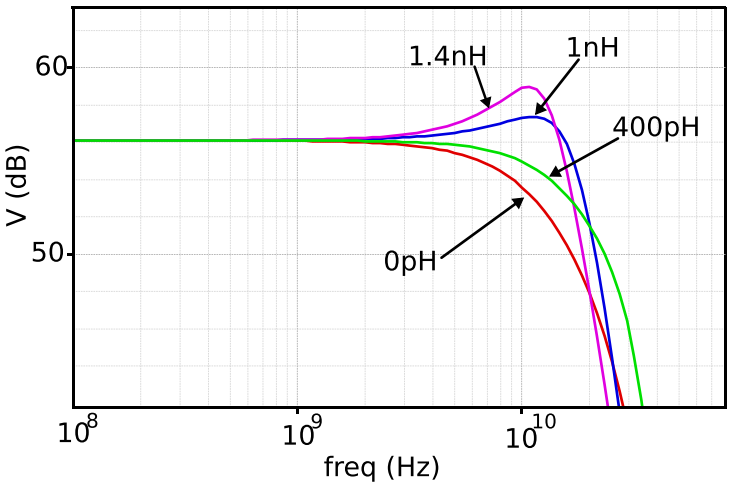


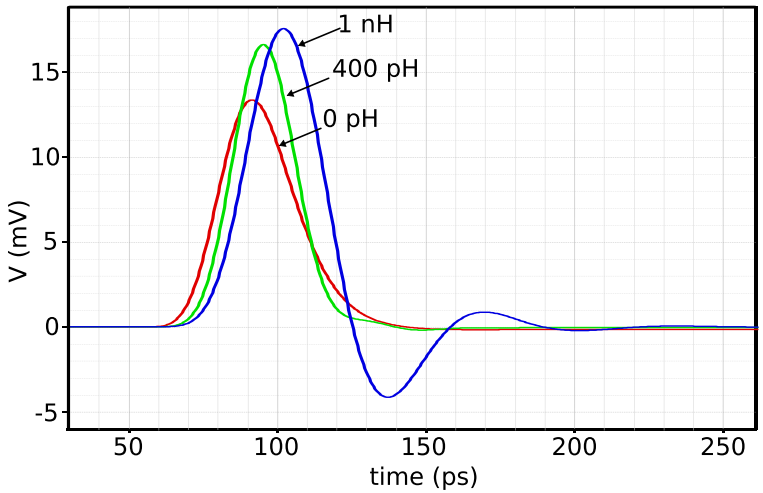
Why transistors are used in feedback?
What is the purpose of the inductor?

What we study here?

$$\frac{C_{i1}}{C_{i2}} = \frac{gm_p}{gm_n} = \frac{C_{o1}}{C_{o2}}.$$

Gain peaking

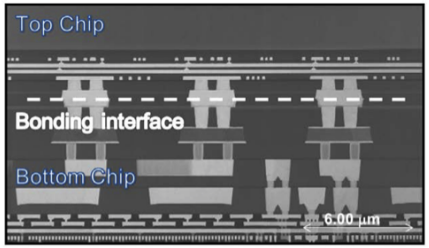


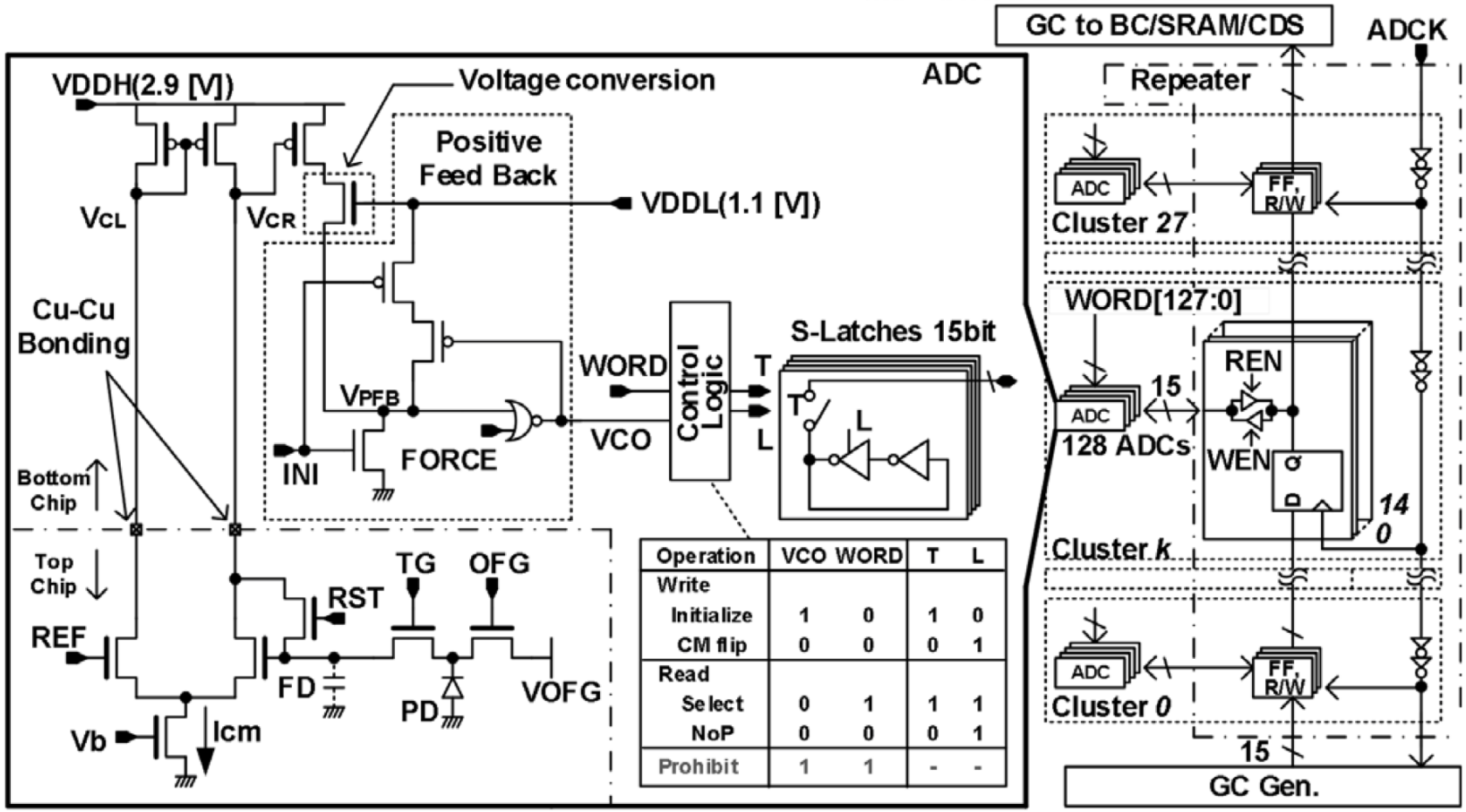


Another use of Wilkinson ADC

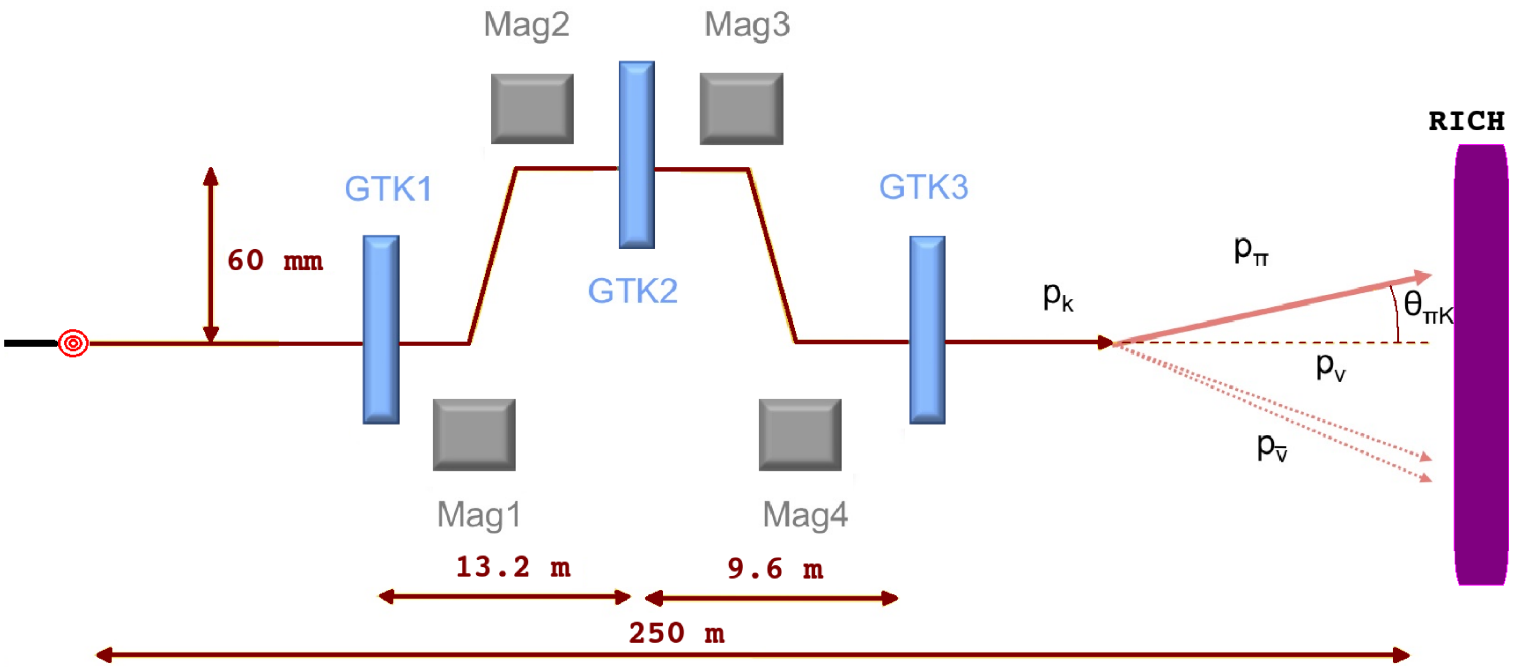
ISSCC 2018 / SESSION 5 / IMAGE SENSORS / 5.1

5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC



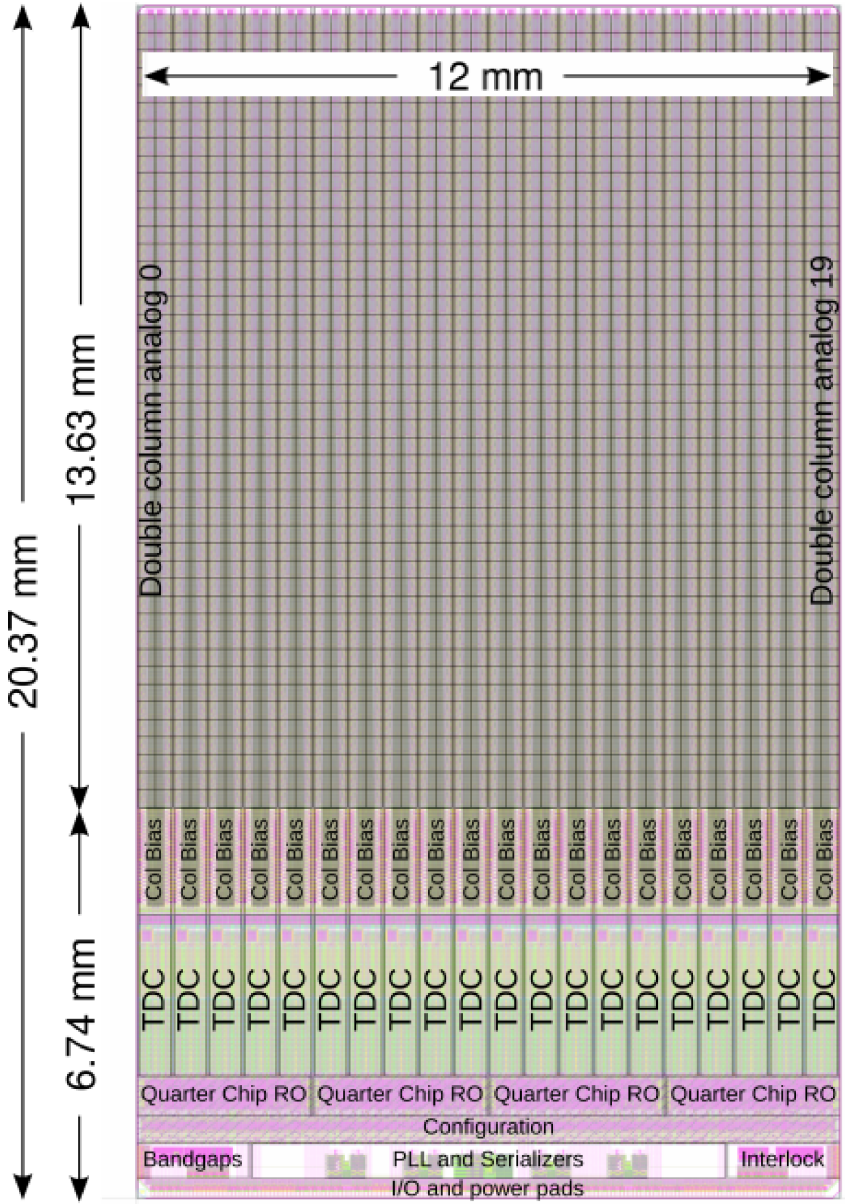


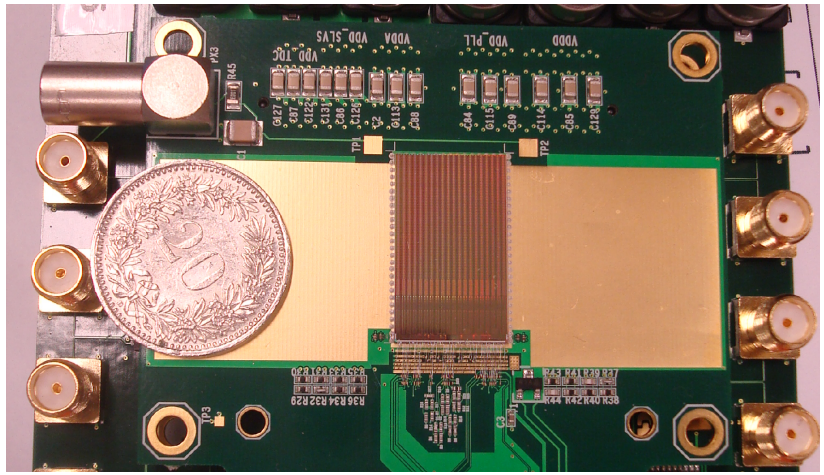
Timing with silicon pixels: The NA62 GTK



- Study of very rare Kaon decay: $K^+ \to \pi^+ \nu\bar{\nu}$
- Time tag the K^+ tracks to match the π^+ track in the RICH
- GTK: three stations of hybrid silicon pixels with $\leq$ 200 ps rms resolution per station
- Sensor area: 60 mm x 27 mm readout by 10 TDCpix chips

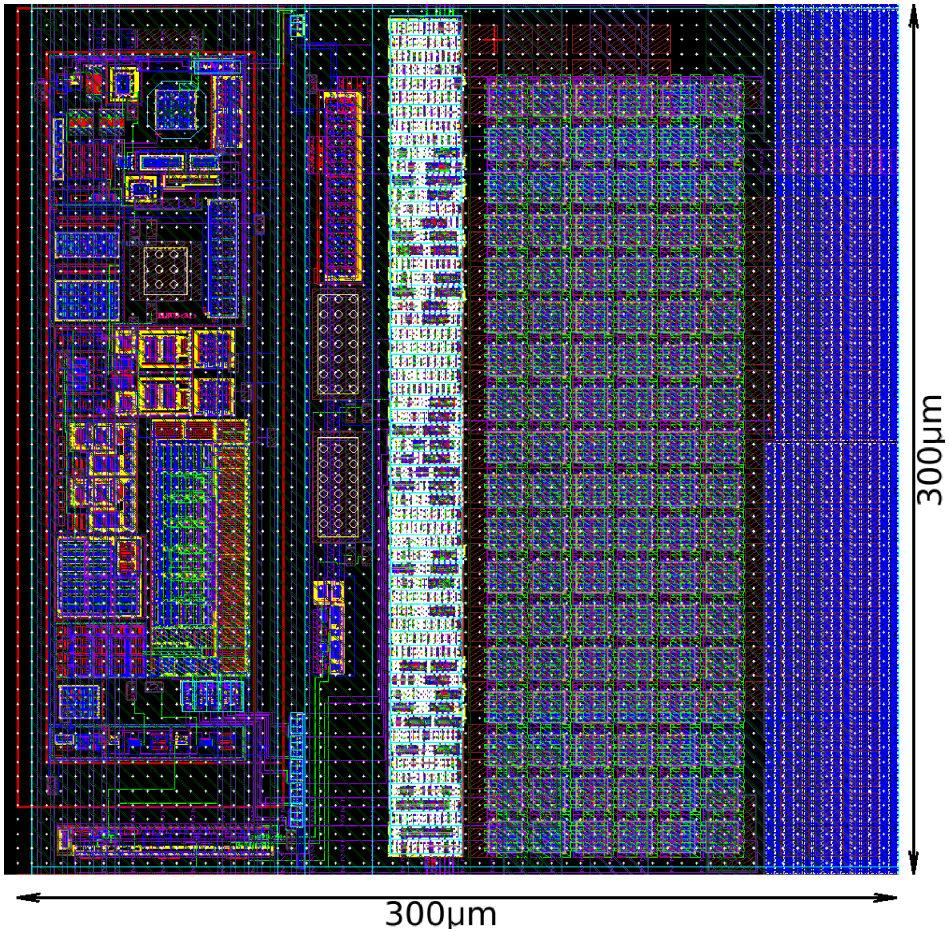
The TDCpix chip at a glance

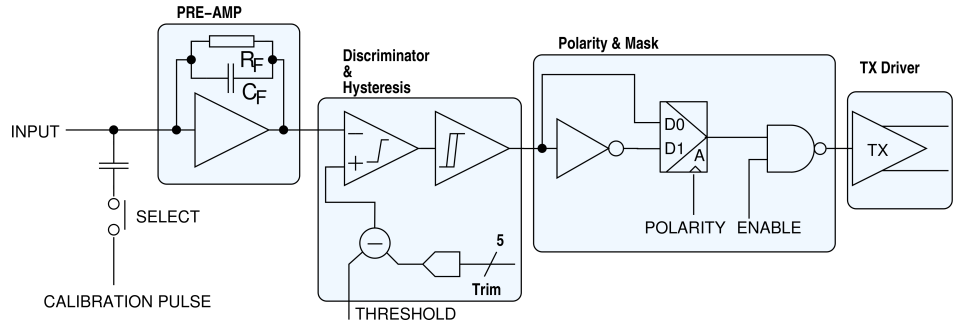




- Timing method: LED + offline ToT compensation
- Pixel area: 300 μm$\times$300μm
- DLL-based TDC in the periphery
- 360 equivalent TDC per chip
- 210 Mhit/s/chip
- 4 $\times$ 3.2 Gbit/s serializers
- CMOS 130 nm, designed at CERN

TDCPix: the pixel

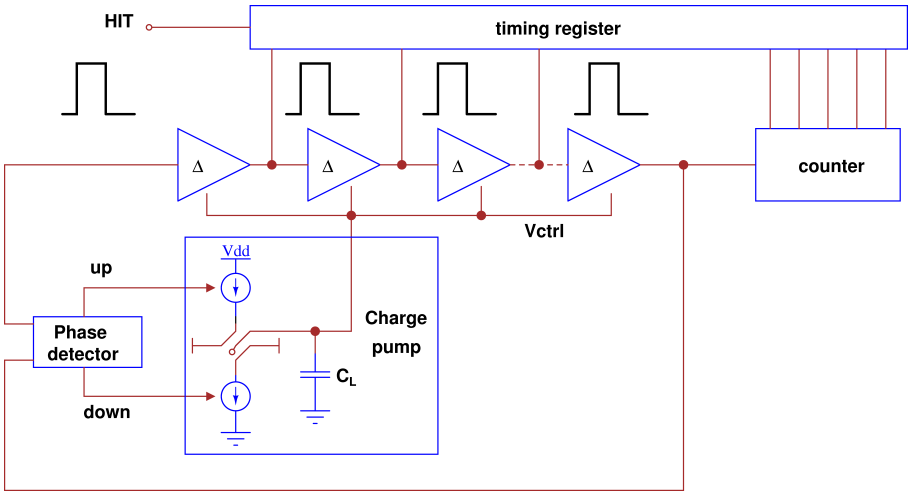


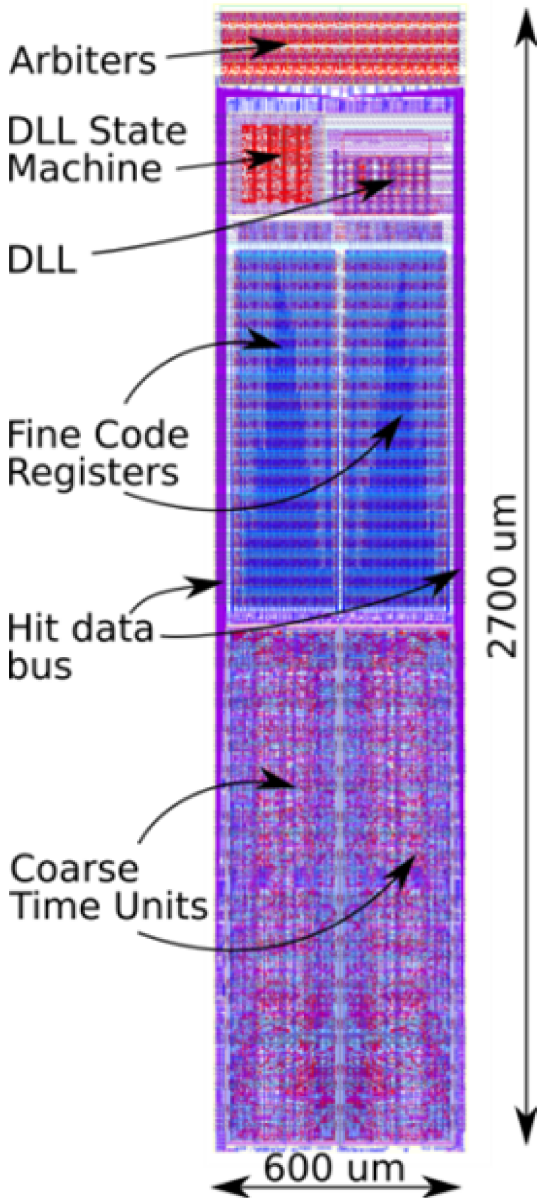


- Transimpedance amplifier followed by leading edge discriminator
- Peaking time ≈ 5 ns
- Only analog electronics and quite configuration registers in the pixel
- Discriminator signal sent to the EoC TDC with integrated t-lines

- Achieve 65 ps rms electronic resolution at 2.4 fC on 1800 pixels!

TDCPix: the TDC



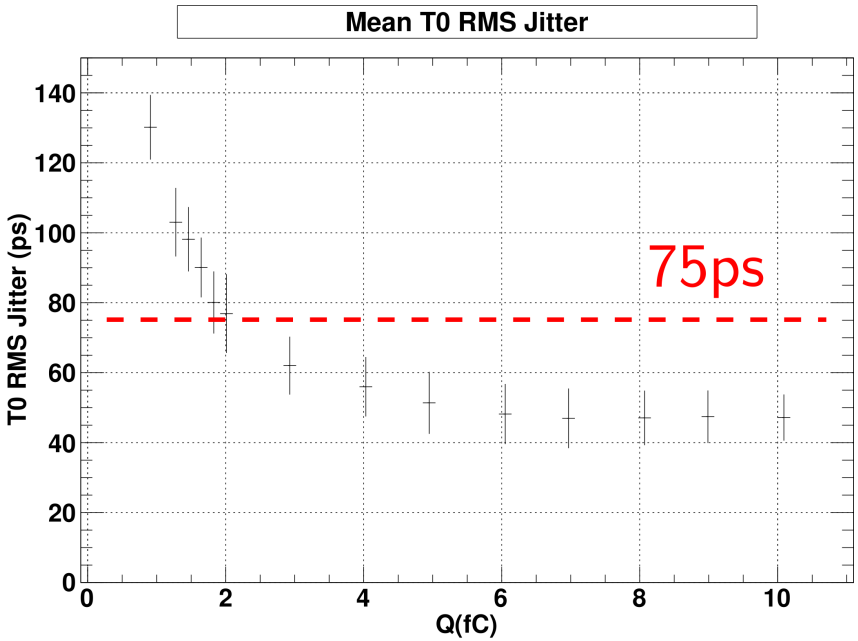


- TDC based on DLL approach
- 320 MHz clock and 32 delay taps
- Differential delay buffers for low noise
- One DLL share among two columns
- One timing register shared among 5 pixels

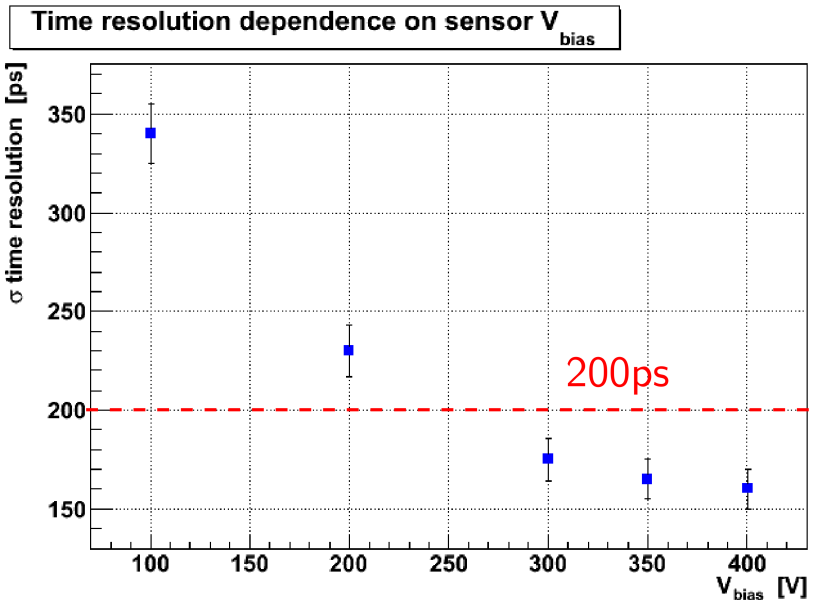
Timing with GTK HPD: some results (1)

RMS time resolution obtained with the TDCPix demonstrator

With laser in the lab...



...and with particles in the beam

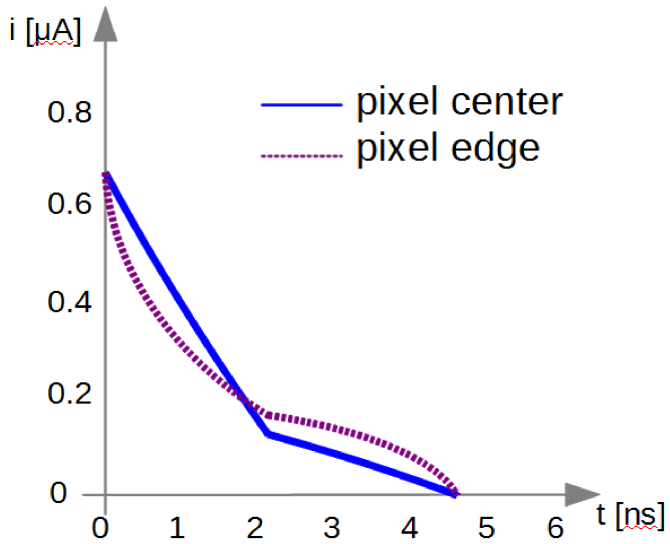


M. Fiorini

Where is the difference?...

Timing with GTK HPD: some results (2)

In the sensor! (and in the physics...)



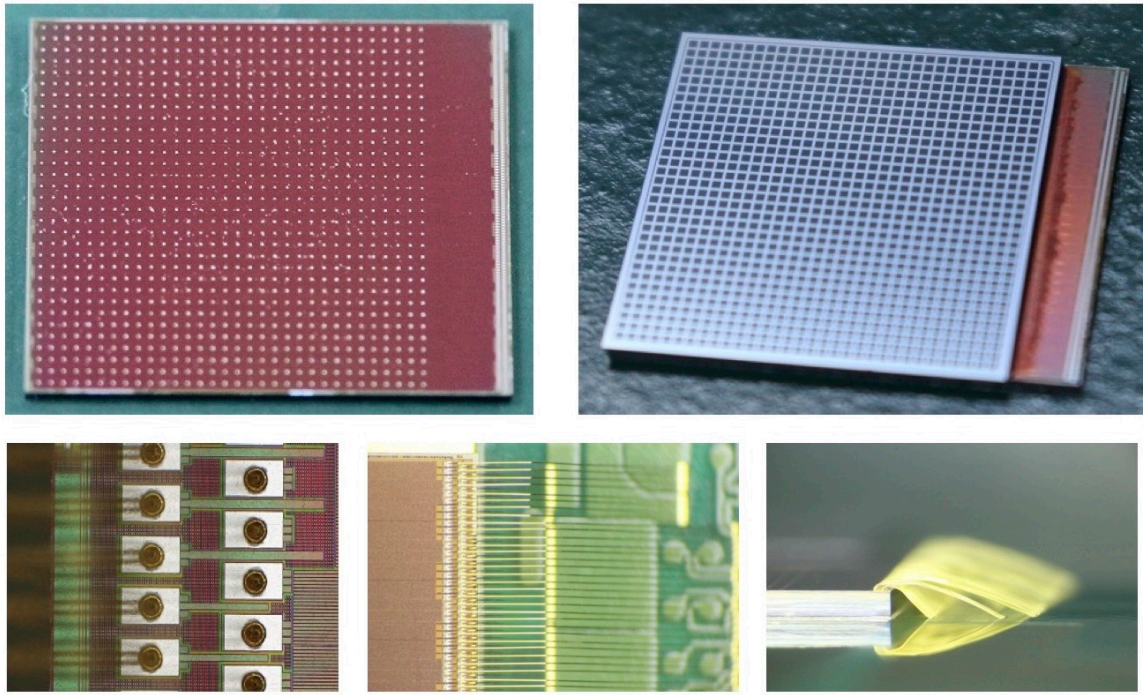
G. Aglieri Rinella

- Weighting field different at the center and at the pixel border
- Particles hitting in different points produce different signal shapes
- This effect has been estimated to contribute about 85 ps
- Charge straggling also contributes $>$ 60 ps

TDCpix references:

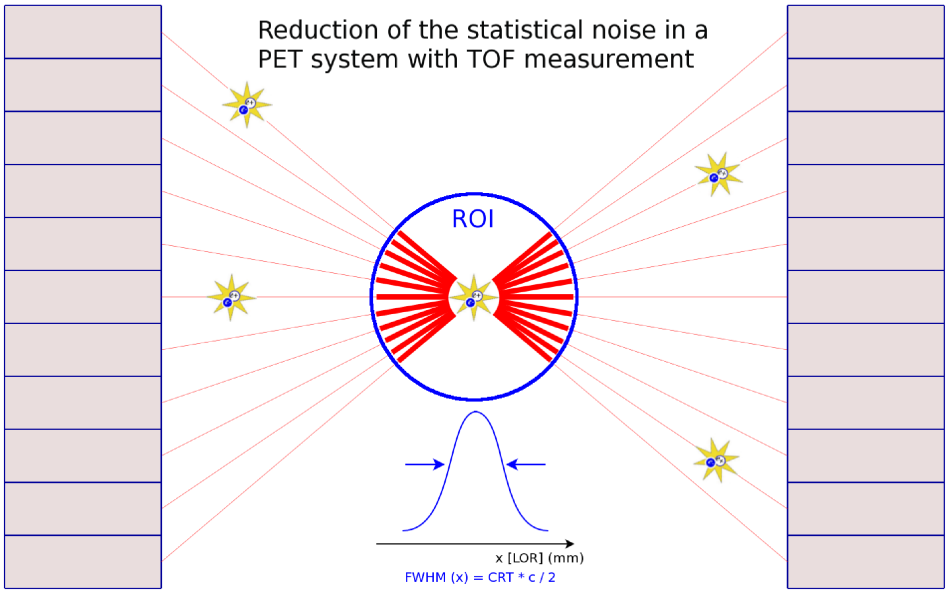
- M. Noy, TDCPix: A High Time Precision Pixel Chip for the NA62 GigaTracker, CERN-PH-ESE Seminar, https://indico.cern.ch/event/302077/
- M. Noy et al.: The TDCPix ASIC: Tracking for the NA62 GigaTracker, TIPP 2014, Proceeding of Science, http:/pos.sissa.it/

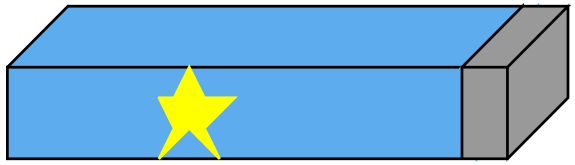
Another timing ASIC for pixels



- Timing front-end ASIC: 1024 channels, 4096 TDC, 20 Gbit/s output bandwitdth
- Technology 110 nm CMOS
- Pixel size 400 μm$\times$400 μm
- TDC binning 20$\div$100 ps, DNL %
- Overall system jitter $\approx$ 30 ps r.m.s.

- Anticipated 50 years ago, but still evolving





- More weight to photons coming from the ROI
- Stronger benefit on larger patients
- Commercial instruments 400 - 500 ps, 300 ps expected soon

$$\Delta x = \Delta t \frac{c}{2}$$

S. Surti, Update on time-of-flight PET imaging, J. Nucl. Med. Jan. 2015; 56 (1); 98-105

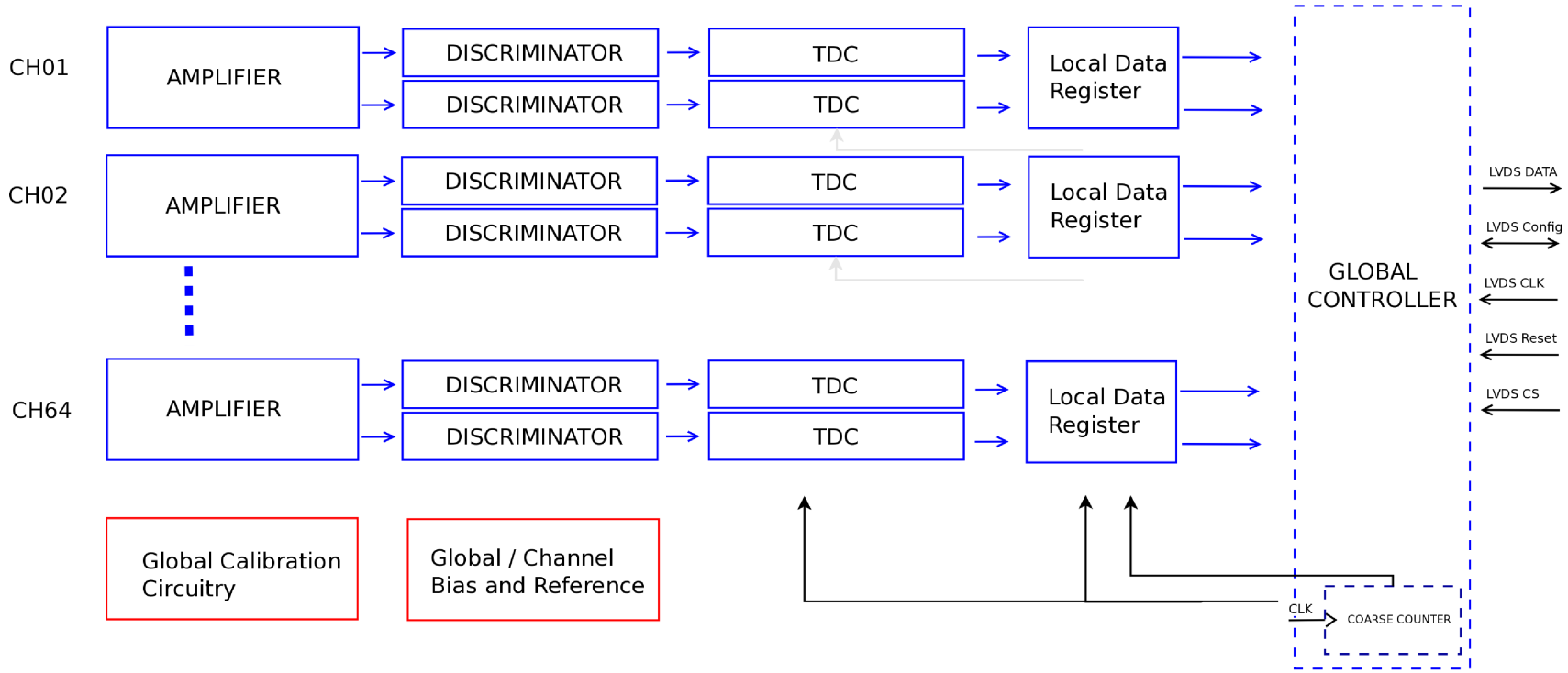
Electronics for SiPM: the TOF-PET

- Chip developed in the framework of the EndoToF-US project
- Sensors: analog SiPM with capacitance in the 75 to 300 pF range

Parameter	Value
Number of channels	64
Clock frequency	$80 - 160$ MHz
Dynamic range of input charge	**300 pC**
SNR ($Q_{in} = 100$ fC)	$>$ 20-25 dB
Amplifier noise (in total jitter)	$<$ 25 ps (FWHM)
TDC time binning	**50 ps**
Coarse gain	G_0, $G_0/2$, $G_0/4$
Max. channel hit rate	100 kHz
Max. output data rate	320 Mb/s (640 w/ DDR)
Channel masking	programmable
SiPM fine gain adjustment	**500 mV (5 bits)**
SiPM	up to 320pF term. cap., 2MHz DCR
Calibration BIST	internal gen. pulse, 6-bit prog. amplitude
Power	**$<$ 10 mW per channel**

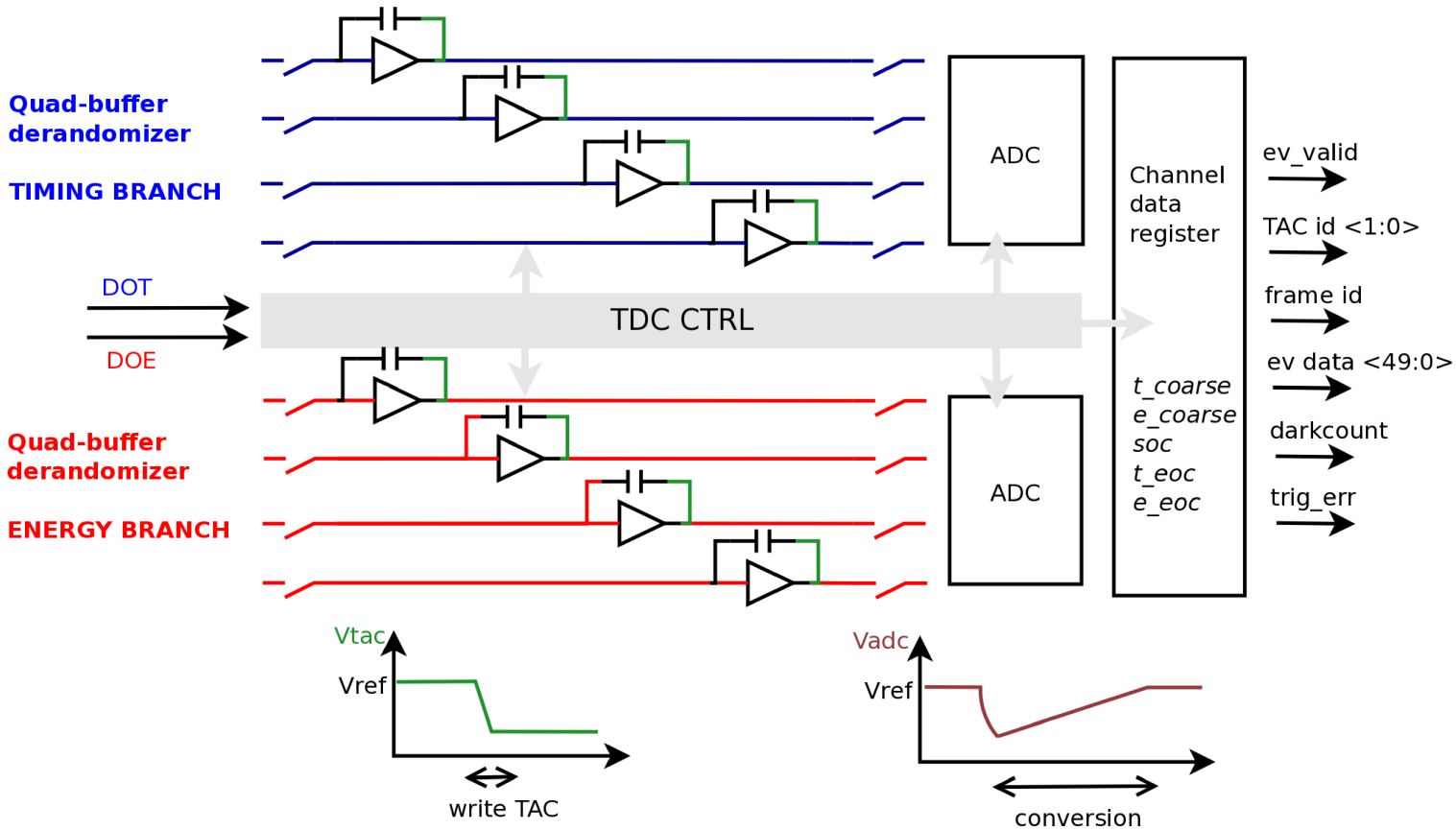
TOFPET architecture

- Charge encoding with Time over Threshold
- Dual treshold system



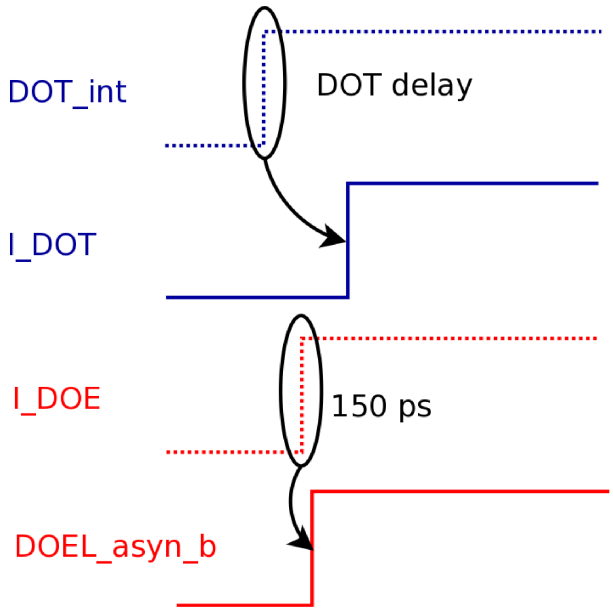
TDC implementation

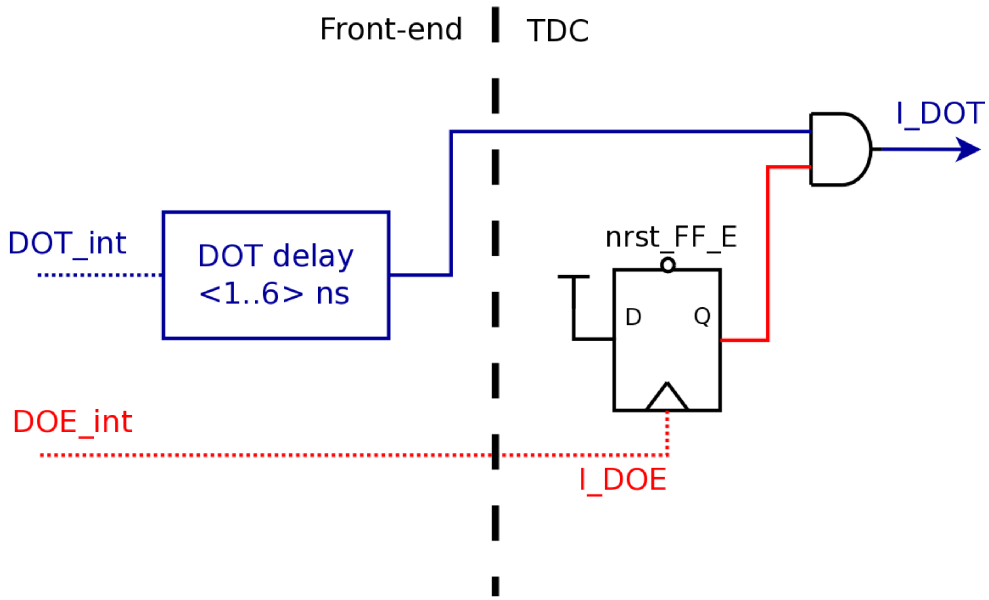
- TDC based on Time to Amplitude Converters
- Four TACs per TDC for derandomization
- Rate capacitance > 300 kHz per channel



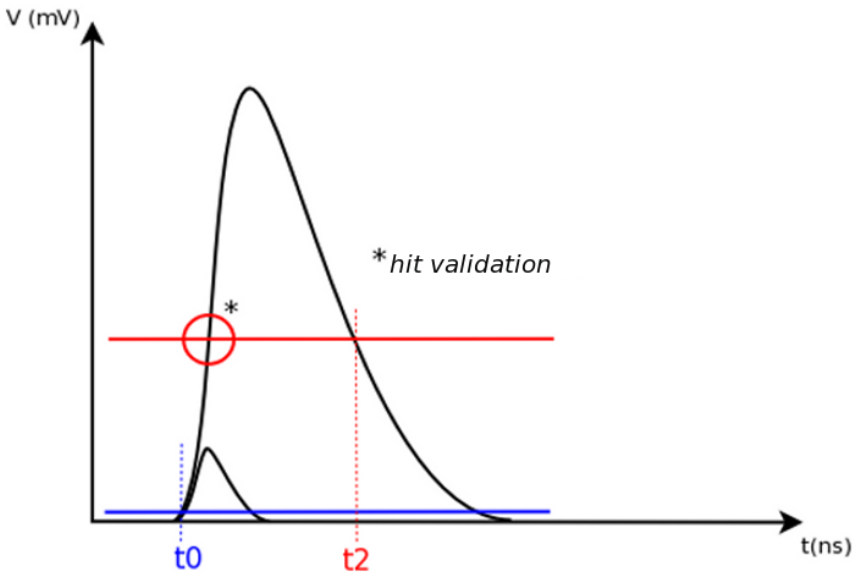
Dark counts management

- Important not to trigger TACs with dark counts
- Timing pulse is delayed and confirmed by energy pulse (higher threshold)



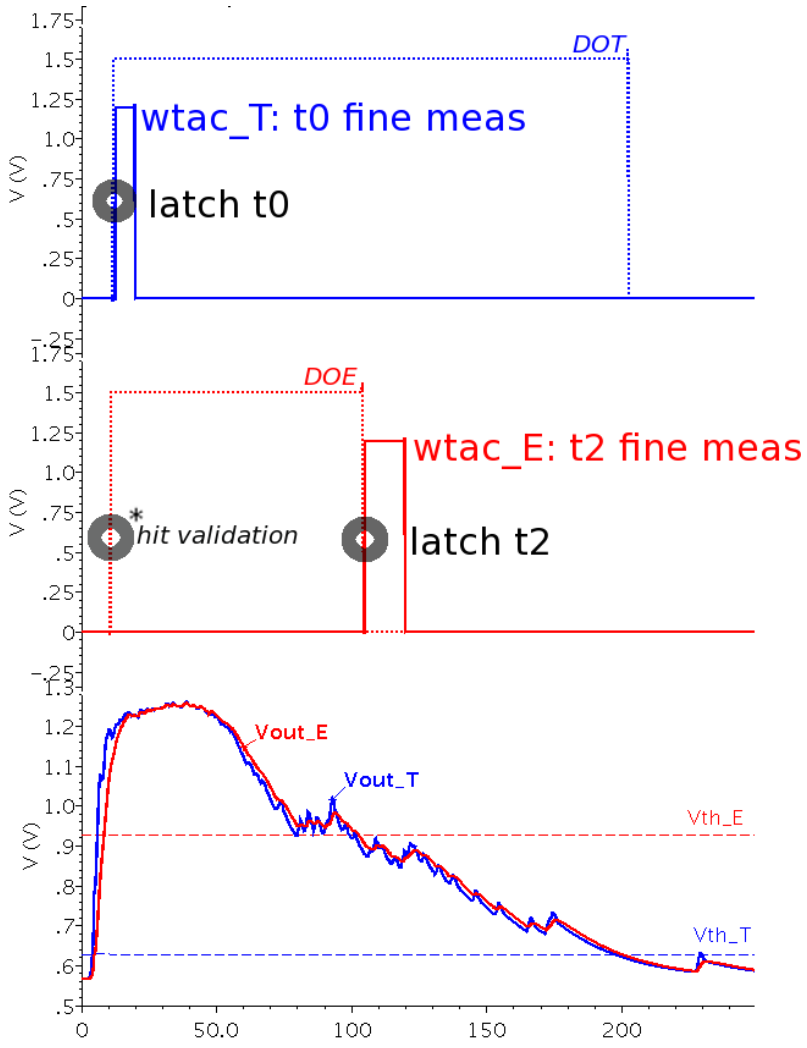


Dual threshold



ToT (energy meas) = t2 - t0

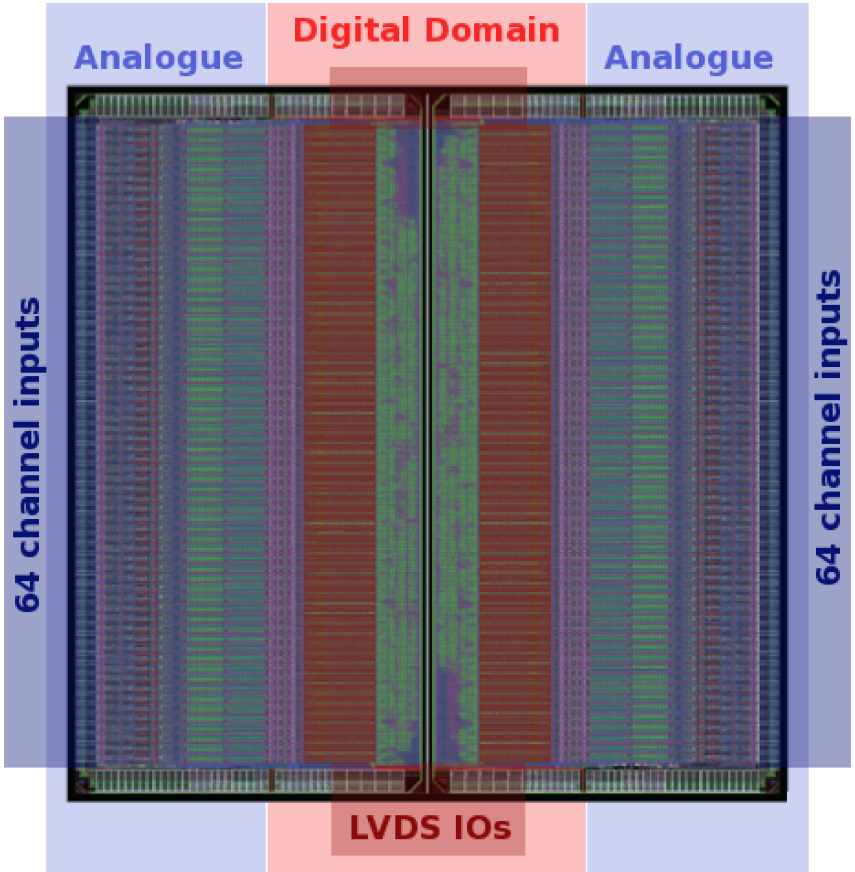
a)

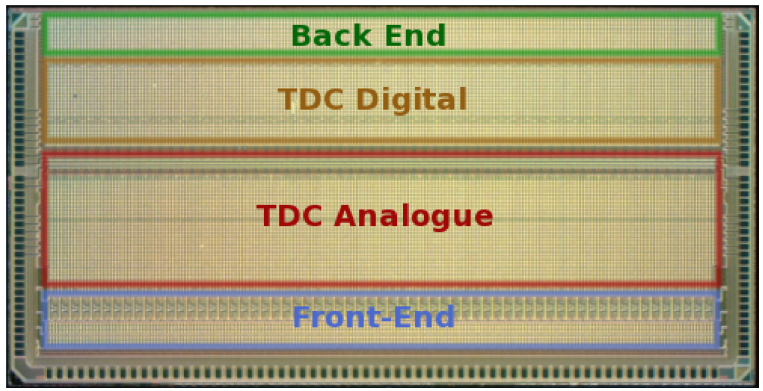


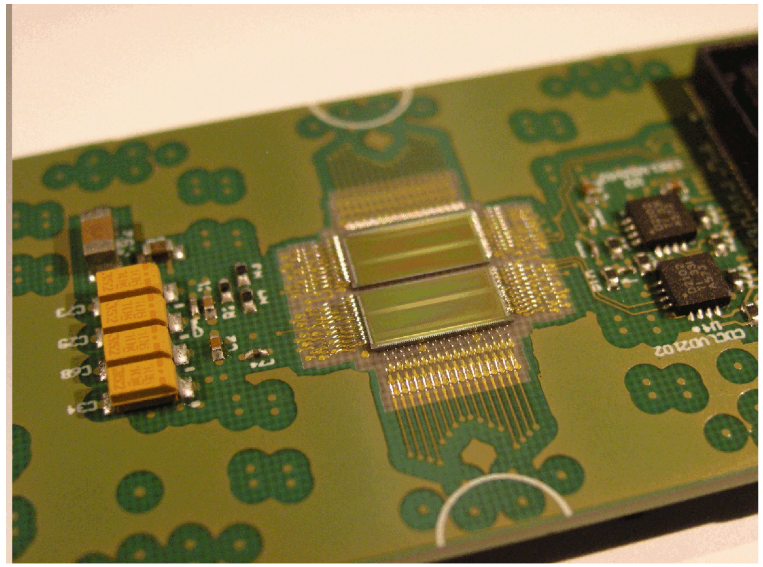
b)

TOFPET in silicon

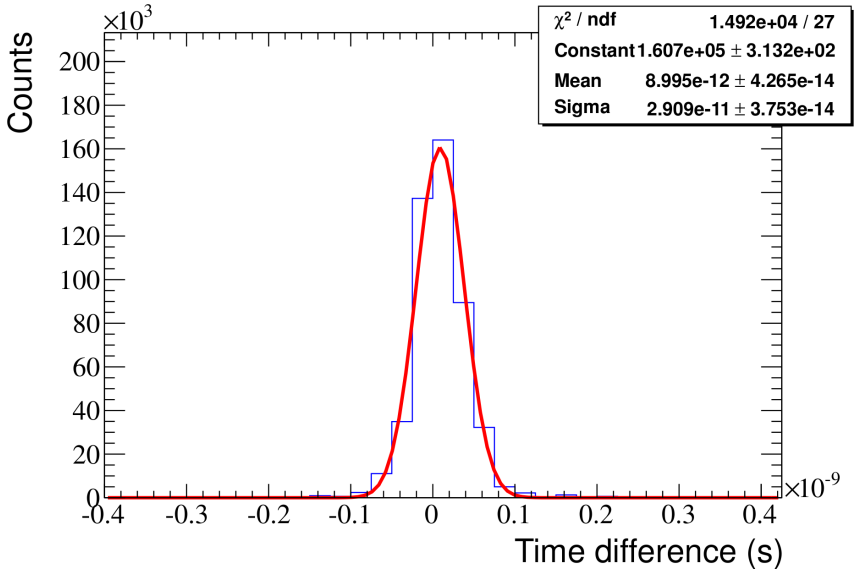
- Two chips can be put side-by-side to get a compact 128 channel system

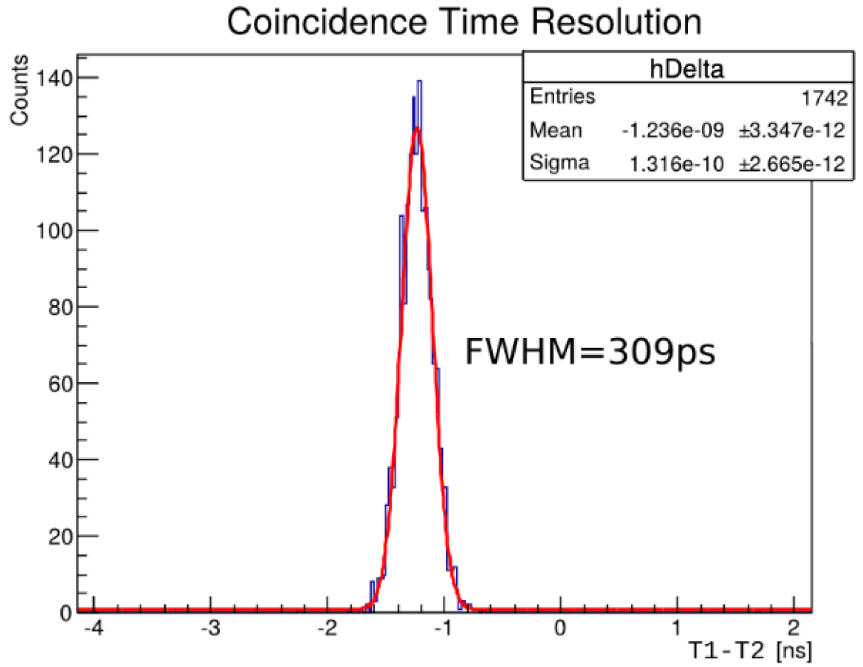






TOFPET performance





TDC resolution $\approx$ 20 ps rms
(with 50 ps bin size)

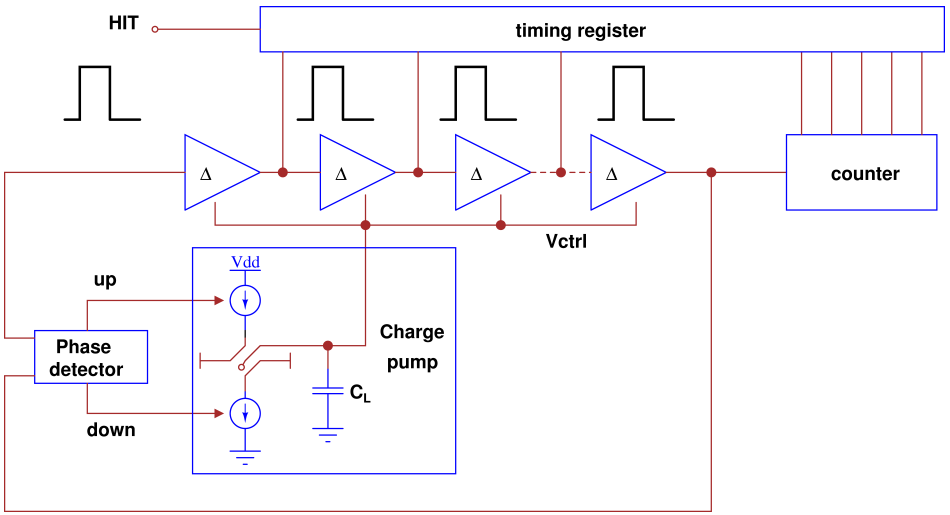
Resolution with crystals and SiPM

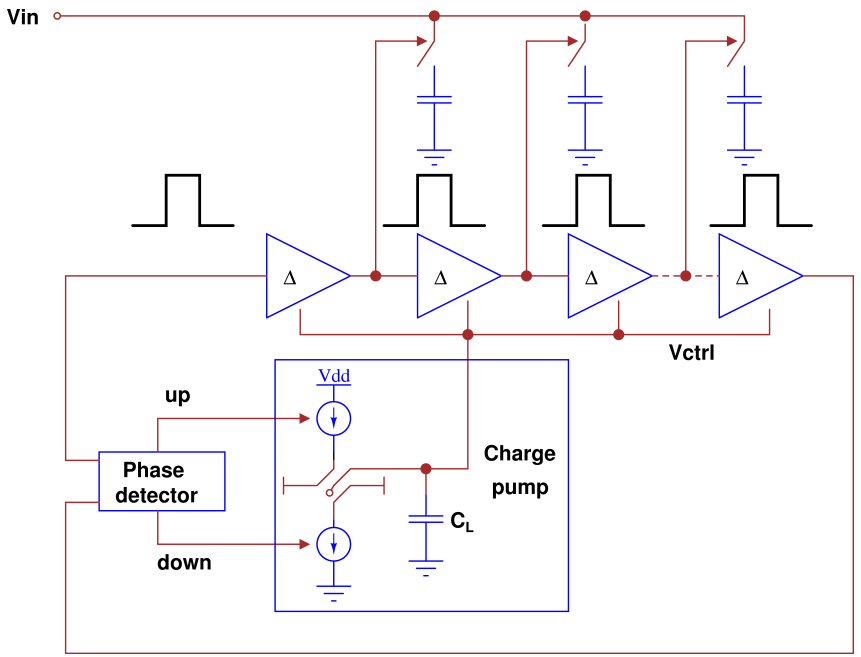
TOF-PET references:

M.D. Rolo et al., TOF-PET ASIC for PET applications, JINST, Vol. 8, Feb. 2013

M.D. Rolo. , Integrated Circuit Design for Time of Flight PET, PhD thesis, Univ. of Torino, 2014

Waveform samplers





- In a TDC, the delayed pulses are captured into registers when the hit arrives
- In a WS, the delayed pulses are used to control the analog storage cells
- Sampling frequency is $1/\Delta$ and can be well above 10 GHz in modern technologies
- In earlier implementations open loop buffers were employed. Today the use of DLL and PLL prevalent (jitter and sampling time uniformity)

Waveform samplers: some example

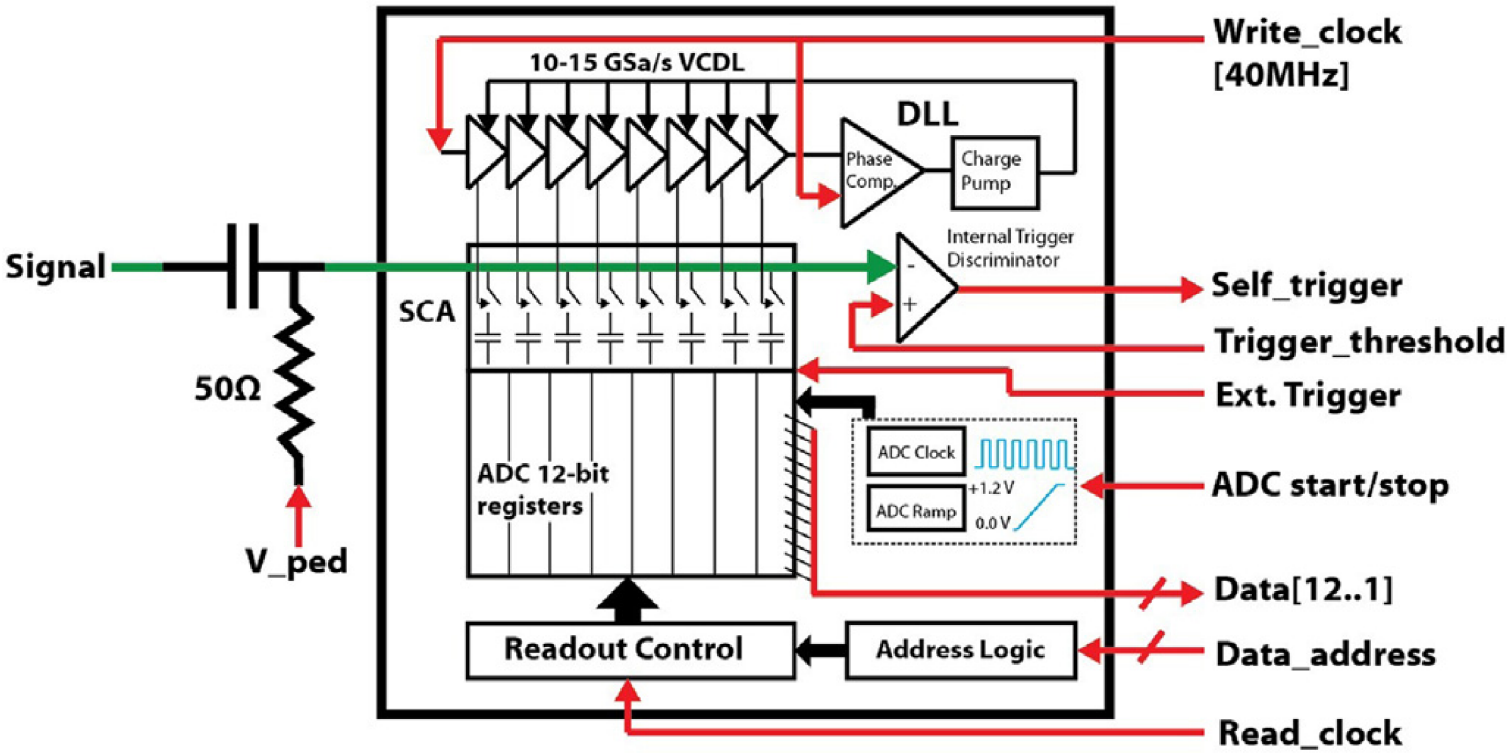
ASIC	Year	Node	Time res.	Max sample/ch.	Channels
LABRADOR3	2005	250 nm	16 ps	260	8
BLAB	2009	250 nm	< 5 ps	65536	1
DRS4	2014	250 nm	≈ 1 ps	1024	8
PSEC4	2014	130 nm	≈ 1 ps	256	6
SamPic	2014	180 nm	$\approx$ 3ps	64	16

- Typical small channel count per ASIC
- Resolution: same pulse split and sent to differnt channels and time difference measured

PSEC4: architecture

E. Oberla et al., A 15 GSa/s, 1.5 GHz bandwidth waveform digitizing ASIC

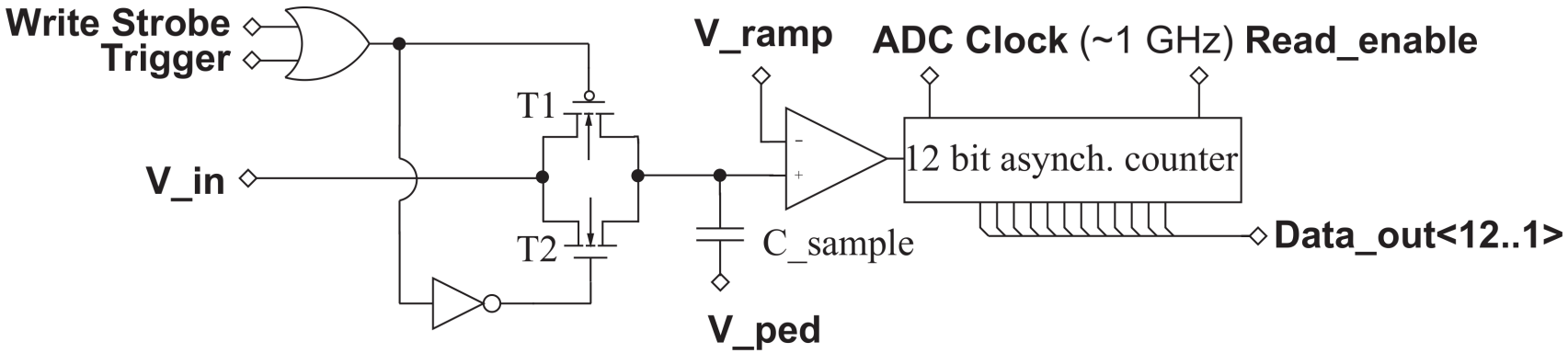
NIM A 735 (2014) 452-461



- Input signal AC coupled (terminations external)
- On chip RF microstrip lines at the input
- DLL with 256 taps fed by a 40 MHz clock

PSEC4: sampling cell

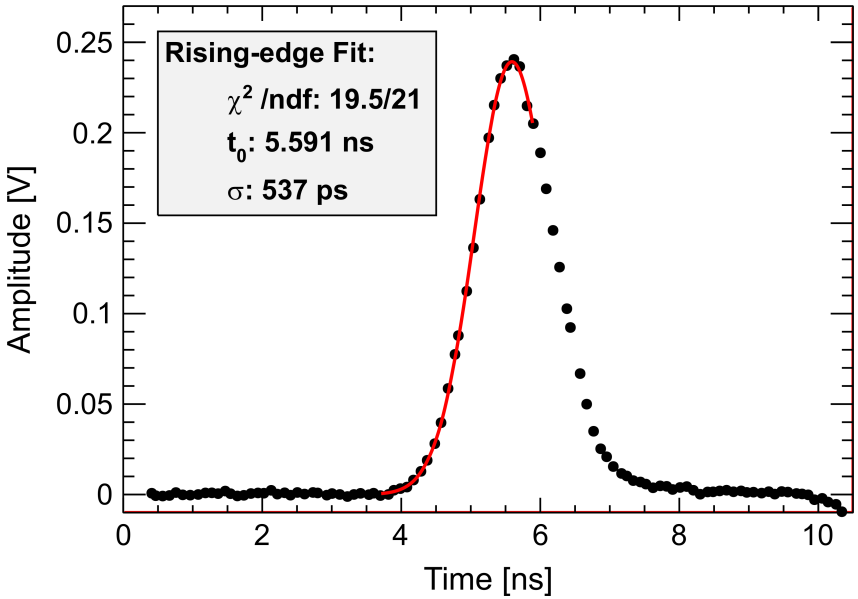
E. Oberla et al., NIM A 735 (2014) 452-461



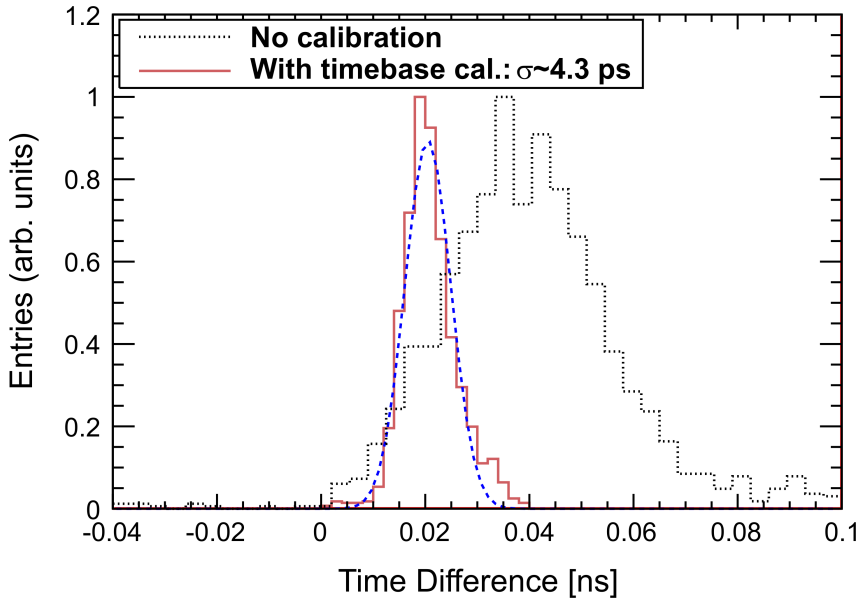
- Small sampling capacitance (20 fF) to guarantee 1.5 GHz analog bandwidth
- A Wilkinson ADC integrated in each cell
- Common ADC ramp generated externally to the cell

PSEC4: performance

E. Oberla et al., NIM A 735 (2014) 452-461



Example of digitized pulse

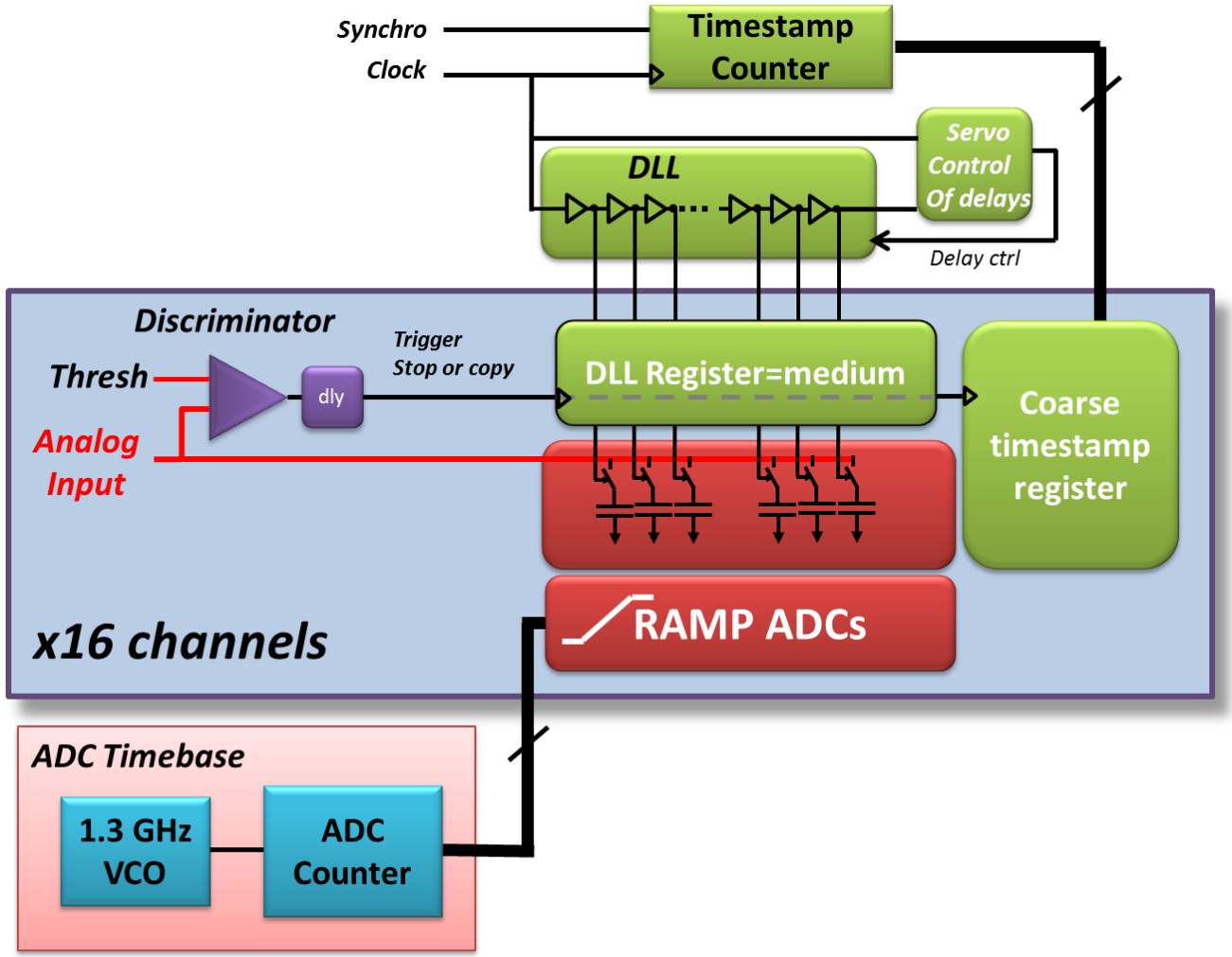


Timing performance

- Time resolution bettern than 5 ps rms obtained after time-base calibration

SAMPIC architecture: merge TDC and WS

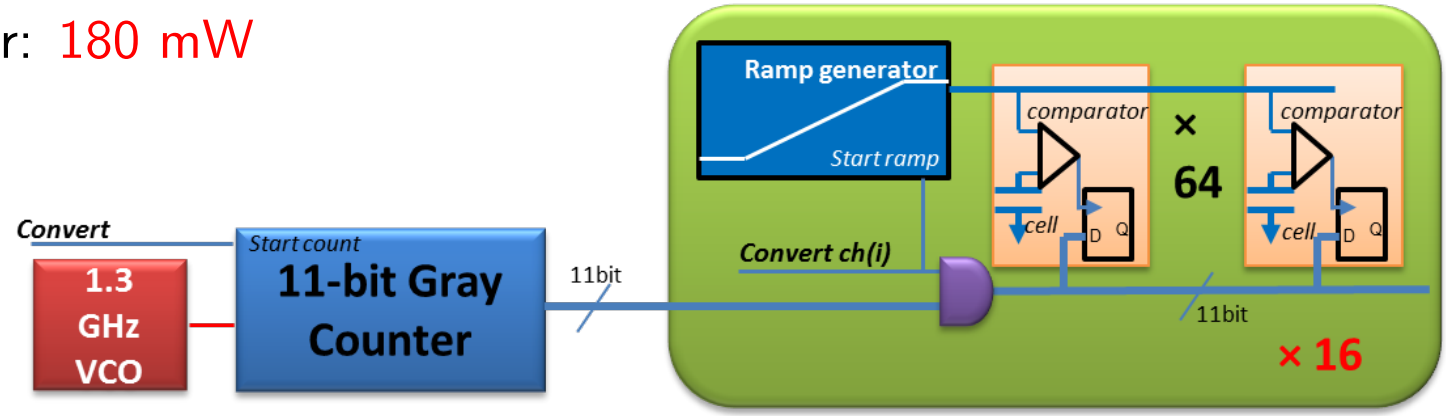
E. Delagnes et al., Reaching a few picosecond timing precision with the 16-channel digitizer and timestamper SAMPIC ASIC NIM A 787 (2015) 245-249



SAMPIC: digitizer

E. Delagnes et al., NIM A 787 (2015) 245-249

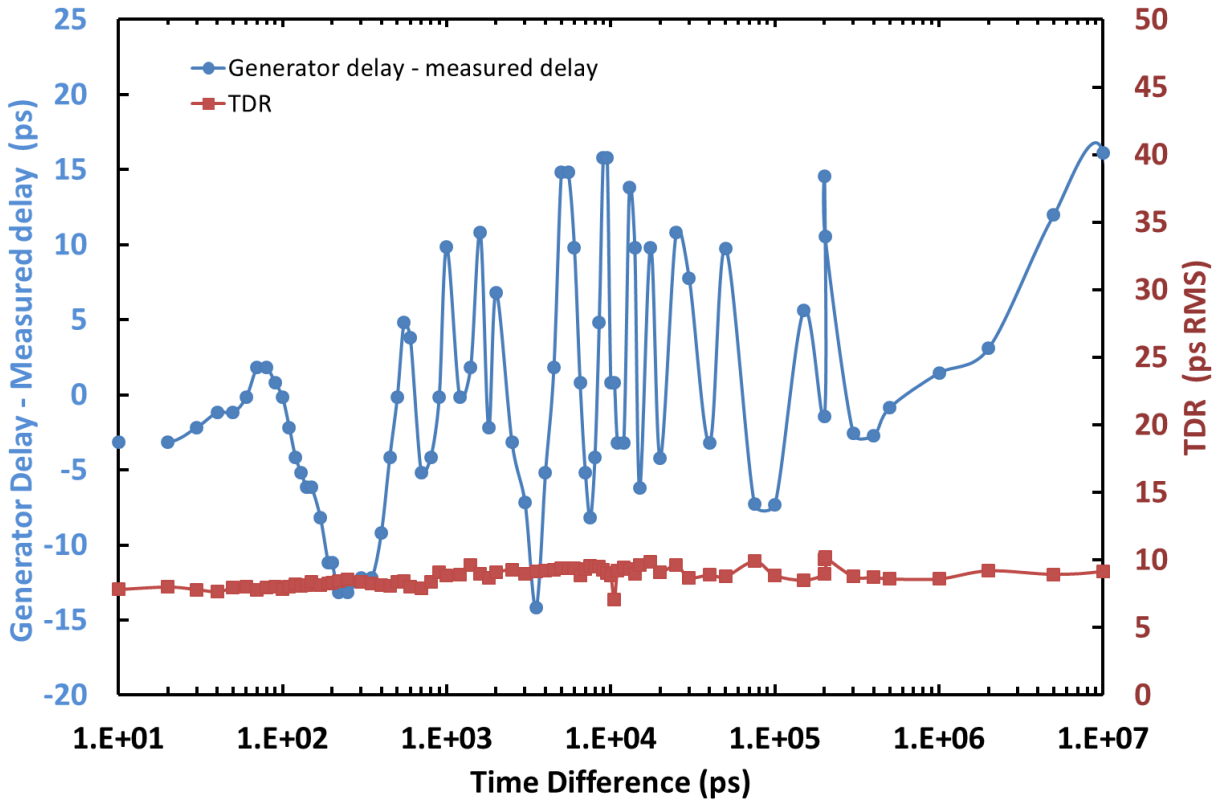
- Technology: AMS 180 nm
- 16 channels per chip
- Power: 180 mW



- Embedded ADC
- Digitization done in parallel for the selected cells
- Dedicated comparator for every cell
- Common Gray counter driven by a 1.3 GHz VCO

SAMPIC: timing performance

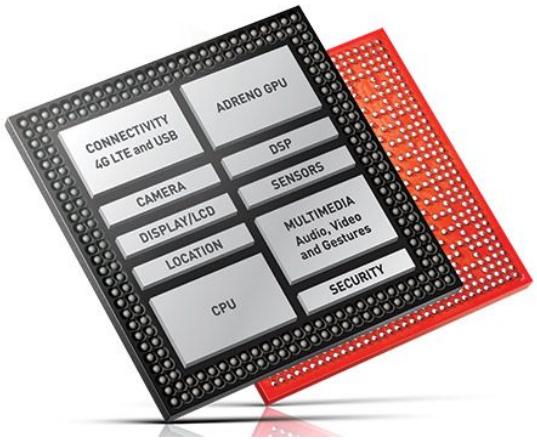
E. Delagnes et al., NIM A 787 (2015) 245-249



- Time resolution:
  - < 20 ps without time-base correction
  - $< 5ps$ with time based correction
  - 10 ps TDR achieved over 10 μs difference between pulses

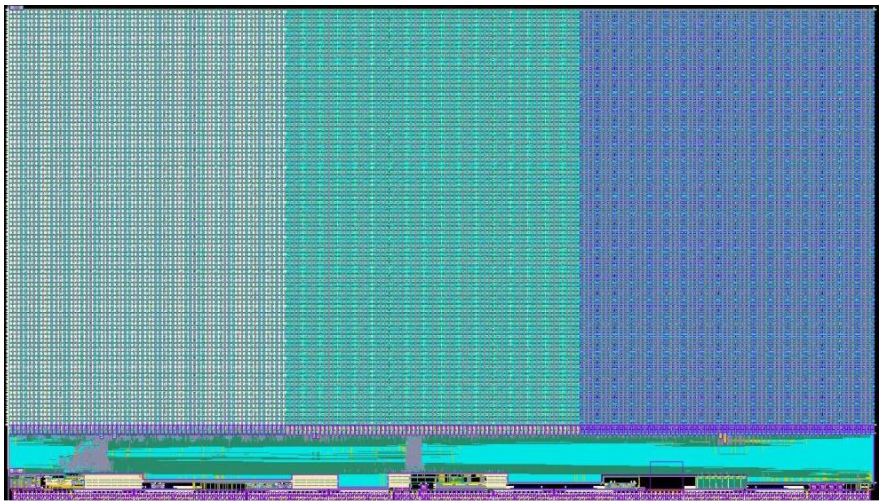
Systems on chip

- SoC for mobile



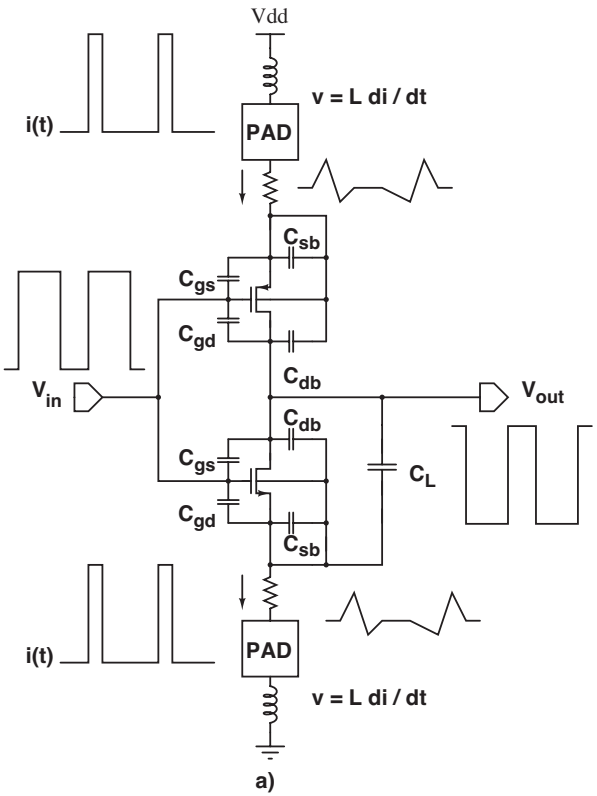
- Different functions implemented in selected areas

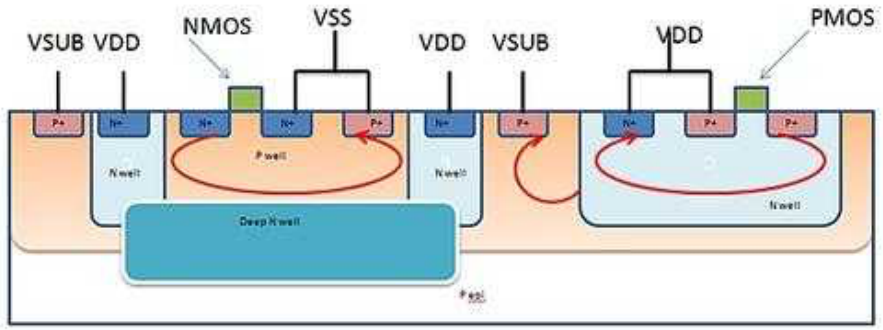
- ASIC for hybrid pixel detectors (RD53A prototype for ATLAS/CMS upgrades)

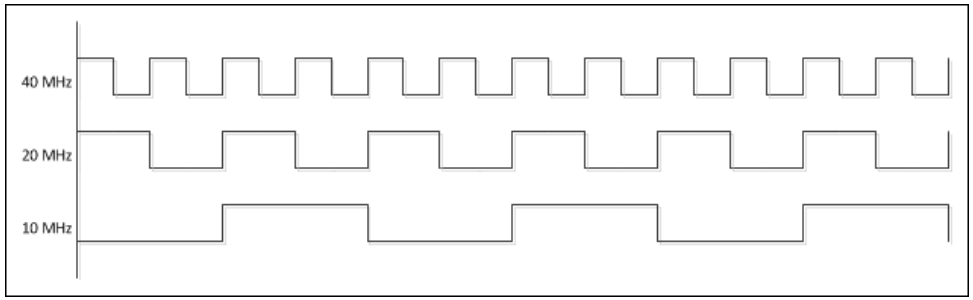


- About 80.000 pixels of 50 μm$\times$50 μm in 65 nm

Mixed-signal noise-1

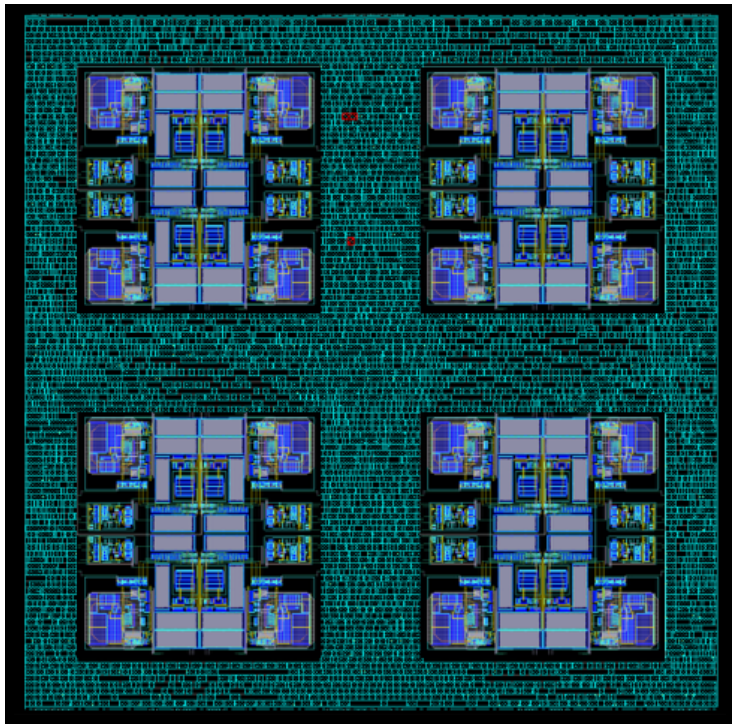






Mixed-signal noise-2

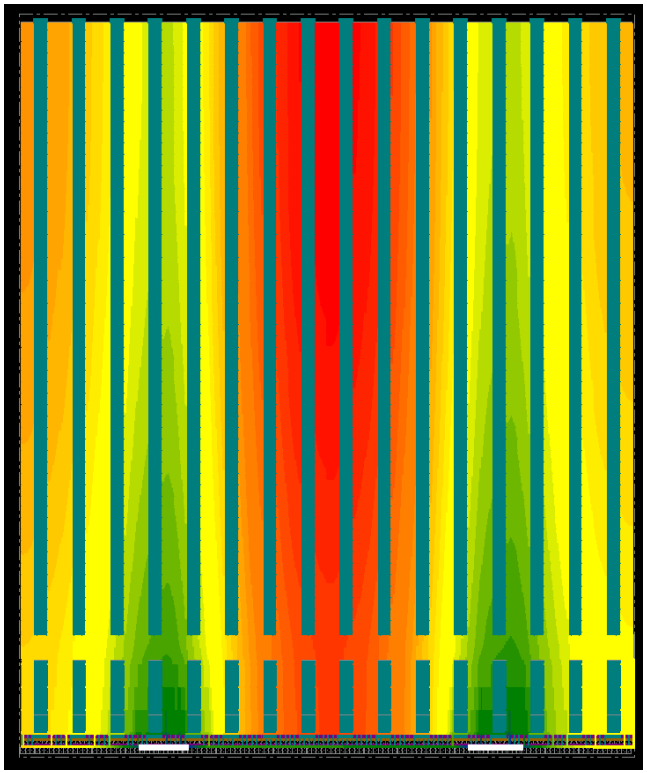
- Analog islands surrounded by digital gates

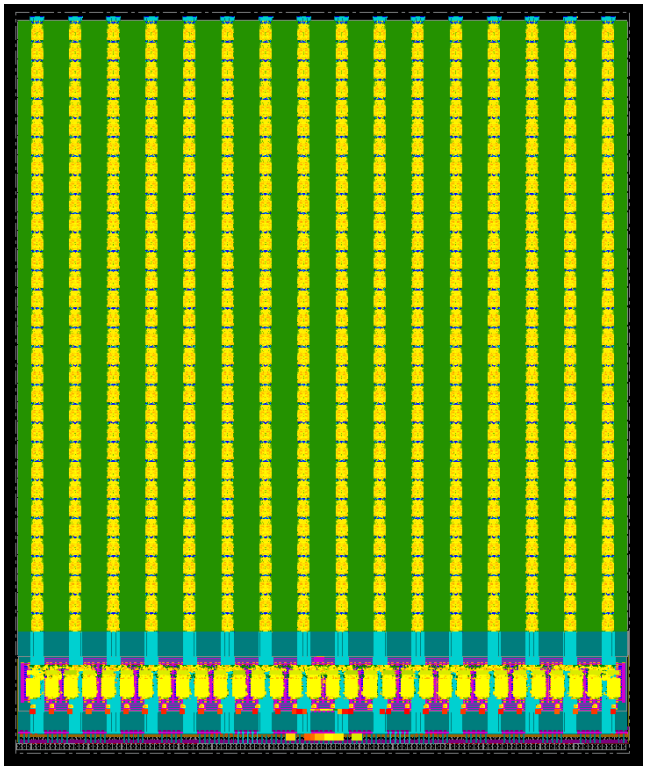


- Most of a typical front-end ASIC is digital
- Low-noise analog and high speed digital can coexist
- Several isolations features offered by modern technologies
- ...but one has to be very careful!

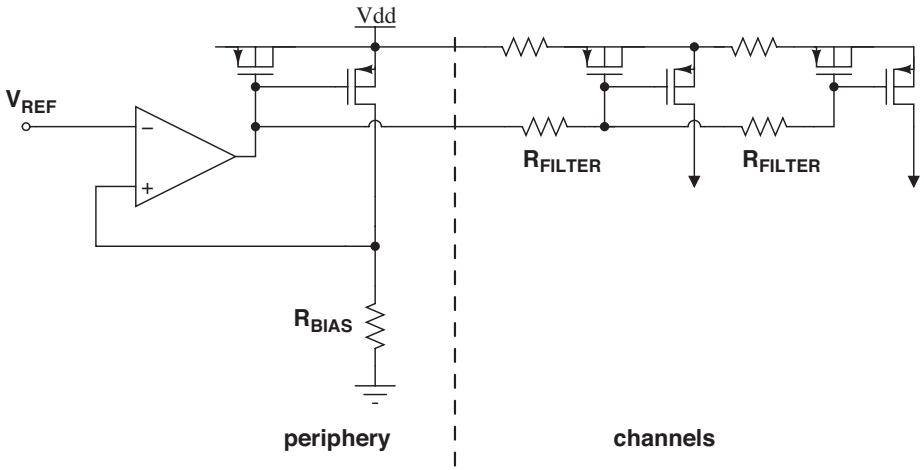
IR drops and PSRR

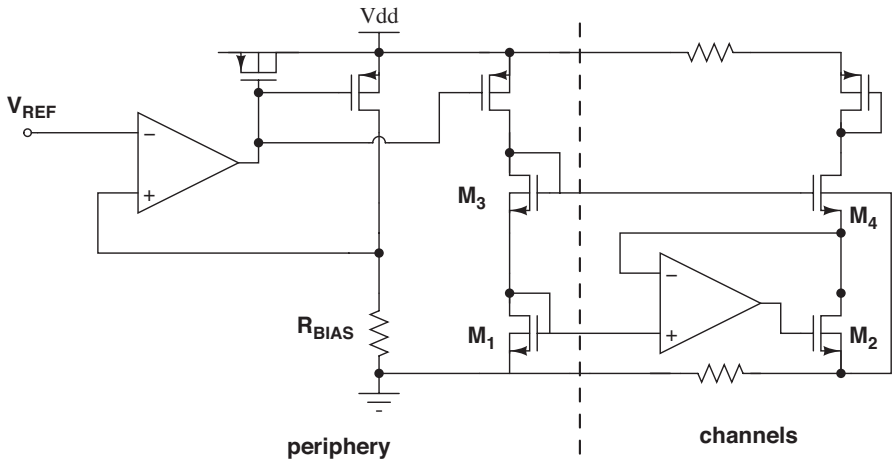
- Chip size $\approx$ 1.2 cm $\times$ 1.8 cm

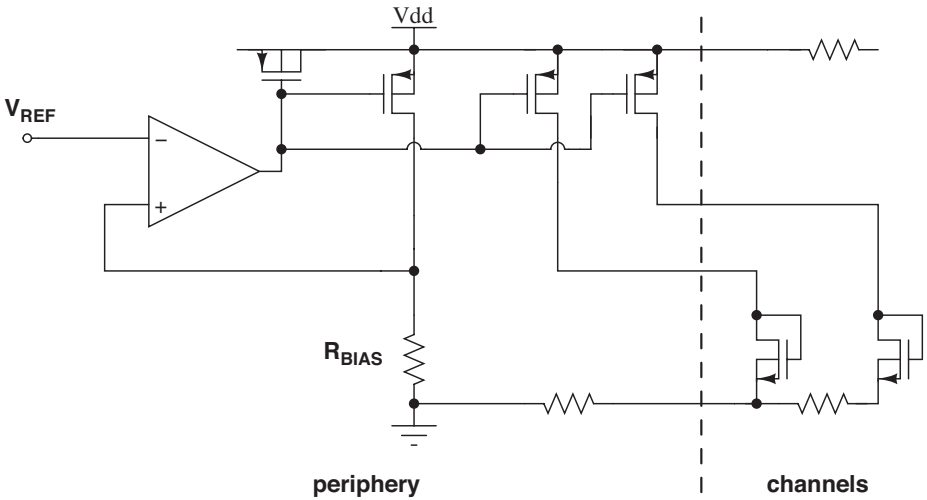




Robust biasing

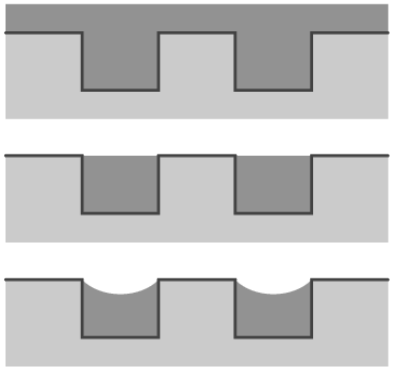


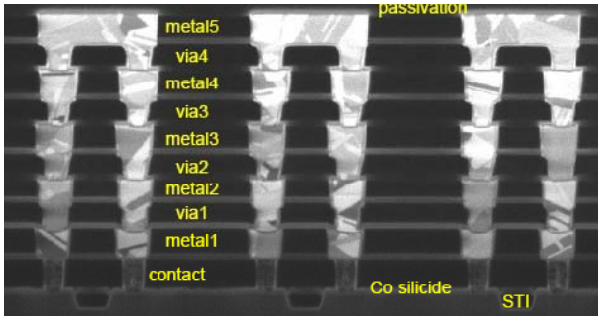


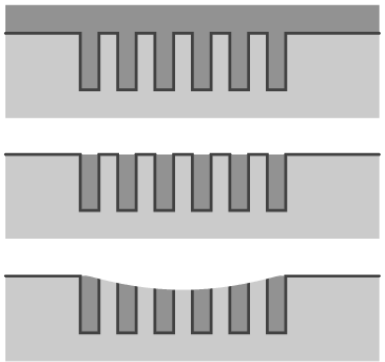


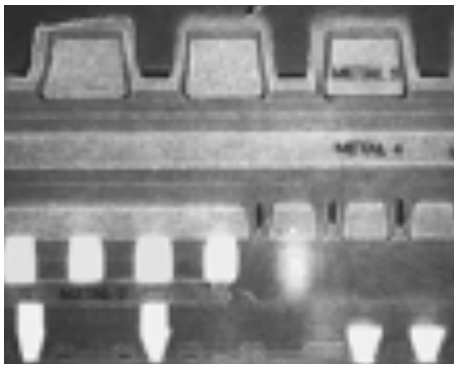
- Uniform bias among channels is a critical issue in large chips
- One of the most common failure reason in large IC
- Must be taken into consideration in early design phase

Pattern density



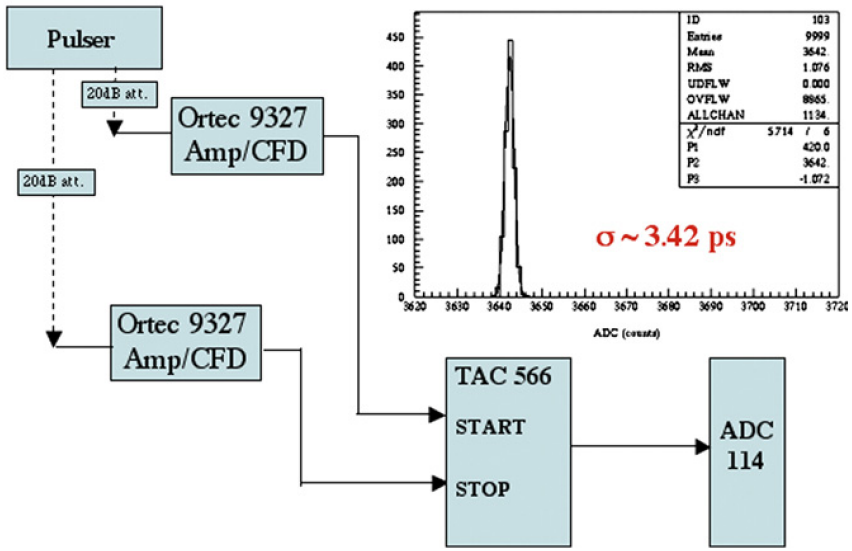


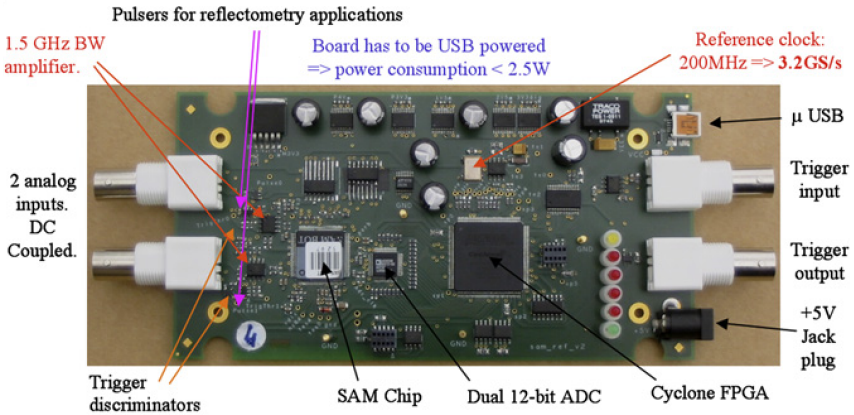


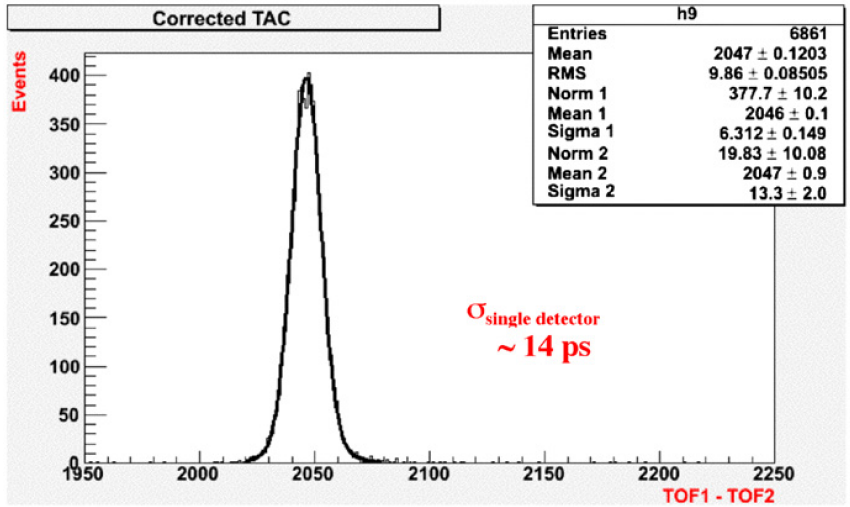


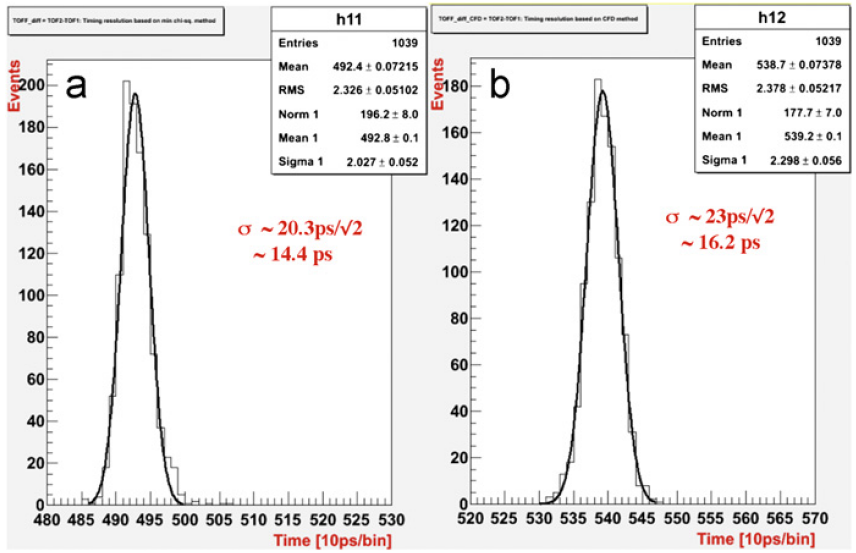
An interesting comparison

D. Breton et al., NIM A 629 (2011) 123-132









To summarize

- Increasing number of applications for timing detectors
- Comparable performance with TDC and waveform sampling
- Trends:
  - Higher integration density
  - Better time resolution (targeting 10 ps and below)
- TDC already achieve 1 ps resolution
- Electronics resolution of waveform samplers comparable
- The key is at the interplay between the sensor and the very front-end
- ...but it's not only the front-end!
- State-of-the-art ASIC for timing are fairly complex SoCs
- Beware of systems aspects
- Take your time to design them!

Thank you!