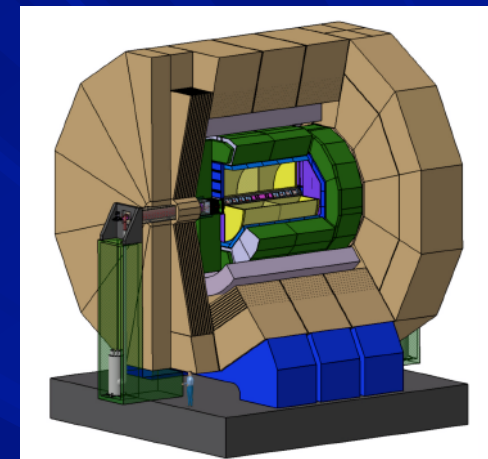
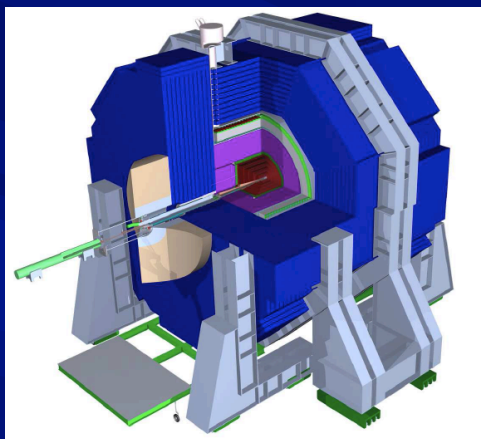


Introduction to TDAQ



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Fast Electronics and Detector Summer School,
SDU/Weihai, China, Aug. 2018

Thanks to Prof. Patrick Le Du for sharing slides

Weihai FEDSS

Questions

- How many people know TDAQ?
- How many people know Trigger?
- How many people know DAQ?
- What is trigger?
- What is DAQ?

Trigger/触发

■ WIKI:

- trigger - lever that activates the firing mechanism of a gun

■ Bing:

- a small device that releases a spring or catch and so sets off a mechanism, especially in order to fire a gun:



Trigger



Triggering: Find & Capture Signal of Interest Powerful Measurement Leverage

Easy, Effective Ways to Monitor Environment for Signal

Look for Expected and Unexpected Signals

Avoid Measuring When No Signal Present

Monitor Other Frequency Bands?

Trigger on Other Activities

- External trigger from your circuit
- Oscilloscope or logic analyzer
- Consider all you know about signals, systems, transitions
- Take advantage of repeating signals, inter-signal timing, pos/neg delays

Triggering Can Enhance Measurement Performance

- Time or synchronous averaging
- Periodic trigger

Trigger a Time Capture

■ Oscilloscope Trigger

- The trigger level and trigger slope are the two basic trigger controls on any oscilloscope whether digital or analogue. The trigger level detects when a certain voltage level has been reached and at this point sets the time-base in operation to sweep across the screen.
- 触发电平: 被选定信号的幅度大于该电平时, 被测信号的波形被抓取并显示在屏幕上。

■ Digital Signal Analyzer

- Triggering: Find & capture Signal of Interest (see left)
- 触发模式: 被选定串行信号满足一定的模式结构时, 被测信号的结构被抓取并被显示在屏幕上。

What is DAQ

■ Wikipedia: Data Acquisition

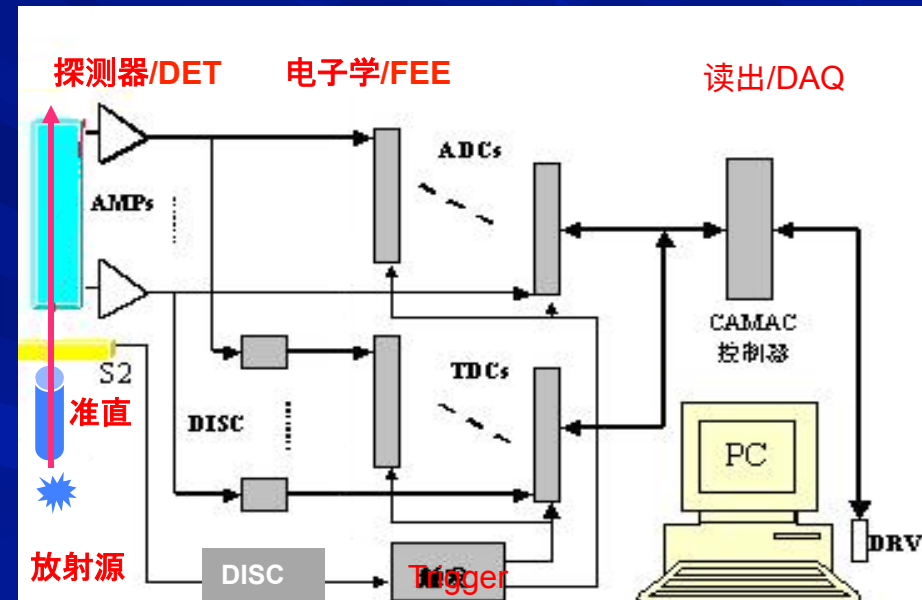
- Data acquisition is the process of sampling signals that measure real world physical conditions and converting the resulting samples into digital numeric values that can be manipulated by a computer. Data acquisition systems, abbreviated by the acronyms DAS or DAQ, typically convert analog waveforms into digital values for processing.

■ BING: What is DAQ?

- DAQ is a broad term that includes a suite of different tools and technologies that are designed to accumulate data. DAQ systems generally consist of DAQ software and hardware along with sensors and actuators, and they generally require underlying network support for data communication between the data acquisition hardware and software.

Trigger/DAQ in Lab Exercise

- Radiation Source based
 - Radiation Intensity
 - Signal Amplitude
 - Discriminator Threshold
- Trigger
 - Providing Gate signal to ADC
 - Providing Common Start to TDC
- DAQ
 - Read data from ADC/TDC
 - Save onto the disk

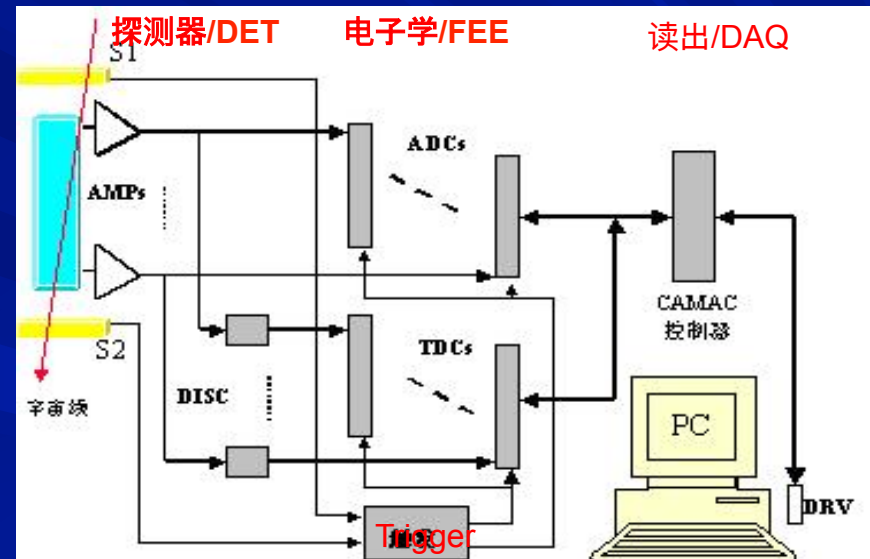


Outlook of this talk: T/DAQ: Evolution of architectures, tools and techniques

- Basic about Trigger and DAQ
 - Common terms, T/DAQ in physics
 - Example with BESIII/BEPC
- Technologie for future experiments
 - LHC upgrade
 - FAIR-PANDA
 - ILC/FCC/CEPC
 - CEPC/SppC
 - What next in TDAQ
 - the 'Ultimate' Trigger concept → The Software trigger
- Summary

Cosmic Ray based Physics Experiment

- Lab Exercise with Cosmic Ray
 - 2 trigger detectors
 - Coverage of the detector volume under checking
- Can this setup search for J /Psi Resonance?
 - Why?
 - Particle ID
 - Efficiency
- Solution
 - Complex system
 - Accelerator based



Must: Accelerator based Spectrometer!

Accelerator based Experiment

■ Advantages

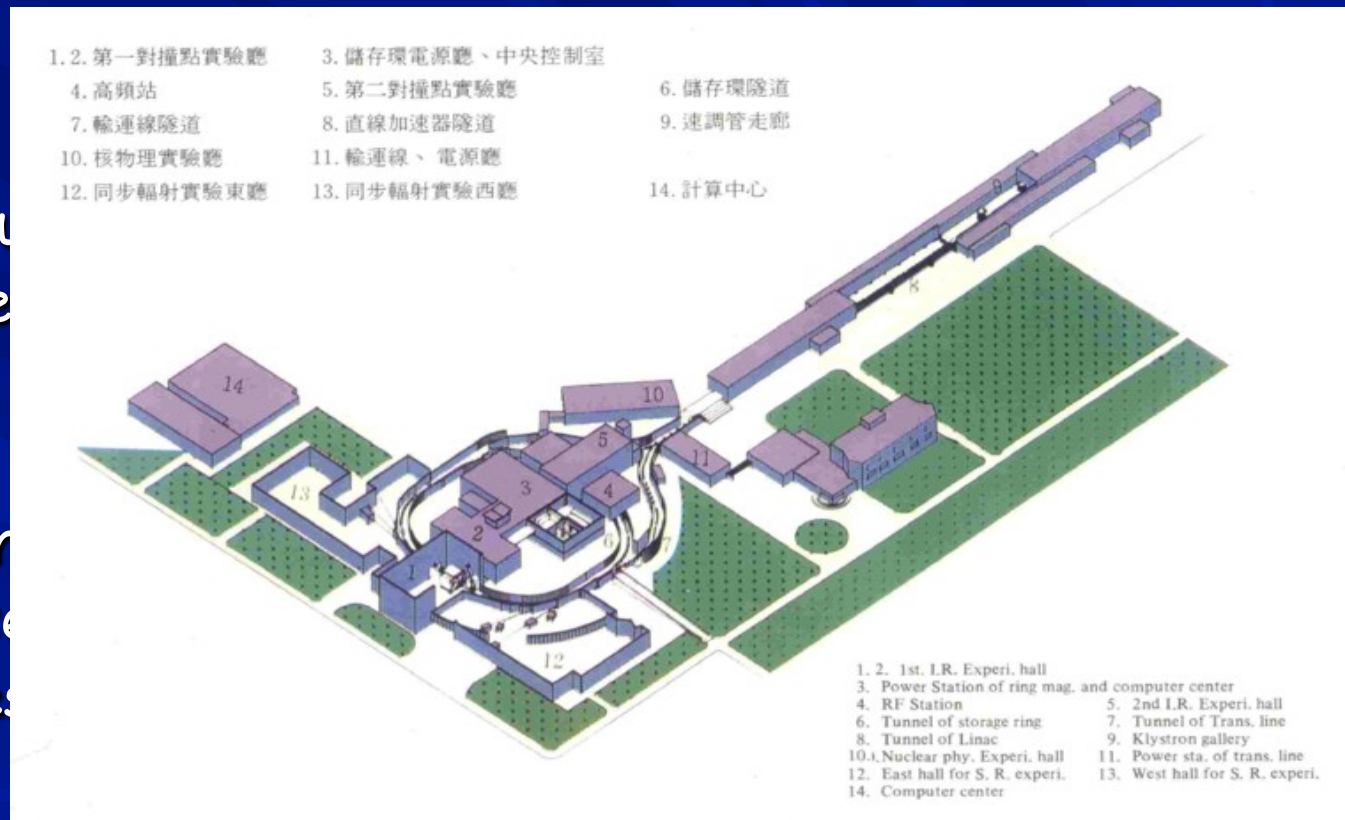
- Energy for Physics interested
- Repeatable
- High efficiency
- Short time for results
- Target controllable

■ Disadvantage

- High background
- Too many fake events
- Tremendous data sets
- Analysis difficulties

■ Solution

- Complex trigger + DAQ

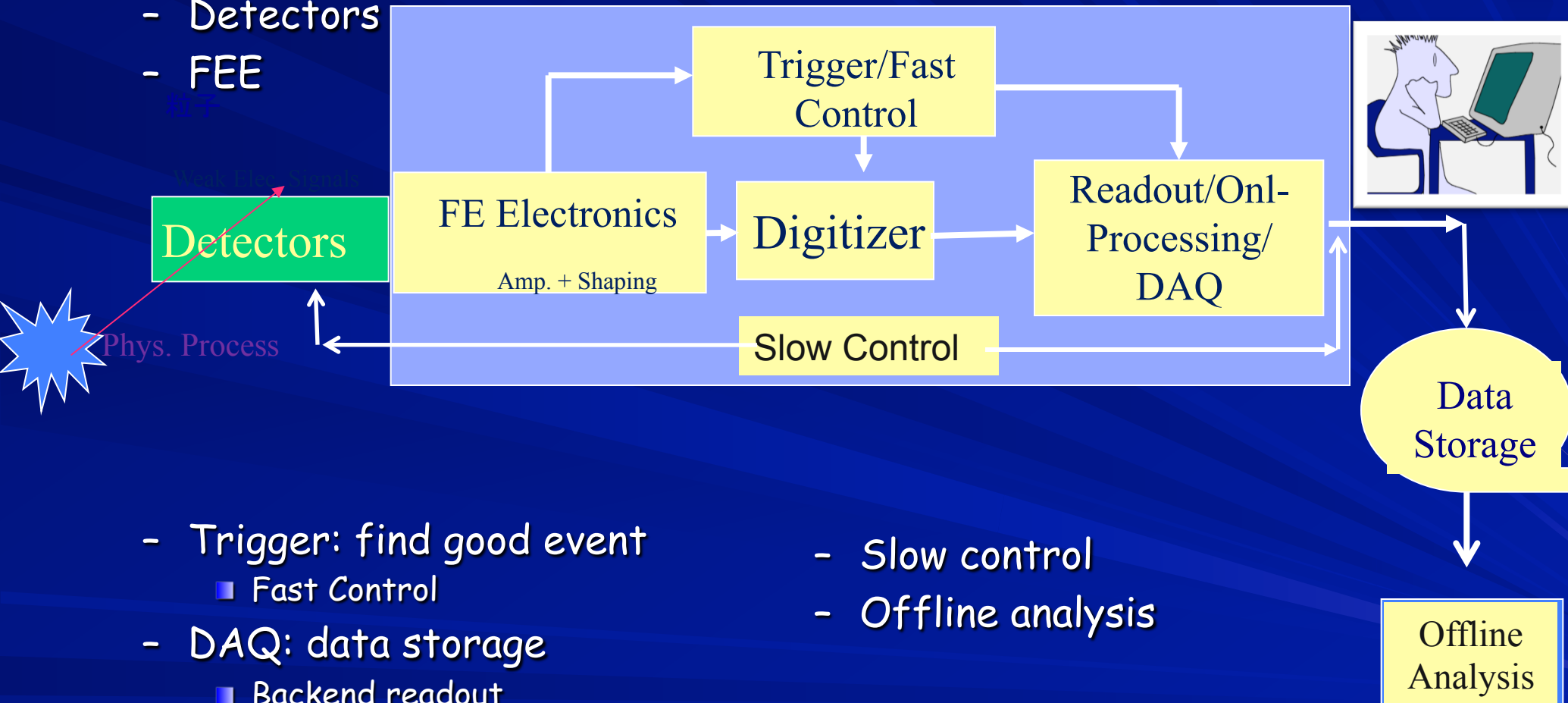


Good Event: find a needle in a Haystack

Trigger+DAQ in Large Physics Experiments

■ Components of Experiment(Spectrometer)

- Detectors
- FEE



- Trigger: find good event
 - Fast Control
- DAQ: data storage
 - Backend readout
 - Online Monitoring

- Slow control
- Offline analysis

Terms, ideas, principles in trigger and DAQ

Target of a Trigger+DAQ system design:

To accept **all** physics event interested (good event), no or fractional loss

To reject as many as possible sorts of backgrounds to the capacity of DAQ to process and save

Small dead time (in some percentages)

■ Good event

- Any event interested in
 - From collision
 - Cosmic ray
- Defined by the experiment
 - BahBah events
 - Cosmic ray events

■ Backgrounds (bad Event)

- Any event not the experiment expecting
- Cosmic ray
- Lost beam particles (unfocused, de-accelerated, Toucheck effect)

■ Trigger Latency

- Time from event produced until trigger decision is made

Trigger Principle

- By timing
 - Time of flight, TOF
- Number of hitting: TOF, muon
- Tracking
 - Charged particle: DC, TPC, Silicon, muon, ...
- Energy
 - Charged particle: EMC, Hcal
 - Neutral particle: EMC
- Corelation
 - Tracks, Clusters, JETs, ...
- more

Multilevels trigger and DAQ

➤ Required rejection is orders of magnitude

➤ **Level 1 is hardware based**

- Hardwired trigger system to make trigger decision with short latency.
- Constant latency buffers in the front-ends
- Crude signatures (hits and tracks, local energy deposit over threshold...)
- Operates on reduced or coarse detector data

➤ **Level 2 is a composite**

- Dedicated custom/DSP/FPGA processing or Processor based (standard CPU's or FIFO buffers with each event getting accept/reject in sequential order)

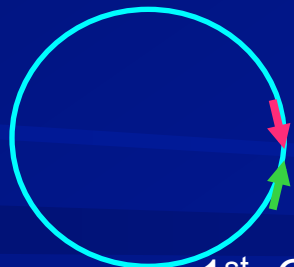
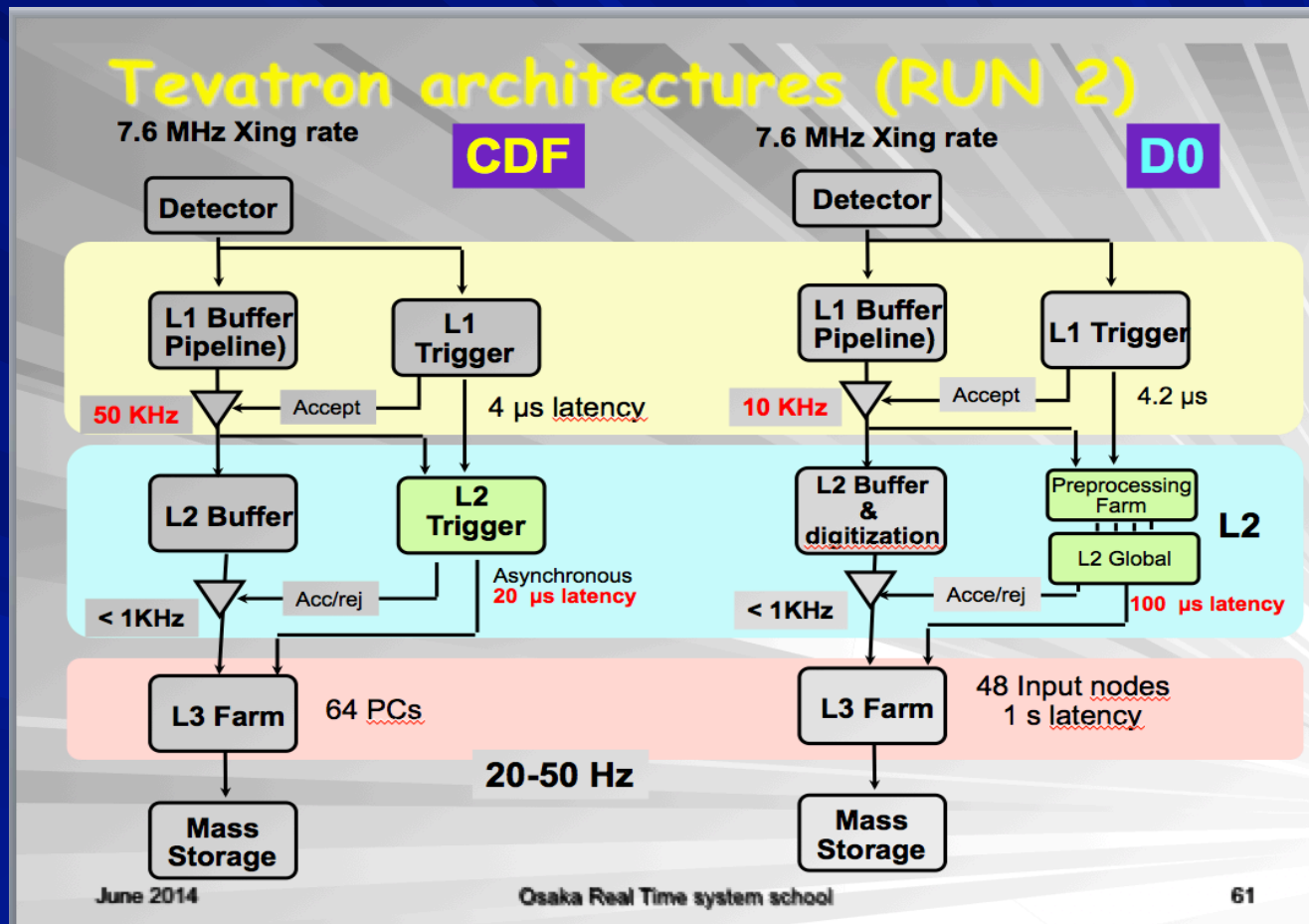
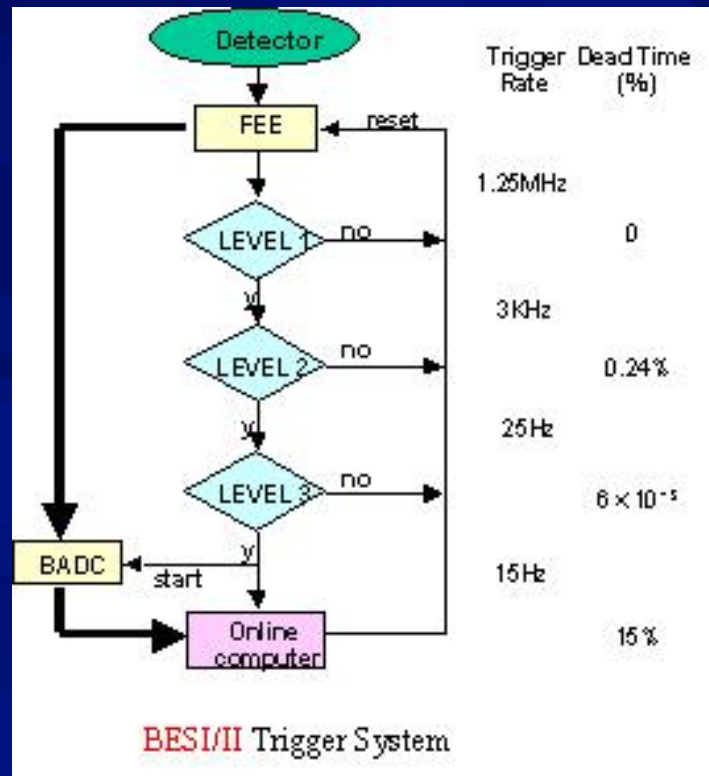
Level 3 is a farm → General Purpose CPUs
hundreds - thousands

Almost every one uses this scheme.

Weihai FEDSS



Pipelined processing vs Latch-Process



1st Cycle

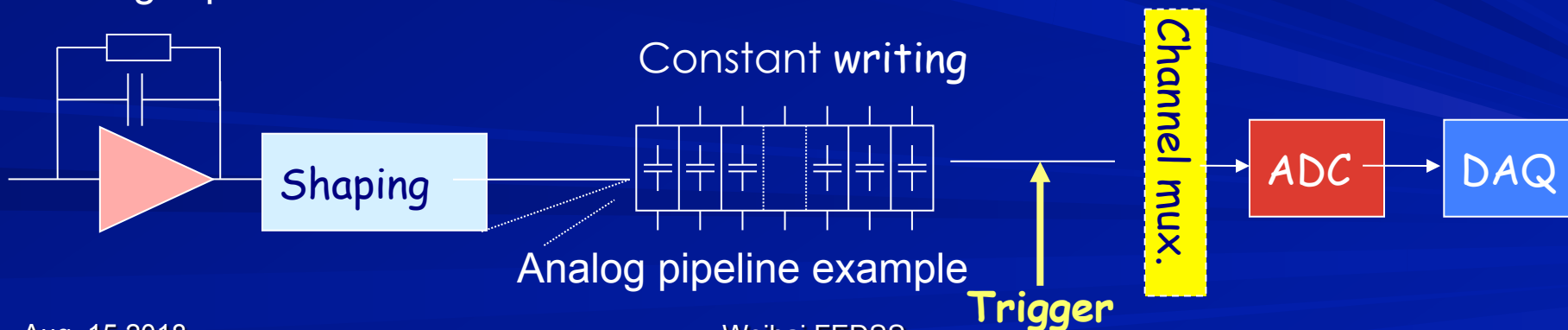
2nd Cycle

3rd Cycle

Terminology :buffer , pipeline & latency

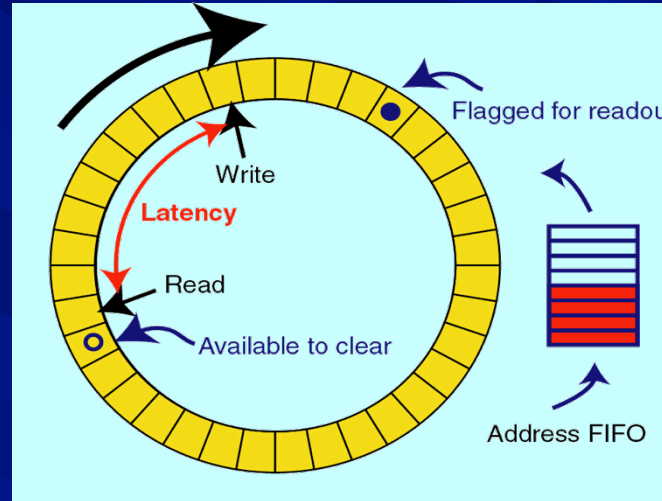
- Trigger processing requires some data transmission and processing time to make decision so front-ends must buffer data during this trigger latency time.
- For constant high rate experiments a "pipeline" buffer is needed in all front-end detector channels: (analog or digital) (e.g. circular buffer →

Analog Pipeline L1P before ADC

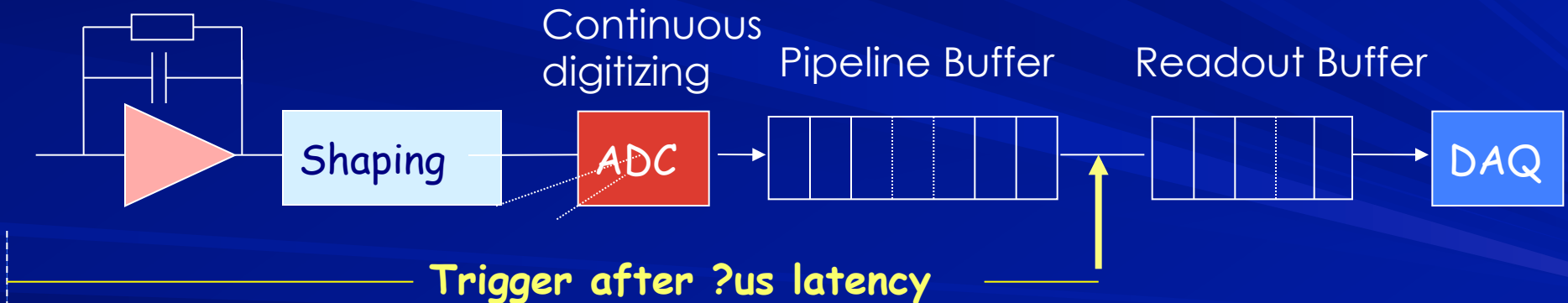


Terminology :buffer , pipeline & latency

- Digital Pipeline L1P after ADC but before Trigger Pass signal



Circular buffer



Digital pipeline example

BESIII Trigger System as example

Requirement to trigger system

■ Event Rate

- Good Event Rate: $\sim 2000\text{Hz}$
- Bhabha event Rate: $\sim 800\text{Hz}$
- CosmicRay Rate: $< 200\text{Hz}$,
rejection $> 10:1$
- Beam Backgd Rate: $< 2000\text{Hz}$,
rejection $> 10000:1$
- Total Trigger Rate: 4000 Hz

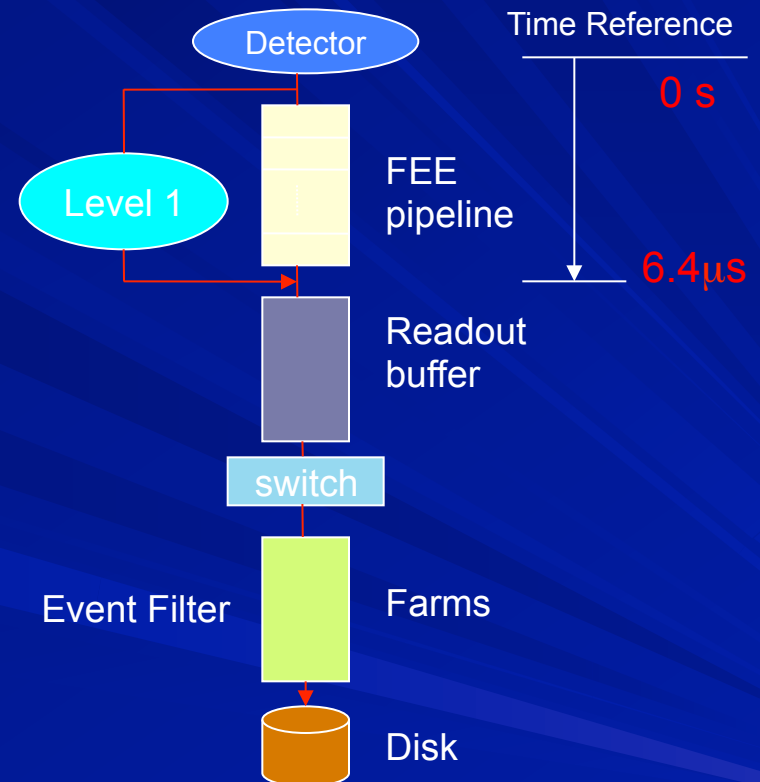
■ Pipeline working mode

- BEPCII Multibunch(93), Bunch
spacing: 8ns

■ L1 Uncertainty: $0.4\ \mu\text{s}$

■ Trigger Latency: $6.4\ \mu\text{s}$

■ L1P is a data Index, not a time
reference



BESIII FEE pipeline and Data flow

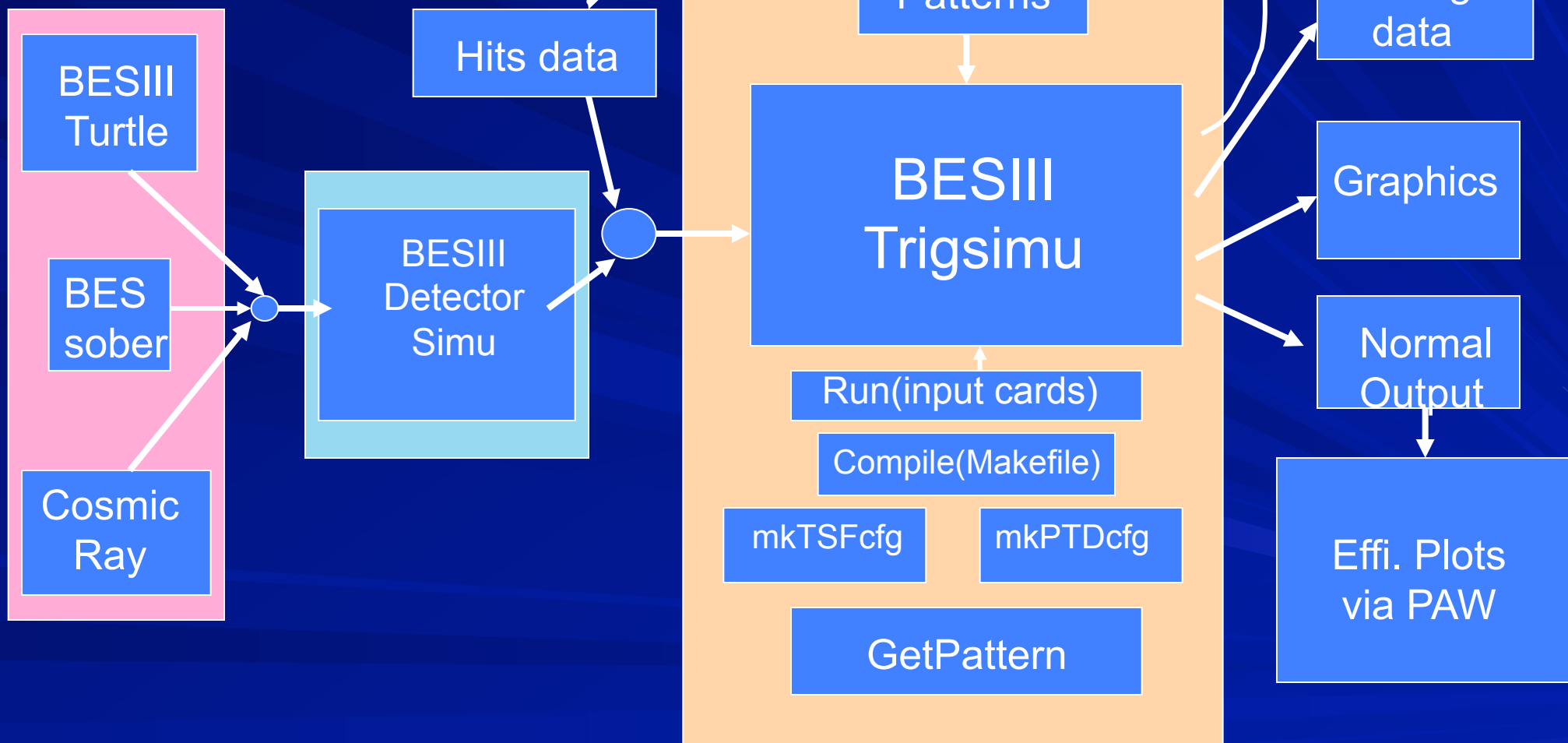
BESIII Trigger Scheme based on Simulation

1:MakePattern

2:Generator

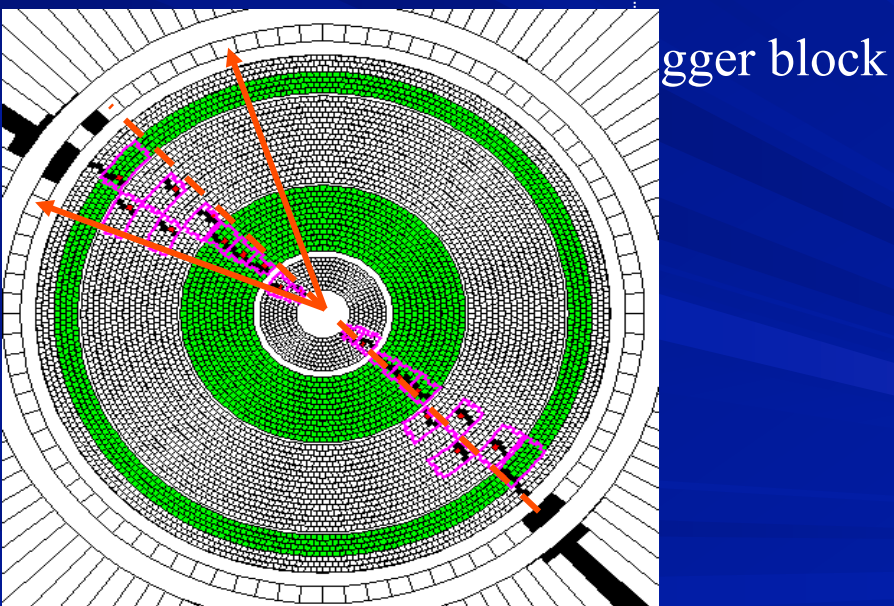
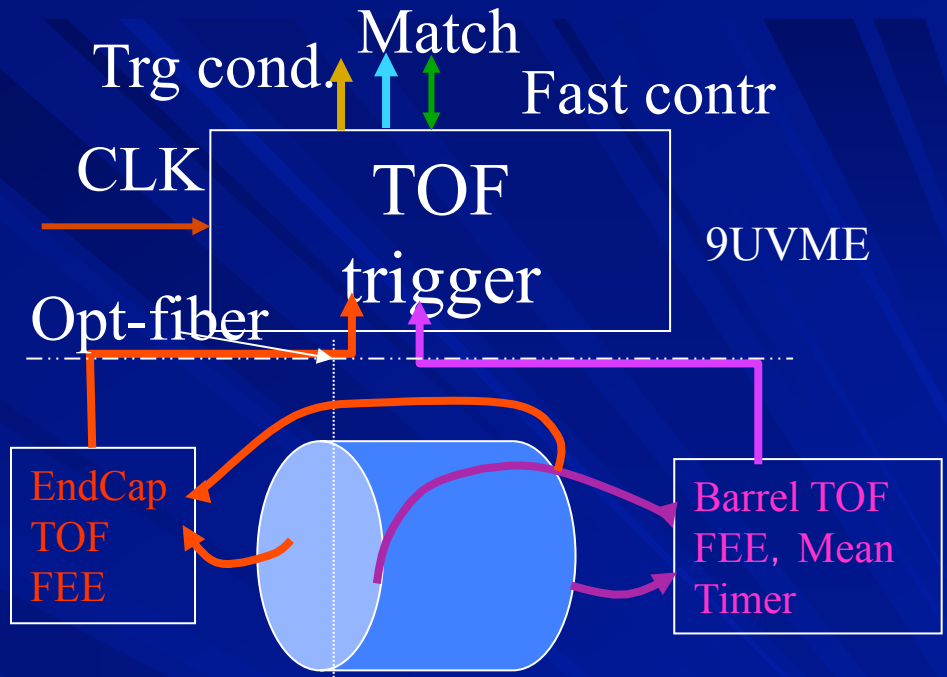
3:Det. Simu

4:Trig.Simu.



TOF trigger Primitives

- Hitting numbers
 - $N_{Btof} \geq 1, N_{Btof} \geq 2$
 - $N_{etof} \geq 1, N_{etof} \geq 2$
- Topology in Barrel: TBB
 - $P_t > 837 \text{ MeV}$
 - 12cells(3x2x2+1), 53°
- Topology in Endcap: ETBB
 - $P_t > 551 \text{ MeV}$
 - 8cells(2x2x2+1), 67°
- Hitting position (TKM):
 - $T_{Bhits}(88), T_{Ehits}(48)$



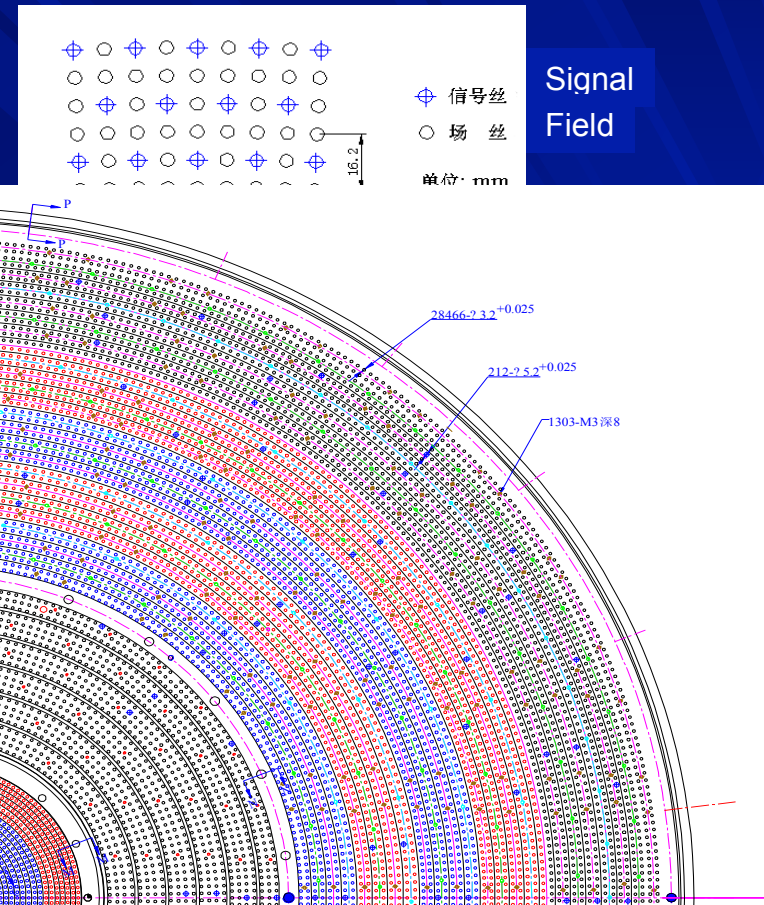
MDC subtrigger BESIII

Parameters of MDC trigger

Super Layer	Wire Layer	# of sig.				# of WL in SL	Pivot Layer	# of pivot cells SL
		L1	L2	L3	L4			
SL-1	ST-1/2/3/4	40	44	48	56	4	3	48
SL-2	ST-5/6/7/8	64	72	80	80	4	3	80
SL-3	AX-9/10/11/12	76	76	88	88	4	3	88
SL-4	AX-13/14/15/16	100	100	112	112	4	3	112
SL-5	AX-17/18/19/20	128	128	140	140	4	2	128
SL-6	ST-21/22/23/24	160	160	160	160	4	2	160
SL-7	ST-25/26/27/28	176	176	176	176	4	2	176
SL-8	ST-29/30/31/32	208	208	208	208	4	2	208
SL-9	ST-33/34/35/36	240	240	240	240	4	2	240
SL-10	AX-37/38/39/40	256	256	256	256	4	2	256
SL-11	AX-41/42/43	288	288	288	0	3	2	288
Total	43	6796				/	/	1784

Inner layers
 Pivotal layers
 Axial layers
 Not used layers

To simplify the hardware implementations, super layers 1st – 5th and 10th are used as MDC trigger sources



How the tracks are found in BESIII:

Track Segment Finding + Track Finding

TSF

Layer D

D3	D2	D1	D0
----	----	----	----

Layer C

C2	C1	C0
----	----	----

Layer B (PL)

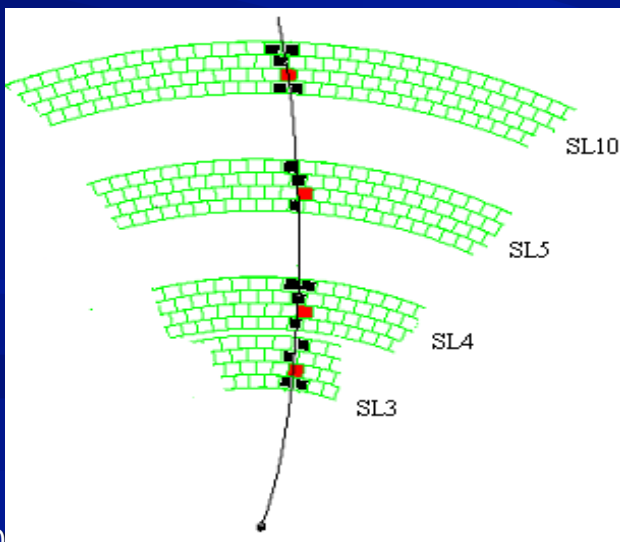
B2	B1
----	----

Layer A

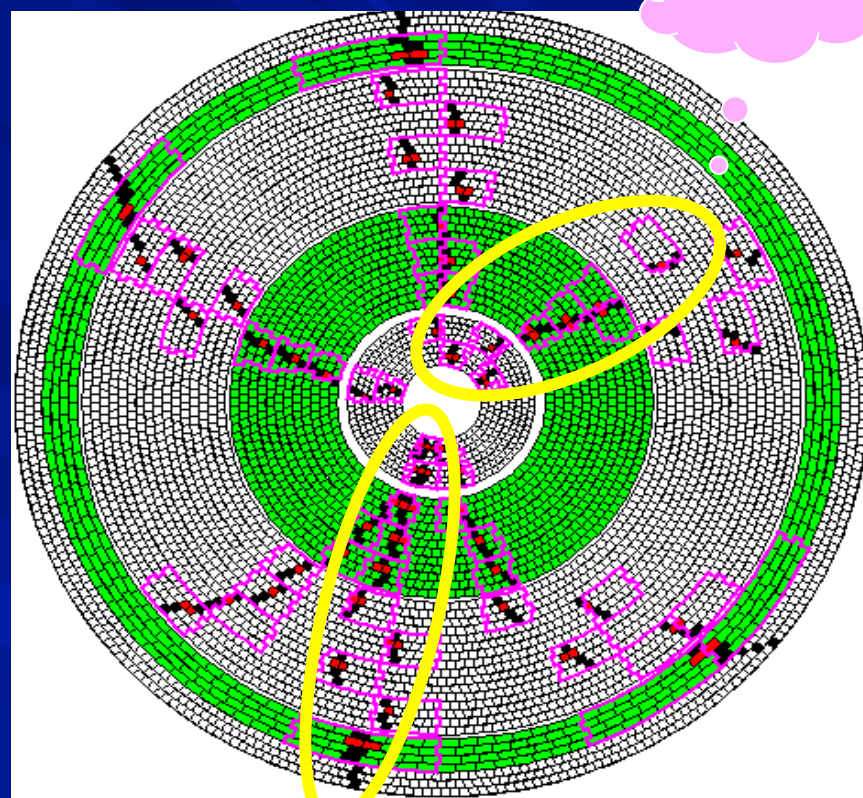
A2	A1	A0
----	----	----



TF



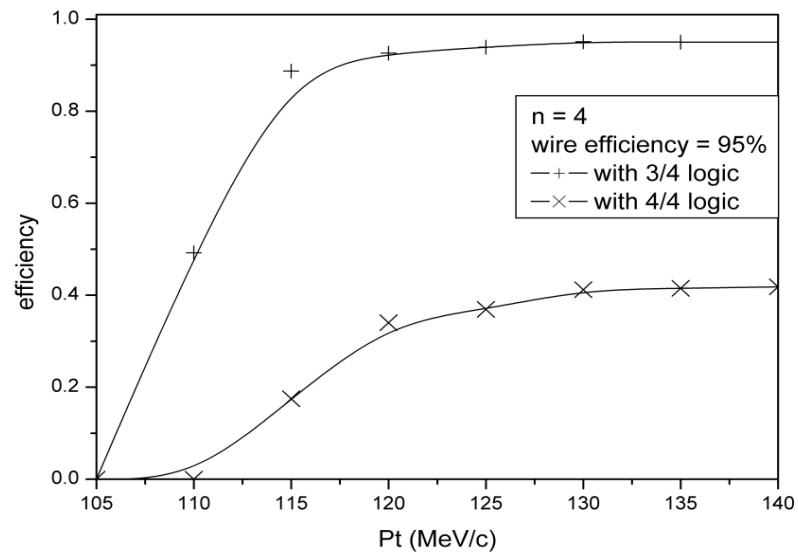
Pivot SL



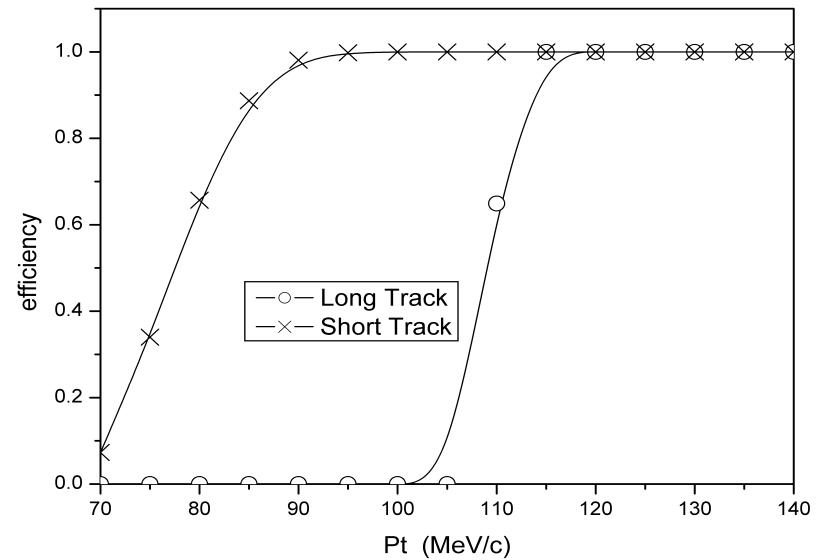
Short Track

Long Track

Some results of simulation



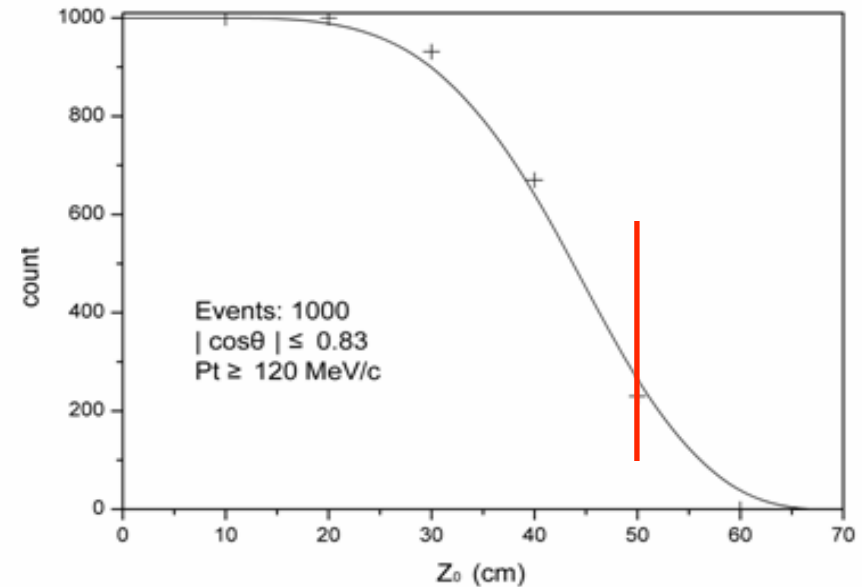
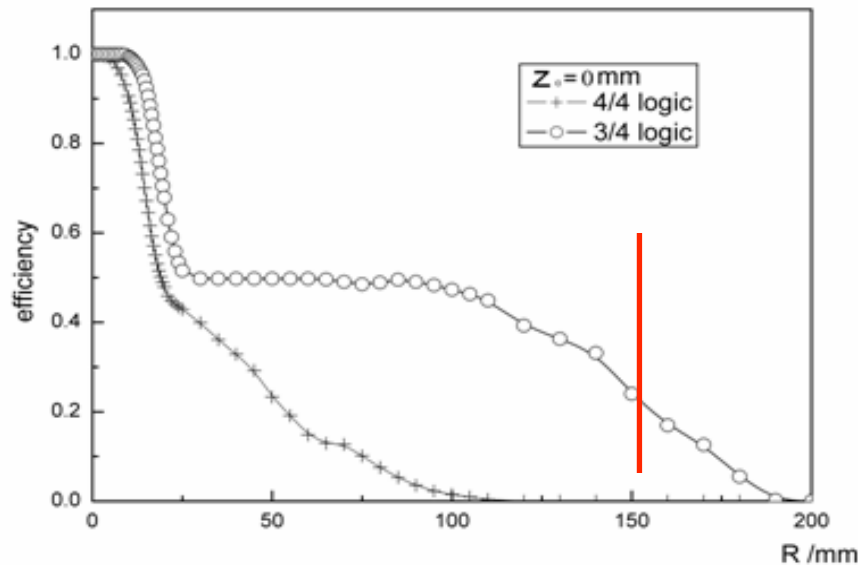
Relations between TSF efficiency and P_t



Relations between TF efficiency and P_t

Some results of simulation (2)

- The track finding efficiencies in the r - ϕ plane and Z direction.
 - For a distance of 15 cm in the r - ϕ plane, the TF efficiency is about 30% for 3/4 TSF logic.
 - For a distance of 50 cm in the Z direction, TF efficiency is about 30%.



It is good to reject backgrounds far from the Interaction Point

MDC Primitive

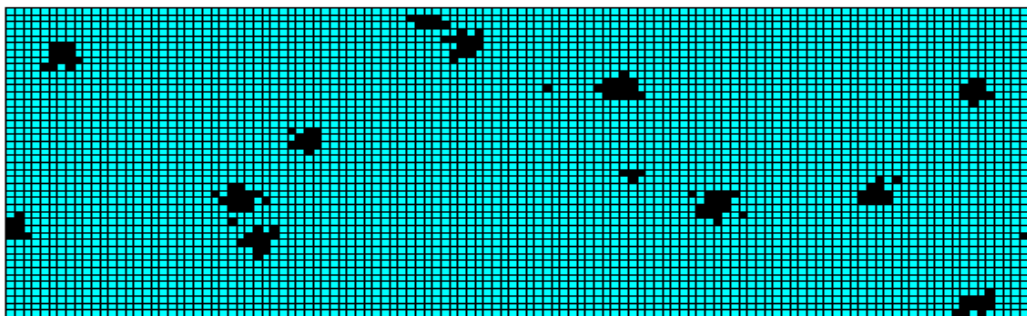
- 10 trigger conditions of the MDC trigger are used in BESIII trigger system
- 3 charged channels:
 - Charge1: $N_{Ltrk} \geq 1 + N_{tof} \geq 1$ (Number of Hits of TOF) + $E_{tot} - l$ (Low threshold of the whole EMC total energy, $\sim 200\text{MeV}$)
 - Charge2: $N_{Ltrk} \geq 1 + N_{Strk} \geq 2$
 - Charge3: $S_{Trk} - BB$

$N_{Ltrk} \geq 1$	Number of long track ≥ 1 ;
$N_{Ltrk} \geq 2$	Number of long track ≥ 2 ;
$N_{Ltrk} \geq N$	for MDC wires' hits of high voltage sudden discharge
$N_{Strk} \geq 1$	Number of short track ≥ 1 ;
$N_{Strk} \geq 2$	Number of short track ≥ 2 ;
$N_{Strk} \geq N$	for MDC wires' hits of high voltage sudden discharge ;
$S_{Trk} - BB$	Short Tracks back to back ;
$N_{Itrk} \geq 1^*$	Number of the Track Segments of the SL1 and SL2 are equal to or greater than 1;
$N_{Itrk} \geq 2^*$	Number of the Track Segments of the SL1 and SL2 are equal to or greater than 2.

* $N_{Itrk} \geq 1$ and $N_{Itrk} \geq 2$ are for backups to reject beam-related backgrounds.
Aug. 15 2018

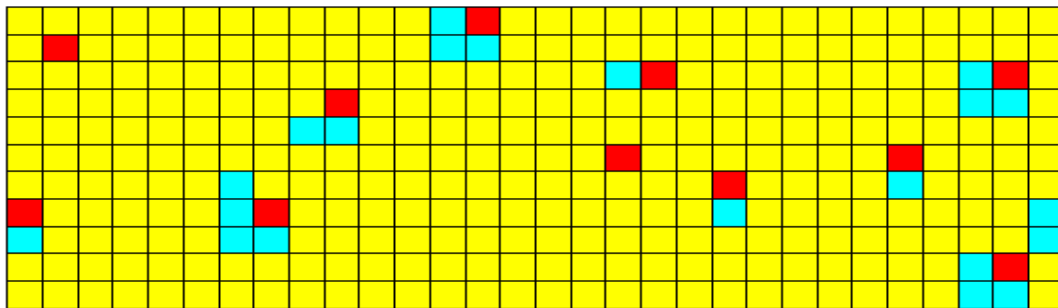
EMC Trigger: TC and Isolated Cluster finding

BEMC CRYSTAL HITS



NUMBER OF CLUSTER 32. GATE THRESH 0. MEDIUM 12.
 NUM OF ISO CLUSTER 11. GATE THRESH 0. MEDIUM 7.

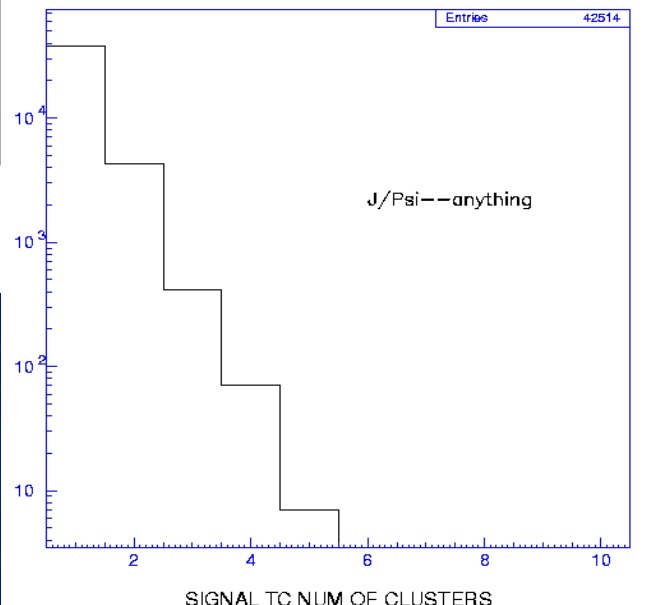
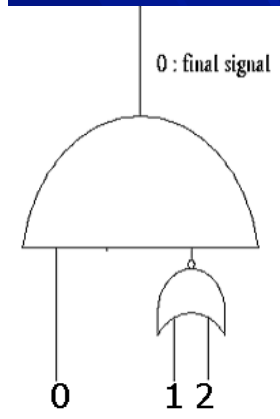
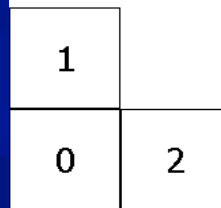
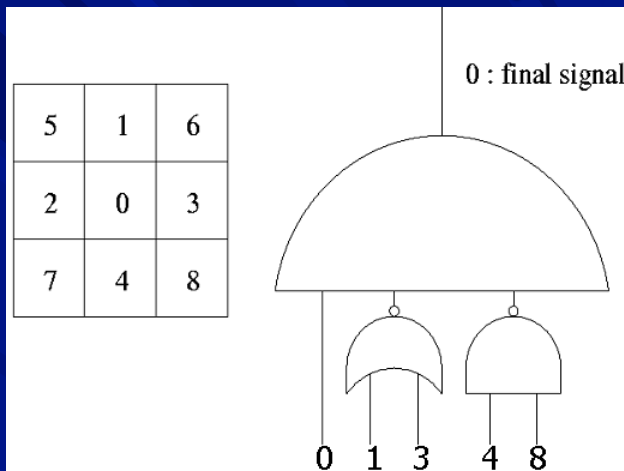
BEMC TC HITS



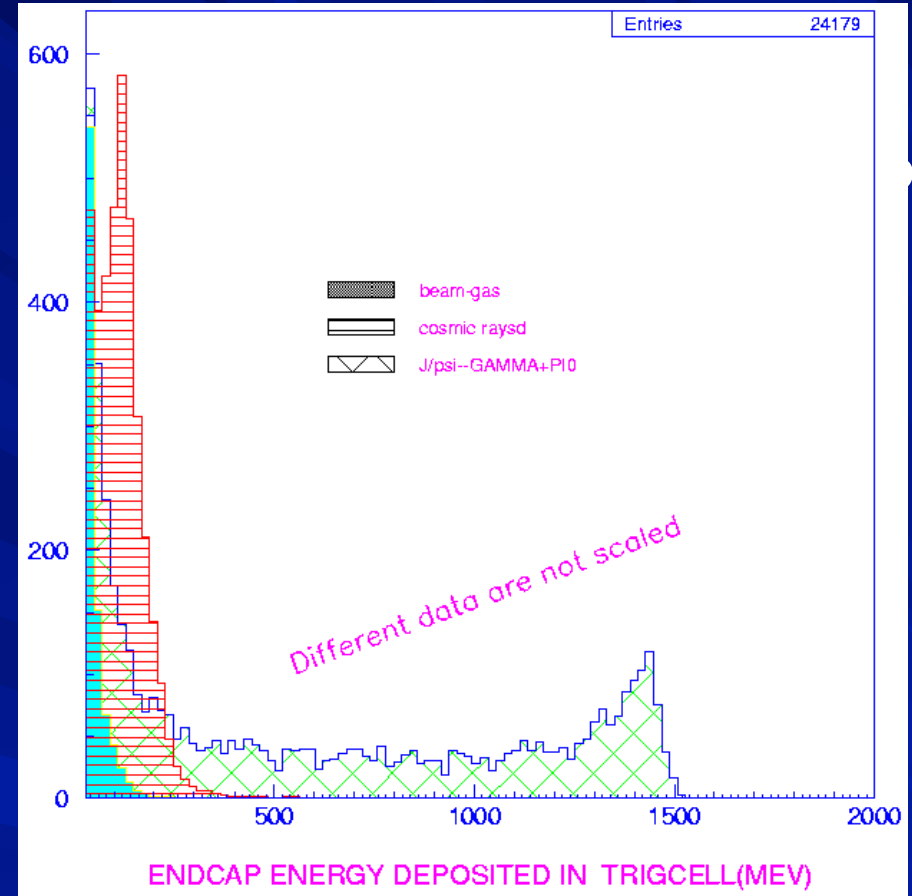
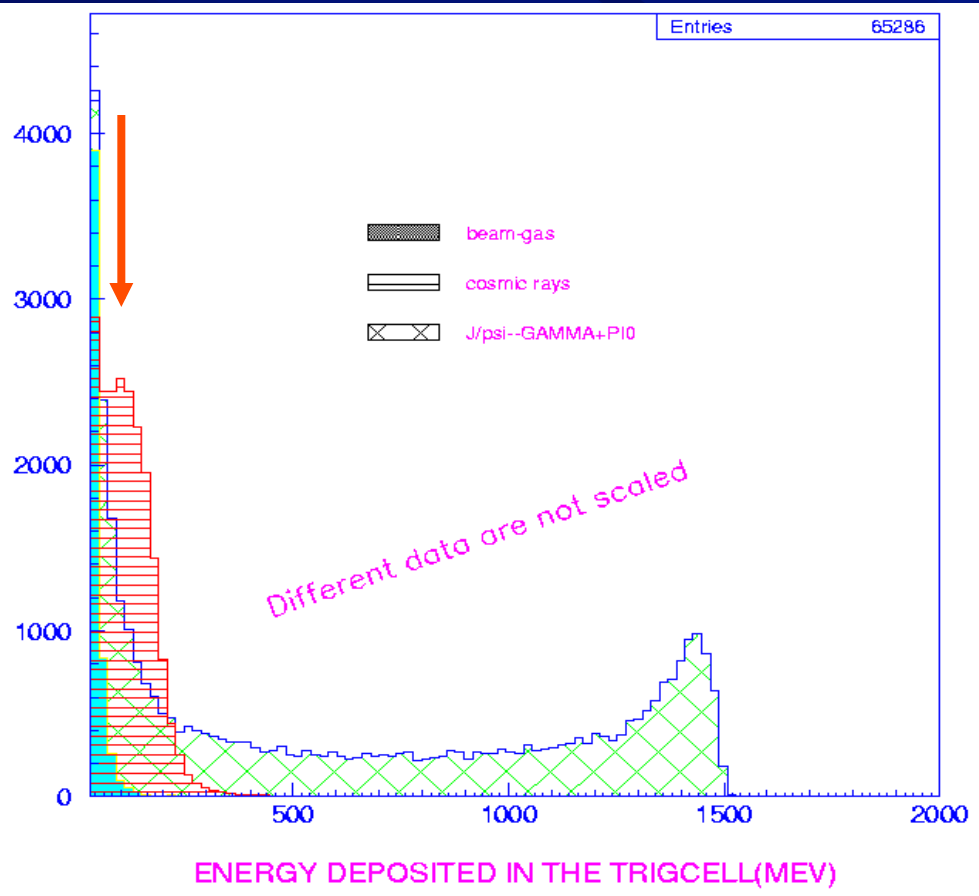
NUMBER OF CLUSTER 32. GATE THRESH 0. MEDIUM 12.
 NUM OF ISO CLUSTER 11. GATE THRESH 0. MEDIUM 7.

- Crystals: 120 x 44
- Trigger Cell(TC): 30 x 11
- TC Energy
- Total Energy

Aug. 15 2018

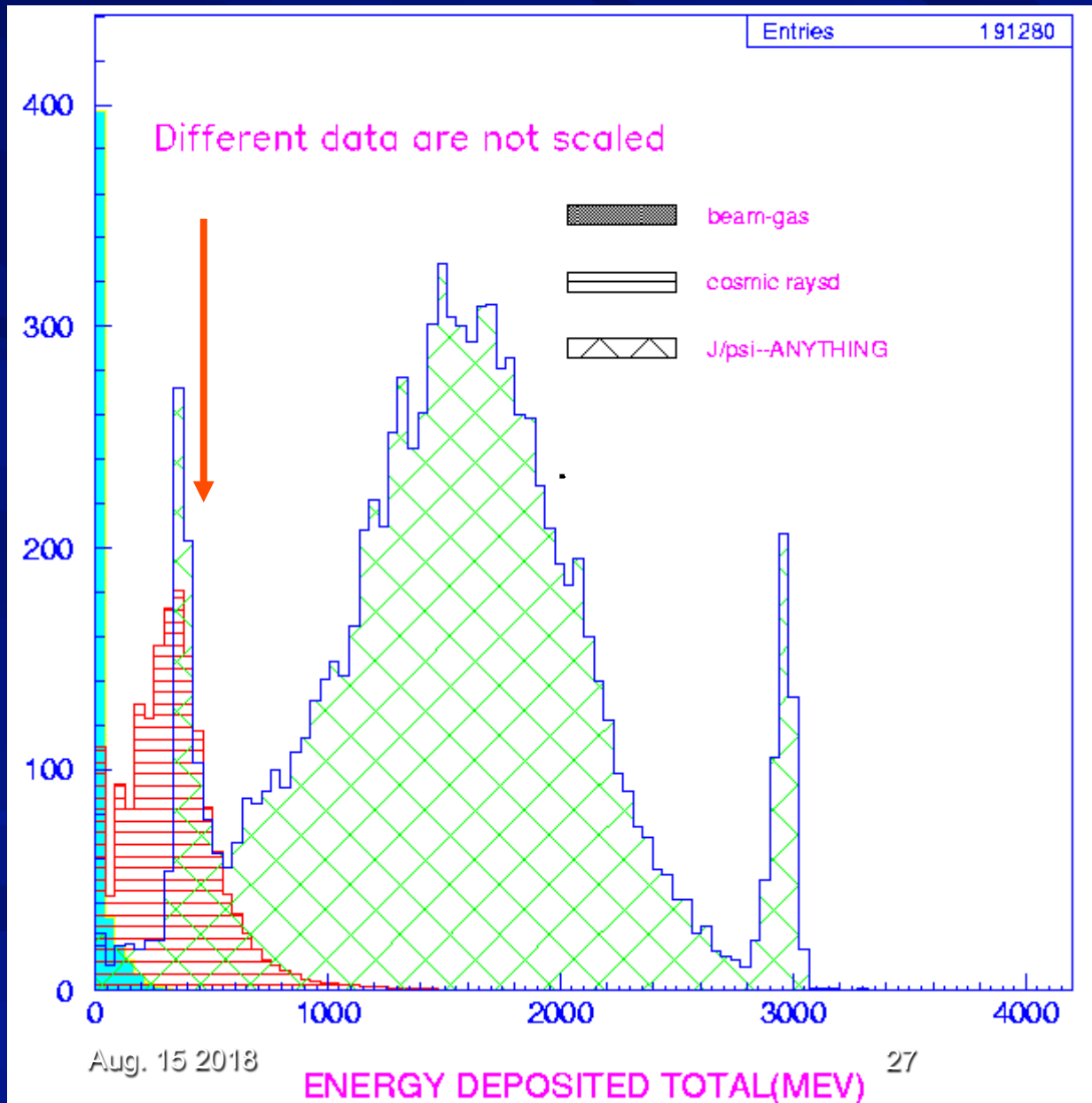


TC Energy Threshold



- Taking the pileup and baseline fluctuation into account, the TC threshold is utilized as 60—80Mev.
- Beam gas background in low energy, so a 60—80Mev threshold can remove most of the BG backgrounds

Total energy



- Etot-L (~200MeV)
Threshold for background events
- Etot-M (~800MeV)
Threshold for neutral events
- Etot-H (~2.5GeV)
Threshold for bhabha event

EMC 触发条件

- NClus \geq 1 Cluster number (\geq 1 for EMC timing)
- NClus \geq 2
- BclusBB Back to back cluster
- EclusBB
- Clus_PHI Cluster balance at φ
- Clus_Z One cluster at each half of EMC
- Diff_B Energy difference between each B half
- Diff_E Energy difference between each E half
- BL_BEMC Energy Balance between half BEMC
- BL_BLK Energy Balance of barrel blocks
- BL_EEMC Energy Balance between half EEMC
- BL_Z Z energy balance (B+E)
- Etot_L Total Energy \gt Thre-l
- Etot_M Total Energy \gt Thre-m
- BEtot_H Total energy of Barrel EMC
- EEtot_H Total energy of Endcap EMC

- To TKM:

- Bemc(40),Eemc(48)

Trigger Table

Detector	Trigger Condition	bits	Comments
TOF	Ntof \geq 1 Ntof \geq 2 TBB	3	TOF hits number (TOF timing) Back to back hits
ETOF	Netof \geq 1 Netof \geq 2 ETBB	3	(ETOF timing)
MDC	NLtrk \geq 1 NLtrk \geq 2 LTrk-BB NLtrk \geq N NStrk \geq 1 NStrk \geq 2 STrk-BB NStrk \geq N Nltrk \geq 1 NITRK \geq 2	10	Full Track number Back to back tracks Many tracks Short Tracks number With Inner DC hit
EMC	NClus \geq 1 NClus \geq 2 BelusBB EclusBB Clus_PHI Clus_Z Diff_B, Diff_E, BL_BEMC, BL_BLK BL_EEMC BL_Z Etot_L, Etot_M BEtot_H EEtot_H	16	Cluster number(EMC timing) Back to back cluster Cluster balance at ϕ One cluser at each half of EMC Energy difference between each B half Energy difference between each E half Energy Balance between half BEMC Energy Balance of barrel blocks Energy Balance between half EEMC Z energy balance (B+E) Tatol Energy >Thre-l Tatol Energy >Thre-m Tatol energy of Barral EMC Tatol energy of Endcap EMC
MATCH	NAttrk \geq 1 NAttrk \geq 2 ATRK-BB NBtrk \geq 1 NBtrk \geq 2 BTRK-BB NCtrk \geq 1 NCtrk \geq 2 CTRK-BB	9	Atrk=MDC Full track+TOF hit OR MDC Full track+TOF hit+ EMC Cluser Btrk= ETOF hit + EEMC Cluster OR ETOF hit + EEMC Cluster +MDC Short Track Ctrk=MDC Track+Inner MDC hit
		41	

Function

- TOF

- Timing and trigger for Charged particles

- Background rejection

- MDC

- Tracking

- Background rejection

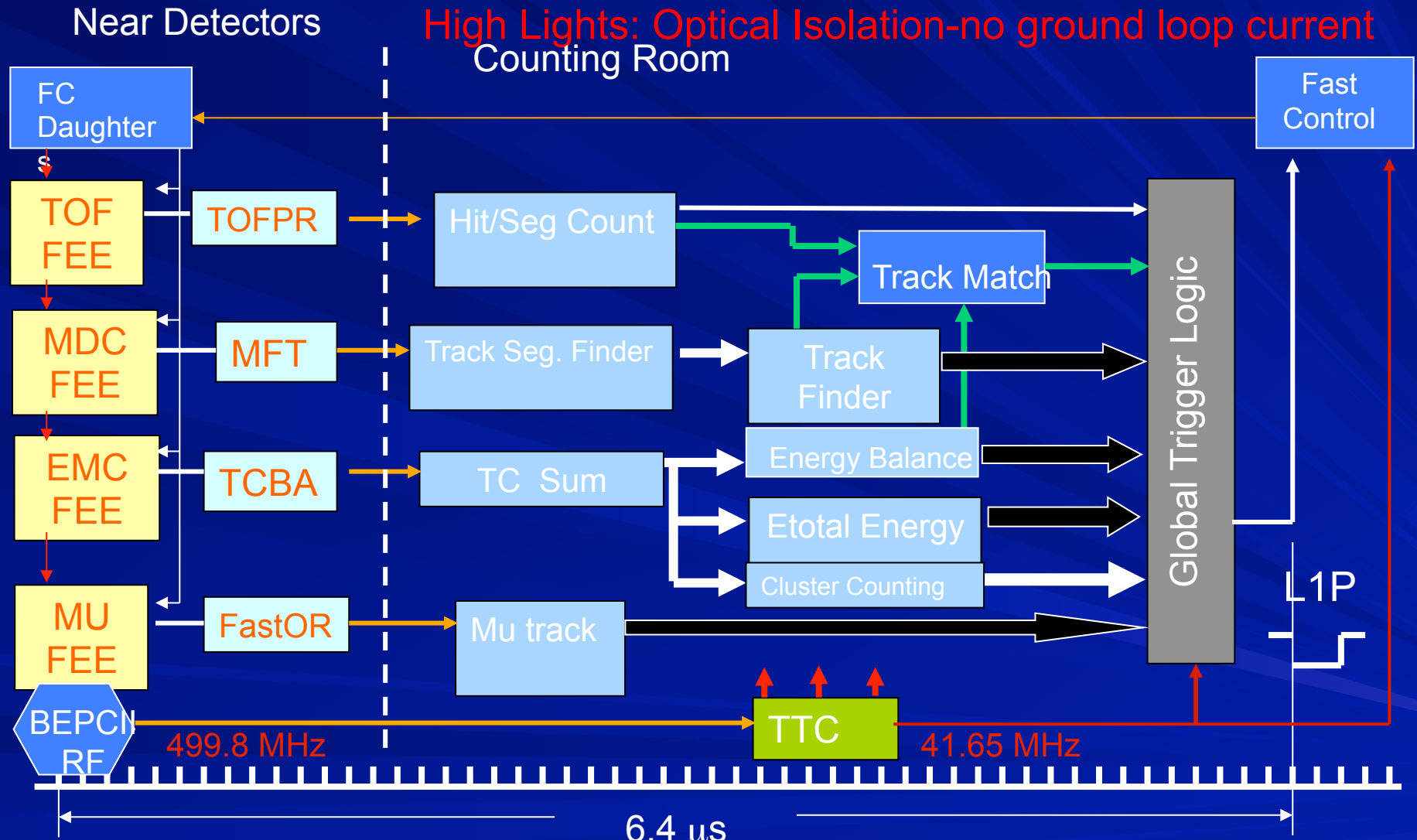
- EMC

- Trigger for neutral (+charged) particles

- Match

- Track/Cluster matching to further background rejection

BESIII L1 trigger block diagram



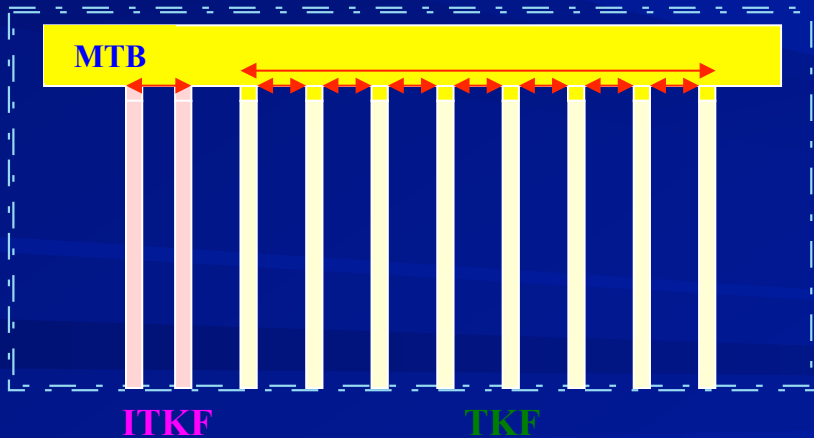
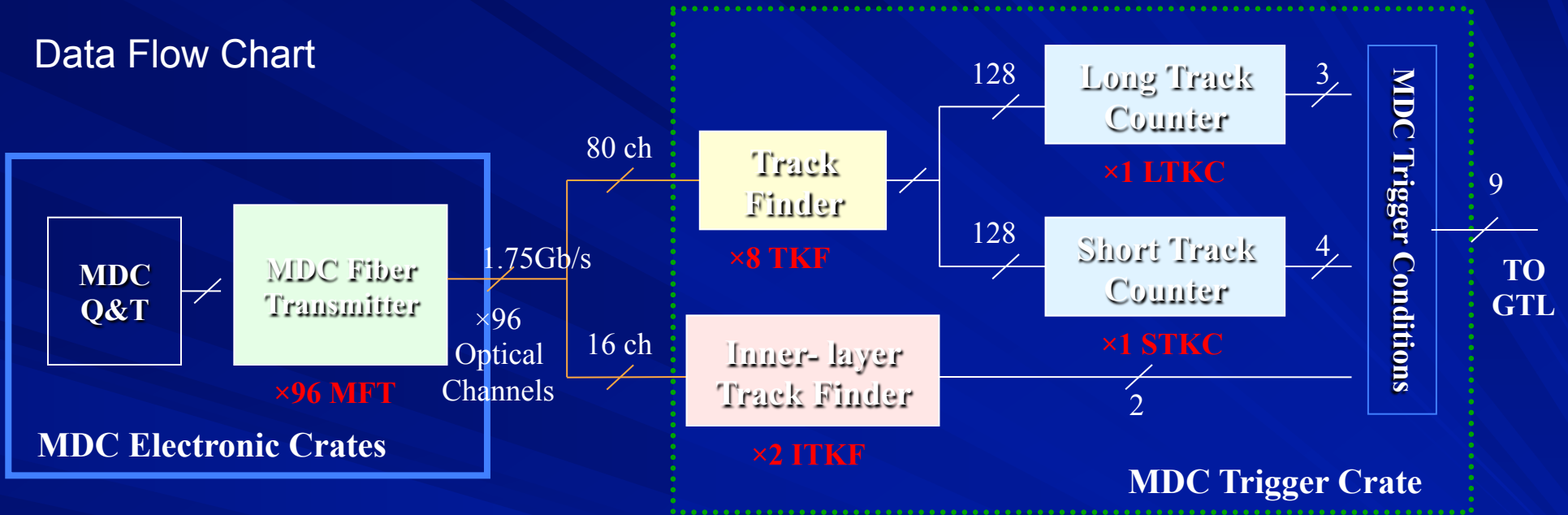
Trigger efficiency from Simulation

Events generated and simulated with <u>Geant</u>	Trigger efficiency(%) / background rate
Bhabha @ 3.097 GeV	100
Radiative BB (3.097 GeV)	100
$J/\psi \rightarrow \gamma \eta \rightarrow 3\gamma$	99.99
$J/\psi \rightarrow \omega \eta \rightarrow 5\gamma$	99.99
$J/\psi \rightarrow K^+ K^- \pi^0$	99.69
$J/\psi \rightarrow P \bar{P}$	99.91
$J/\psi \rightarrow$ anything	99.80
$J/\psi (2S) \rightarrow$ anything	99.50
$J/\psi (3770) \rightarrow$ anything	99.90
Lost beam backgrounds	1.85 kHz
Cosmic-ray backgrounds	86 Hz

■ Showed good results

Hardware Implimentation (MDC as example)

Data Flow Chart



	Type of PCB	Board name	# of boards	FPGA firmware
MDC Fiber Transmitter	1	MFT	96	1
TracK Finder	1	ITKF	2	2
		TKF	8	8
TracK Counter	1	LTKC	1	1
		STKC	1	1
MDC Trigger Backplane	1	MTB	1	
Total	4		109	13

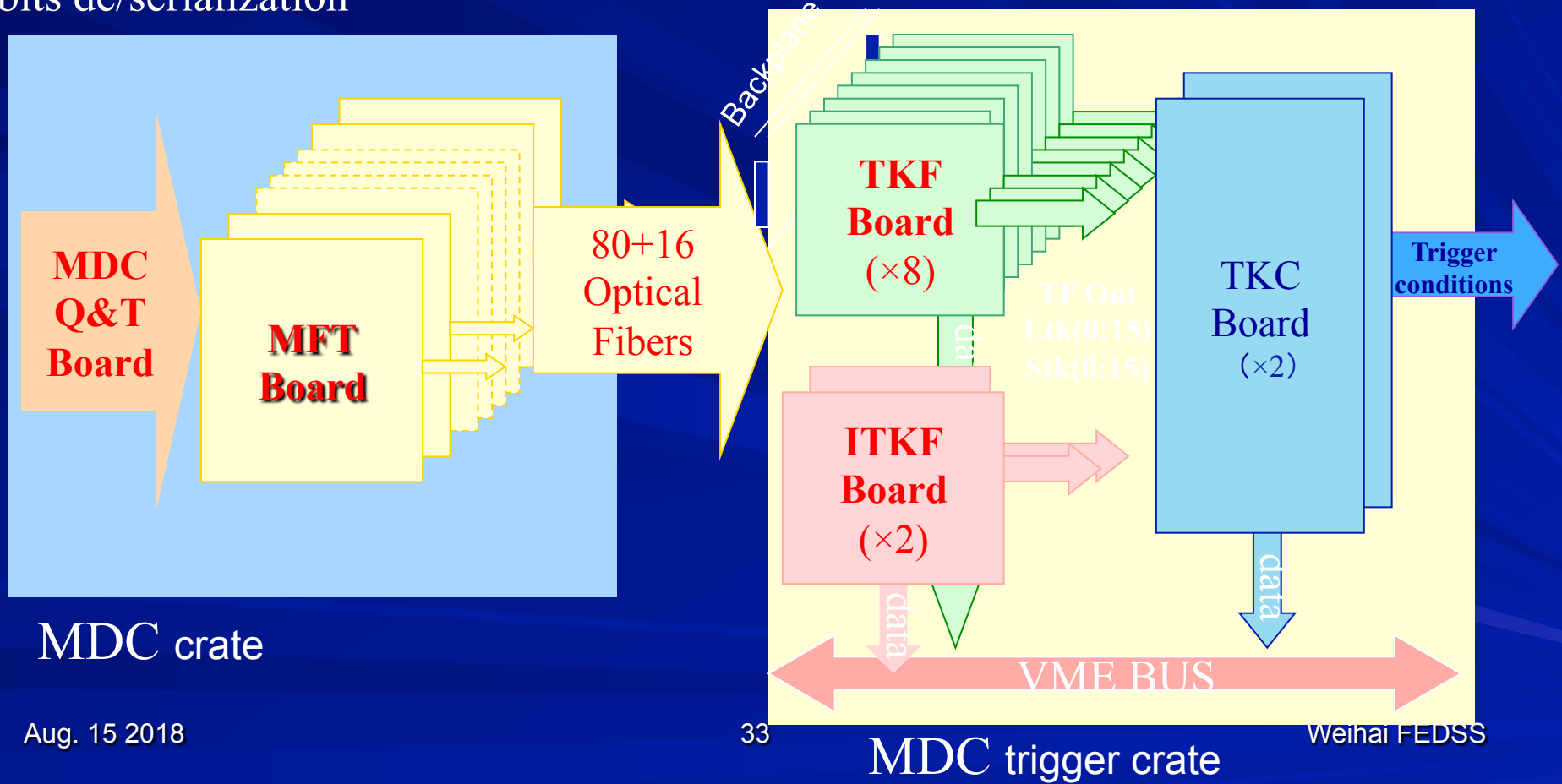
Processing boards allocation

- Xilinx VirtexII Pro
- RocketIO 1.6Gbps
- 32bits de/serialization

MFT: one fiber per board

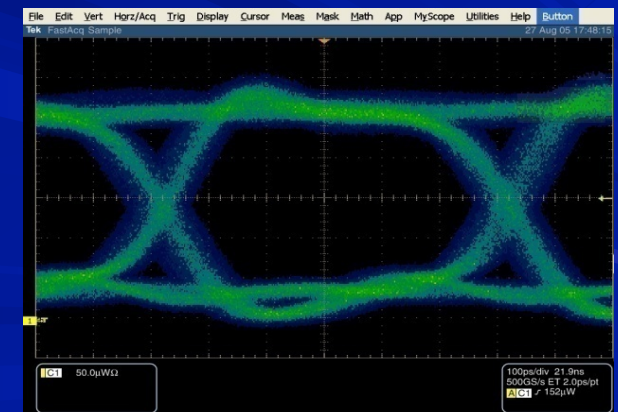
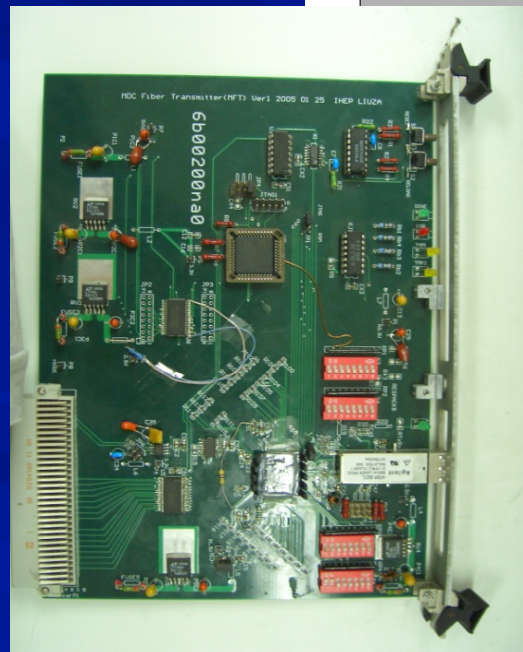
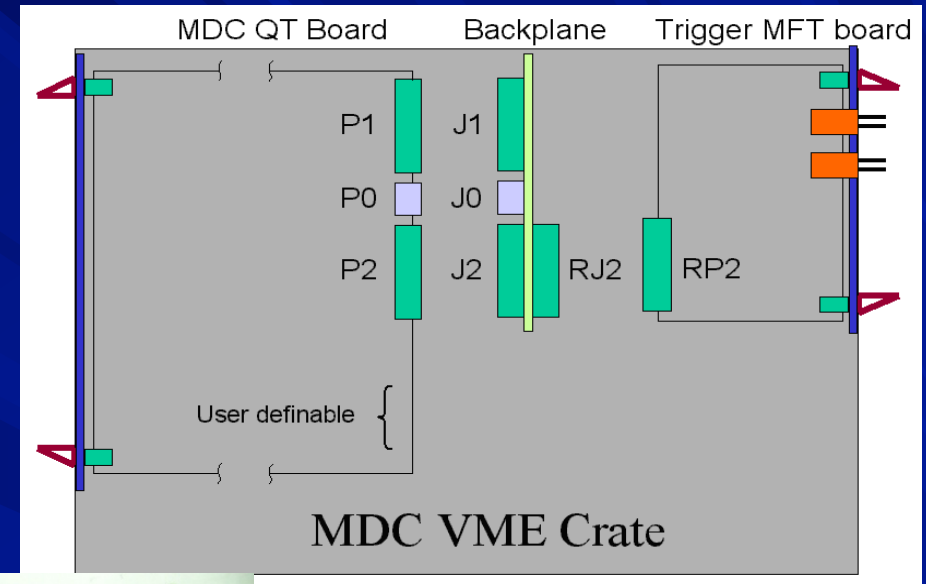
TKF: 8 boards hardware same

FPGA software similar



MFT (MDC Fiber Transmitter)

- 2796 hits signals from MDC QT boards are collected in MFT, 32 channels per MFT
- Optical fibers are used between MFT and TKF(ITKF) to eliminate common-ground noises
- Virtex-II Pro FPGA: XC2VP2
- 8 layers PCB



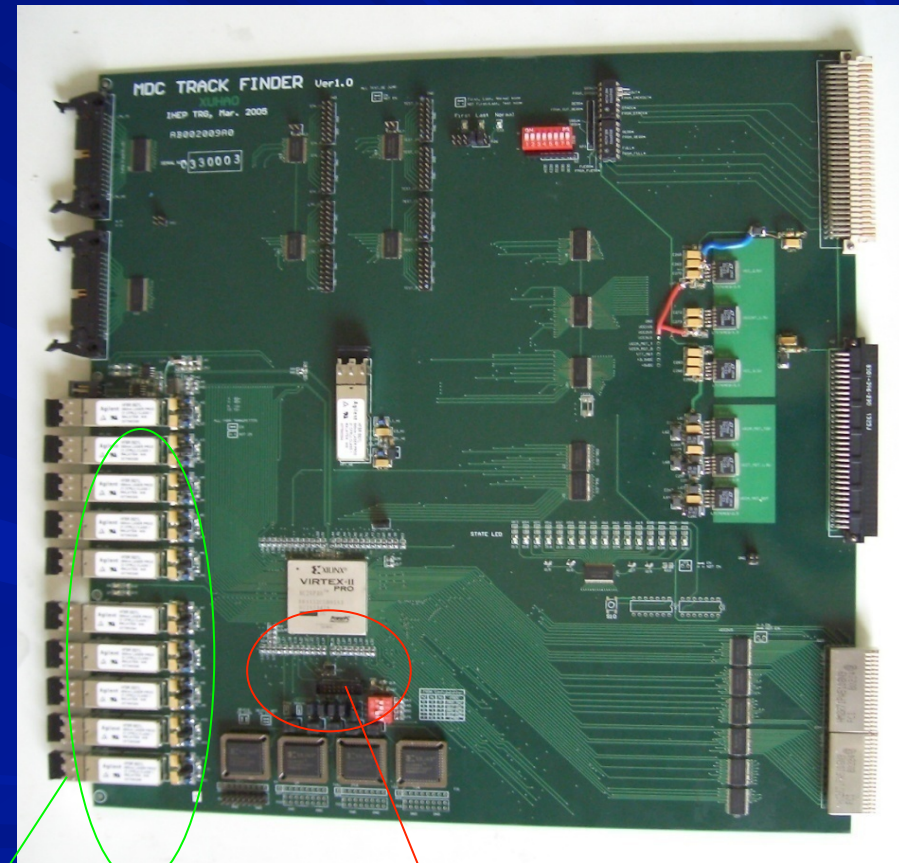
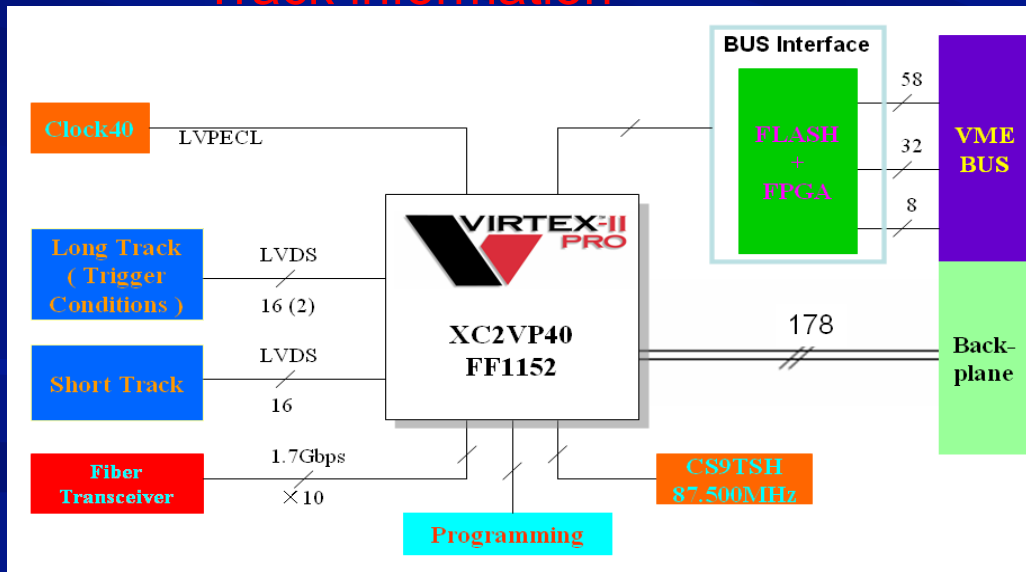
TKF (Track Finder)寻迹板

XC2VP40 : FF1152, 804 user I/Os, 43,632 logic cells, 3,456Kbit BRAM, 12 RocketI/Os, 2 PowerPCs, 192 multiplier blocks

10 layers 9UVME PCB

Functions:

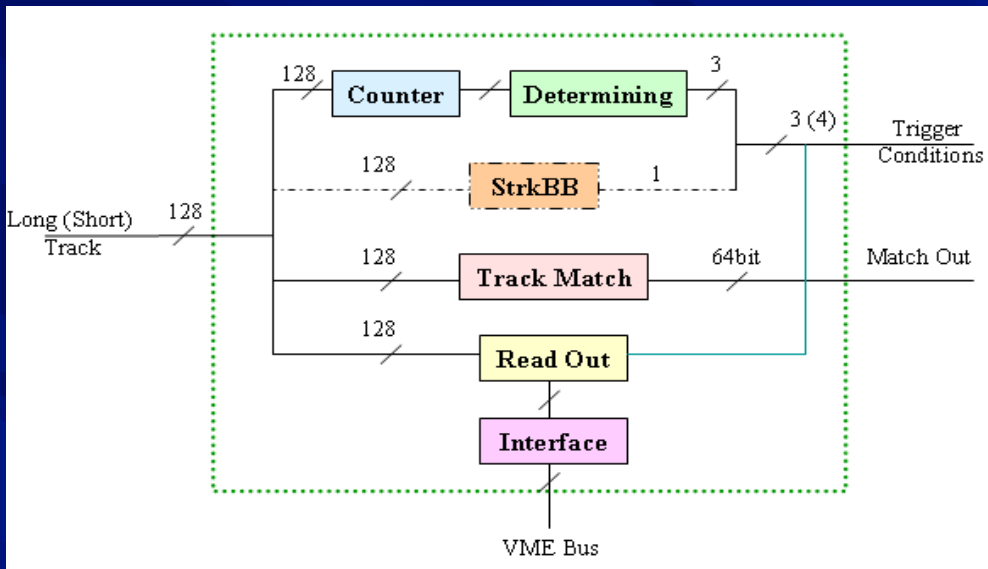
- TSF
- TF
- Track information



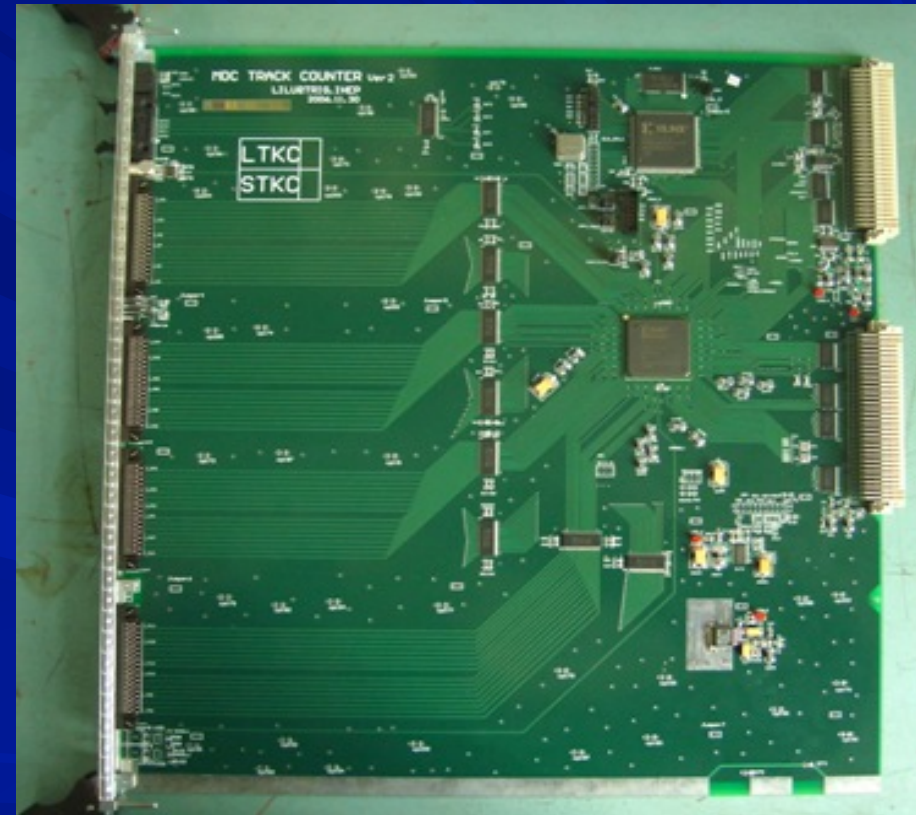
HFBR5921L
35

XC2VP40

TKC (Track Counter)径迹计数板

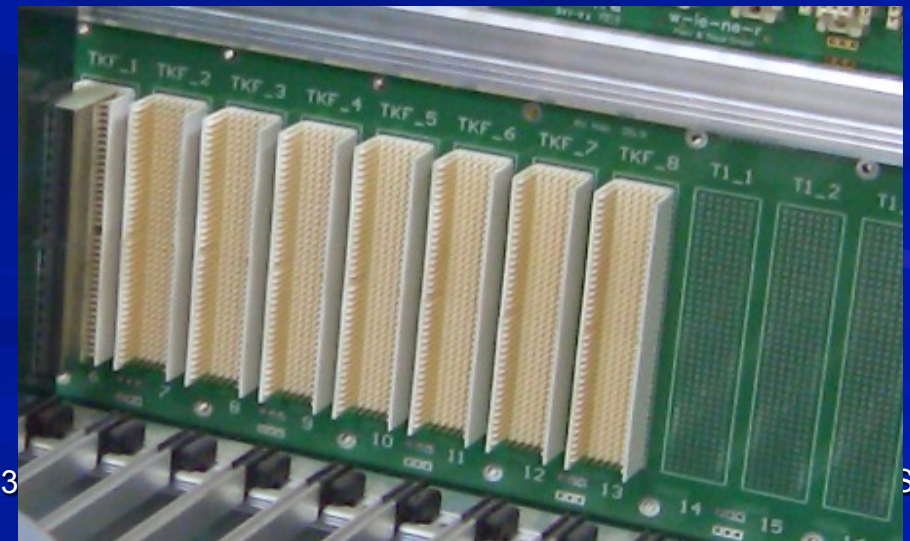
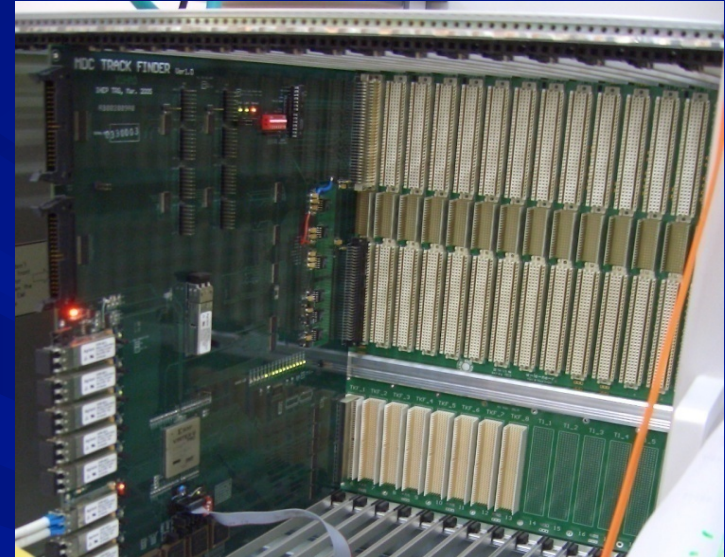


- **LTKC** (Long Track Counter) receives the number of long tracks from TKF and sends the trigger conditions to global trigger
- **STKC** (Short Track Counter) receives the number of short tracks from TKF and sends the trigger conditions to global trigger
- 8 layers PCB



MTB (MDC Trigger Backplane)

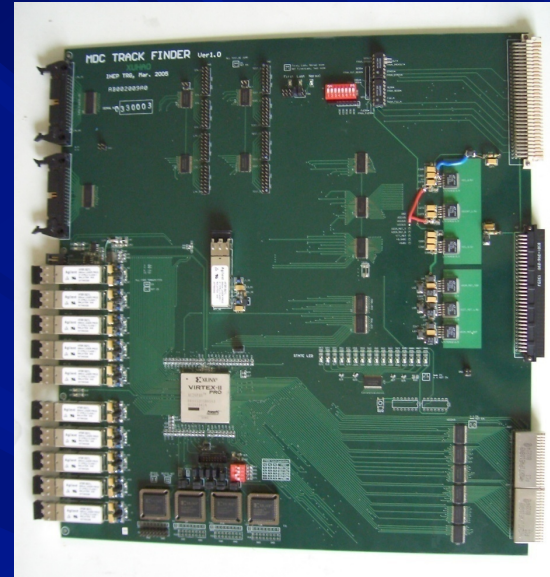
- Limited Bandwidth
- Inter-link neighbor boards, to reduce the cables.
- 12 layers PCB
- SI & EMC
- The experience in solving the difficulties met at BESIII Trigger Design, lead to collaborate for the **new xTCA standard** after VME.



Example of evolution



Demonstrator at
the end of the 90's

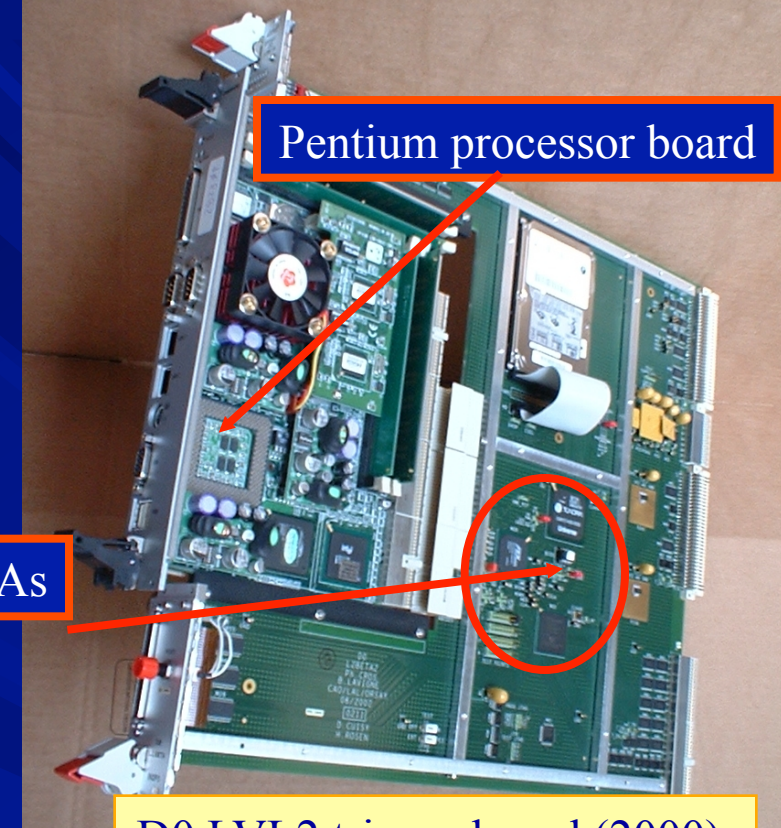


Final version
installed

- Muon trigger board for ATLAS
 - Handles 13 input links, each of them receiving 32-bit every 25ns
 - ~17 Gb/s processed
- MDC Trigger board for BESIII(right)

LVL2 examples

- Alpha = many years of efforts ...hardware and software
- PC (Commercial): few months to implement! No hardware!

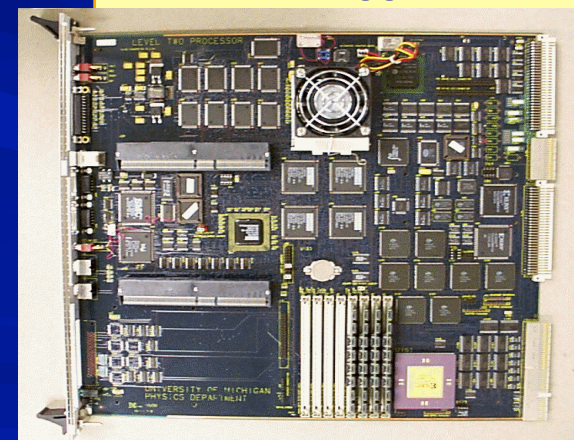
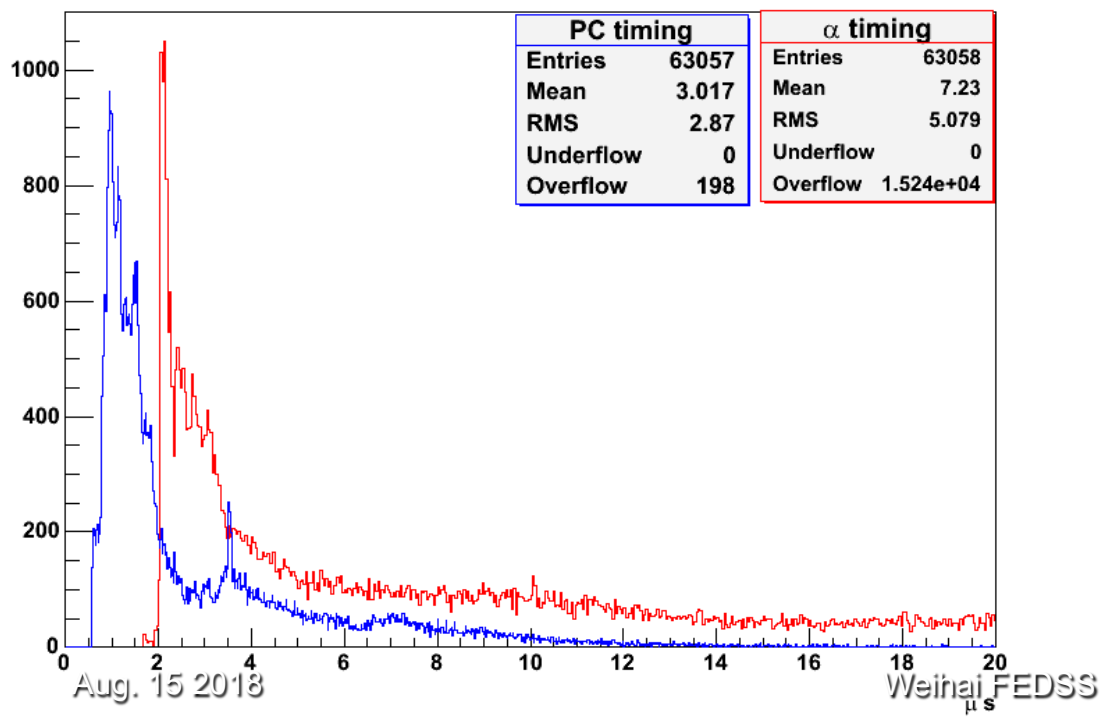


Pentium processor board

2 FPGAs

D0 LVL2 trigger board (2000)

α vs. PC L2 algorithm timing



Alpha Processor board

Specification of BESIII DAQ requirement (Thanks to Prof. Kejun Zhu for DAQ Infor)

- Trigger Rate: 4KHz
- Event Length: 12KB
- Data Bandwidth:
48MB/s
- Dead Time < 5%

Sub-Detector	Channels
MDC (T+Q)	6796+6796
EMC	6240
TOF (T+Q)	448+448
MUC	9088
Total	~ 30K

1000 * BESII DAQ

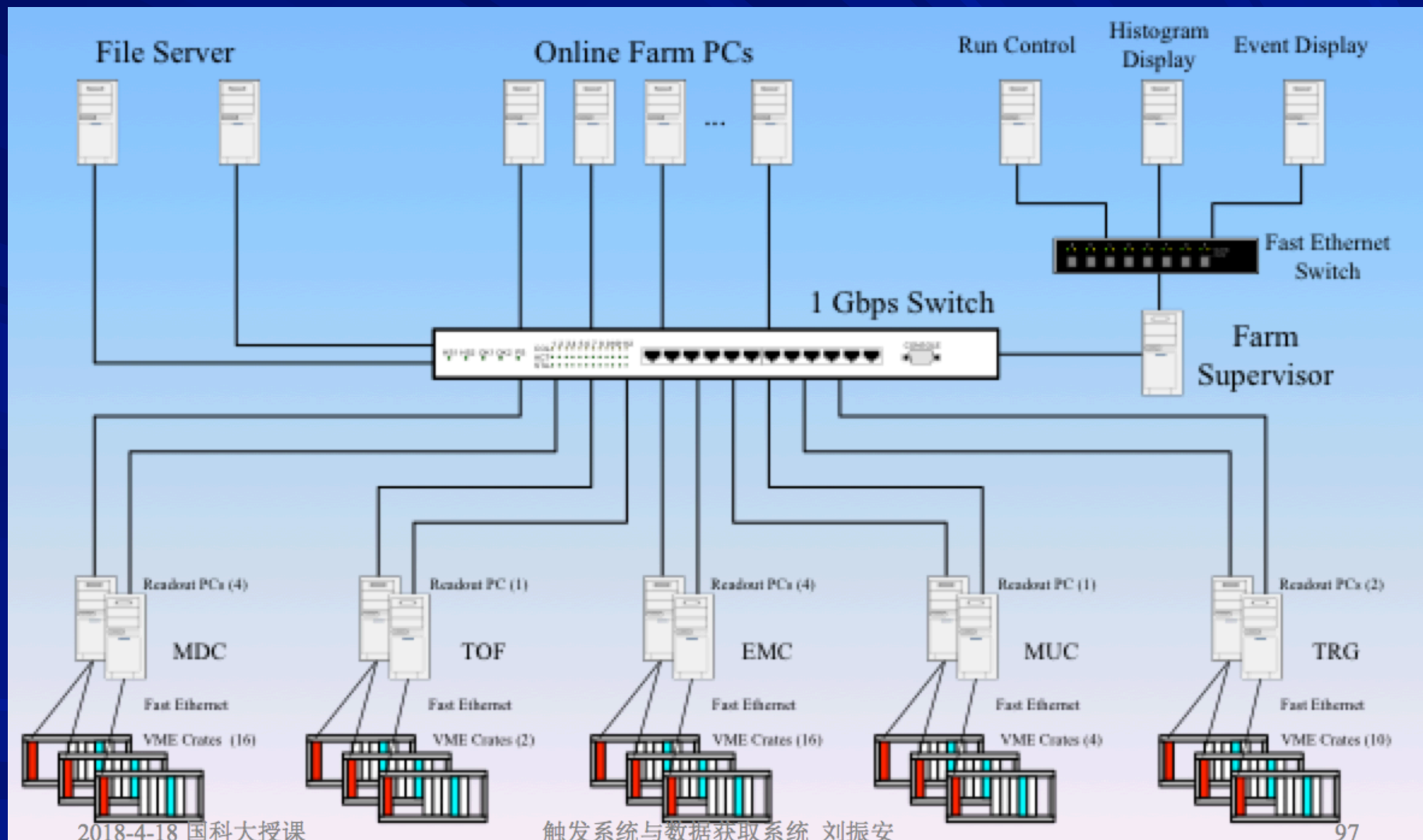
Function of BESIII DAQ

- Data acquisition including readout, packing and online filter 数据获取，包括数据读出、组装和在线过滤等
- Data storage 数据存储
- Run Control 运行控制
- Monitoring 数据监测，如单事例、直方图显示
- DataBase Configuration 配置数据库
- Error reporting 报错和容错

Techniques 技术措施

- Distributed Parallel Computing, Layered architecture 分布式并行计算、层次结构
- Multithread and Object Oriented 多线程技术、面向对象
- Based on Network Exchanging 基于网络交换技术
 - A multi-processor distributed environment
 - Parallel data streams working independently and concurrently
- Multi Layer Data Buffer 多级数据缓存
- Upgradability and Expendability 易升级和扩展
- Reliable and Stable 系统可靠、稳定

Structure of BESIII DAQ

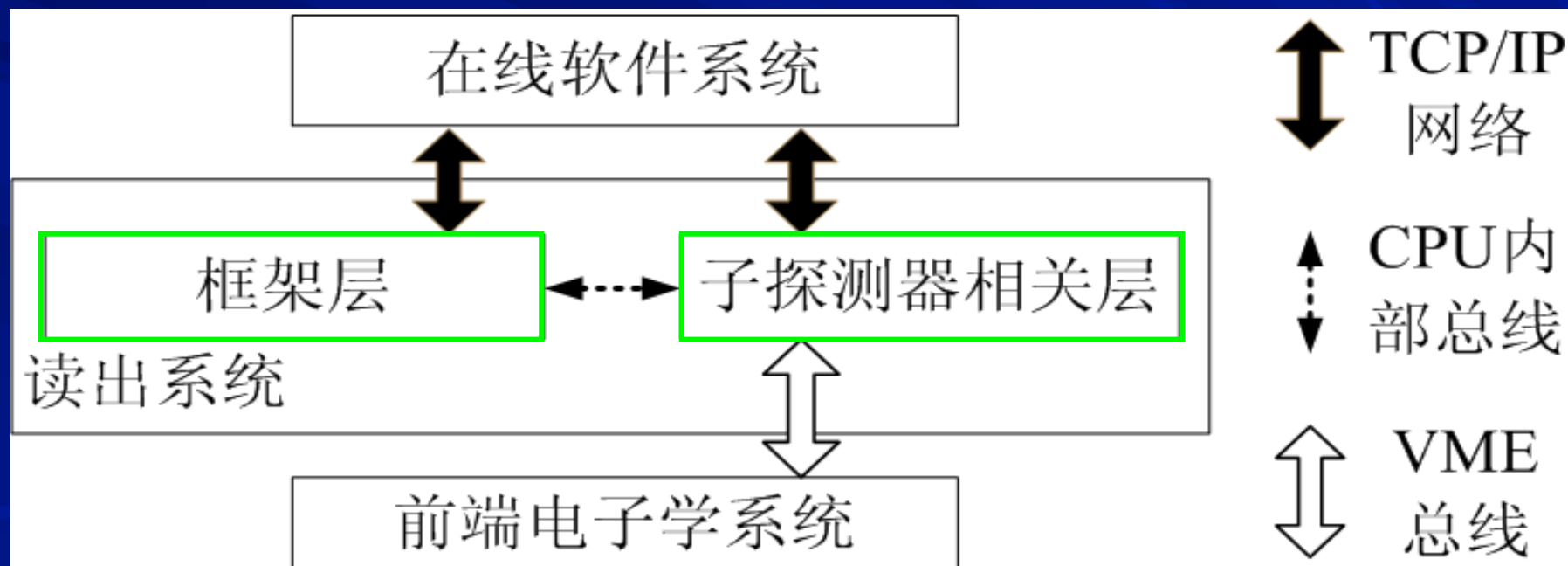


DAQ系统组成

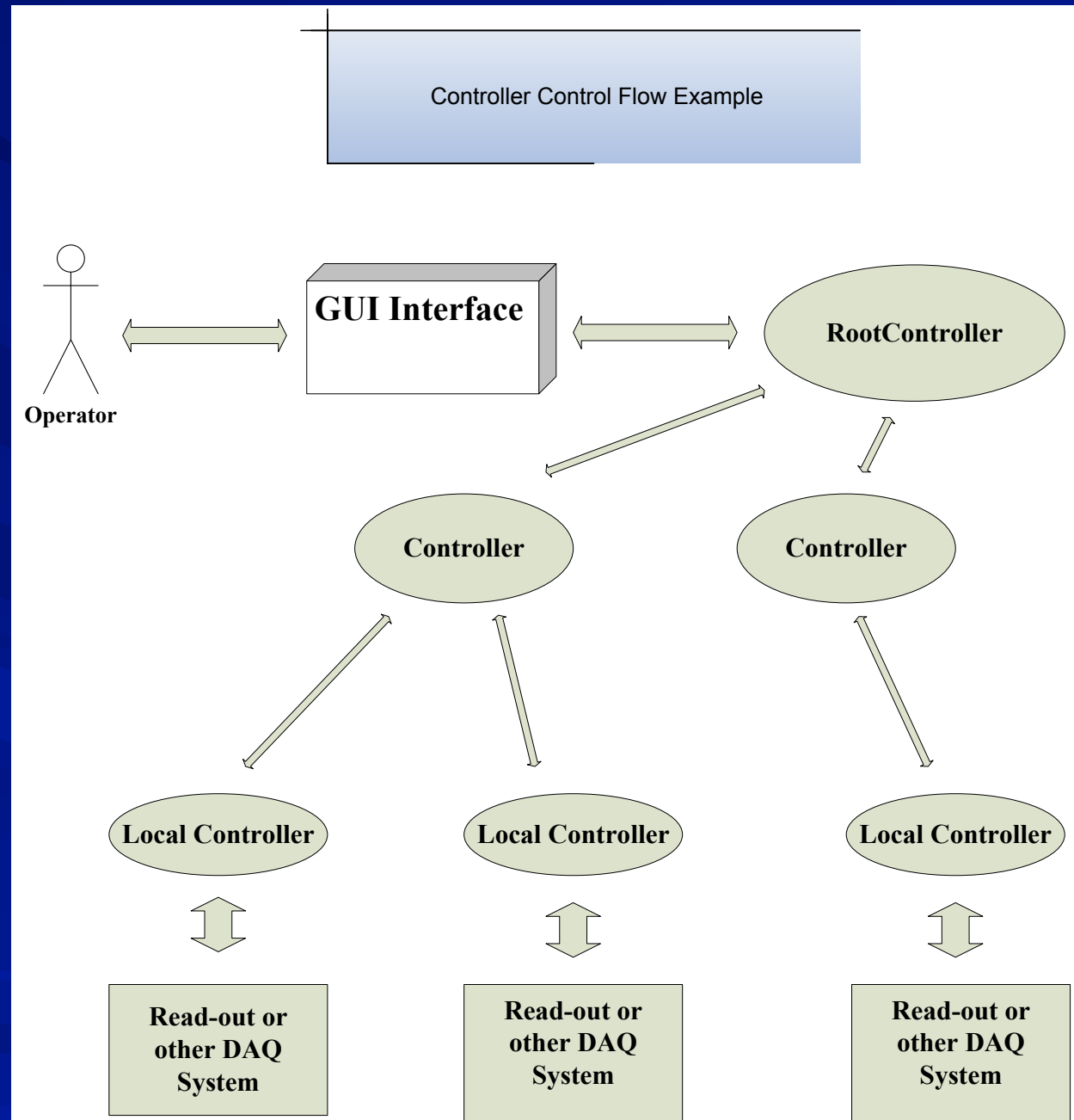
- 前端电子学读出：通过VME总线由PowerPC读出插件中的数据
 - 采用CBLT (Chained Block Transfer) DMA数据读出方案
 - 采用多事例读出方案
- 数据流：负责探测器数据通过网络传送
 - 插件→PowerPC→读出PC→在线机群→服务器→计算中心
- 在线软件：负责取数、测试和刻度运行过程中的控制和管理，还提供报错、运行参数管理、直方图和实时监测等功能
- 采用ATLAS TDAQ软件作为BESIII数据获取系统的基本框架

FrontEnd Readout Software 前端VME数据读出框架

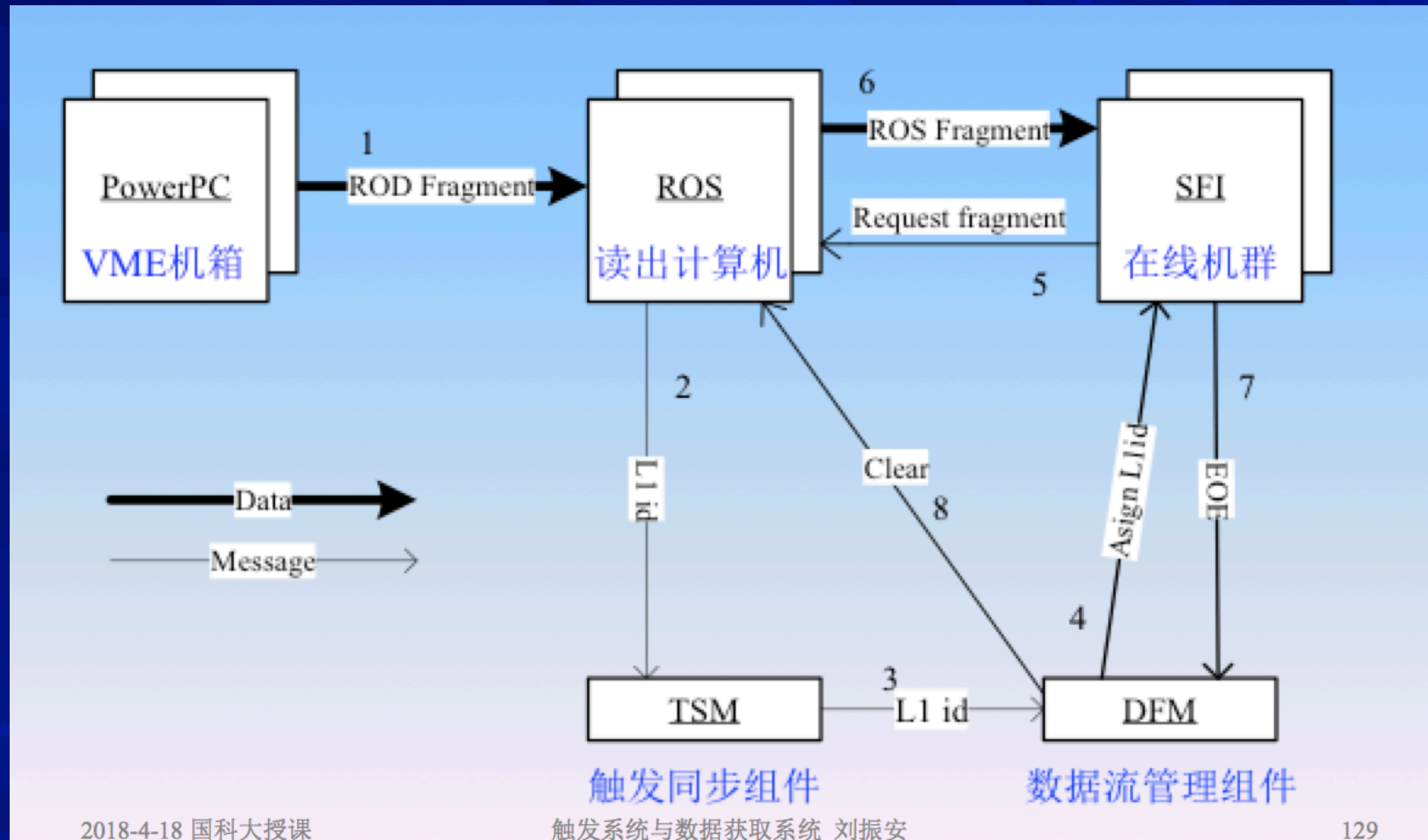
结构



RUN Control



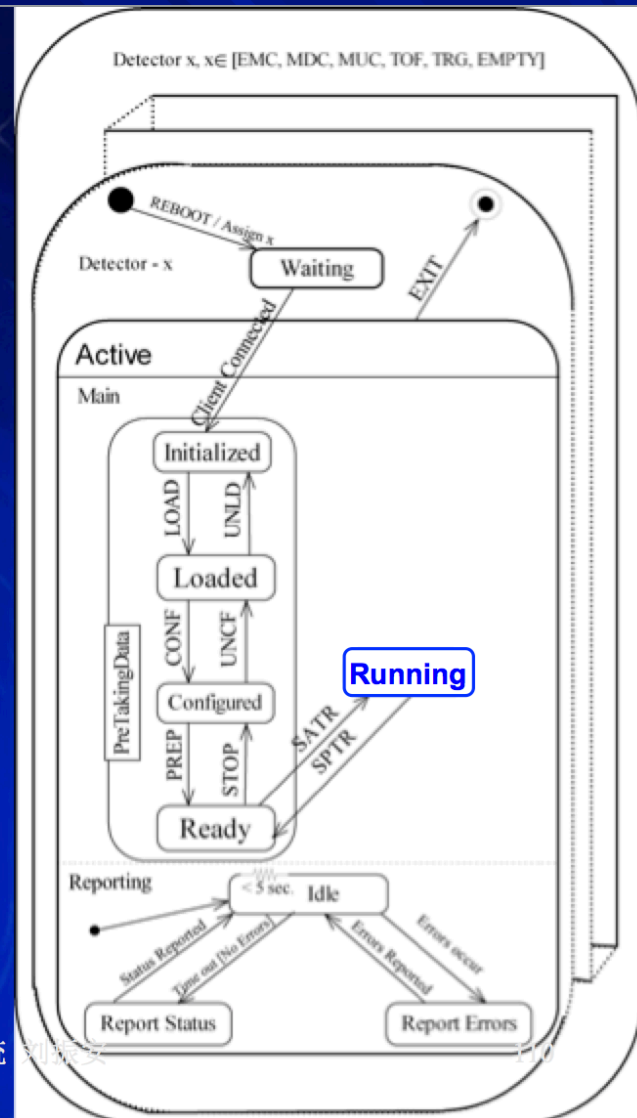
Control and Data Stream



Run States

状态图

Running状态



2018-4-18 国科大授课

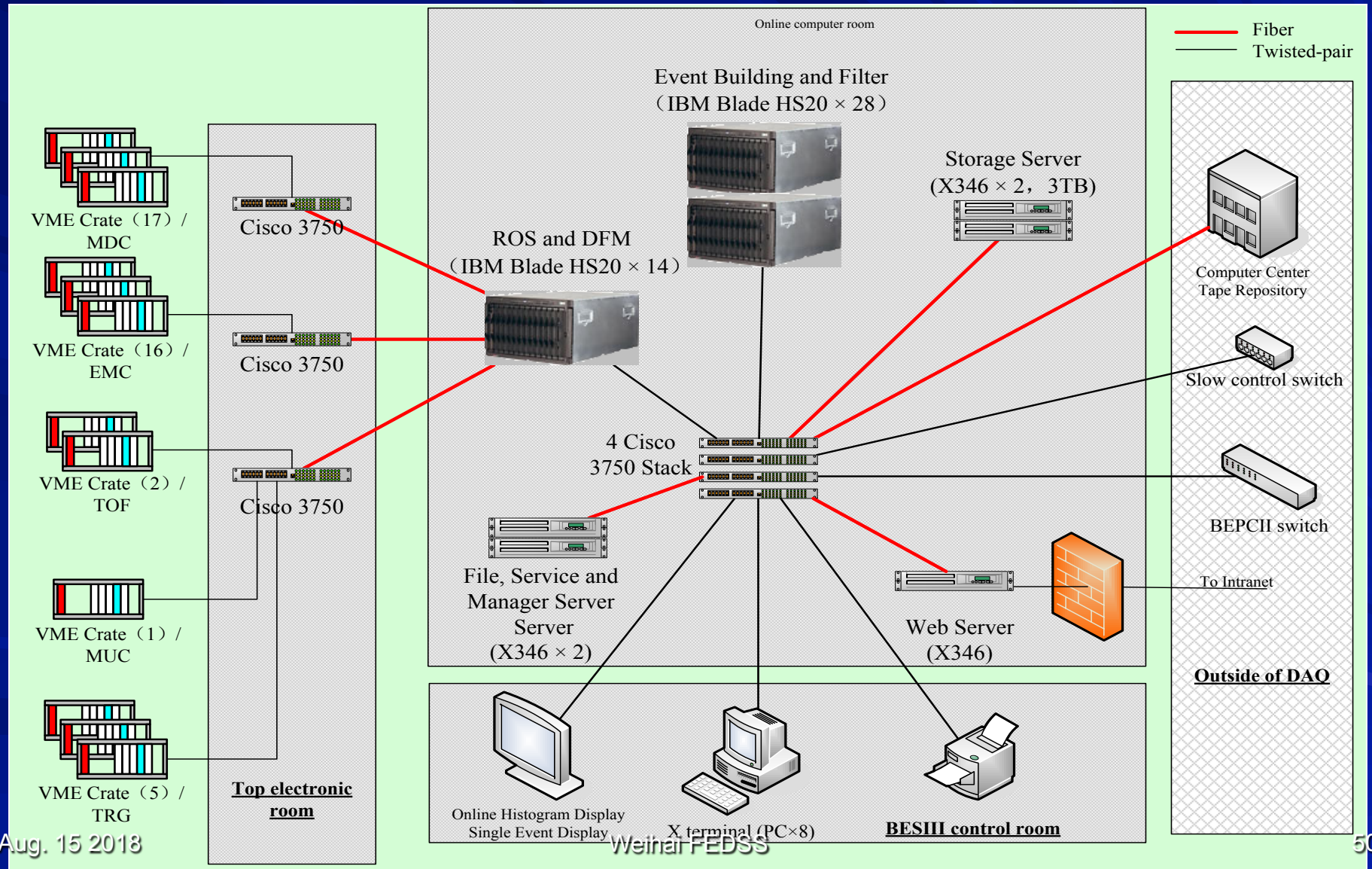
触发系统与数据获取系统

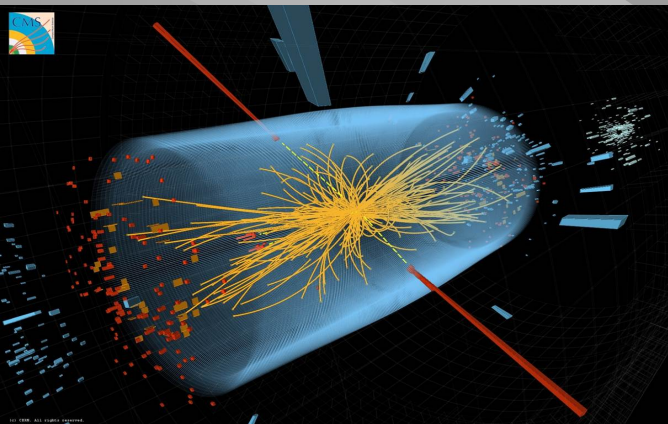
More on Hardware

- Ethernet Switch以太网交换机
 - 9 x Catalyst 3750 24 10/100/1000 + 4 SFP
- IBM服务器
 - 2个IBM刀片中心: 2 x 3.2GHz处理器 + 2 GB内存
 - 1个IBM刀片中心: 2 x 3.2GHz处理器 + 2 GB内存+ 1块千兆光纤网卡
 - 5台IBM x346服务器: 2 x 3.2GHz处理器 + 2 GB内存 + 1块千兆光纤网卡 + 1.5TB磁盘

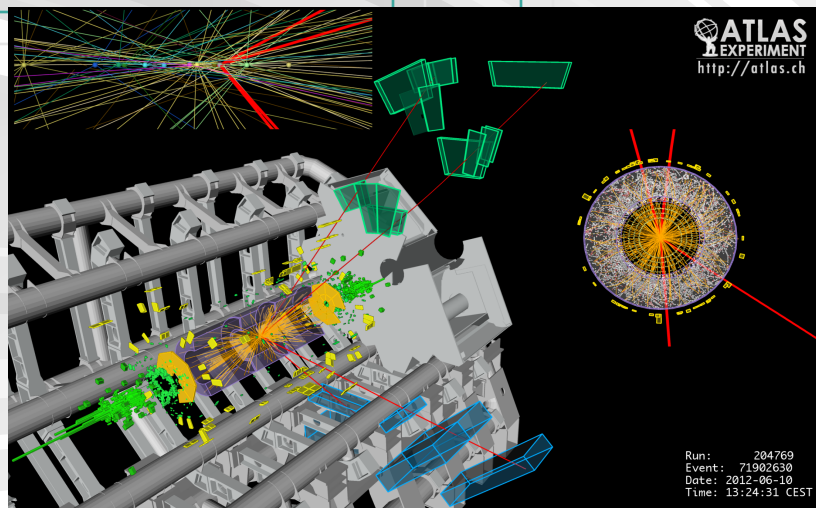


DAQ系统部署





Trigger and Data Acquisition for LHC experiments

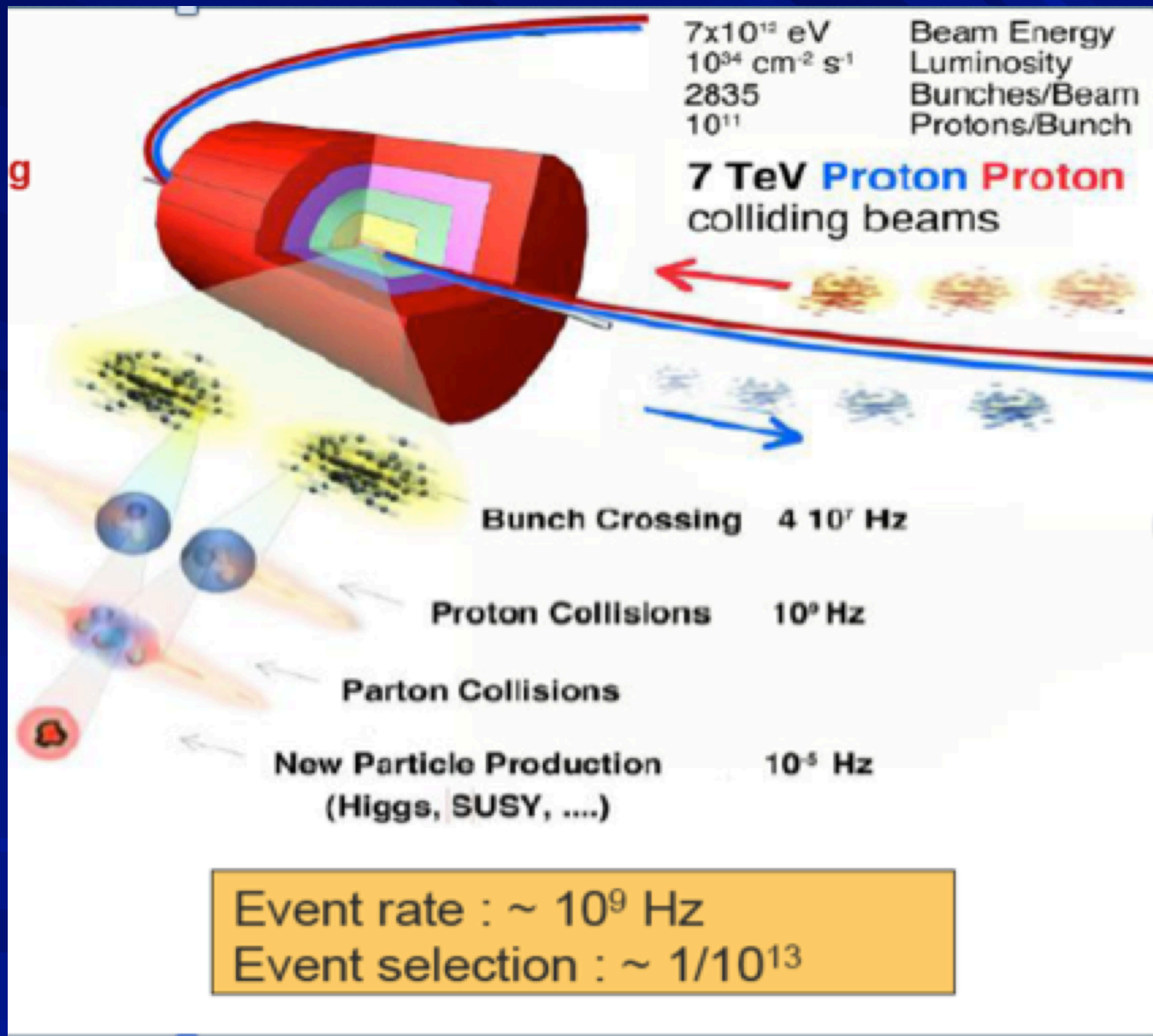


Aug. 15 2018

Weihai FEDSS

Run: 204769
Event: 71902630
Date: 2012-06-10
Time: 13:24:32 CEST

Challenging : The LHC T/DAQ



→ Collision Every 25 ns

Quarks

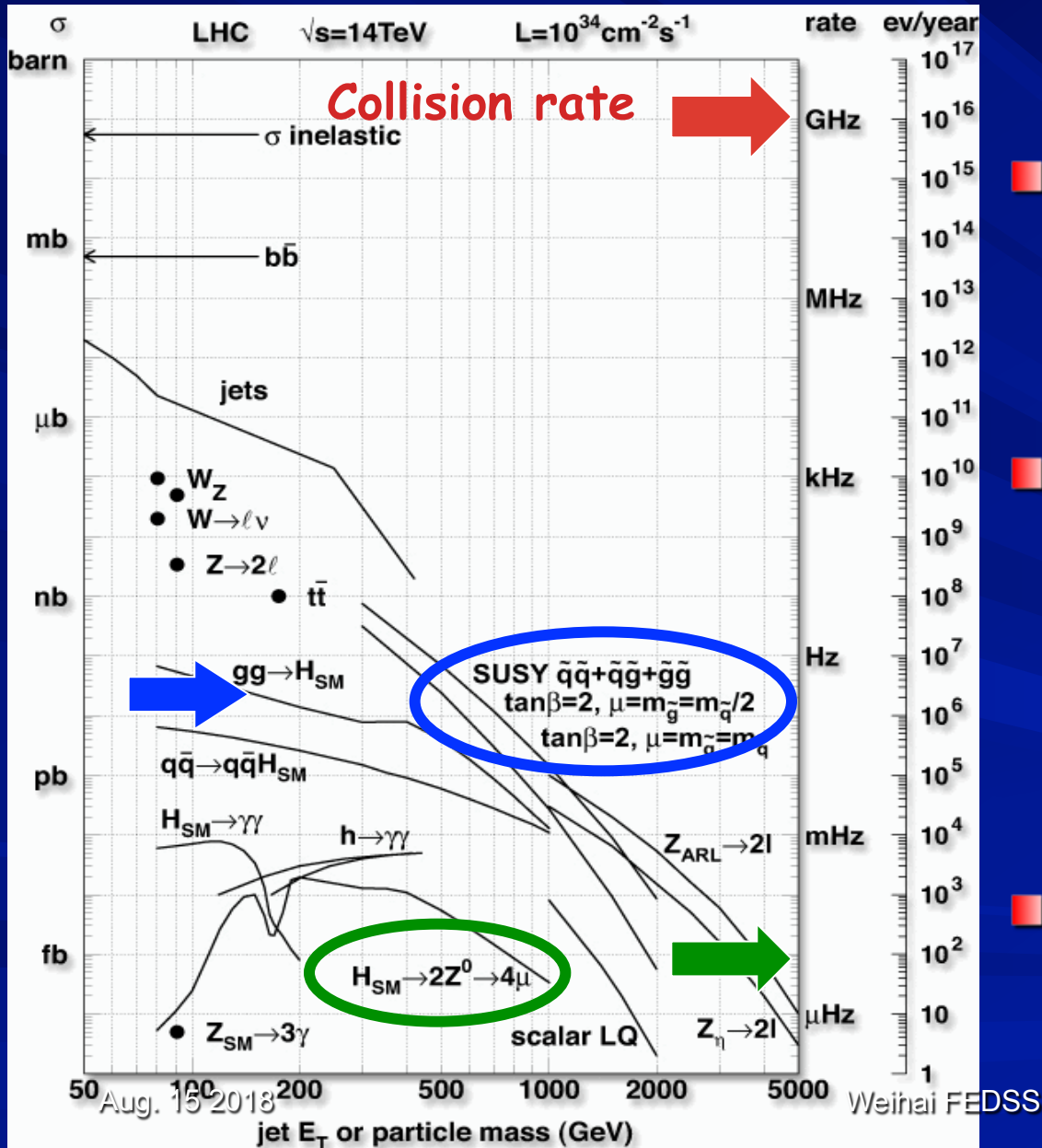
The LHC challenge

- "Interesting" physics is about 6-8 orders of magnitude below (EWK & Top)

- "Exciting" physics involving new particles/discoveries is ≥ 9 orders of magnitude below σ_{tot}

- We *just* 😊 need to efficiently identify these rare processes from the background before reading out & storing the whole event

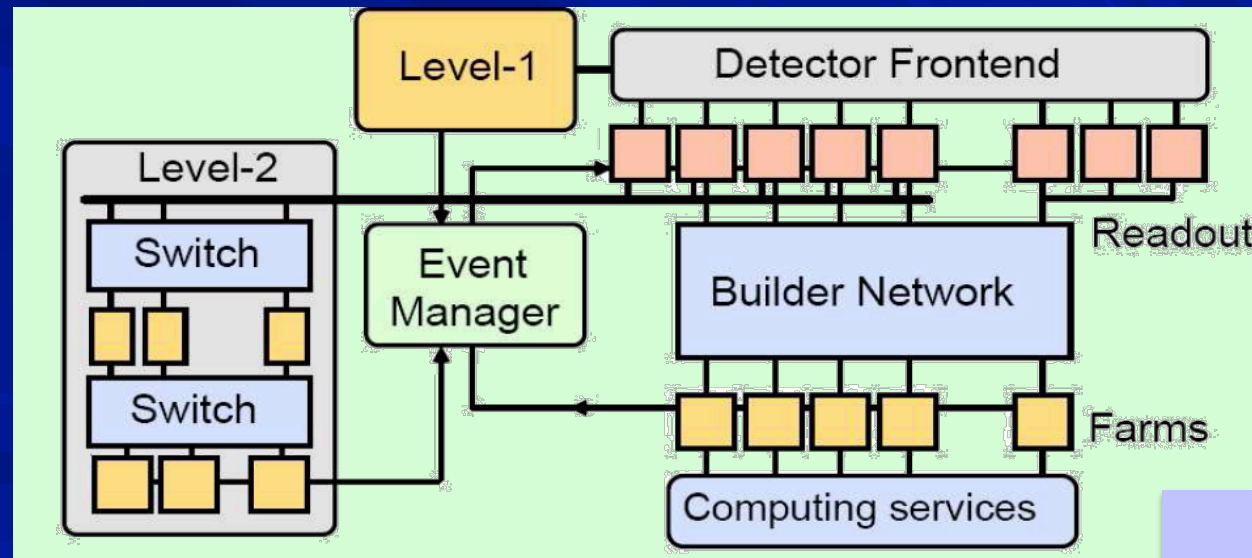
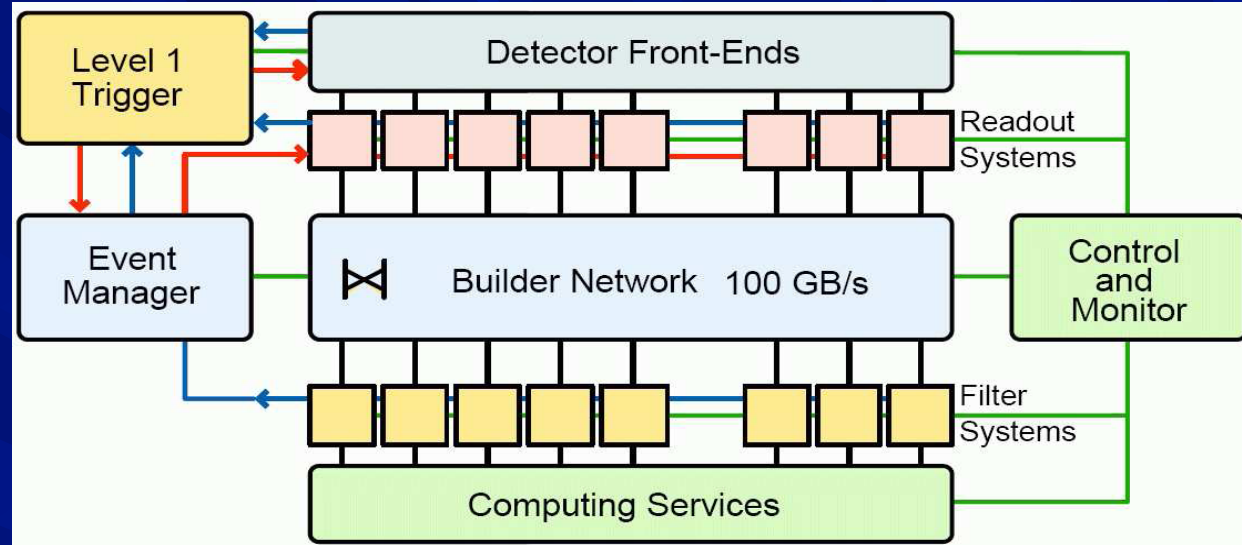
- Conclusion: Need to watch out for high transverse momentum electrons, jets or muons



After L1 → Two philosophies

- Send everything, ask questions later (ALICE, CMS, LHCb)
- Send a part first, get better question
Send everything only if interesting (ATLAS)

Push vs. Pull
That is the question?

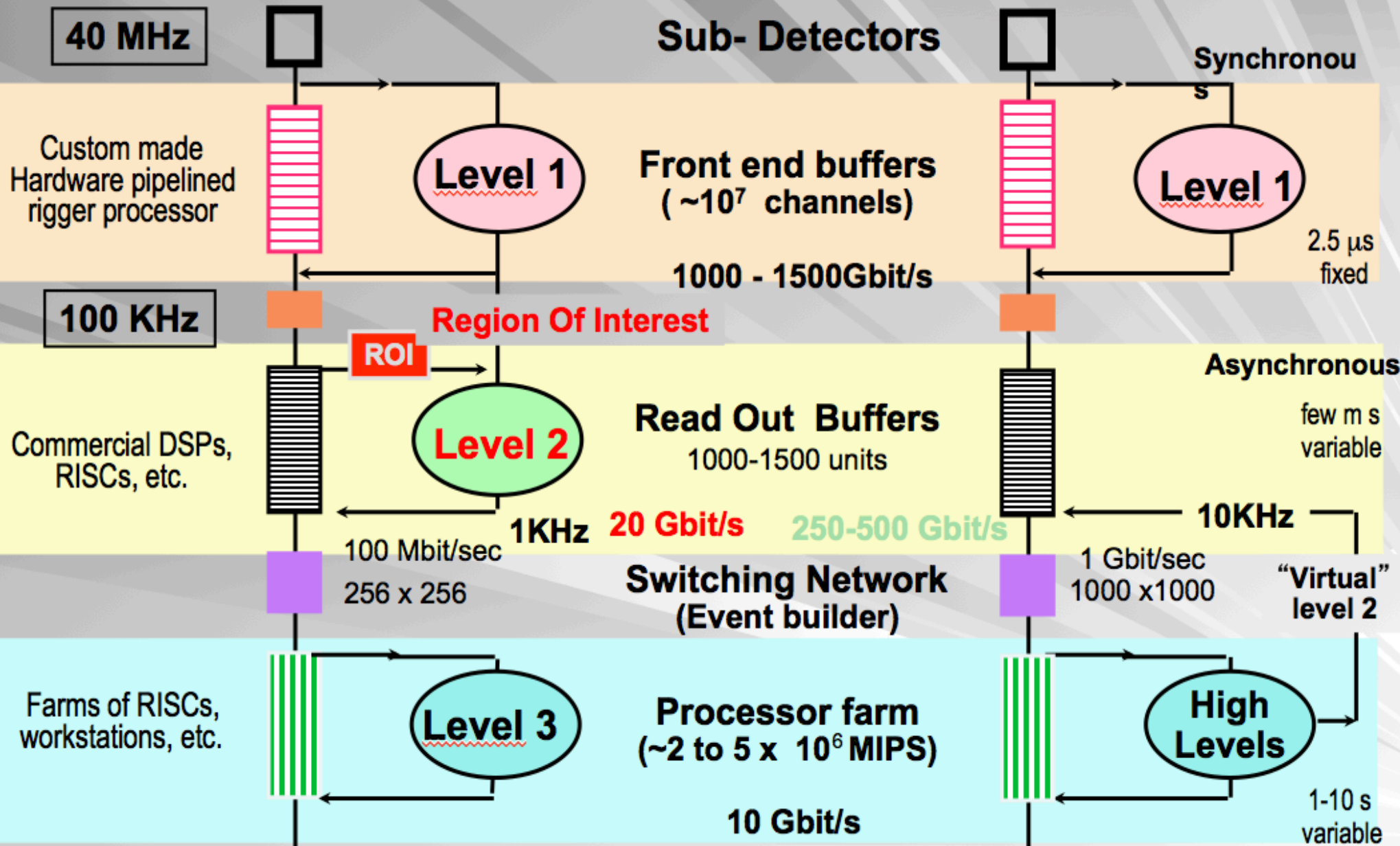


LHC Logical structure

ATLAS

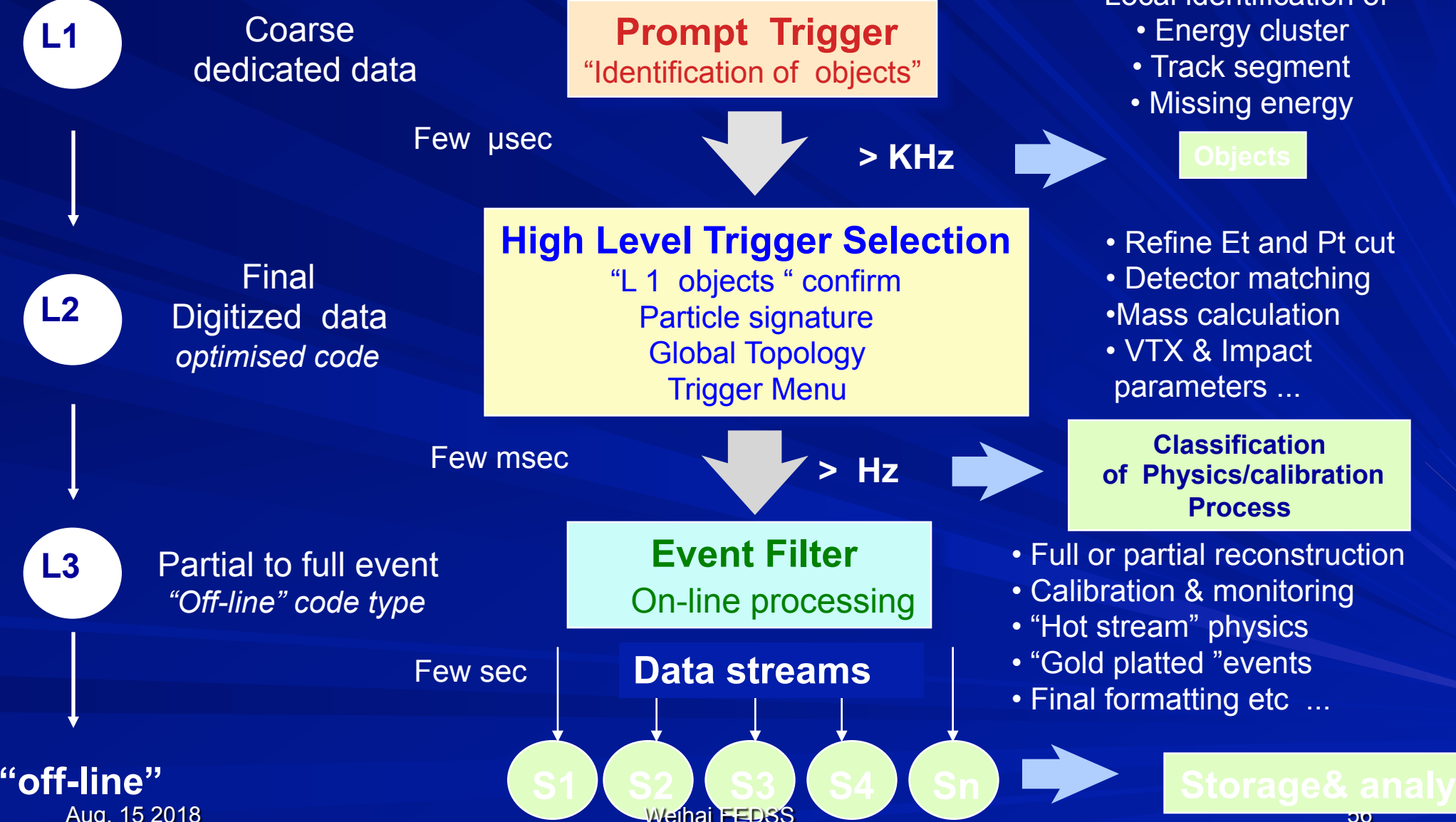
CMS

Sub-Detectors



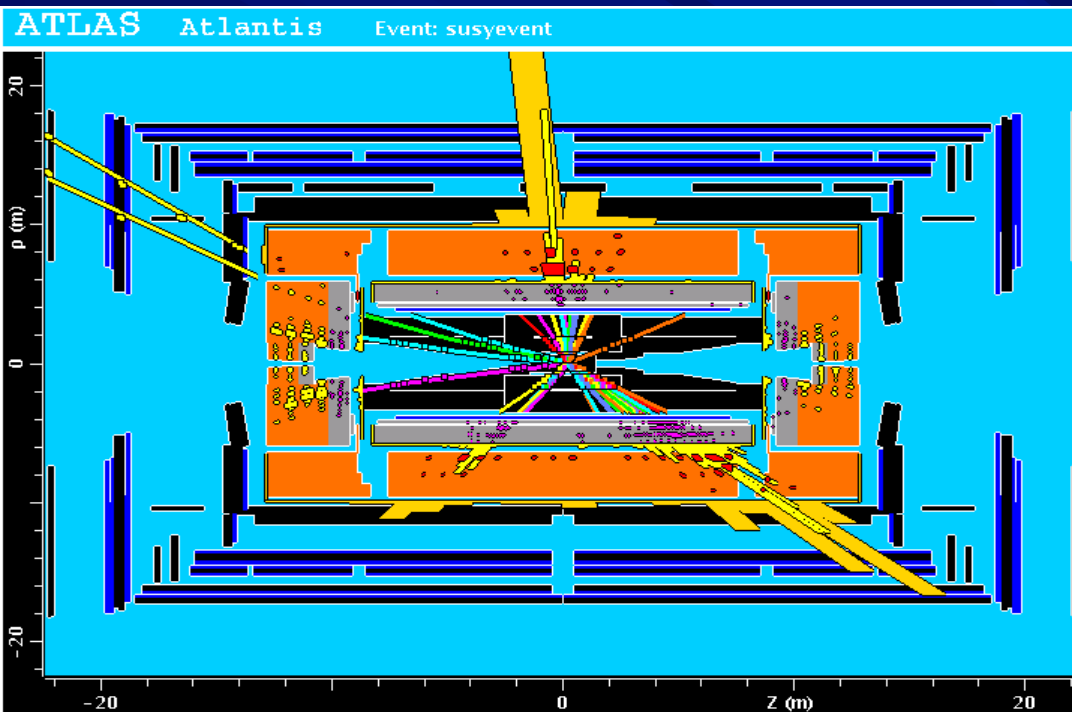
"Logical Strategy" for event selection

Logical steps

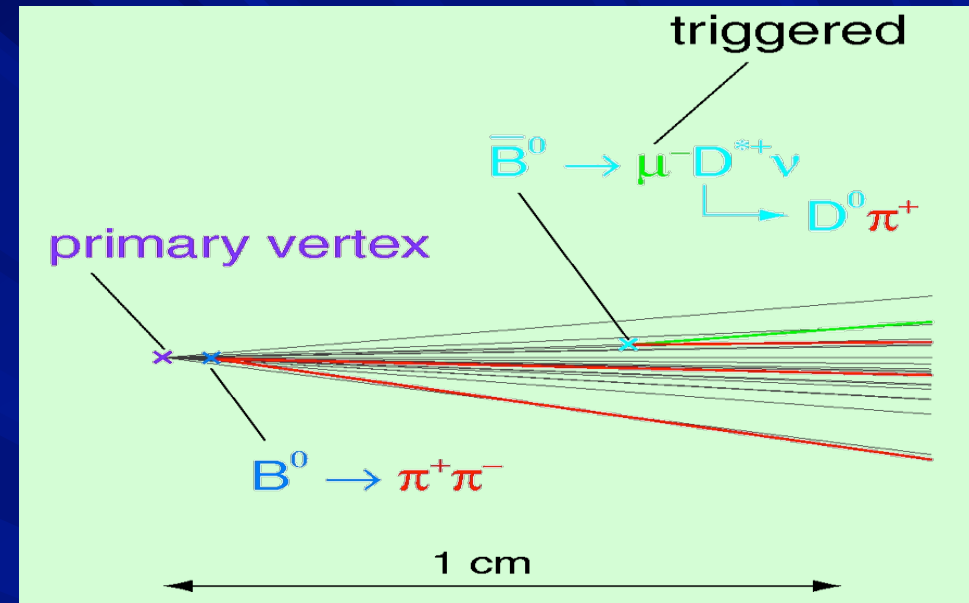


"off-line"

High Level Triggers



Complicated Event structure with hadronic jets (ATLAS) or secondary vertices require full detector information



Methods and algorithms are the same as for offline reconstruction

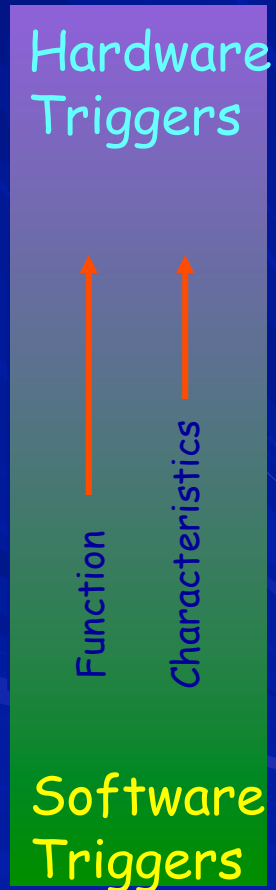
On-Off line boundaries

- **Detectors are becoming more stable and less faulty**
 - High efficiency, Low failure rate
 - Powerfull “on-line” diagnostics and error recovery (expert systems)
- **On-line computing is increasing and not doing only “data collection”**: More complex analysis is moving on-line
 - » “Off-line” type algorithms early in the selection chain (b tag ..)
 - » Selection of “data streams” --> Important role of the “Filter”
 - » Precise alignment needed for triggering
 - » Detector calibration using Physics process available
 - » On-line calibration and correction of data possible
- **Common aspect** →
 - Algorithms, Processing farms, Databases...
 - use similar hw/sw components (PC farms..)

Boundaries become flexible

Present evolution (SLHC ...)

- Higher level trigger decisions are migrating to the lower levels → **Software Migration is following functional migration**
 - Correlations that used to be done at Level 2 or Level 3 in are now done at Level 1.
 - More complex trigger (impact parameter!) decisions at earlier times (HLT) → Less bandwidth out of detector?
- **Boundaries**
 - L2 and L3 are merging into High Levels Triggers
 - DAQ and trigger data flow are merging
 - On-line and off-line boundaries are flexible
- **Recent Developments in Electronics**
 - Line between software and hardware is blurring
 - Complex Algorithms in hardware (FPGAs)
 - Possible to have logic designs change after board layout
 - Fully commercial components for high levels.



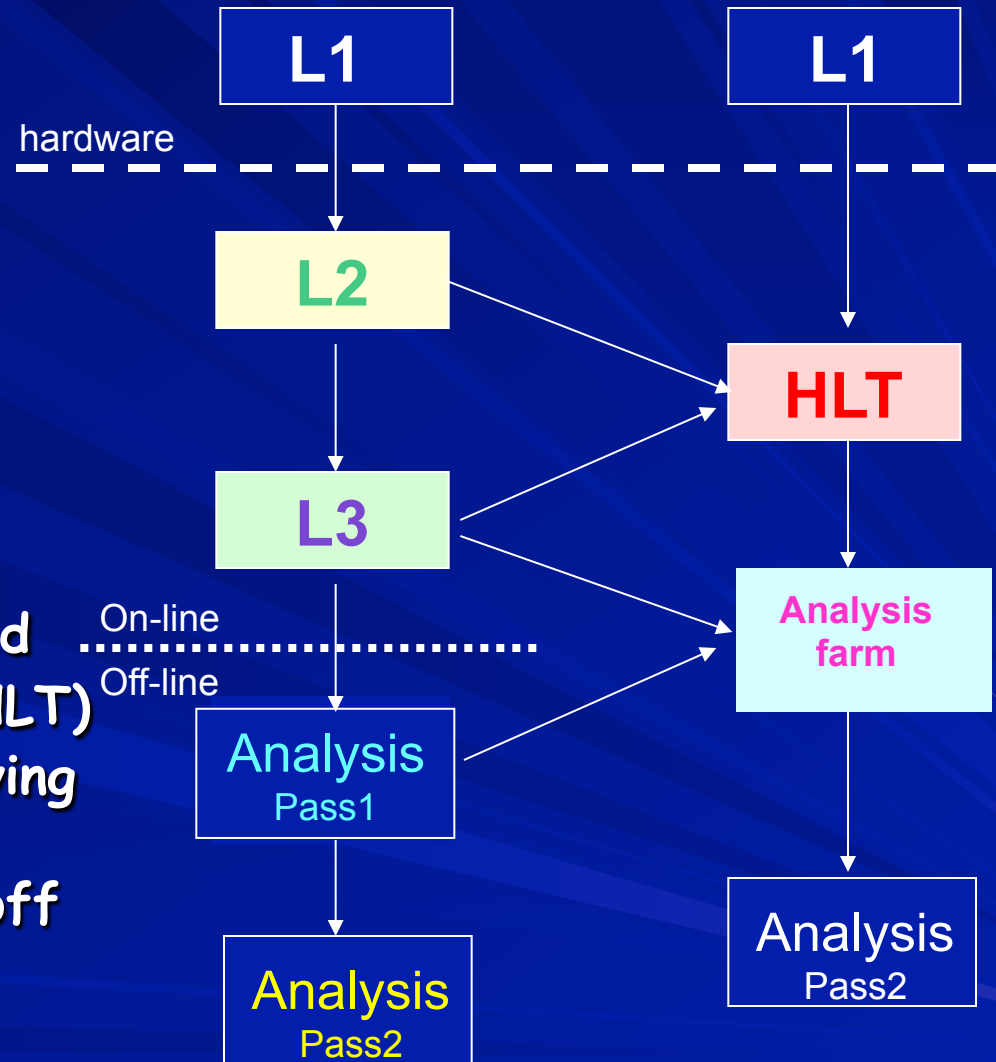
Summary of T/DAQ architecture evolution

■ Today

- Tree structure and partitions
- Processing farms at very highest levels
- Trigger and DAQ dataflow are merging

■ Near future

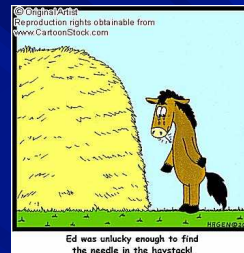
- Data and control networks merged
- Processing farm already at L2 (HLT)
- More complex algorithms are moving on line
- Boundaries between on-line and off-line are flexible
- Commodity components at HLT



Backups

实验物理中Trigger/触发的困难

大海捞针：find a needle in a Haystack



1. 怎么办哪??
无从下手!!

5. 愁死
啦!!!

2. 苦干加
实干不
信找不
到!!



4. 有没有
可能???



3. 不行啊,
哪天能
找到
啊!!



6. 别愁啦, 快找
触发组啊!!

实验物理中的Trigger/触发

加速器物理实验中的触发判选

- 设计高效的触发判选
 - 定义好事例(缝衣针)和本底(麦秸)的特征
 - 找出不同(界限)
 - 节省资源
 - 高效
 - 实时



本底事例



本底事例



好事例



找到的好事例