Introduction fo Front-End Electronics in Particle Physics

FEDSS 2018 Weihai 威海

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Organization for Micro-Electronics desiGn and Applications

Outline

1. Low noise charge preamps : pixel readout
2. Large dynamic range/high speed designs : calorimeters
3. Trends and future

Lectures for physicists, not electronics engineers => will concentrate on front-end and performance of detector, not on detailed engineering

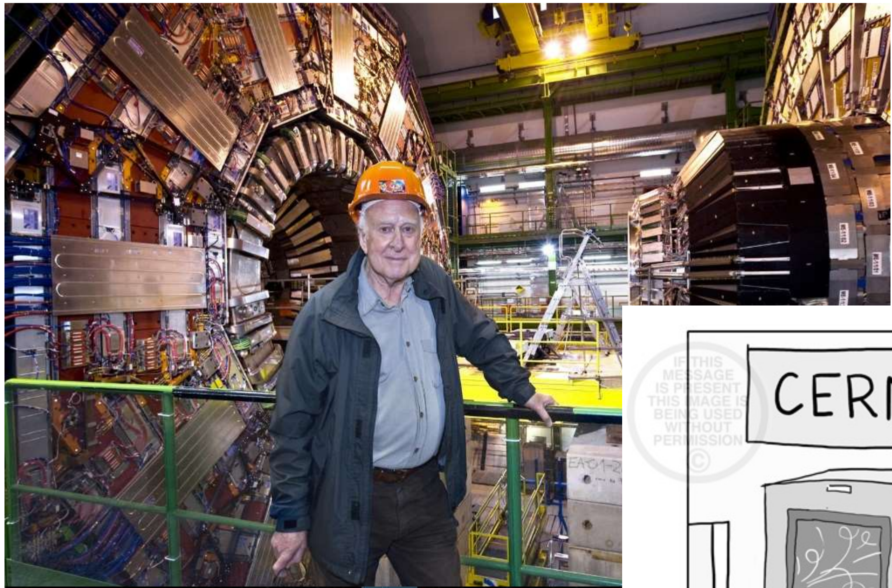
Many more slides than allocated time : don’t be afraid !

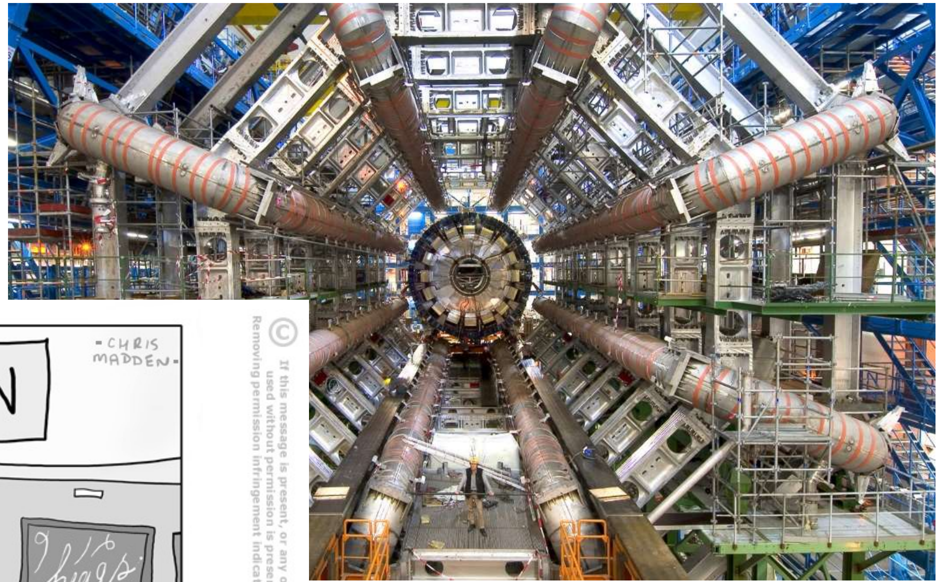
I will skip many details : they are for further reference

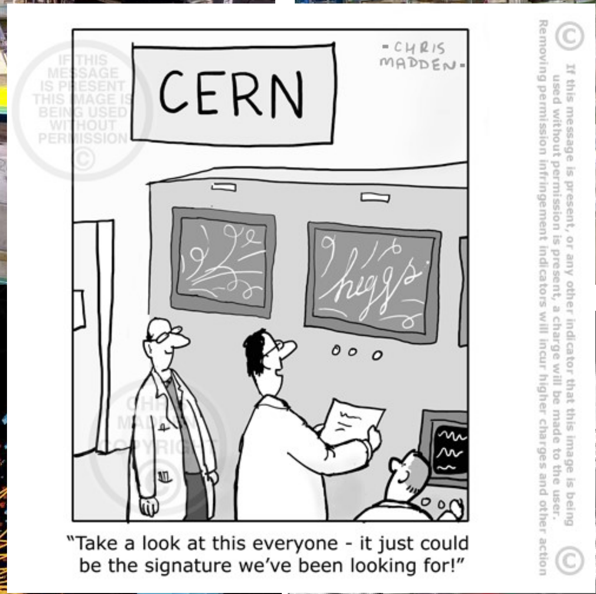
Many thanks to the organizers for their kind invitation : 谢谢

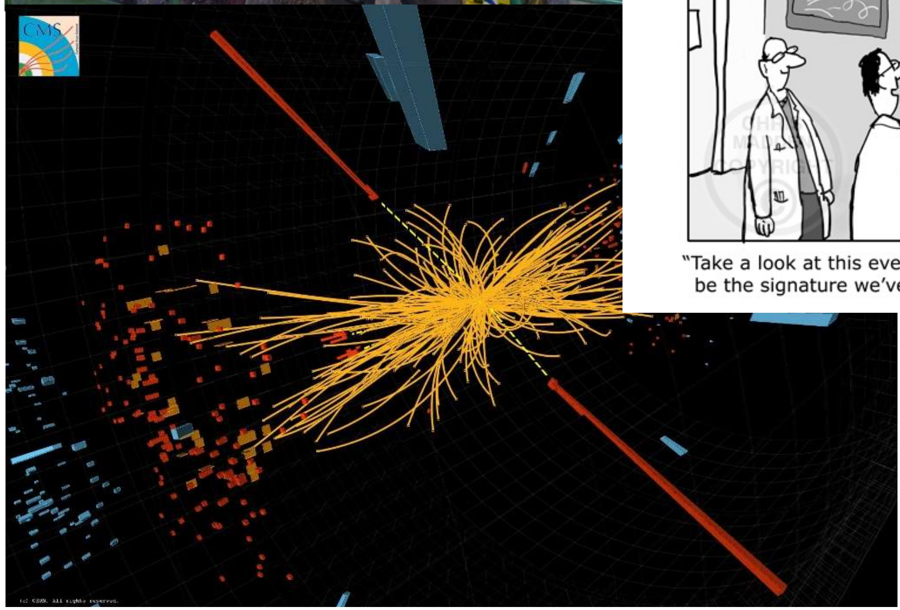
Electronics in experiments

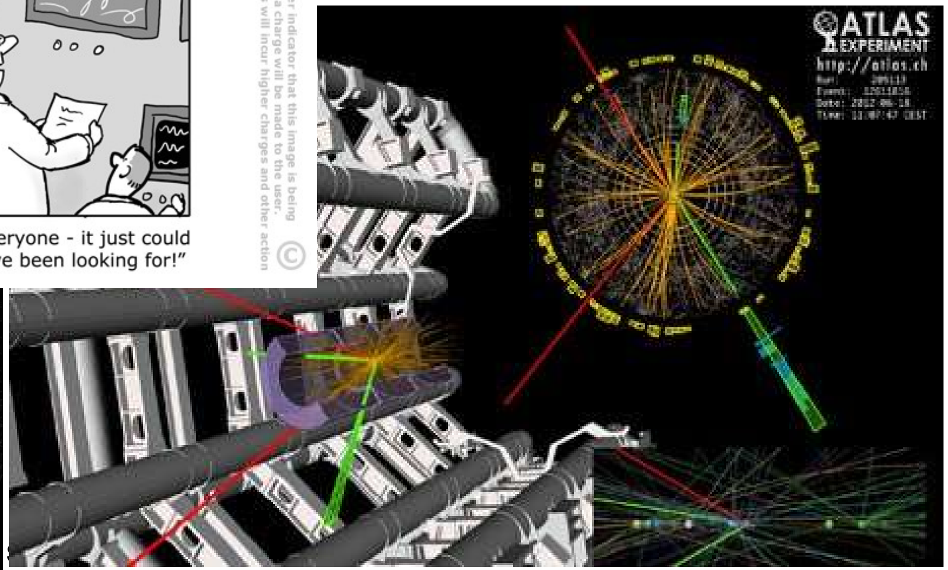
- A lot of electronics in the experiments…which impacts the detectors





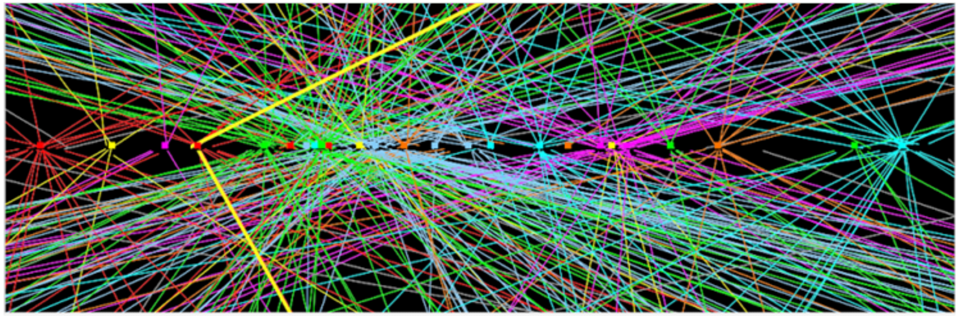


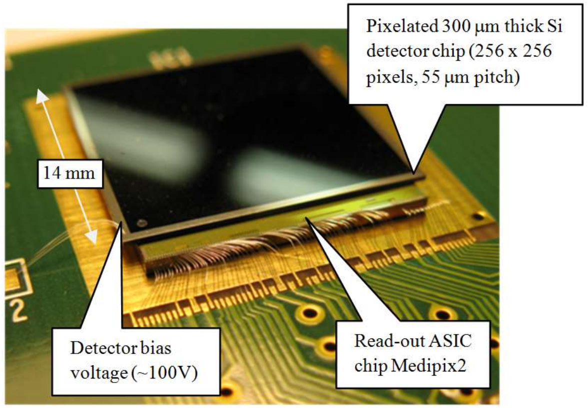


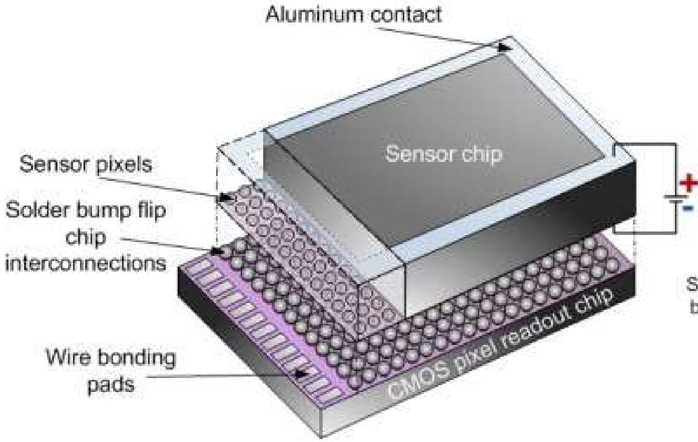


Electronics enabling new detectors : trackers

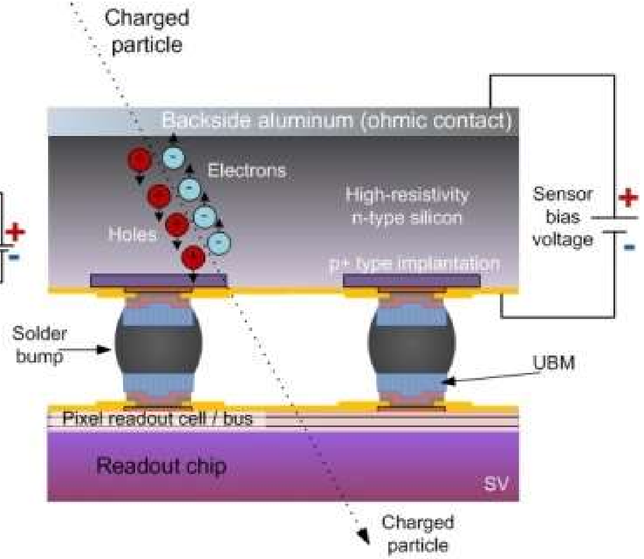
- Measurement of (charged) particle tracks
  - millions of pixels (~100 µm)
  - binary readout at 40 MHz
  - High radiation levels
  - Made possible by ASICs







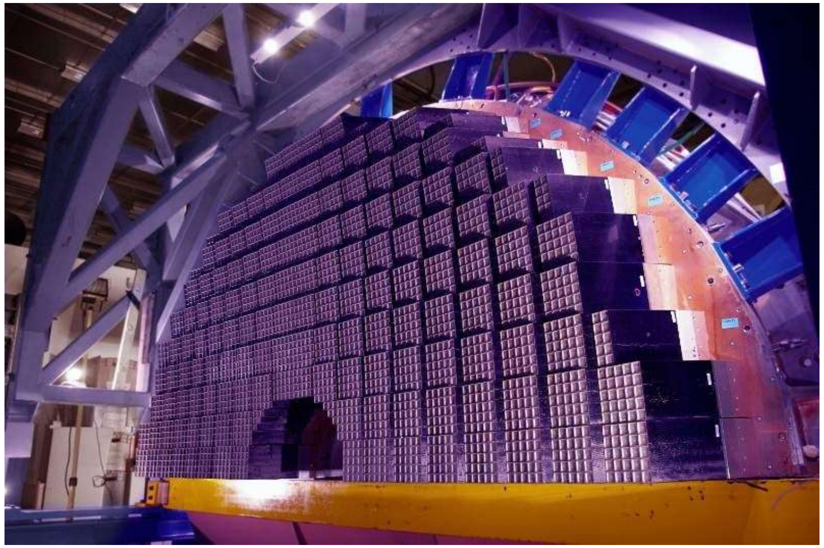
Generic pixel detector



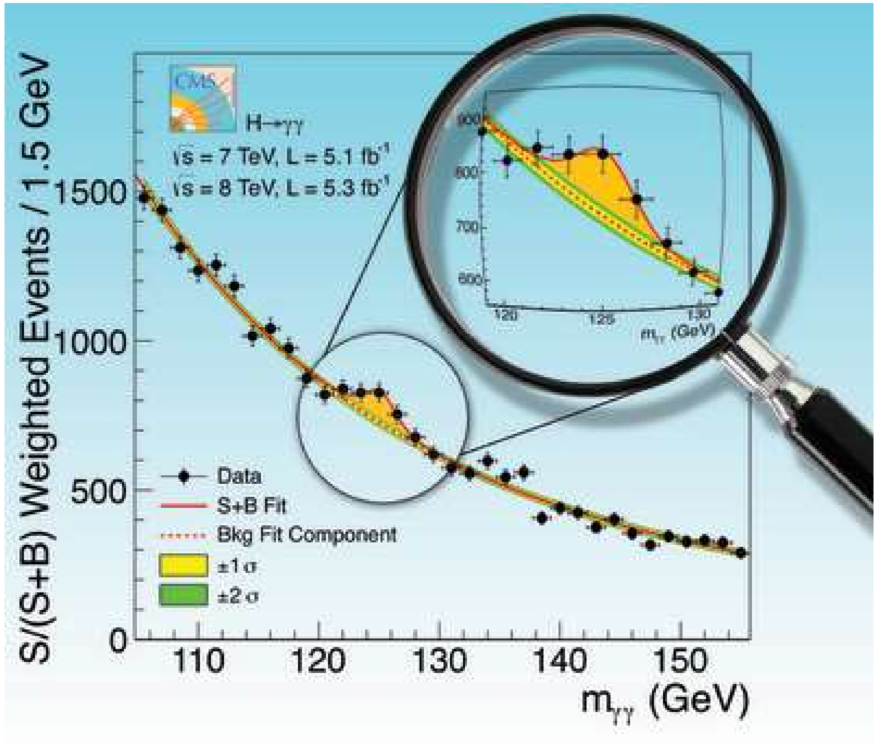
Cross-sectional cut

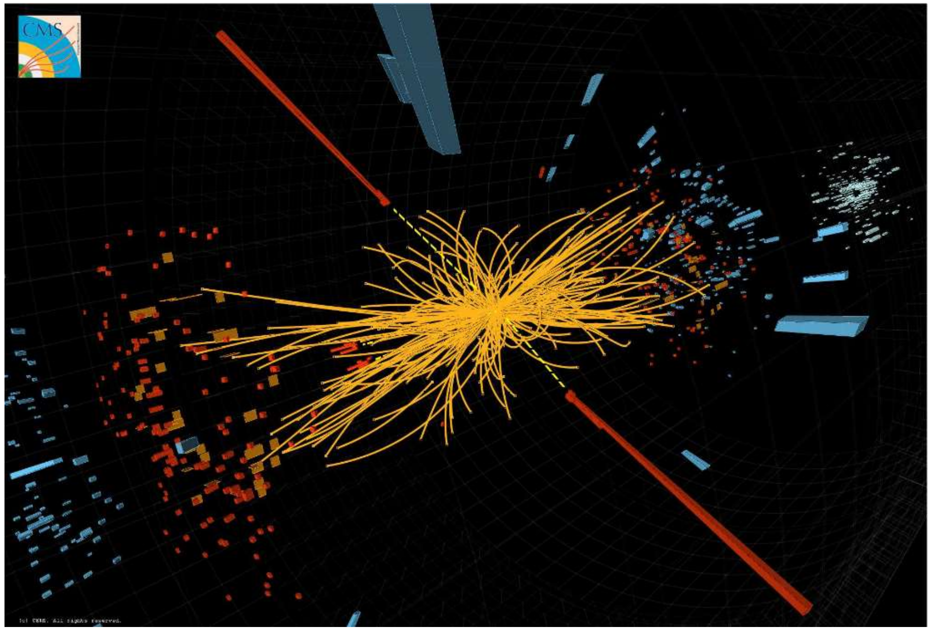
Importance of electronics : calorimeters

- Large dynamic range (10^4-10^5)
- High Precision ~1%
  - Importance of low noise, uniformity, linearity…
  - Importance of calibration



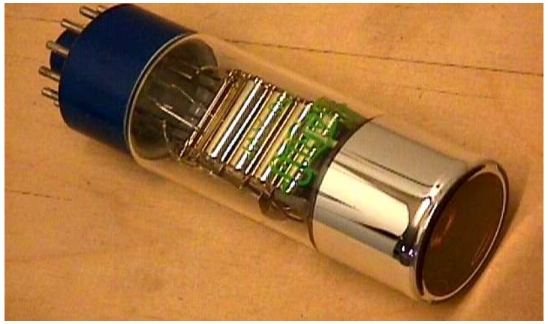
H -> γ γ in CMS calorimeter

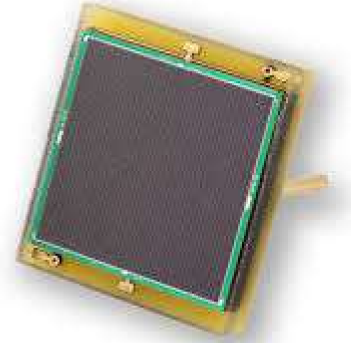


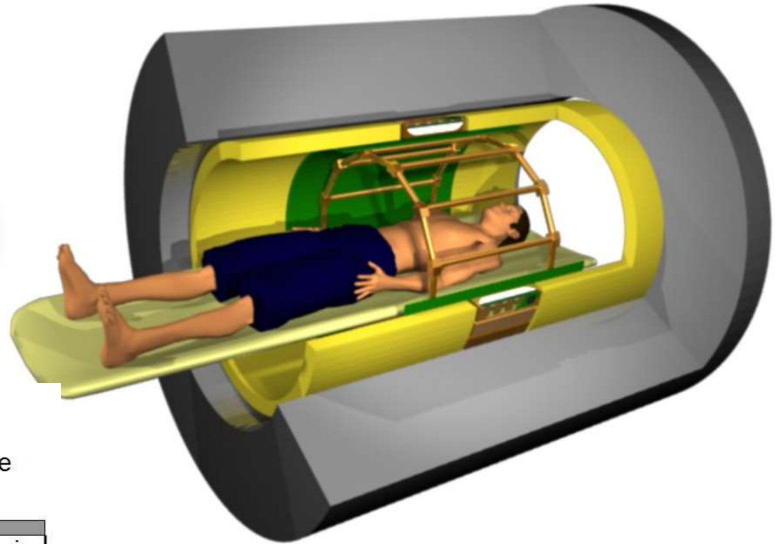


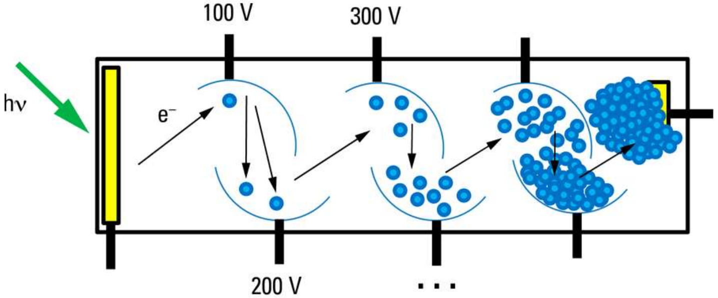
Single photon sensors & timing information

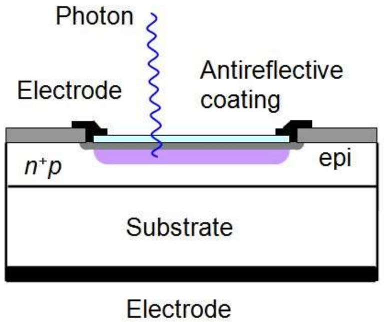
- Photomultipliers, silicon photomultipliers

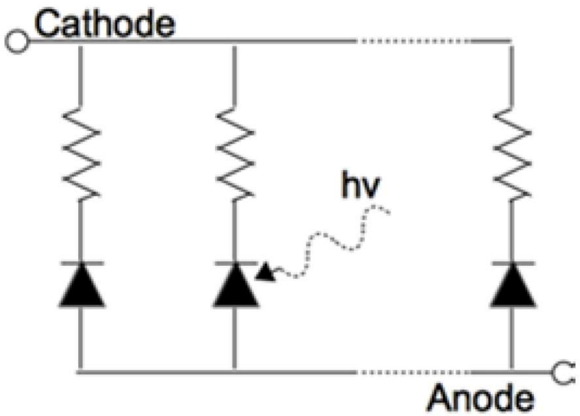


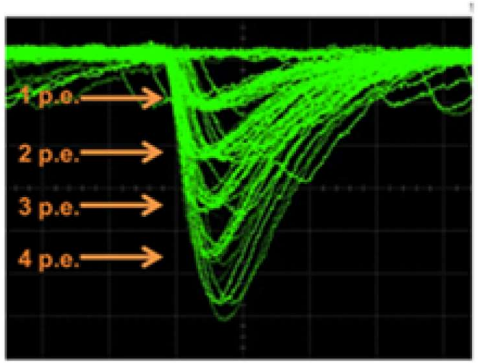


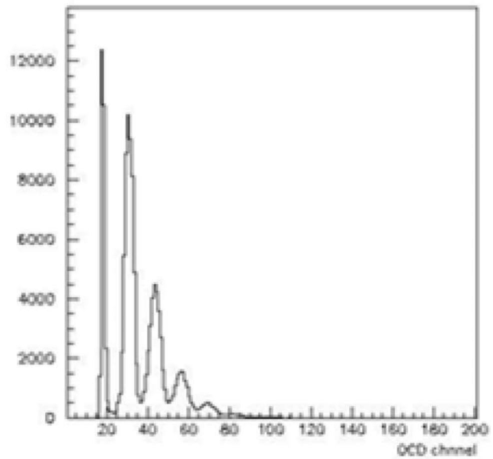






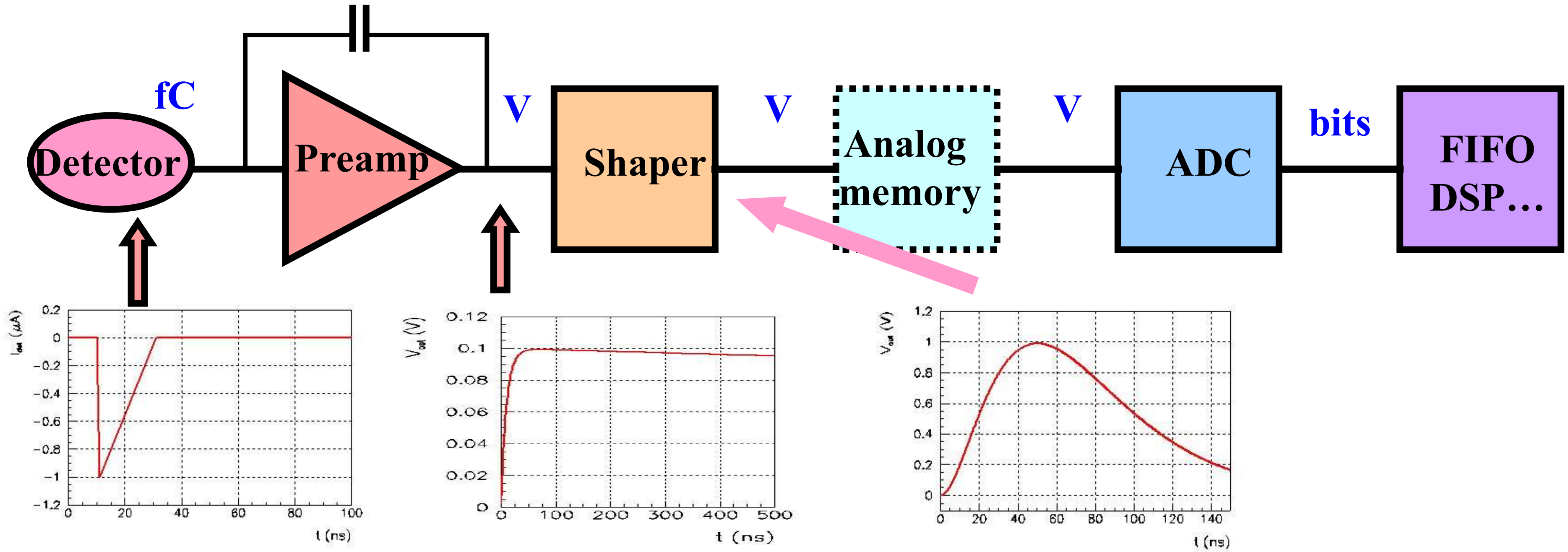






Overview of readout electronics

- Most front-ends follow a similar architecture



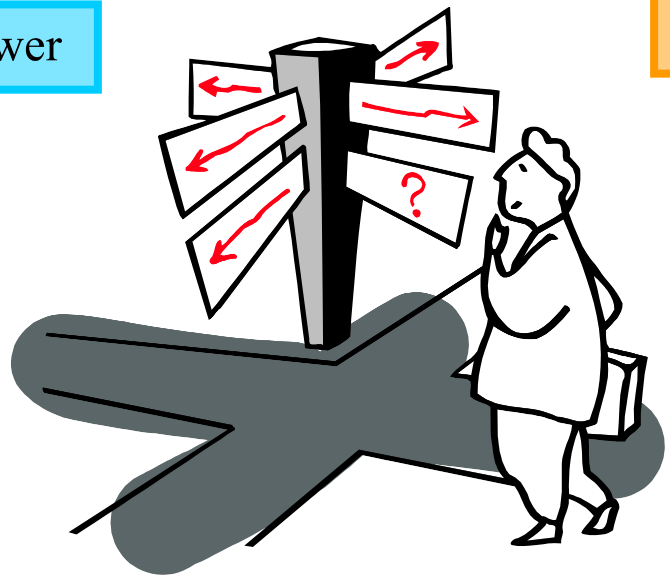
- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discris, TDCs)
- Several thousands to millions of channels
- Trends : high speed, low power

Readout electronics : requirements

Low noise

Low power

High speed



Large dynamic range

High reliability

Radiation hardness

Low material

Low cost !

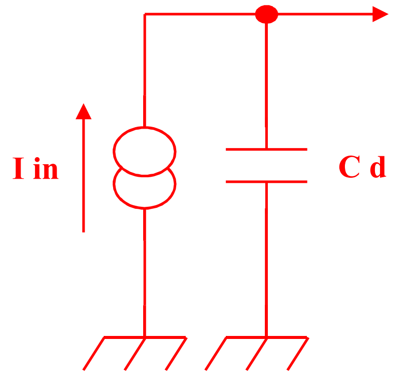
(and even less)

Detector modelization

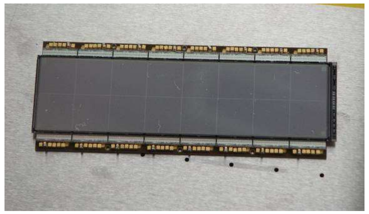
- Detector = capacitance Cd
  - Pixels/strips : 0.1-10 pF
  - PMs/SiPMs : 3-300 pF
  - Ionization chambers 10-1000 pF
  - Sometimes effect of transmission line

- Signal : current source
  - Pixels : ~100e-/µm
  - PMs : 1 photoelectron -> 10^5-10^7 e-
  - Modelized as an impulse (Dirac) : $i(t)=Q_0\delta(t)$

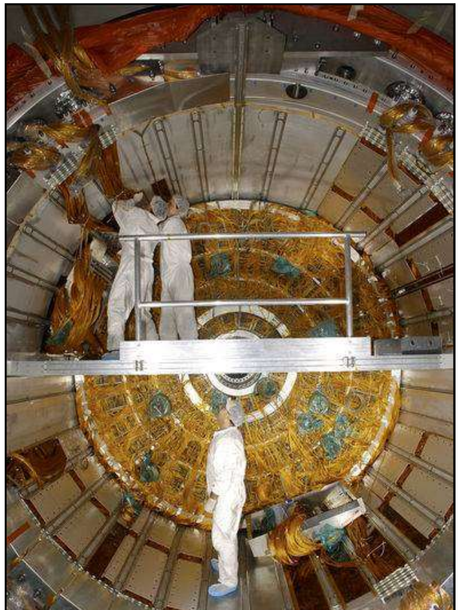
- Missing :
  - High Voltage bias
  - Connections, grounding
  - Neighbours
  - Calibration…



Detector modeilization



CMS pixel module



ATLAS LAr calorimeter

Vacuum Photomultipliers

G = $10^5 - 10^7$

Cd ~ 10 pF

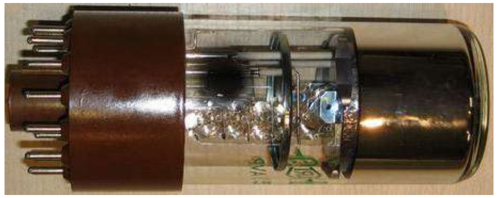
L ~ 10 nH

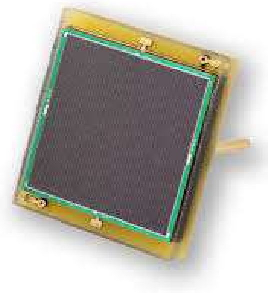
Silicon Photomultipliers

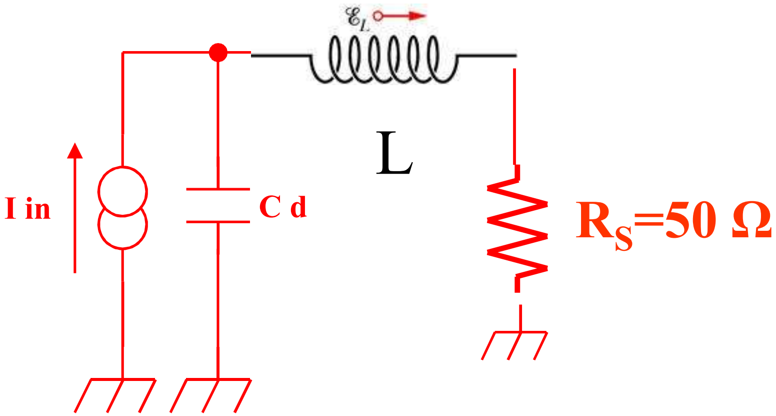
G = $10^5 - 10^7$

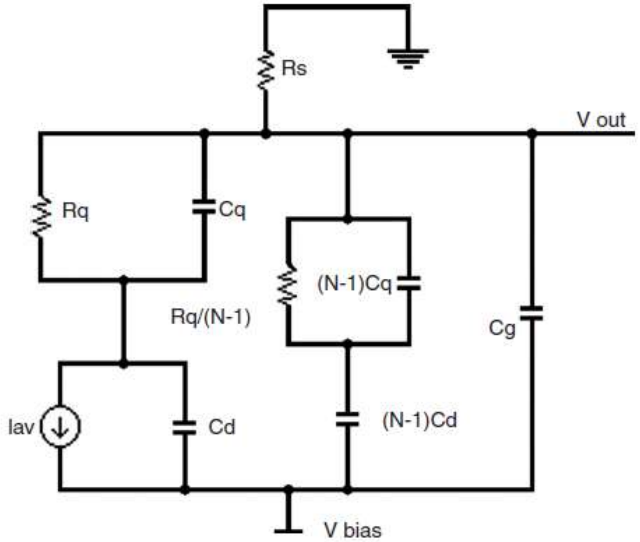
C = 10 - 400 pF

L = 1 – 10 nH









Optimizing signal shape for timing

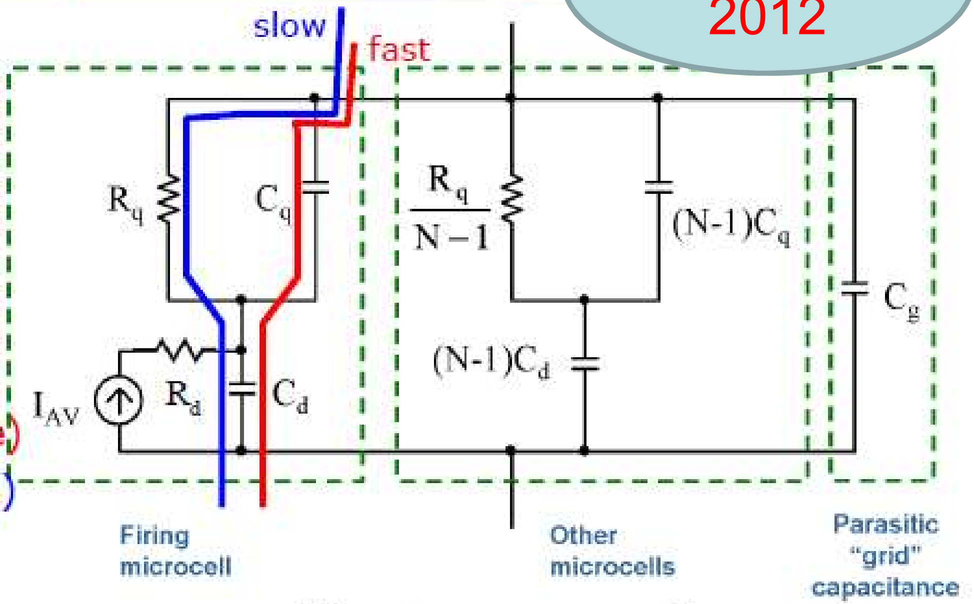
Collazuol 2012

Single cell model → $(R_d||C_d)+(R_q||C_q)$

SiPM + load → $(||Z_{cell})||C_{grid} + Z_{load}$

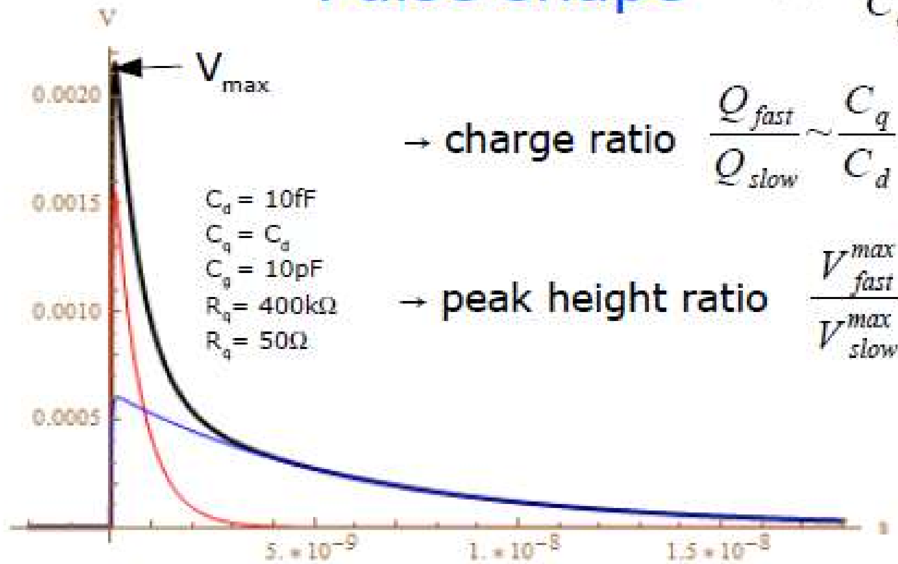
Signal = slow pulse ($\tau_{d\ (rise)}, \tau_{q\text{-}slow\ (fall)}$) +
+ fast pulse ($\tau_{d\ (rise)}, \tau_{q\text{-}fast\ (fall)}$)

- $\tau_{d\ (rise)} \sim R_d(C_q+C_d)$
- $\tau_{q\text{-}fast\ (fall)} = R_{load}\ C_{tot}$ (fast; parasitic spike)
- $\tau_{q\text{-}slow\ (fall)} = R_q\ (C_q+C_d)$ (slow; cell recovery)



Pulse shape

$$V(t) \simeq \frac{Q}{C_q+C_d}\left(\frac{C_q}{C_{tot}} e^{\frac{-t}{\tau_{FAST}}} + \frac{R_{load}}{R_q}\frac{C_d}{C_q+C_d} e^{\frac{-t}{\tau_{SLOW}}}\right)$$



→ charge ratio $\frac{Q_{fast}}{Q_{slow}} \sim \frac{C_q}{C_d}$

→ peak height ratio $\frac{V_{fast}^{max}}{V_{slow}^{max}} \sim \frac{C_q^2 R_q}{C_d C_{tot} R_{load}}$

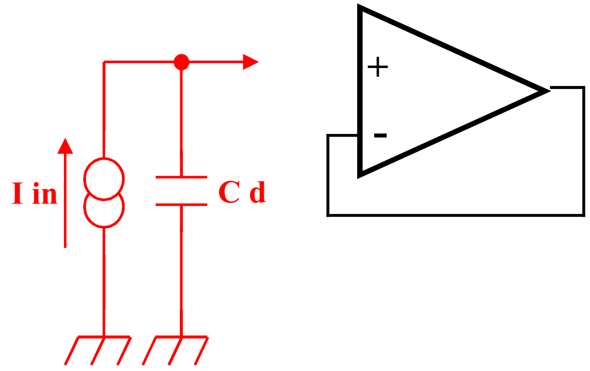
increasing with Rq and $1/R_{load}$
(and Cq of course)

Increasing C_q/C_d or/and R_q/R_{load}
→ spike enhancement
→ better timing

G.Collazuol - PhotoDet 2012

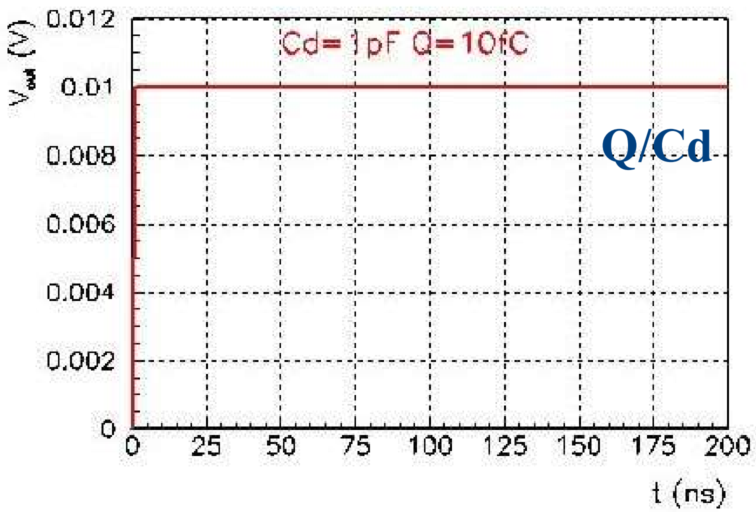
Reading the signal

- Signal
  - Signal = current source
  - Detector = capacitance C_d
  - Quantity to measure
    - Charge => integrator needed
    - Time => discriminator + TDC



- Integrating on Cd
  - Simple : $V = Q/C_d$
  - « Gain » : $1/C_d$: 1 pF -> 1 mV/fC
  - Need a follower to buffer the voltage… => parasitic capacitance
  - Gain loss, possible non-linearities
  - crosstalk
  - Need to empty Cd…

Voltage readout

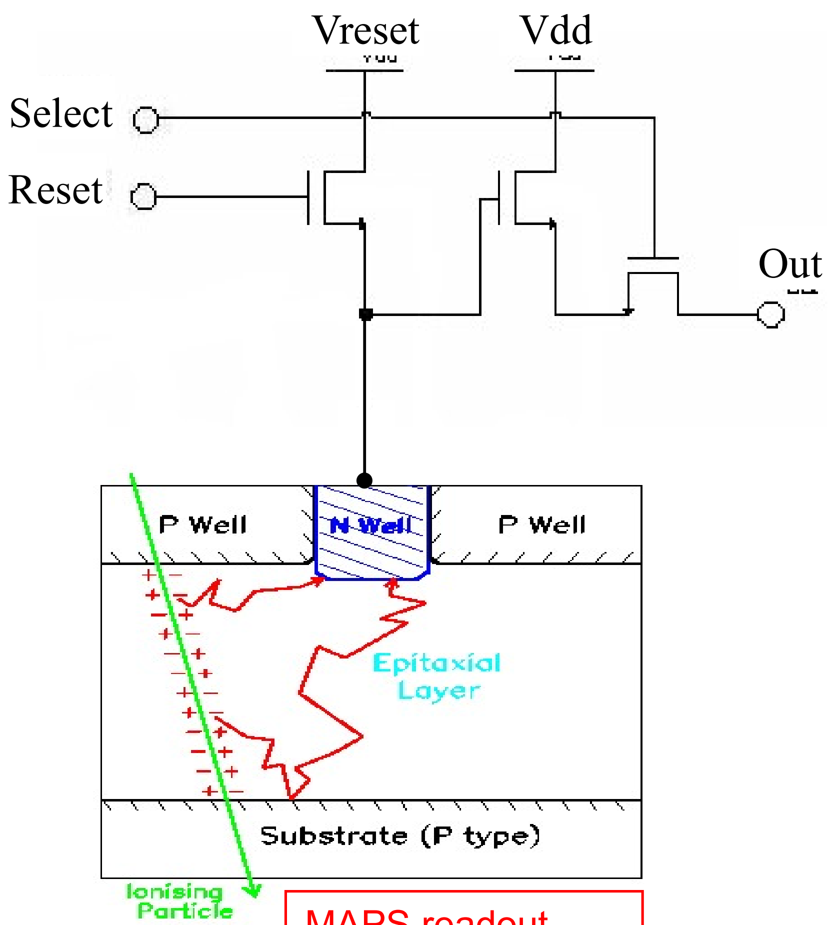


Impulse response

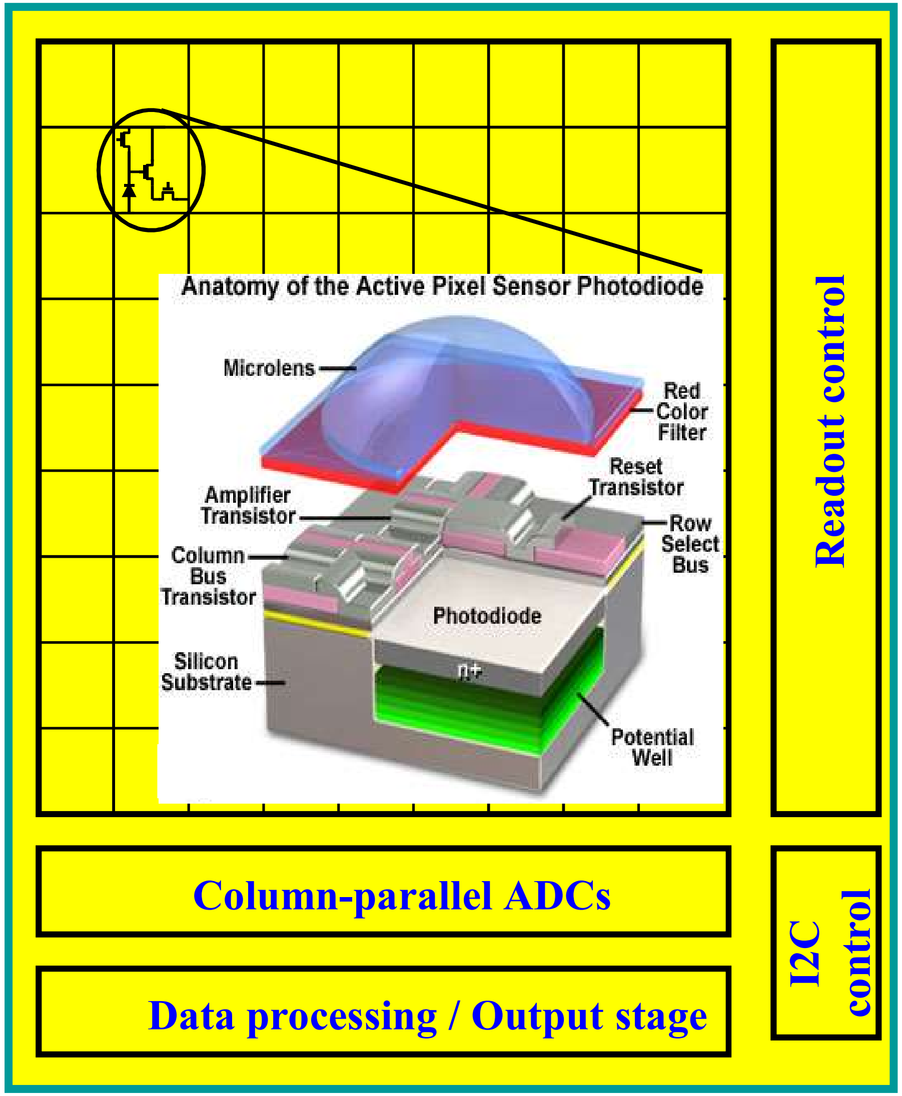
Example : Monolithic active pixels

© R Turchetta RAL

- Epitaxial layer forms sensitive volume (2-20μm)
- Charge collection by diffusion
- Read ~100 e- on Cd~10fF = few mV



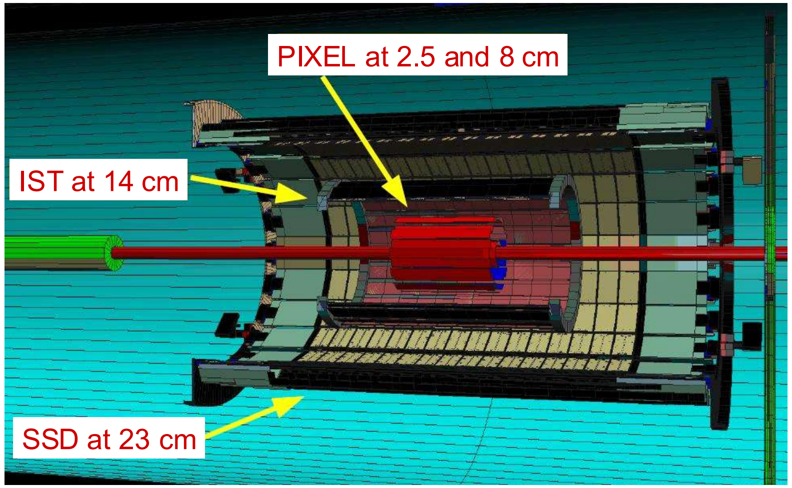
MAPS readout

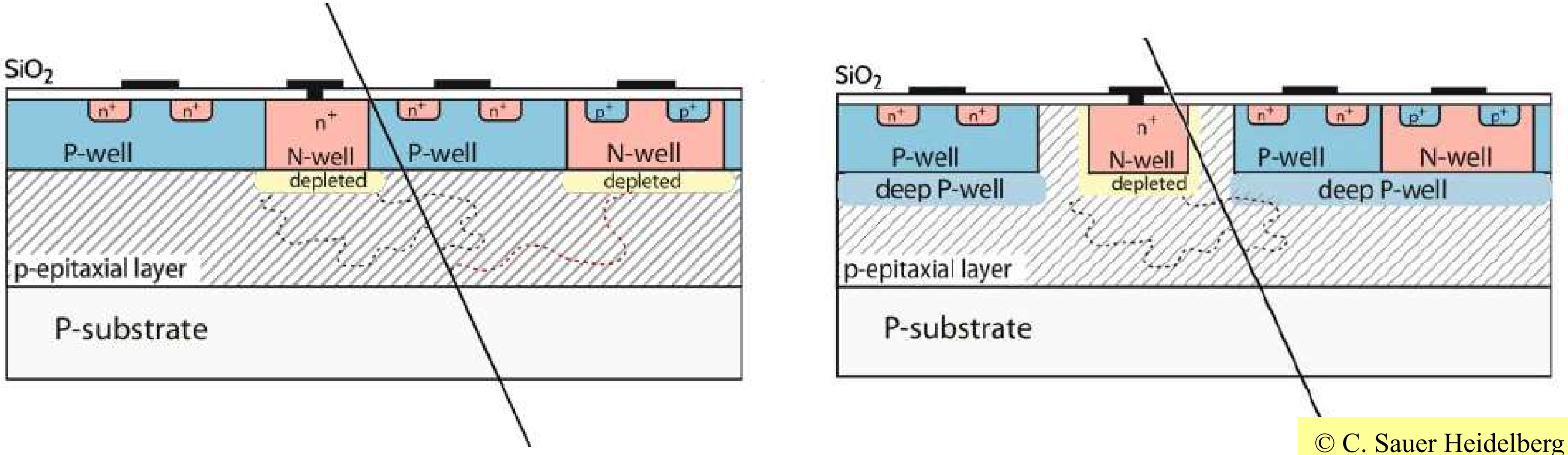


MAPS in HEP : see talk by C. Hu

- MIMOSTAR [ÏPHC strasbourg et al.]
  - First use in HEP : STAR detector 2014
  - 2 cm² ASIC with21x21 um pixels

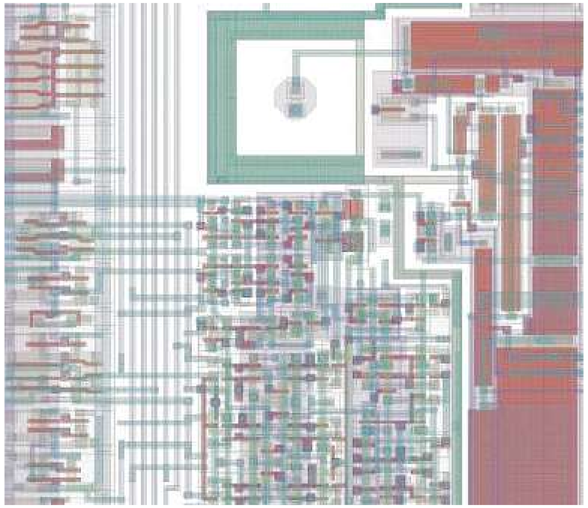
- ALPIDE for ALICE upgrade [CERN et al.]
  - Several process and design improvements
  - Deep pwell to allow CMOS
  - In-pixel preamp and comparator
  - P = 40 nW/pixel (5 mW/cm²)

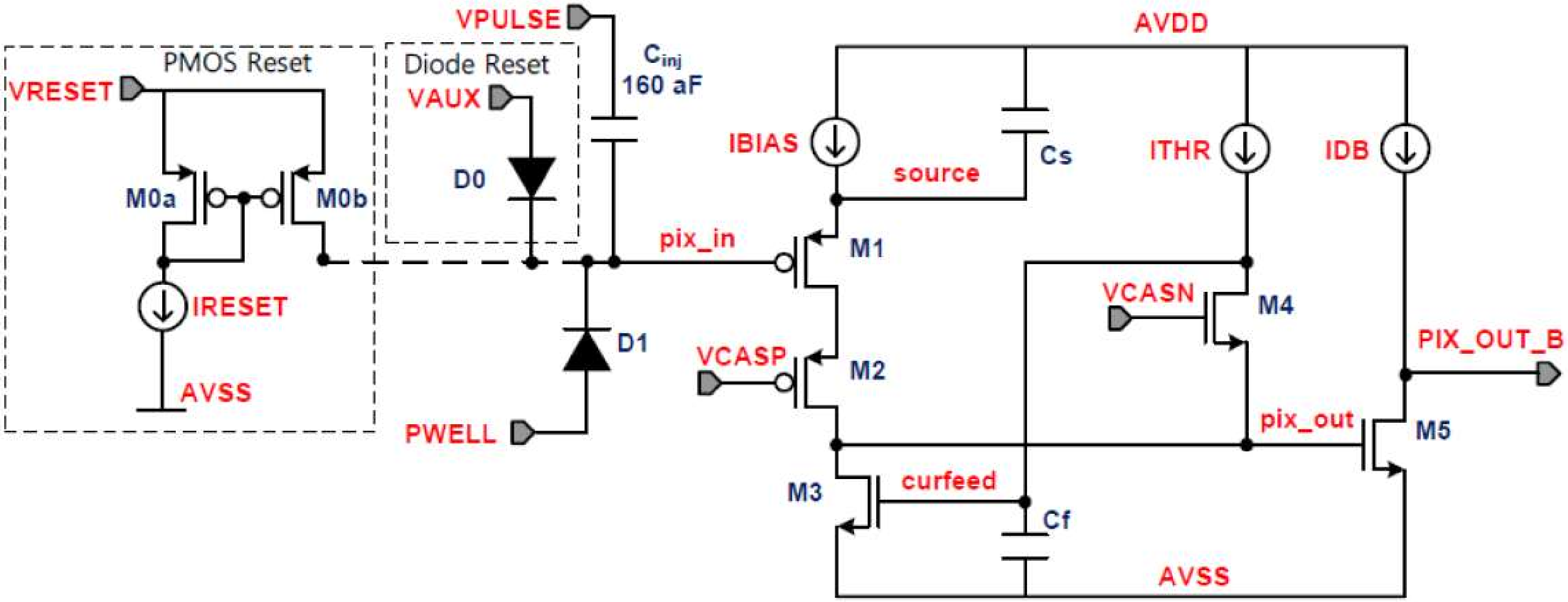




ALPIDE preamplifier

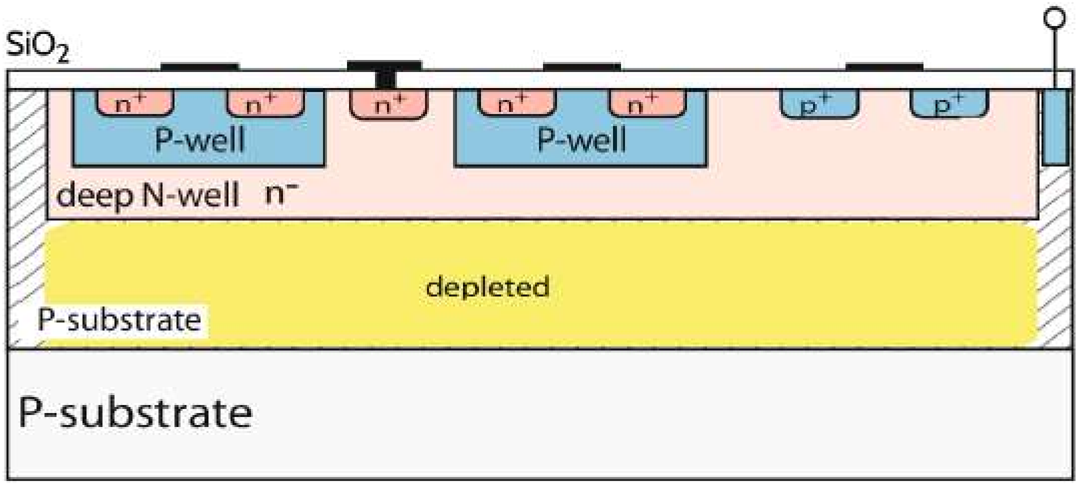
- Far from the 3T design…





Evolution of MAPs

- Going to HV-MAPS [I. Peric U. Bonn]
  - HV CMOS process => partial/full sensor depletion
  - Collection by drift and not diffustion => fast signal ~ns
  - Better radiation tolerance
  - Nanosecond timing capability
  - Proposed for ATLAS upgrade and µ3e

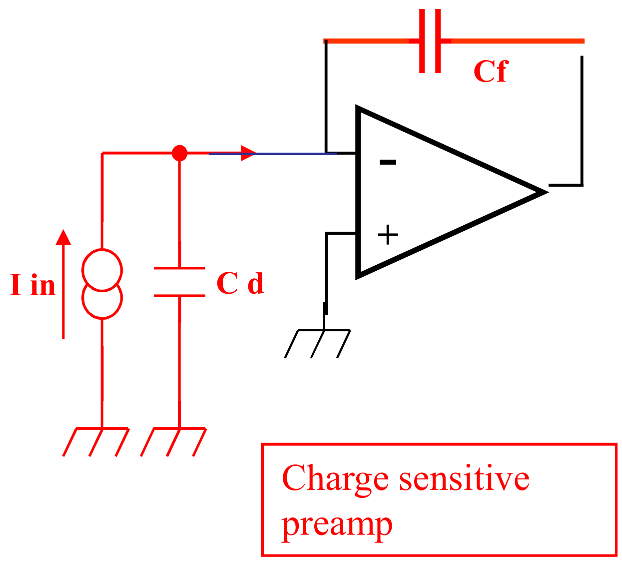


Ideal charge preamplifier

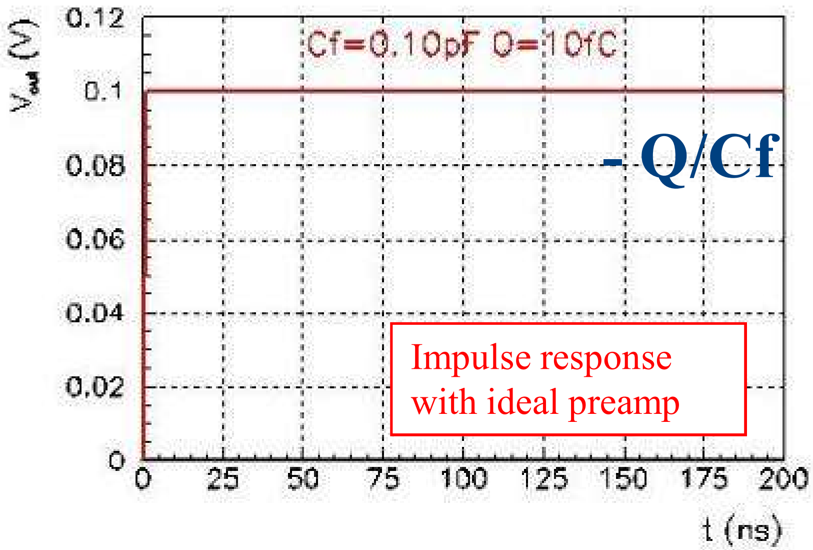
- ideal opamp in transimpedance ($C_f << C_d$)
  - Shunt-shunt feedback : low Z_{in}, low Z_{out}
    - $i_{in}(\omega) = j\omega C_d V_{in}(\omega) + j\omega C_f (V_{in}(\omega) - V_{out}(\omega))$
    - $V_{out}(\omega) = - G V_{in}\omega)$ (opamp gain)
  - => $V_{out}(\omega)/i_{in}(\omega) = - 1/j\omega C_f (1 + C_d / GC_f)$
  - Ideal opamp : $G \rightarrow \infty$
  - $V_{out}(\omega)/i_{in}(\omega) = - 1/j\omega C_f$
  - Integrator : $v_{out}(t) = -1/C_f \int i_{in}(t)dt$

$$v_{out}(t) = - Q/C_f$$

  - « Gain » : $1/C_f$: 0.1 pF -> 10 mV/fC
  - C_f determined by maximum signal



- Integration on Cf
  - Simple : $V = - Q/C_f$
  - Unsensitive to preamp capacitance C_{PA}
  - Turns a short signal into a long one
  - The front-end of 90% of particle physic
  - But always built with custom circuits…

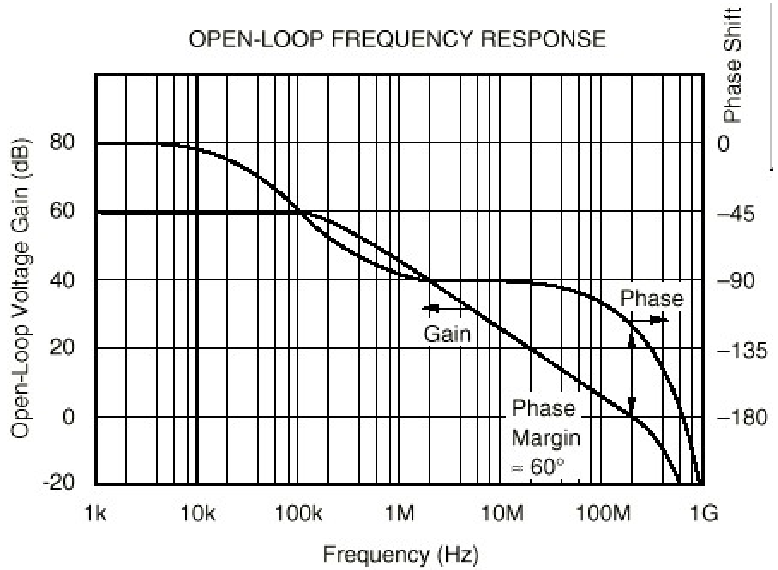


Preamp speed

- Finite opamp gain
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + C_d / G_0 C_f)$
  - Small signal loss in $C_d/G_0C_f \ll 1$
    (ballistic deficit)

- Finite opamp bandwidth
  - First order open-loop gain
  - $G(\omega) = G_0/(1 + j\,\omega/\omega_0)$
    - G_0 : low frequency gain
    - $G_0\omega_0$: gain bandwidth product
  - $V_{out}(\omega)/i_{in}(\omega) = - 1/j\omega C_f\,(1+j\omega C_d/G_0\omega_0 C_f)$

- Preamp risetime
  - Time constant : τ *(tau)*
  - $\tau = C_d/G_0\omega_0 C_f$
  - Rise-time : $t_{10\text{-}90\%} = 2.2\,\tau$
  - Rise-time optimised with w_{C} or C_f



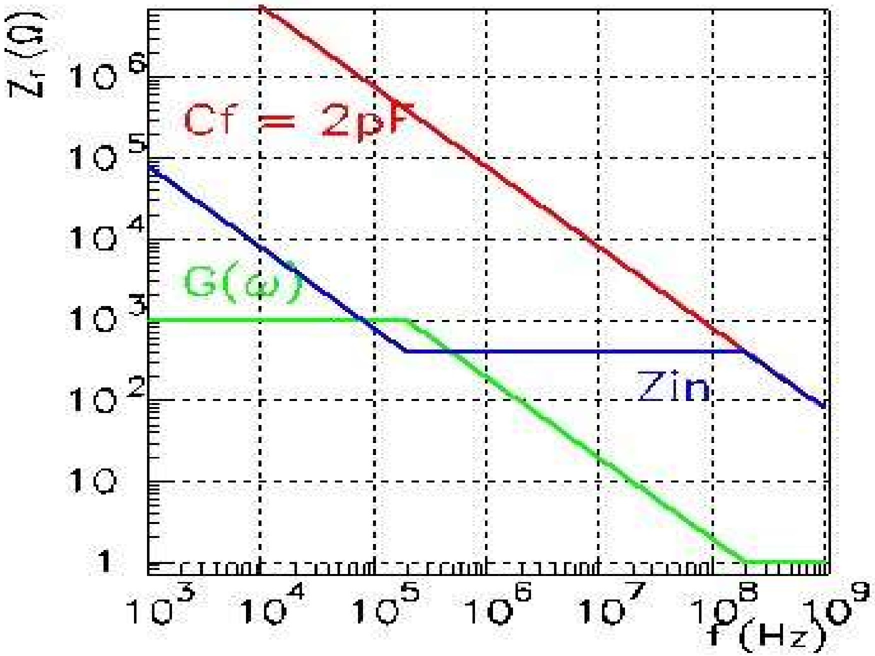
Impulse response with non-ideal preamp

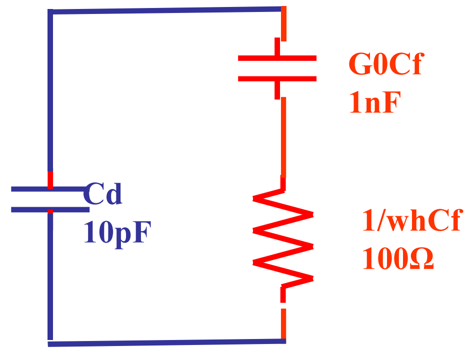
Charge preamp seen from the input

- Input impedance with ideal opamp
  - Zin = Zf / G+1
  - Zin->0 for ideal opmap
  - « Virtual ground » : Vin = 0
  - Minimizes sensitivity to detector impedance
  - Minimizes crostalk

- Input impedance with real opamp
  - Zin = $1/j\omega\, G_0C_f + 1/\, G_0\omega_0\, C_f$
  - Resistive term : Rin = $1/\, G_0\omega_0\, C_f$
    - Exemple : $w_C = 10^{10}$ rad/s C_f= 1 pF => Rin = 100 Ω
  - Determines the input time constant : $t = R_{eq}C_d$
  - Good stability= (…!)
  - Equivalent circuit :

Input impedance or charge preamp





Electronically cooled resistors [TNS 73]

SIGNAL, NOISE AND RESOLUTION IN POSITION-SENSITIVE DETECTORS*

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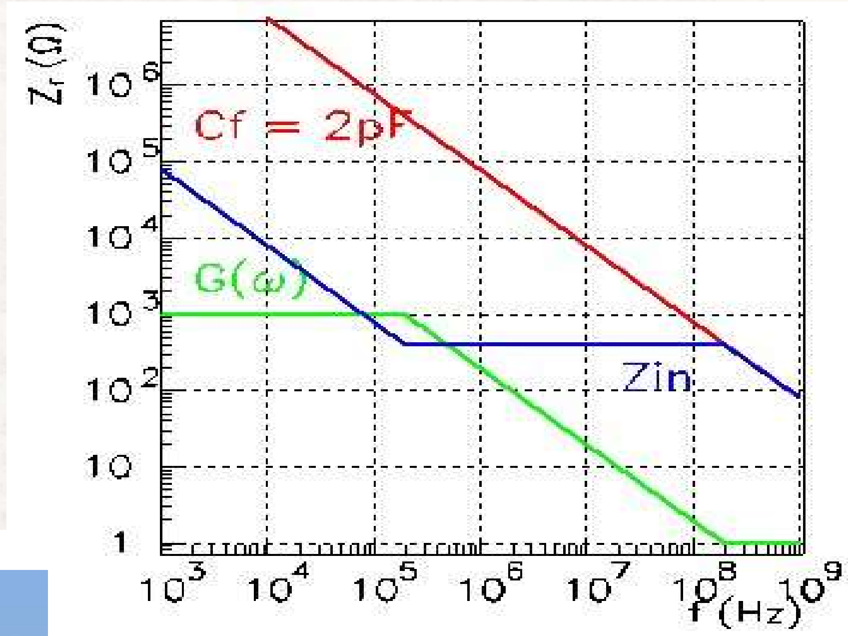
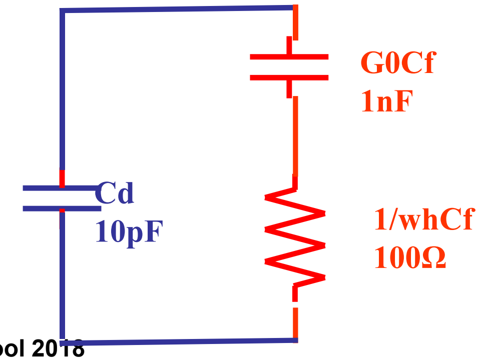
ABSTRACT

An analysis is presented of signal, noise and position resolution relations for some of the most interesting position-sensing methods. "Electronic cooling" of delay line terminations is introduced in order to reduce noise in the position-sensing with delay lines. A new method for terminating transmission lines and for "noiseless" damping which employs a capacitance in feedback is presented. It is shown that the position resolution for the charge division method with resistive electrodes is determined only by the electrode capacitance and not by the electrode resistance, if optimum filtering is used.

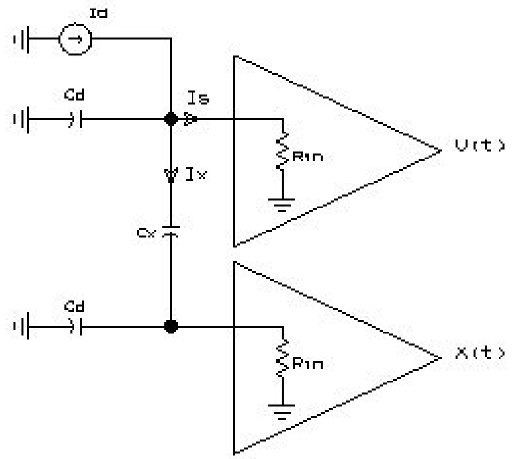


$$Zin = 1/j\omega\, G_0 C_F + 1/\, G_0 \omega_0\, C_F$$

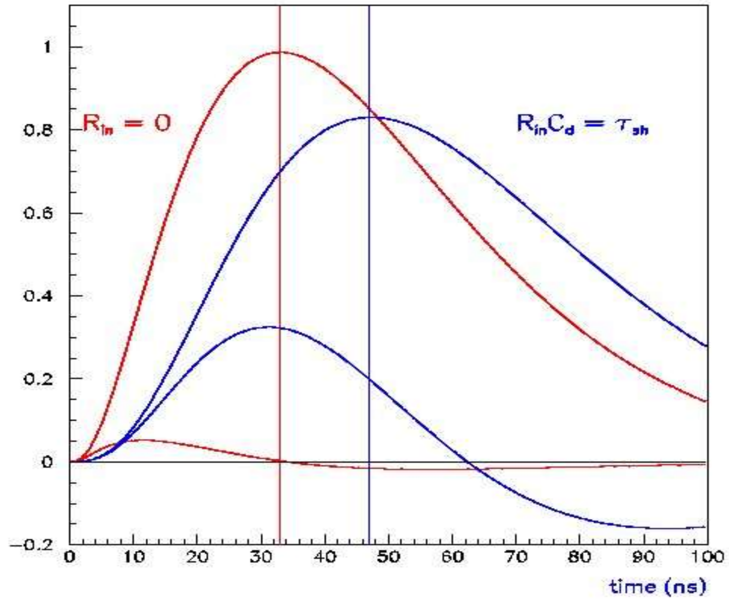


Crosstalk

- Capacitive coupling between neighbours
  - Crosstalk signal is differentiated and with same polarity
  - Small contribution at signal peak
  - Proportionnal to Cx/Cd and preamp input impedance
  - Slowed derivative if RinCd ~ tp => non-zero at peak

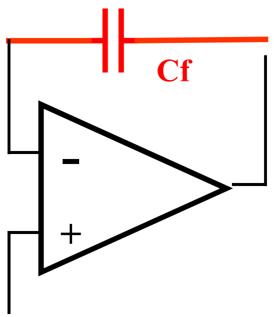


Crosstalk electrical modelization

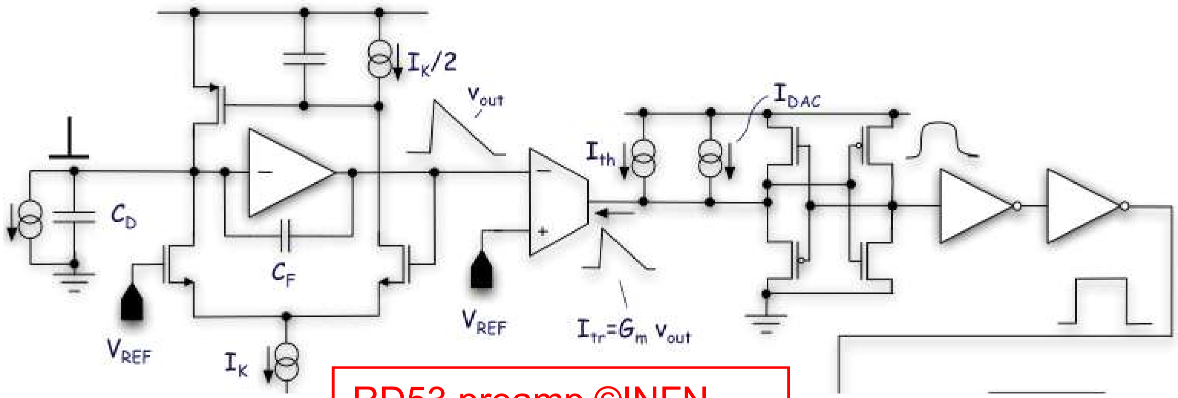


- Long distance crosstalk
  - Inductive/resistive common ground return
  - References impedance
  - Connectors : mutual inductance

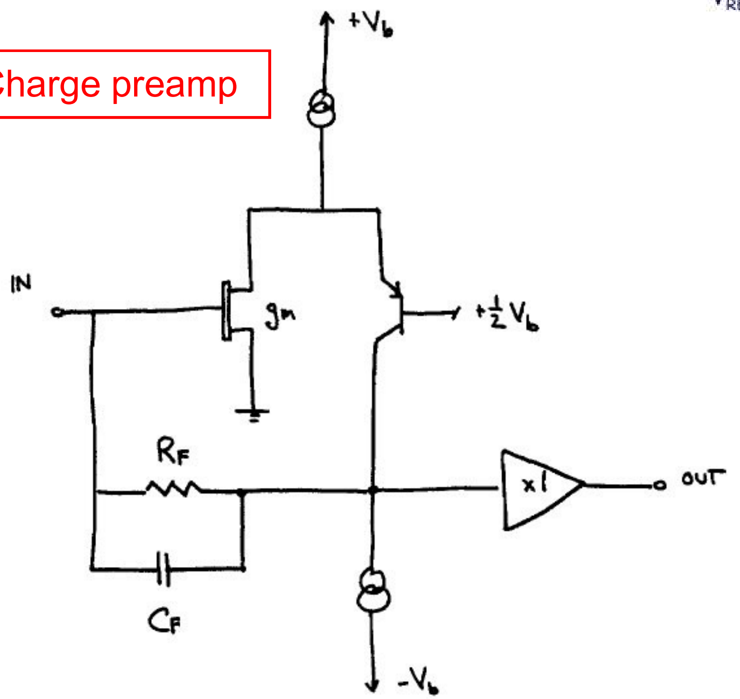
- More details after the section on noise



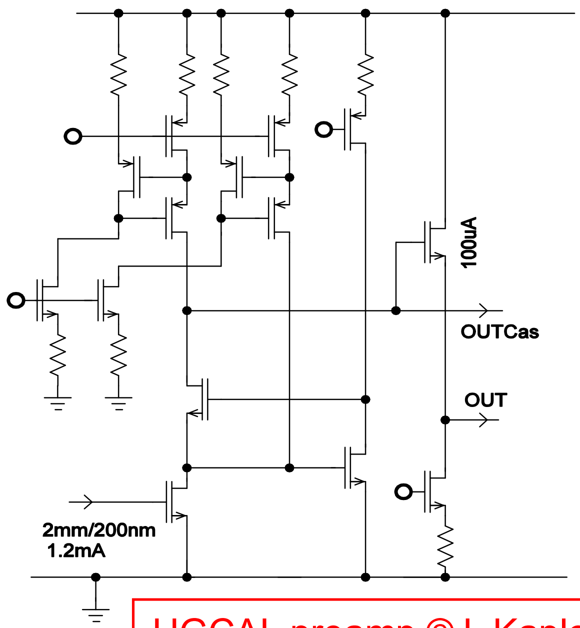
Charge preamp



RD53 preamp ©INFN



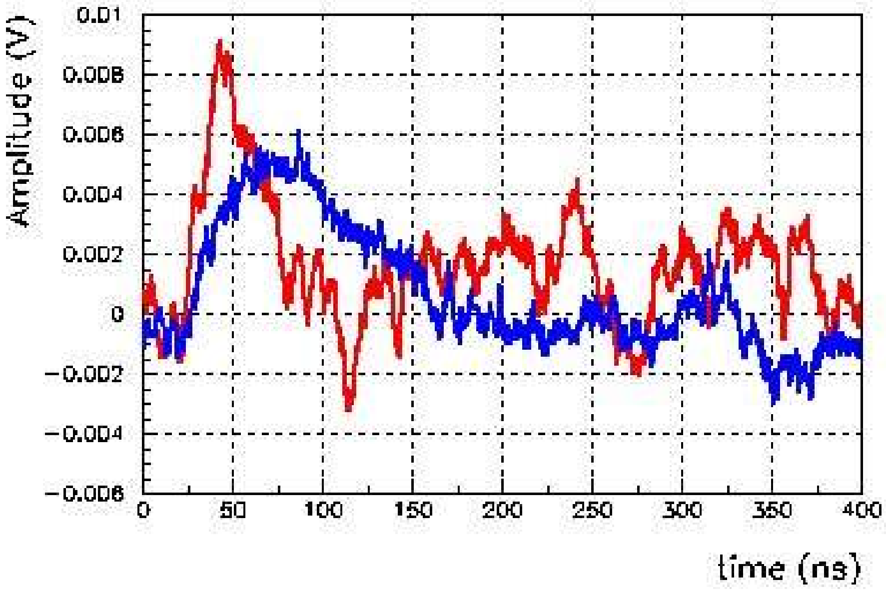
Charge preamp ©Radeka 68



HGCAL preamp ©J. Kaplon

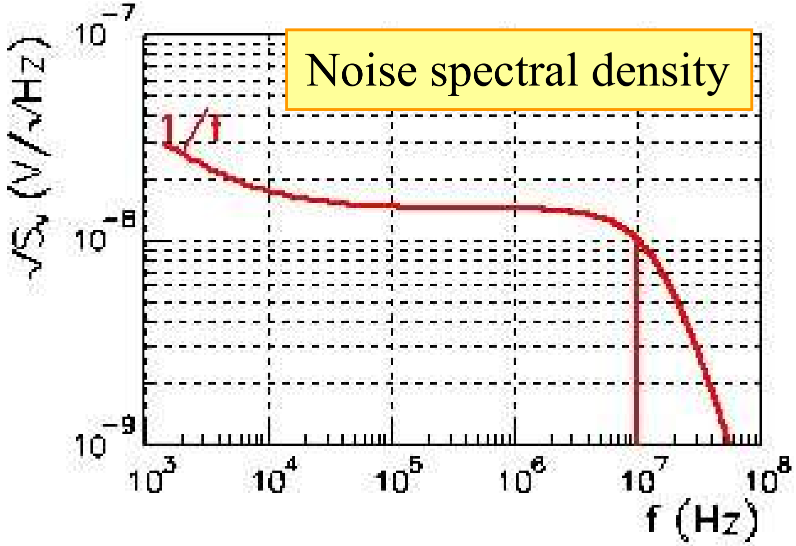
- Definition of Noise
  - Random fluctuation superposed to interesting signal
  - Statistical treatment

- Three types of noise
  - Fundamental noise (Thermal noise, shot noise)
  - Excess noise (1/f …)
  - Parasitics -> EMC/EMI (pickup noise, ground loops…)

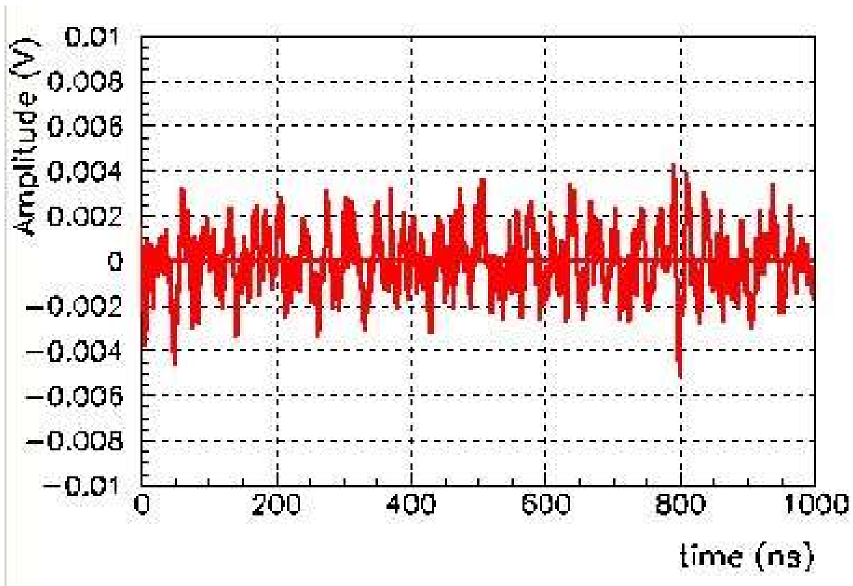


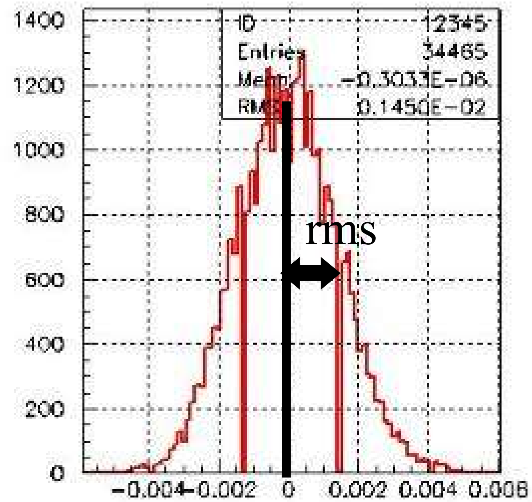
Electronics noise

- Modelization
  - Noise generators : e_n, i_n,
  - Noise spectral density of e_n & i_n : S_v(f
  - $Sv(f) = | \mathcal{F}(e_n) |^2$ (V^2/Hz)



- *Rms* noise Vn
  - $V_n^2 = \int e_n^2(t)\, dt = \int Sv(f)\, df$
  - White noise (e_n) : $v_n = e_n \sqrt{\tfrac{1}{2}\pi f_{-3dB}}$

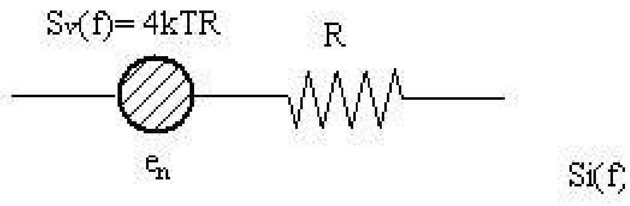




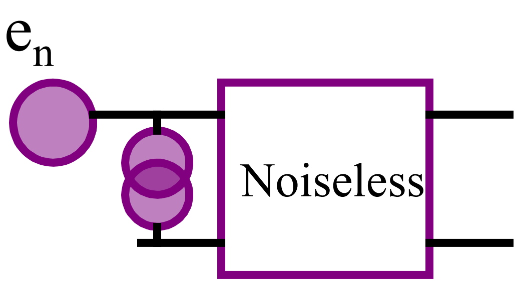
Rms noise vn

Calculating electronics noise

- Fundamental noise
  - Thermal noise (resistors) : Sv(f) = 4kTR
  - Shot noise (junctions) : Si(f) = 2qI



- Noise referred to the input
  - All noise generators can be referred to the input as 2 noise generators :
  - A voltage one e_n in series : series noise
  - A current one i_n in parallel : parallel noise
  - Two generators : no more, no less…



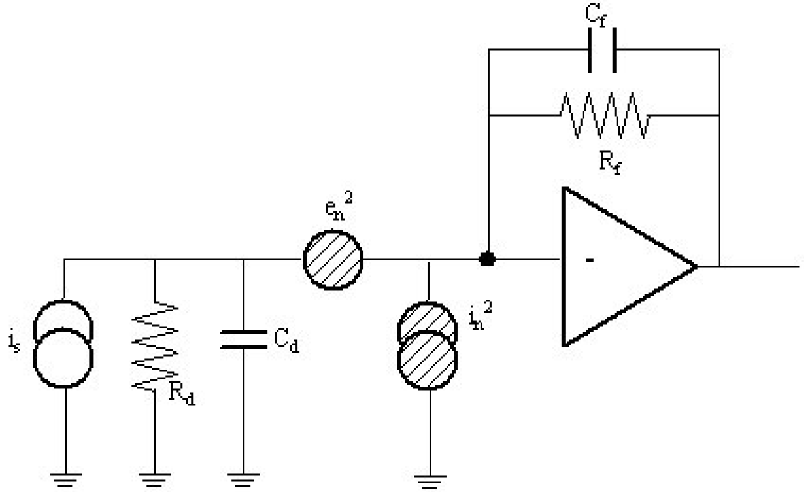
Noise generators referred to the input

- **To take into account the Source impedance**

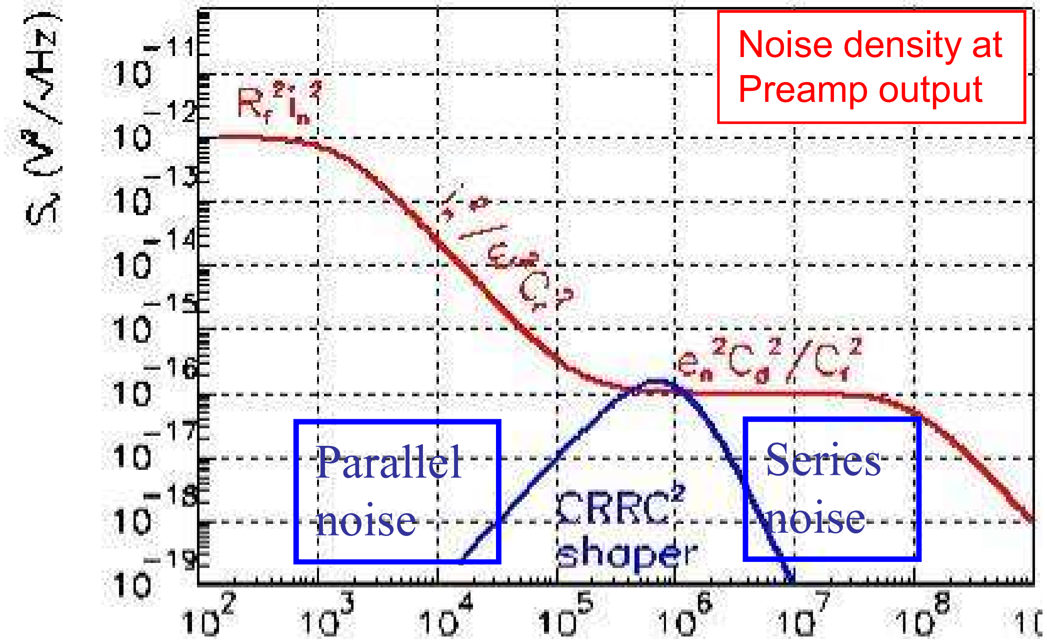
- **Golden rule :**
  - **Always calculate the signal before the noise what counts is the signal to noise ratio**

Noise in transimpedance amplifiers

- 2 noise generators at the input
  - Parallel noise : (i_n^2) (leakage)
  - Series nosie : (e_n^2) (preamp)
- Output noise spectral density :
  - $Sv(\omega) = (i_n^2 + e_n^2/|Z_d|^2) * |Z_f|^2$
- For charge preamps
  - $Sv(\omega) = i_n^2 /\omega^2 C_f^2 + e_n^2 C_d^2/C_f^2$
  - Parallel noise in $1/\omega^2$
  - Series noise is flat, with a « noise gain » of C_d/C_f
- *rms* noise V_n
  - $V_n^2 = \int Sv(\omega)\, d\omega/2\pi \rightarrow \infty$
  - Benefit of shaping…

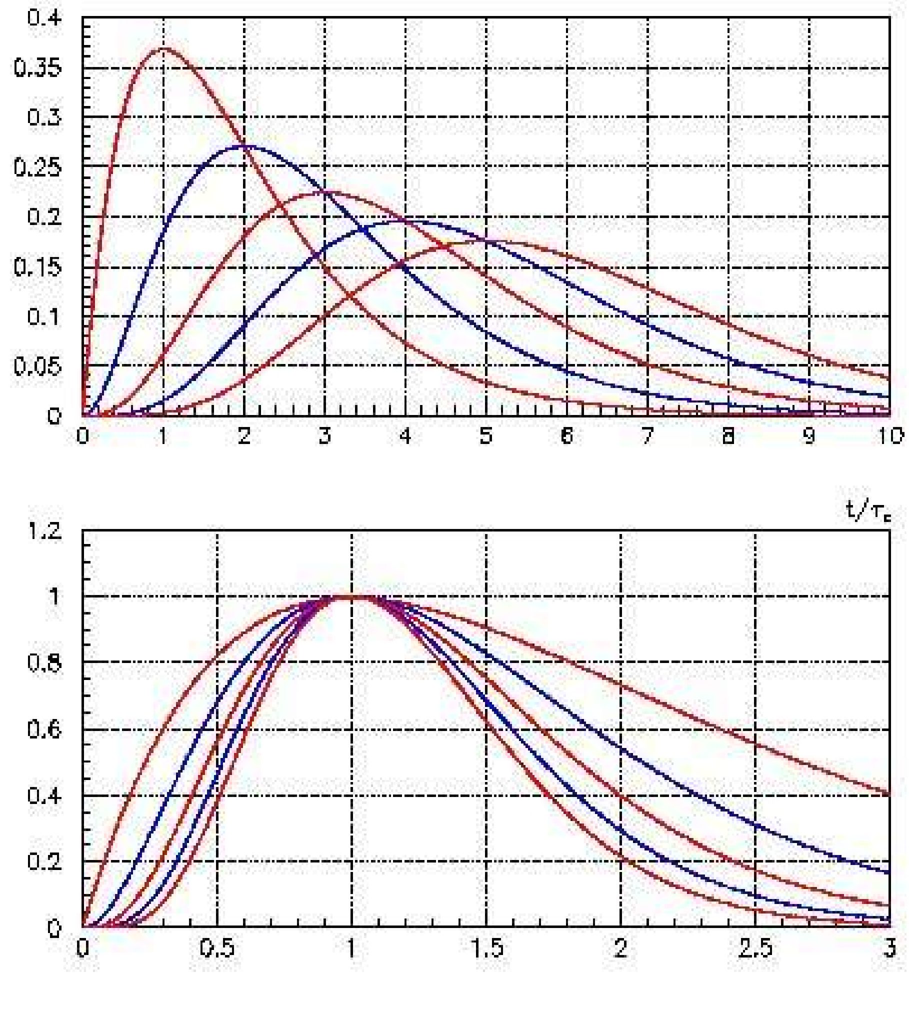


Noise generators in charge preamp



Equivalent Noise Charge (ENC) after $CRRC^n$

- Noise reduction by optimising useful bandwidth
  - Low-pass filters (**RC^n**) to cut-off high frequency noise
  - High-pass filter (**CR**) to cut-off parallel noise
  - -> pass-band filter $CRRC^n$
- Equivalent Noise Charge : ENC
  - Noise referred to the input in electrons
  - $ENC = Ia(n)\, e_n C_t/\sqrt{\tau} \oplus Ib(n)\, i_n^* \sqrt{\tau}$
  - Series noise in $1/\sqrt{\tau}$
  - Paralle noise in $\sqrt{\tau}$
  - 1/f noise independant of τ
  - Optimum shaping time $\tau_{opt} = \tau_c/\sqrt{2n-1}$

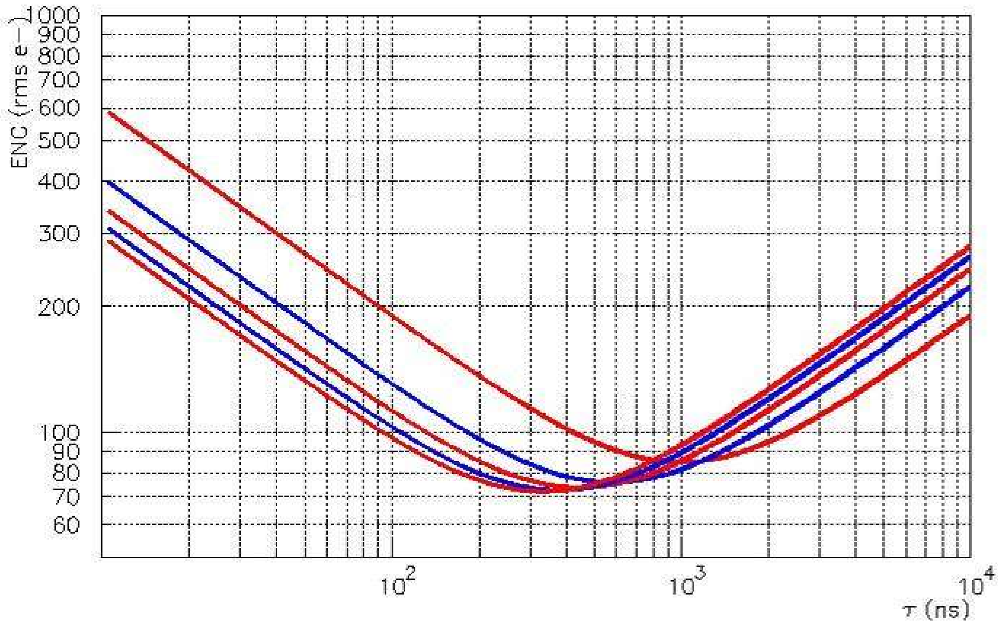


Step response of CR RCn shapers

Equivalent Noise Charge (ENC) after $CRRC^n$

- Peaking time tp (5-100%)
  - ENC(**tp**) independent of n
  - Also includes preamp risetime

- Complex shapers are getting obsolete :
  - Power of digital filtering
  - Analog filter = CRRC ou $CRRC^2$
  - antialiasing



ENC vs tau for CR RCn shapers

Equivalent Noise Charge (ENC) after CRRC^n

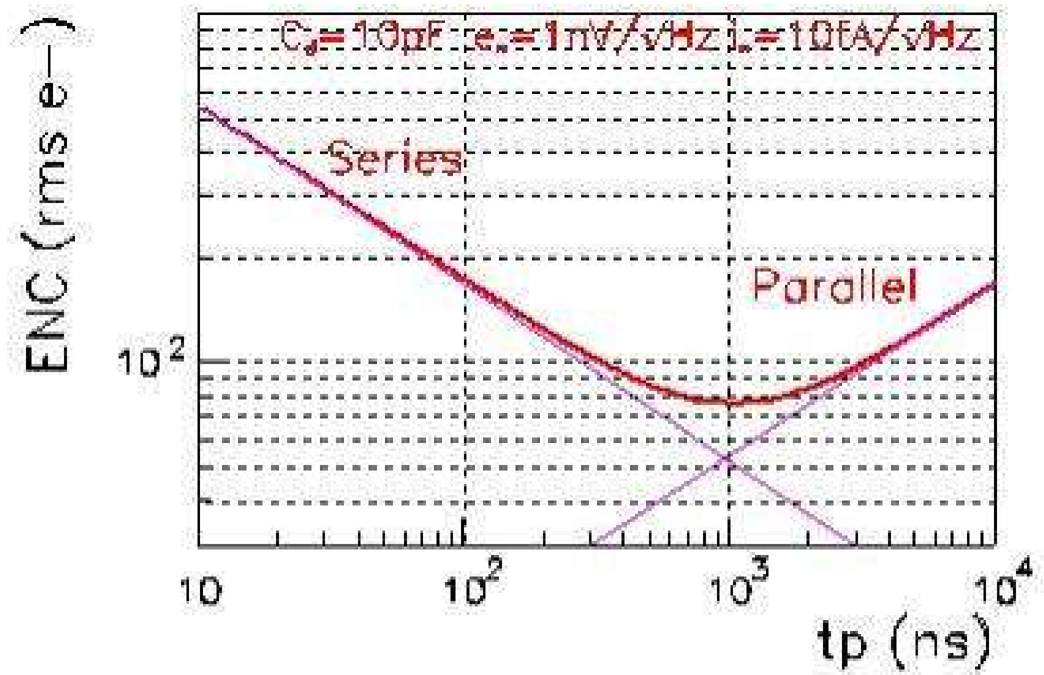
- A useful formula : **ENC (e- rms) after a CRRC^2 shaper :**

$$ENC = 174\, e_n C_{tot}/\sqrt{t_p}\ (\delta) \oplus 166\, i_n \sqrt{t_p}\ (\delta)$$

  - e_n in nV/ √Hz, i_n in pA/ √Hz are the preamp noise spectral densities
  - C_{tot} (in pF) is dominated by the detector (C_d) + input preamp capacitance (C_{PA})
  - t_p (in ns) is the shaper peaking time (5-100%)

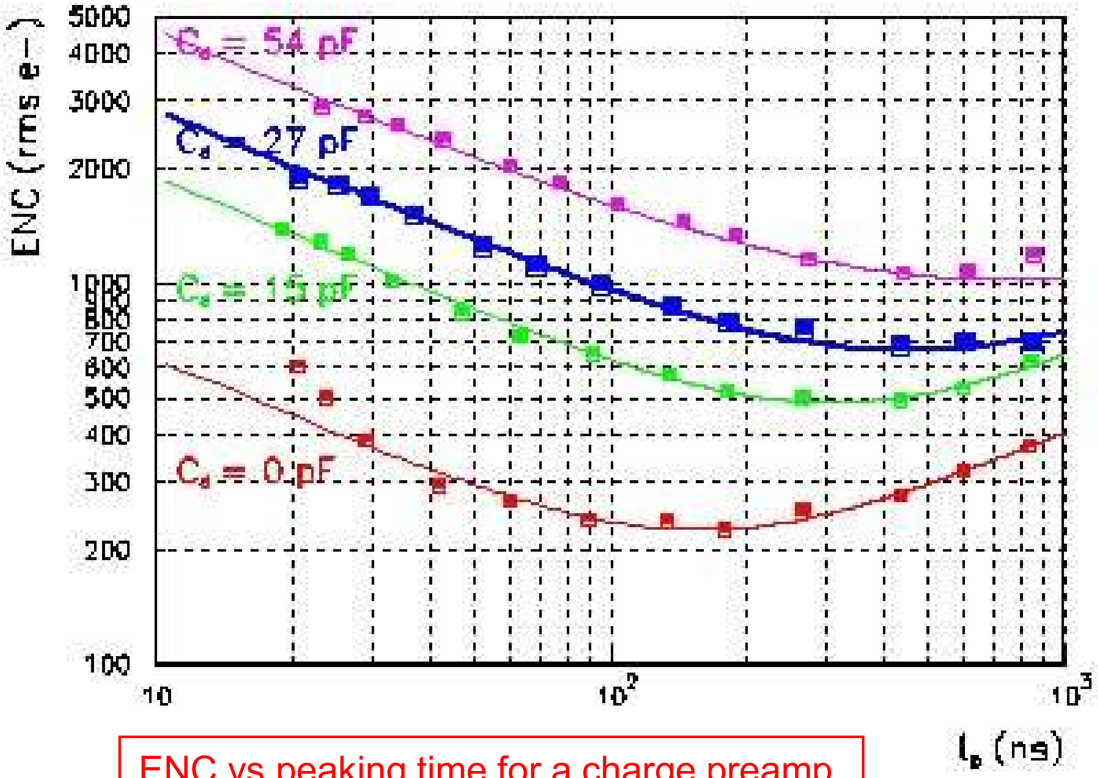
- **Noise minimization**
  - Minimize source capacitance
  - Operate at optimum shaping time
  - Preamp series noise (en) best with high trans-conductance (g_m) in input transistor

    => large current, optimal size

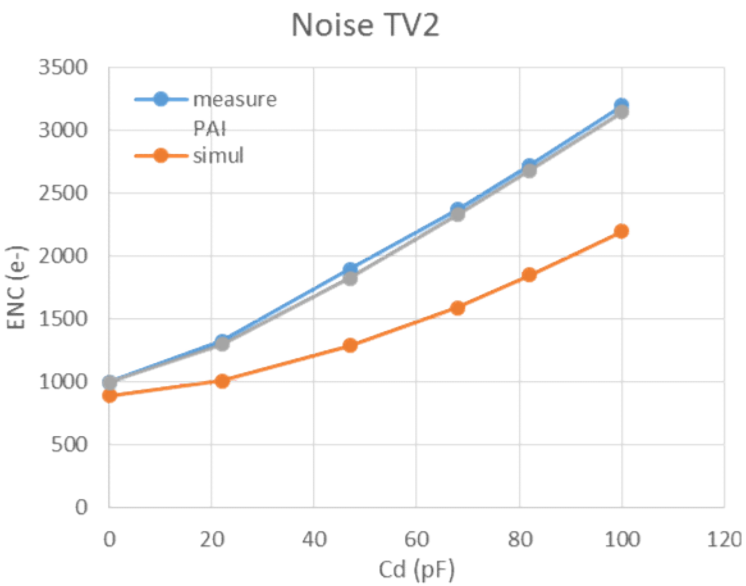


Example of ENC measurement

- 2000/0.35 PMOS 0.35µm SiGe Id=500 µA
  - Series : e_n = 1.4 nV/√Hz, C_{PA} = 7 pF , 1/f noise : 12 e-/pF, Parallel : in = 40 fA/√Hz
  - Series noise e_n and Preamp capacitance extraction fitting ENC(Cd)
  - NB : linear fit wrong for e_n and C_{PA}, use quadratic fit :
    - $ENC^2(Cd) = A\, e_n^{\,2}(Cd+Cpa)^2/tp + B\, i_n^2 tp +$ 2^{nd} stage
    - $ENC^2(Cd) - ENC^2(0) = A\, e_n^{\,2} Cd^2 + 2A\, e_n^{\,2}(Cd+Cpa)$



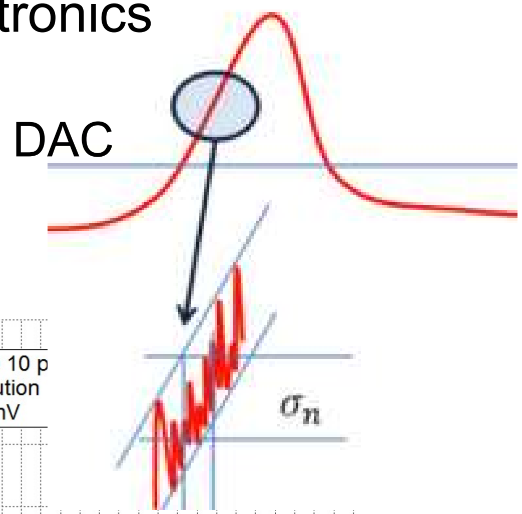
ENC vs peaking time for a charge preamp

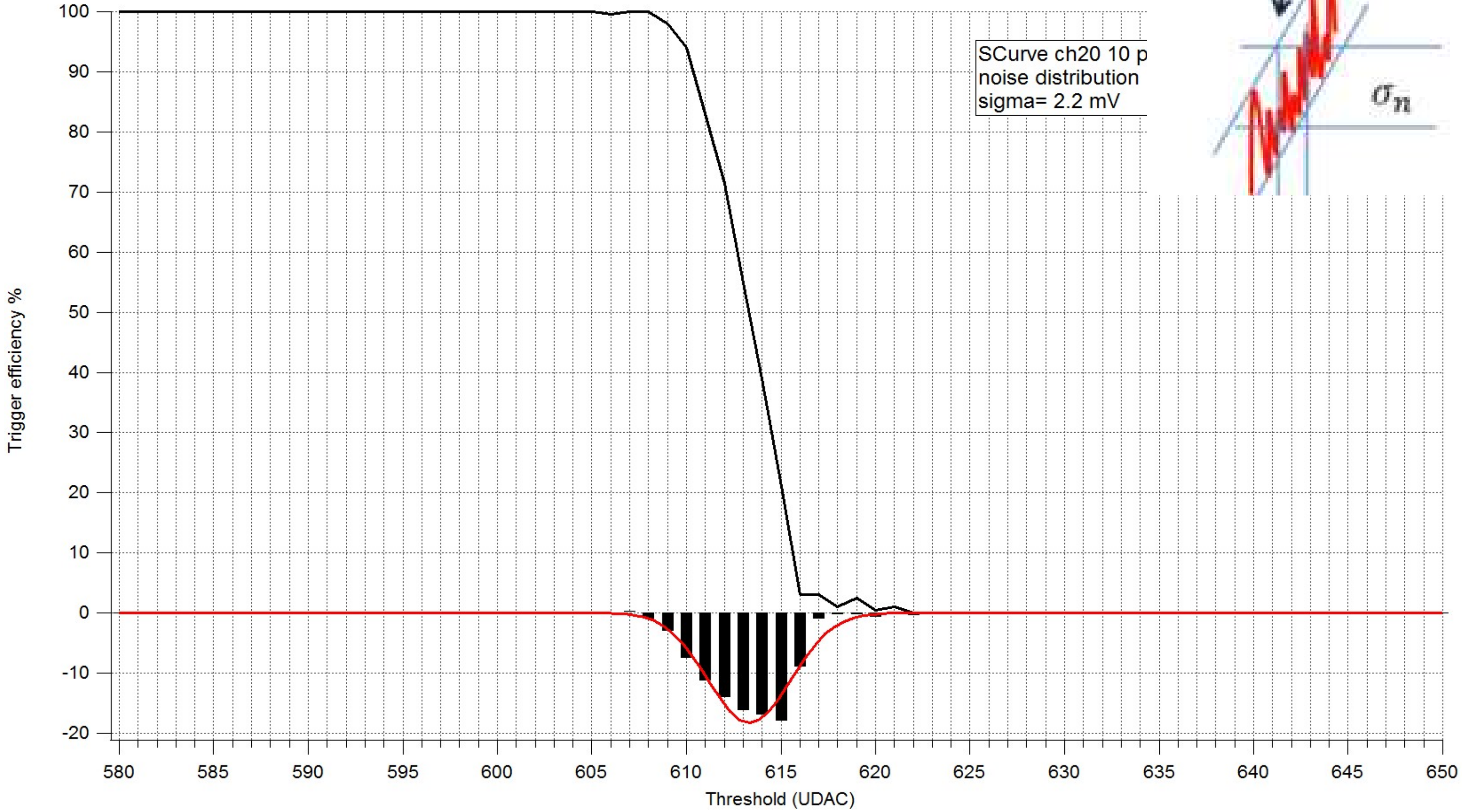


ENC vs Capacitance (other preamp)

Trigger efficiency

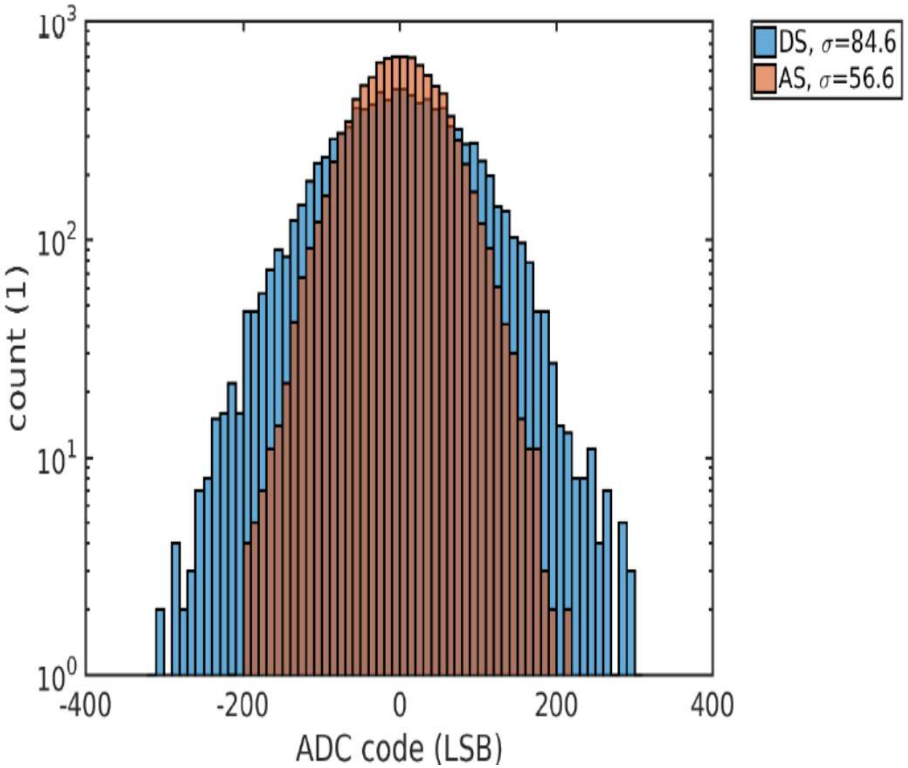
- Preamp + discriminator front-end = tracker electronics
- scanning the DAC produces « s-curves »
- Derivative gives the noise

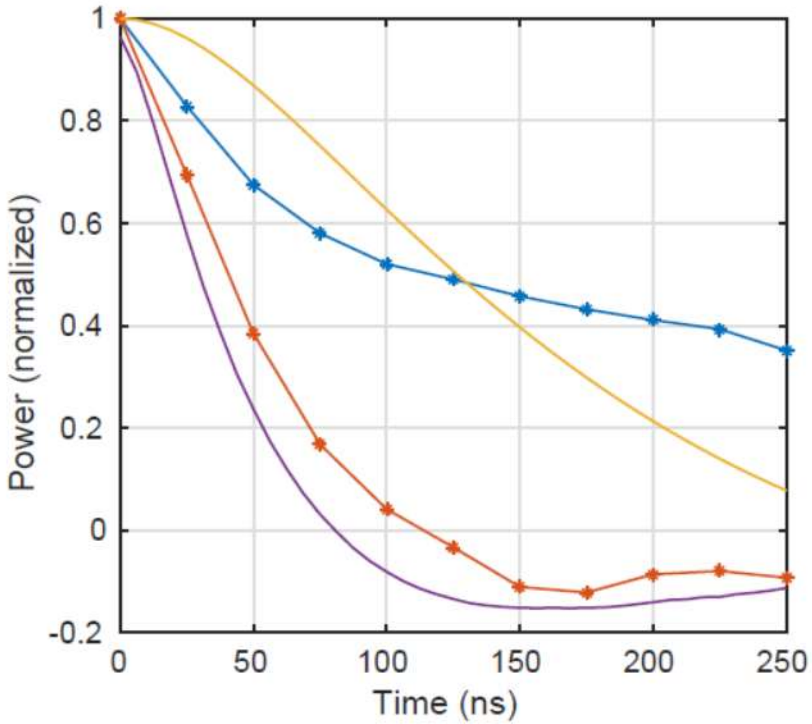




Coherent and incoherent noise

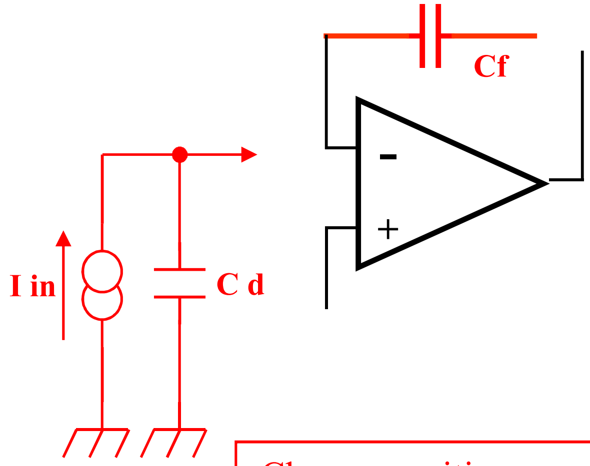
- A constant concern in calorimetry
  - Coherent noise extracted by comparing direct and alternate sums on n channels (n=64) : DS = ∑ ped[i] ; AS = ∑ (-1)^i ped[i]
  - Incoherent noise IN = rms(AS) / √n
  - Coherent noise : CN = $\sqrt{var(DS) - var(AS)}$ / n
- Need to show that CN / IN ~ 10% can be obtained at system level





Summary of lecture 1

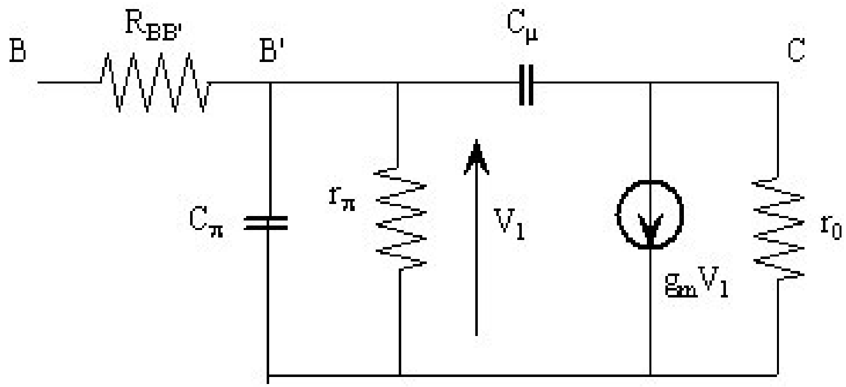
- Importance of front-end on electronics on physics performance
- Benefits of charge preamplifiers : low noise, low crosstalk
  - The front-end of 90% of particle physics detectors…
  - But always built with custom circuits…



Charge sensitive preamp :
Vout = -Q/Cf

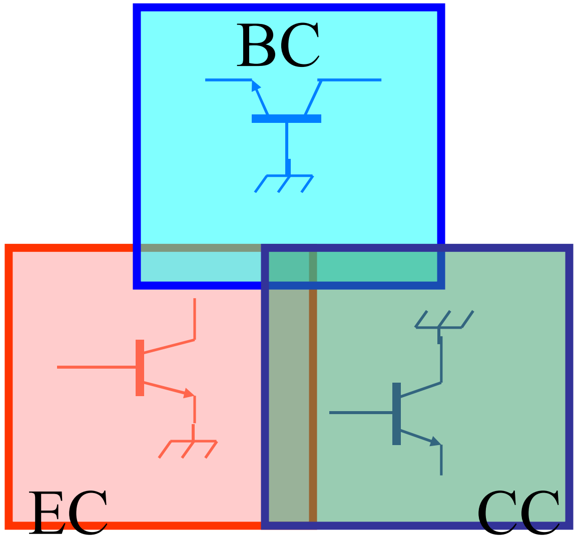
Summary of transistor level design

- Performant design is at transistor level
- Simple models
  - hybrid π model
  - Similar for bipolar and MOS
  - Essential for design



High frequency hybrid model of bipolar

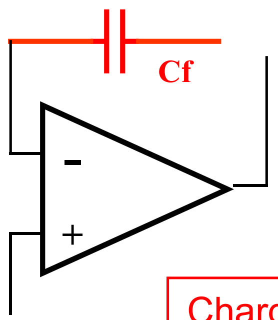
- **Three basic configurations**
  - Common emitter (CE) = V to I (transconductance)
  - Common collector (CC) = V to V (voltage buffer)
  - Common base (BC) = I to I (current conveyor)
- **See backup slides**



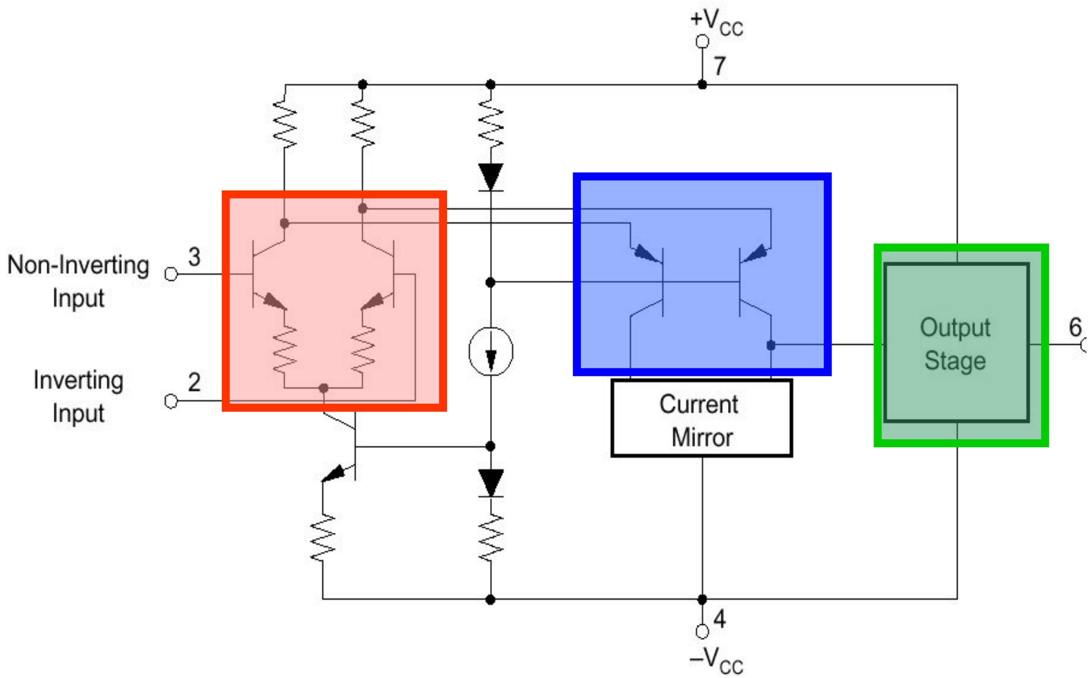
The *Art* of electronics design

- Numerous « composites »
  - Darlington, Paraphase, Cascode, Mirrors…

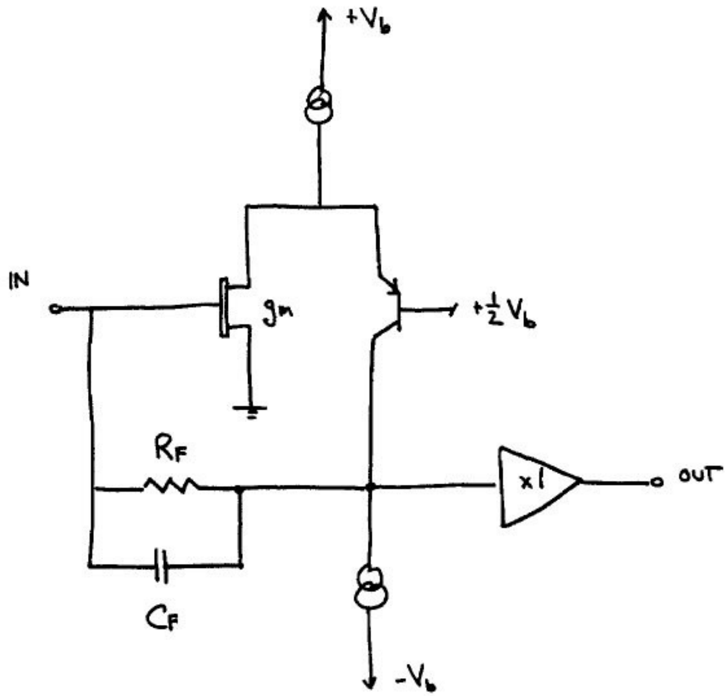
- From the schematic of principle
  - Using of a fast opamp (OP620)
  - Removing unnecessary components…
  - Similar to the traditionnal schematic «Radeka 68 »
  - Optimising transistors and currents



Charge preamp



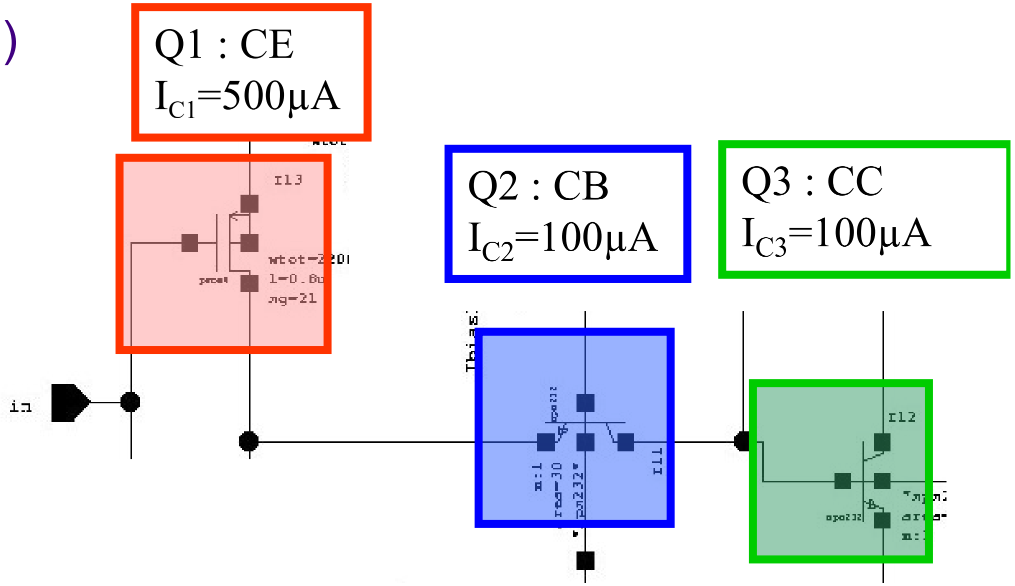
Schematic of a OP620 opamp ©BurrBrown



Charge preamp ©Radeka 68

Example : designing a charge preamp (2)

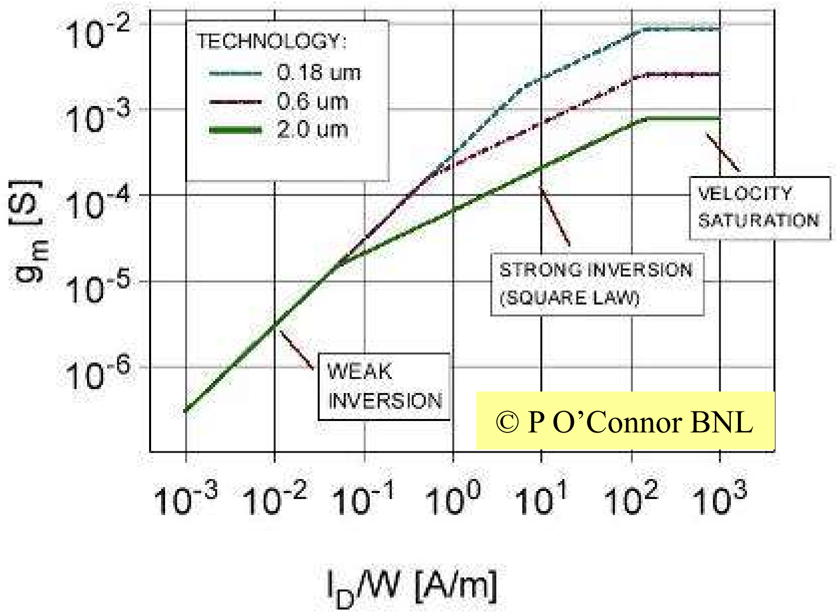
- Simplified schematic
- Optimising components
  - What transistors (PMOS, NPN ?)
  - What bias current ?
  - What transistor size ?
  - What is the noise contribution of each component ?
  - how to minimize it ?
  - What parameters determine the stability ?
  - Waht is the saturation behaviour
  - How vary signal and noise with input capacitance ?
  - How to maximise the output voltage swing ?
  - What is the sensitivity to power supplies, temperature…



Simplified schematic of Charge preamp

MOS input transistor sizing

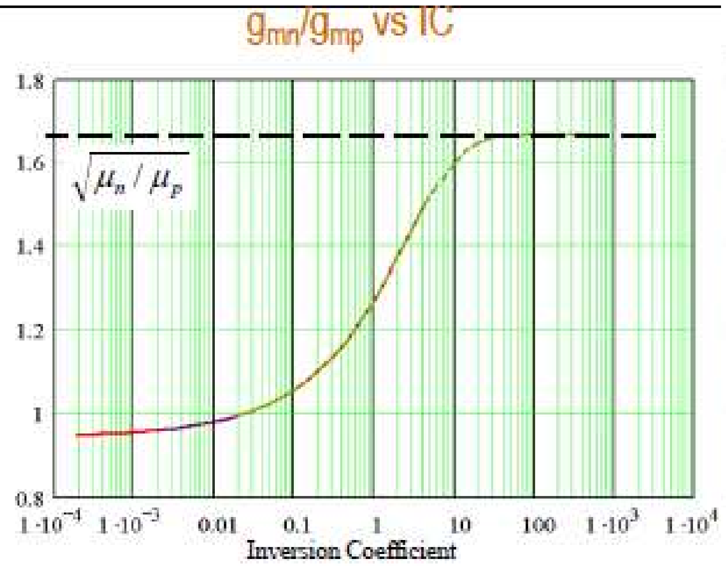
- Capacitive matching : strong inversion
  - g_m proportionnal to W/L $\sqrt{I_D}$
  - C_{GS} proportionnal to W*L
  - ENC propotionnal to (Cdet+C_{GS})/ $\sqrt{gm}$
  - Optimum W/L : C_{GS} = 1/3 Cdet
  - Large transistors are easily in moderate or weak inversion at small current

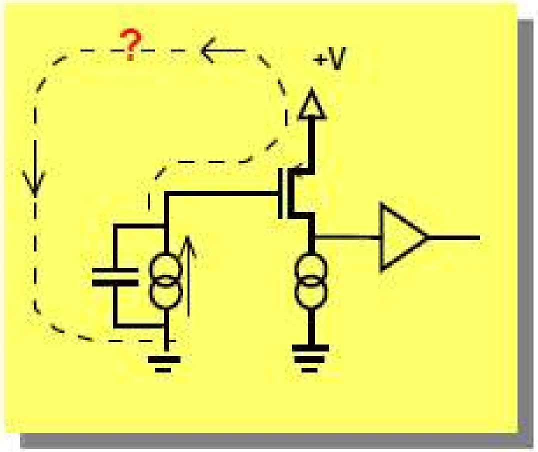


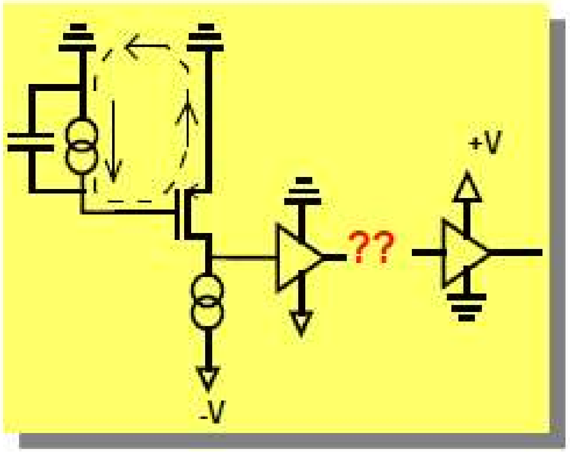
- Optimum size in weak inversion
  - g_m proportionnal to I_D (indep of W,L)
  - ENC minimal for C_{GS} minimal, provided the transistor remains in weak inversion

PMOS vs NMOS [Paul O'Connor BNL]

- *PMOS lower 1/f noise*
- *NMOS white series noise advantage over PMOS diminishes each generation*
- *PMOS can be operated at reverse V_{BS} to reduce bulk resistance noise*
- *PMOS lower tunneling current at ultra-thin t_{ox}*
- *Single-supply operation of PMOS-input preamp awkward:*

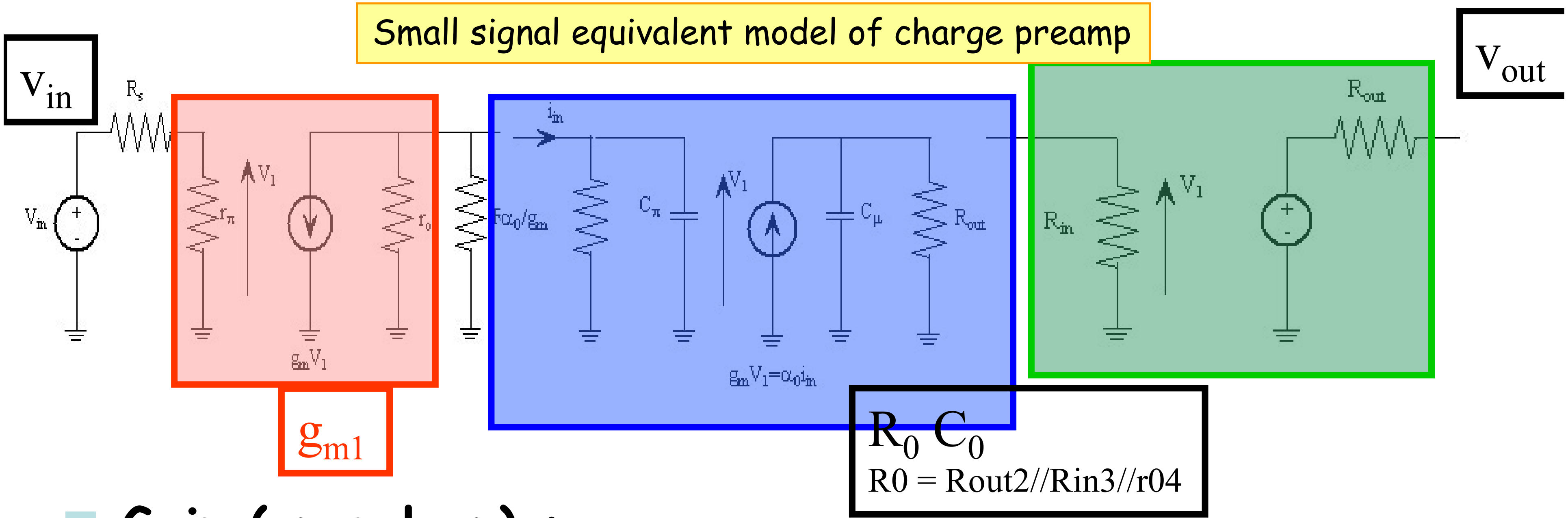






Example : designing a charge preamp (3)

- Small signal equivalent model
  - Transistors are replaced by hybrid π model
  - Allows to calculate open loop gain

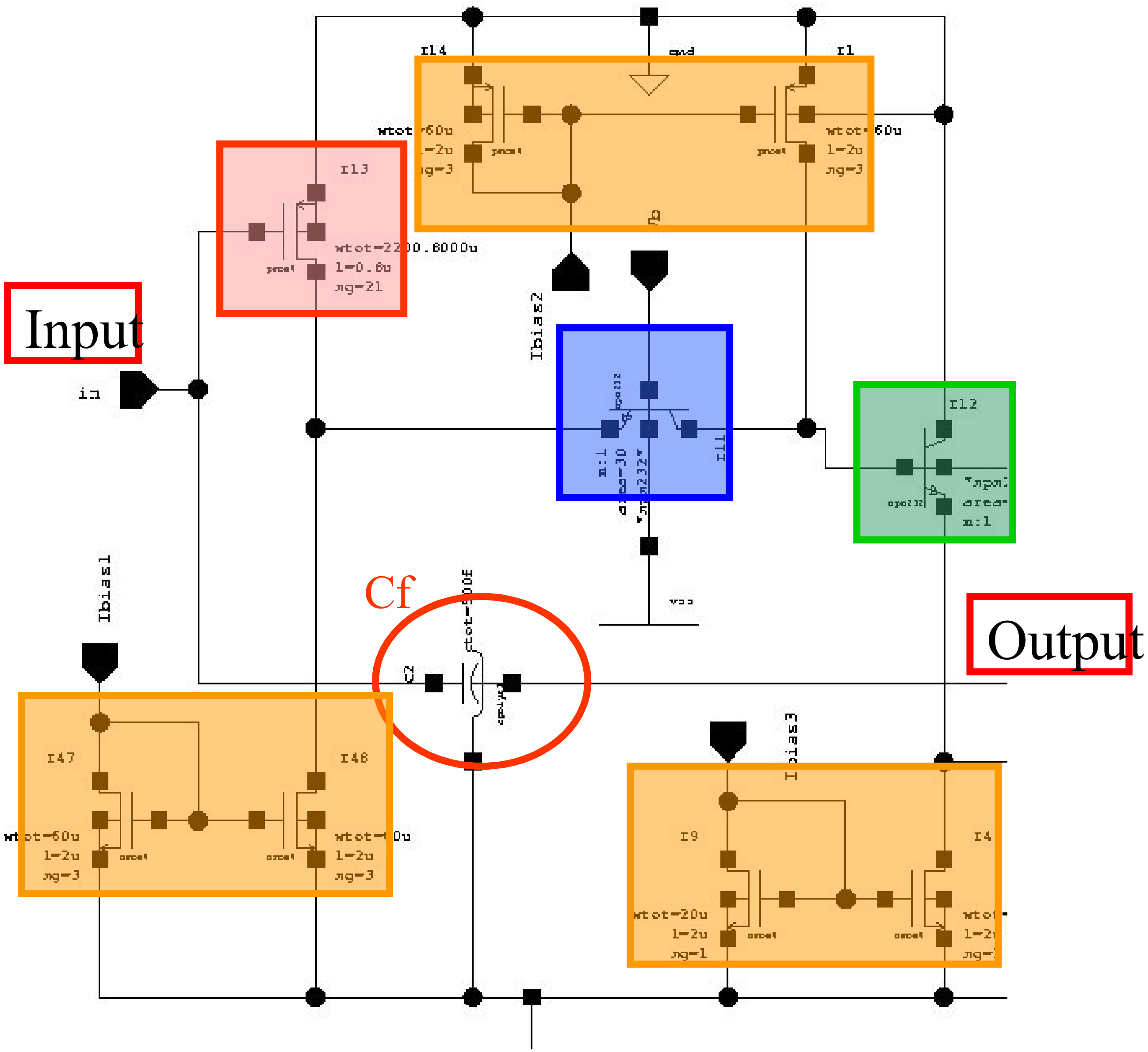


Gain (open loop) :

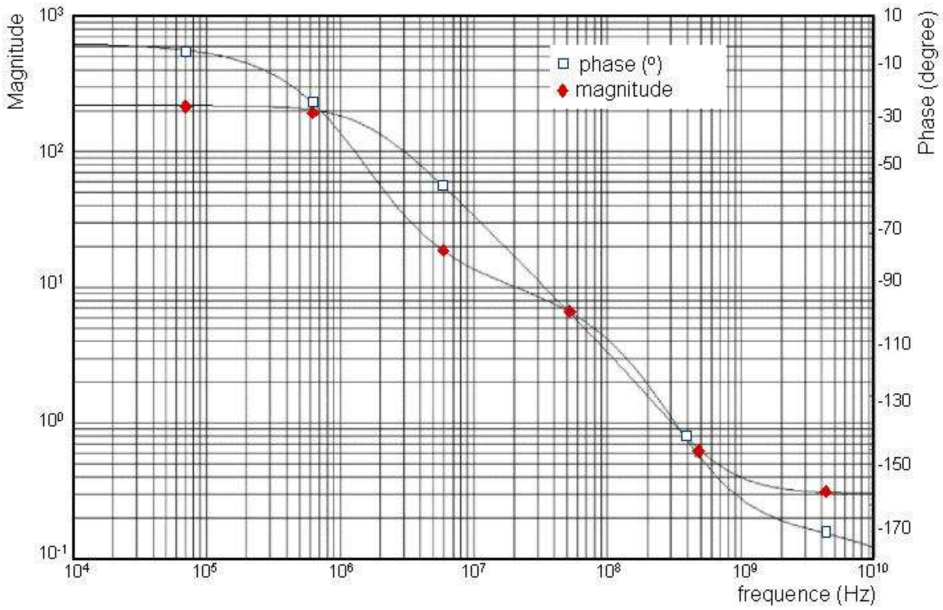
$$v_{out}/v_{in} = -\,g_{m1} R_0 / (1 + j\omega\, R_0 C_0)$$

- *Ex : g_{m1}=20mA/V , R_0=500kΩ, C_0=1pF => $G_0=10^4$ $\omega_0=2 10^6$ $G_0\omega_0=2\ 10^{10}$ = 3 GHz !*

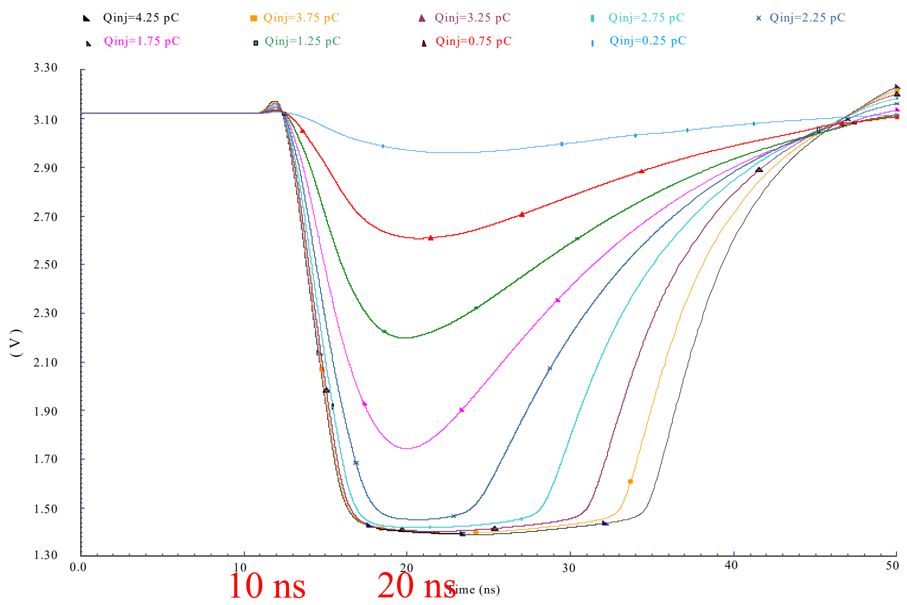
- Complete schematic
  - Adding bias elements



- Complete simulation
  - Checking hand calculations against 2nd order effects
  - Testing extreme process parameters (« corner simulations »)
  - Testing robustness (to power supplies, temperature…)



Simulated open loop gain



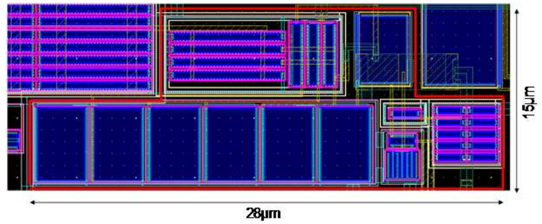
Saturation behaviour

Example : designing a charge preamp (6)

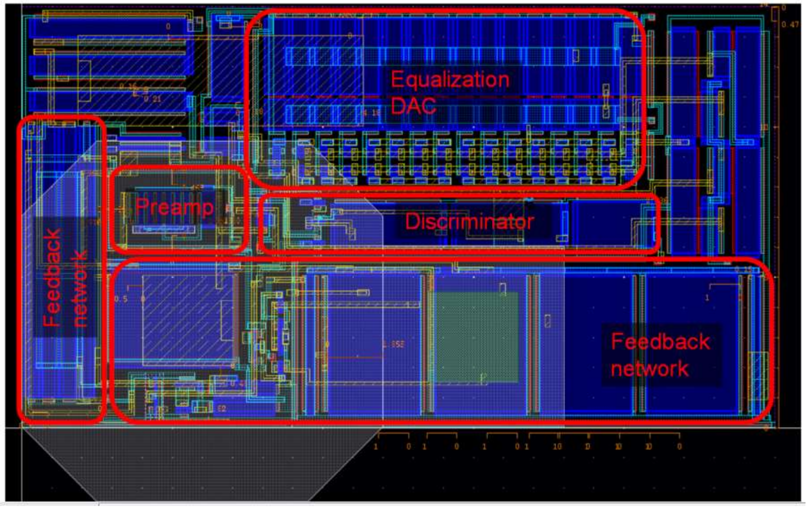
- Layout
  - Each component is drawn
  - They are interconnected by metal layers

- Checks
  - DRC : checking drawing rules (isolation, minimal dimensions…)
  - ERC : extracting the corresponding electrical schematic
  - LVS (layout vs schematic) : comparing extracted schematic and original design
  - Simulating extracted schematic with parasitic elements

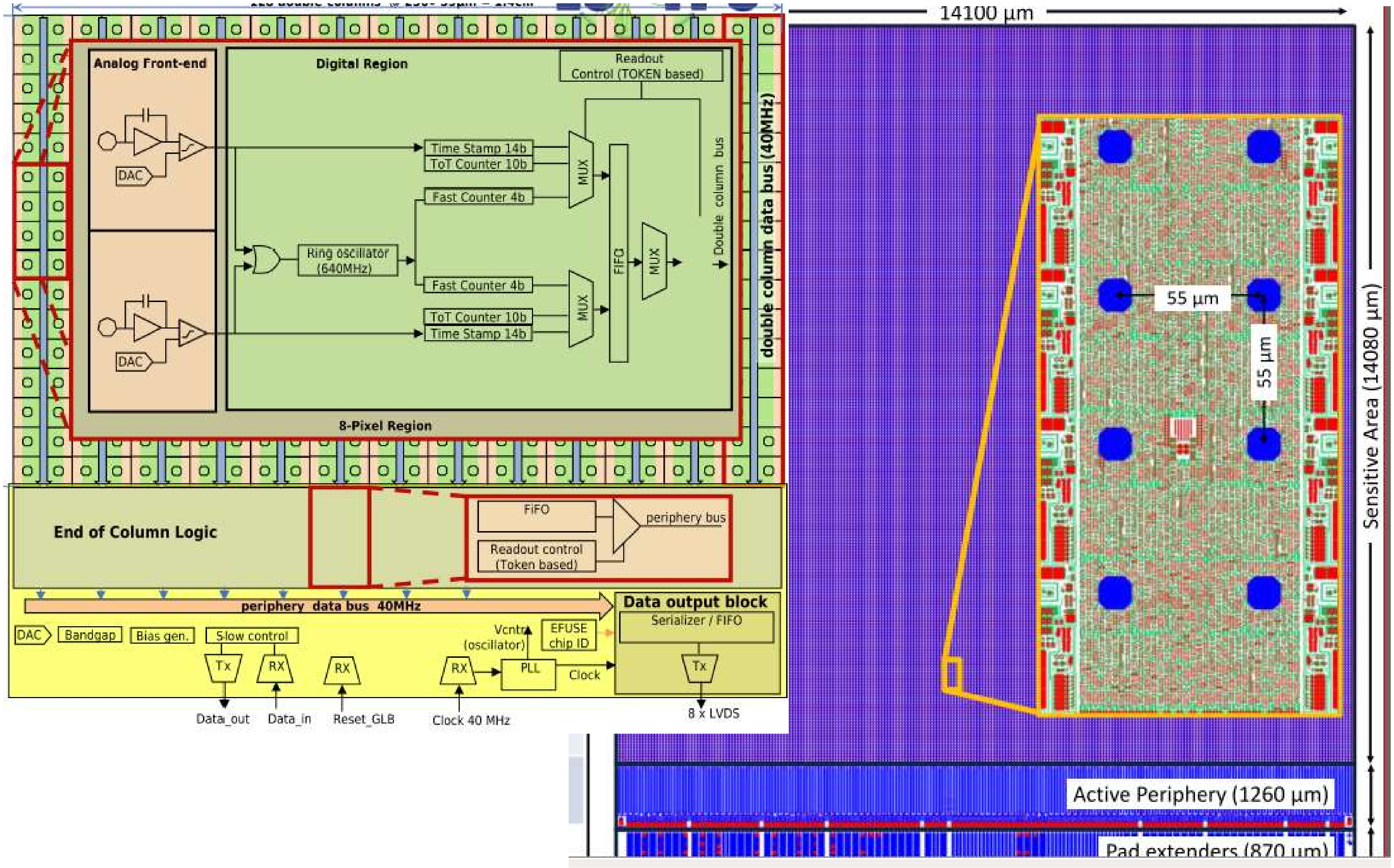
- Generating GDS2 file
  - Fabrication masks : « reticule »



Charge preamp in 65nm
Clicpix P. Valerio (CERN 2013)

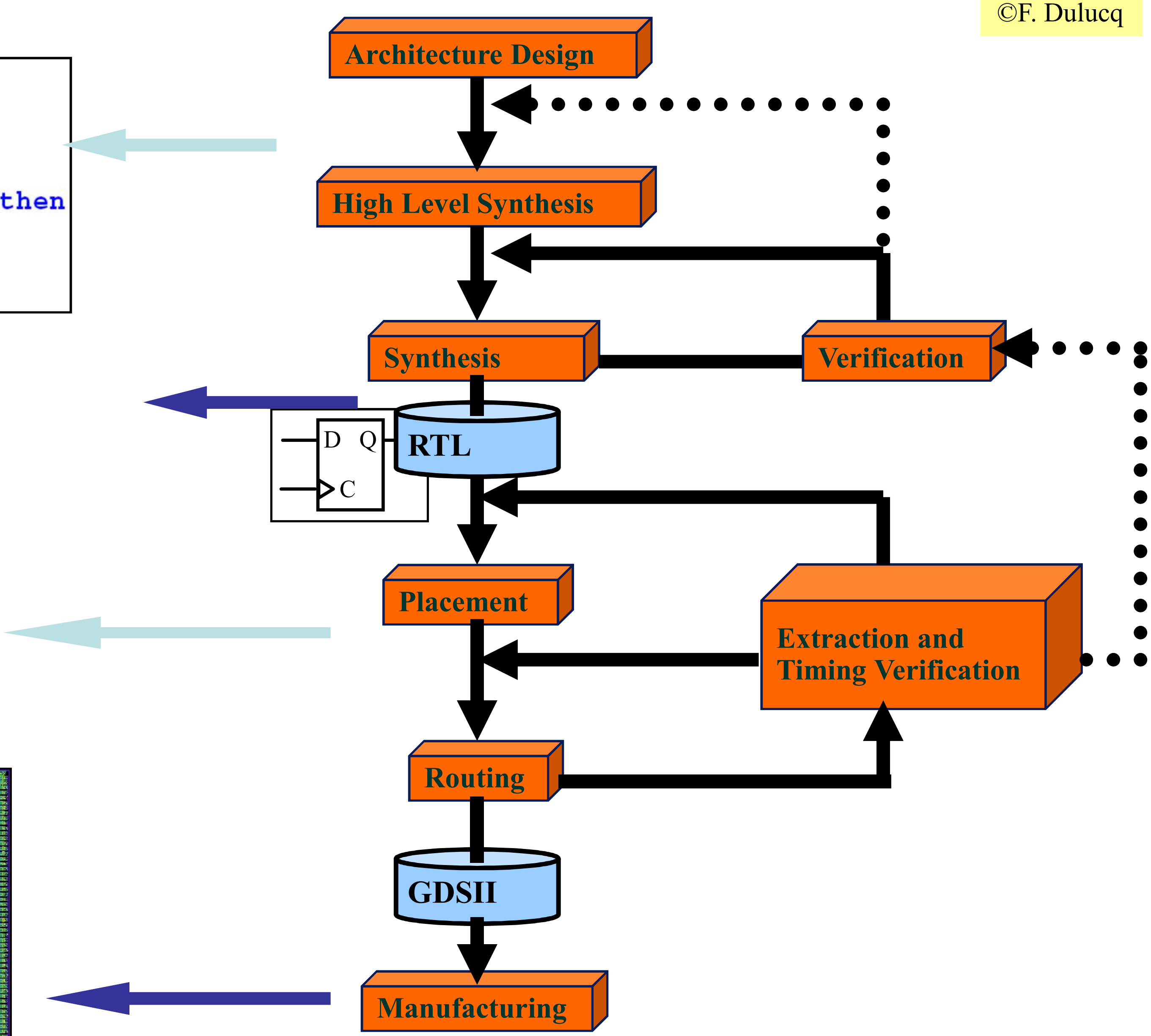


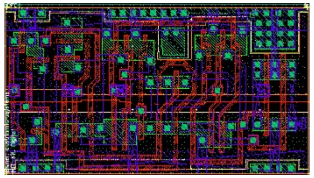
From preamp to chip : Timepix 3…

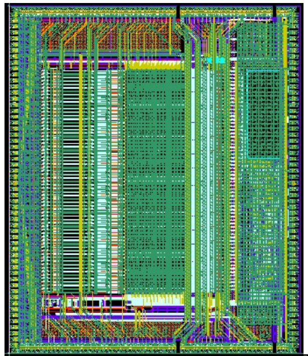


Digital implementation global Flow

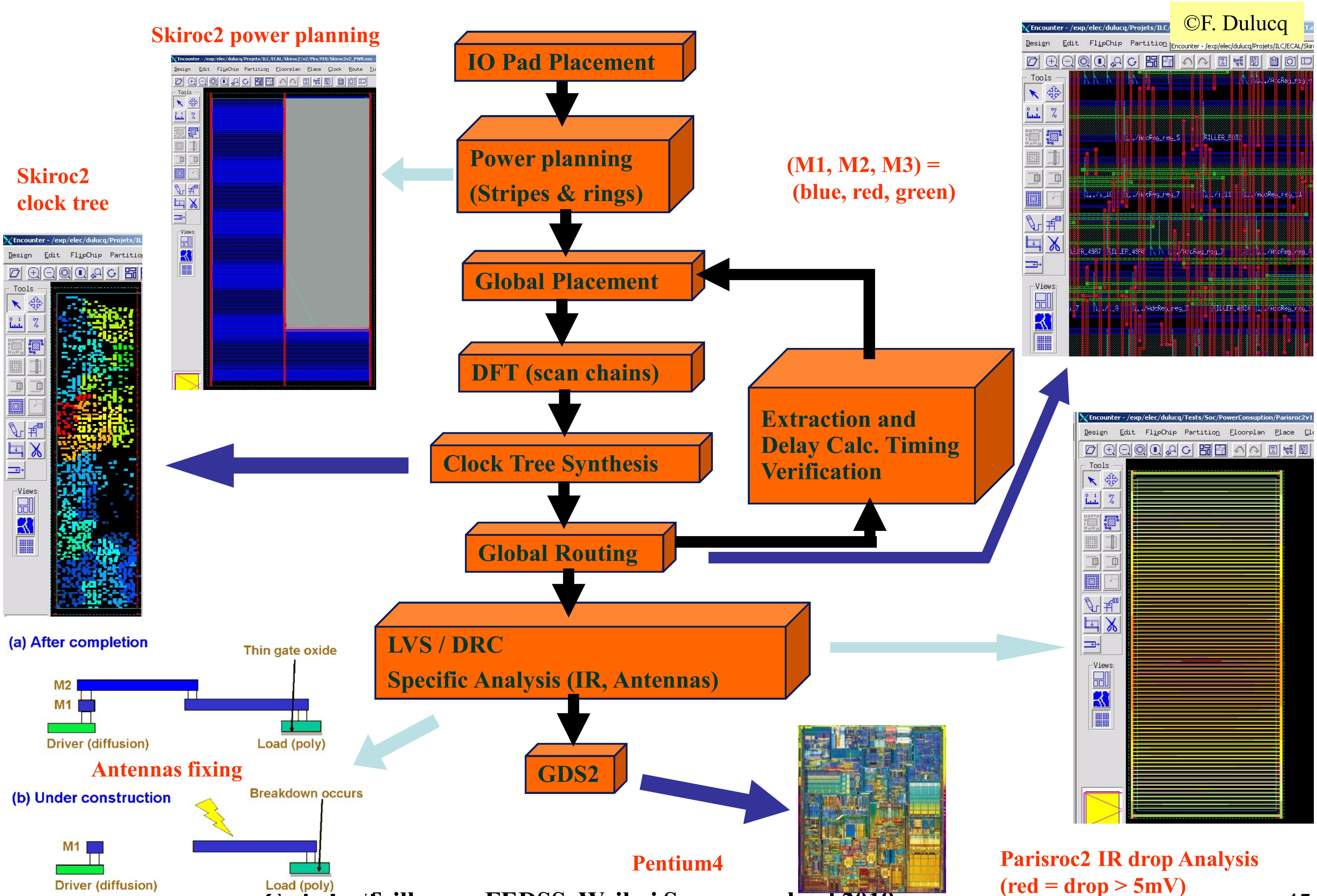

```
process(Rstb, Clk)
begin
  if Rstb ='0' then
    Q <= '0';
  elsif rising_edge Clk then
    Q <= D;
  end if;
end process;
```







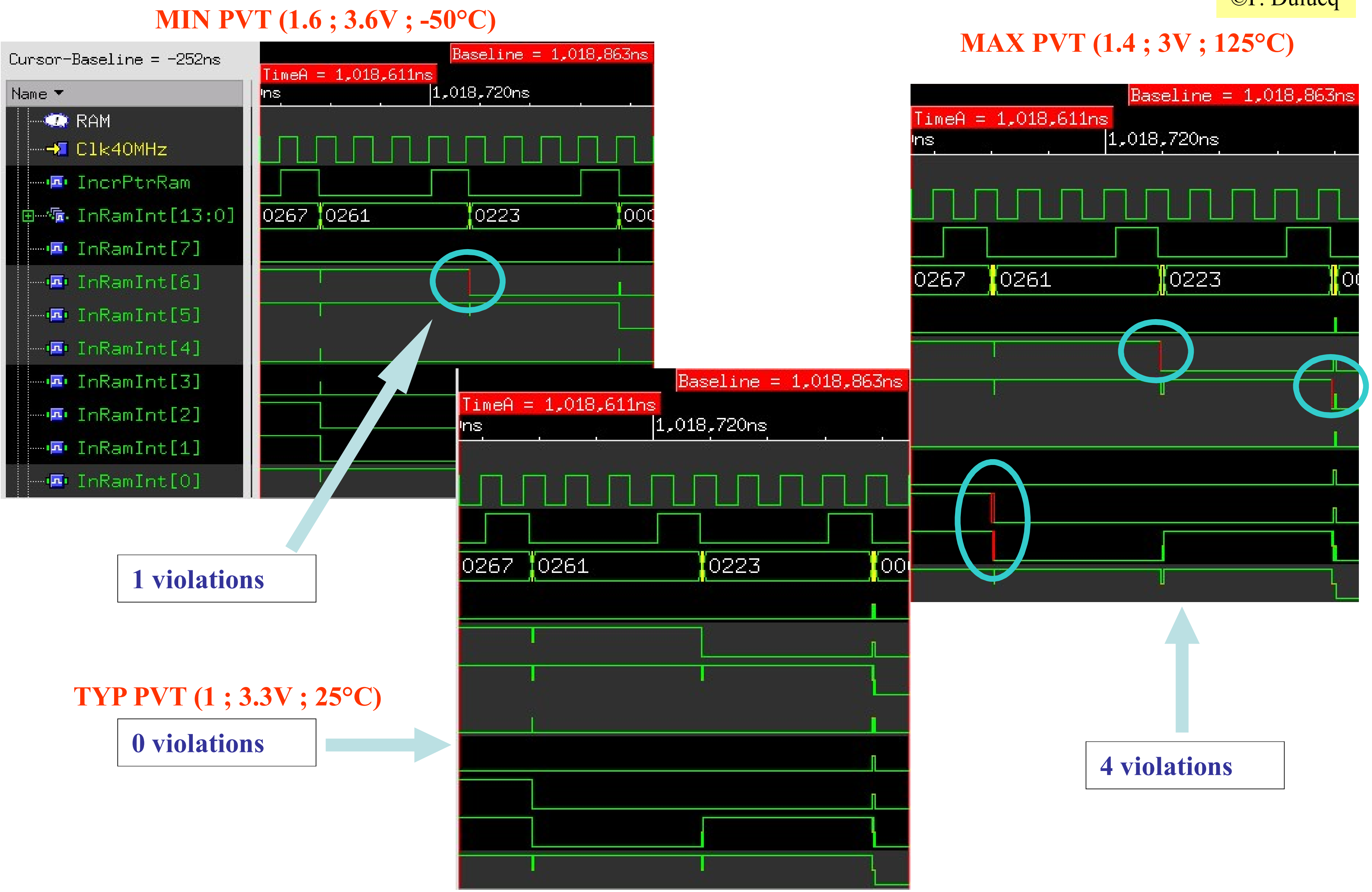
ASIC specific flow for digital routing



Post layout simulation (extracted RC)

Ωmega

©F. Dulucq

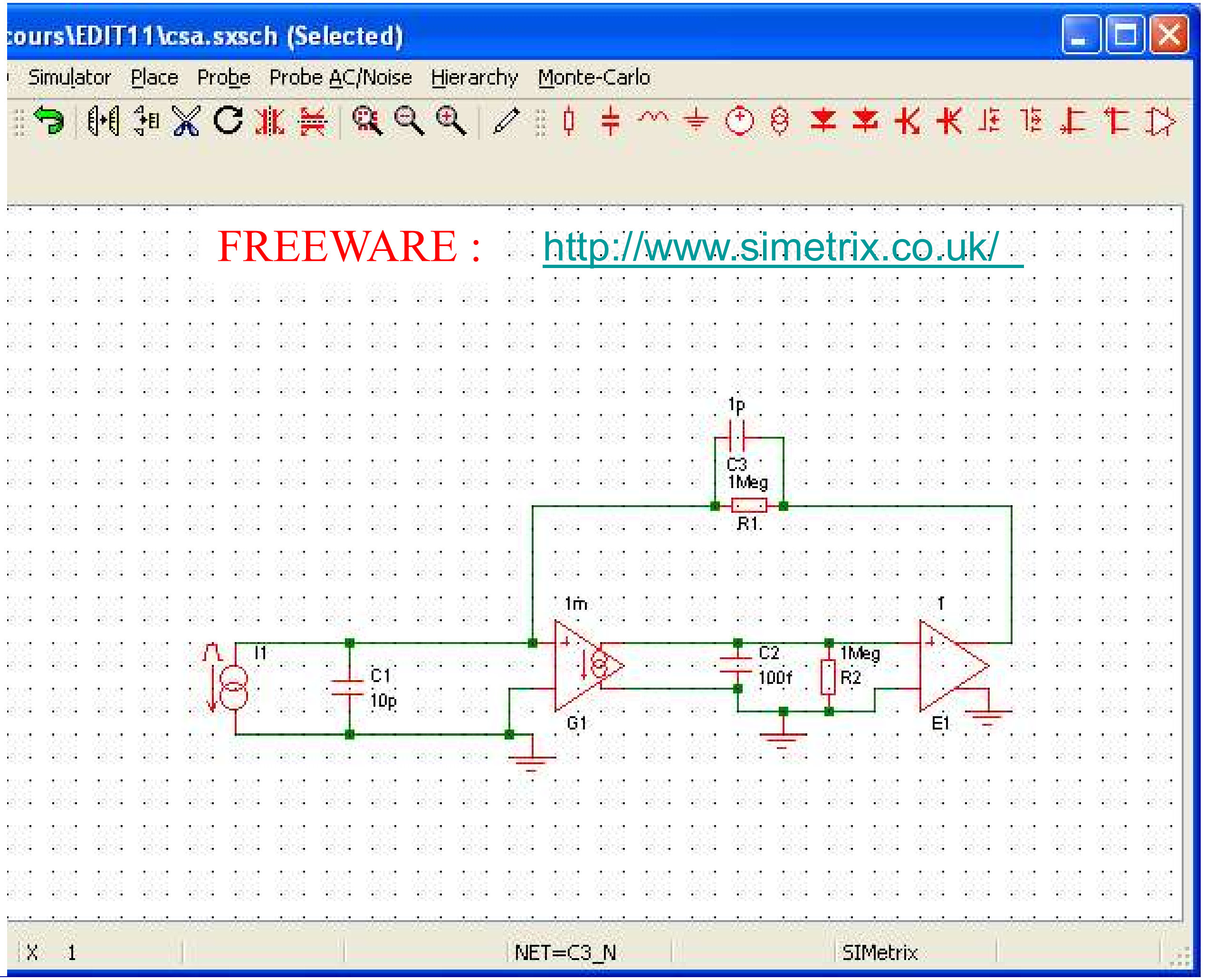


- Coexistence analog-digital
  - Capacitive, inductive and common-impedance couplings
  - A full lecture !
  - A good summary : there is no such thing as « ground », pay attention to current return

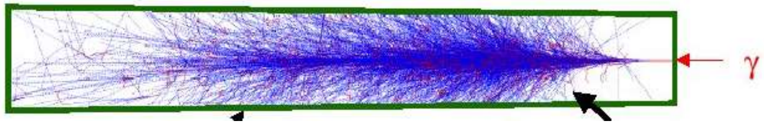
Simple simulations : Simetrix freeware

Example : bandwidth and EMC of simple charge preamp

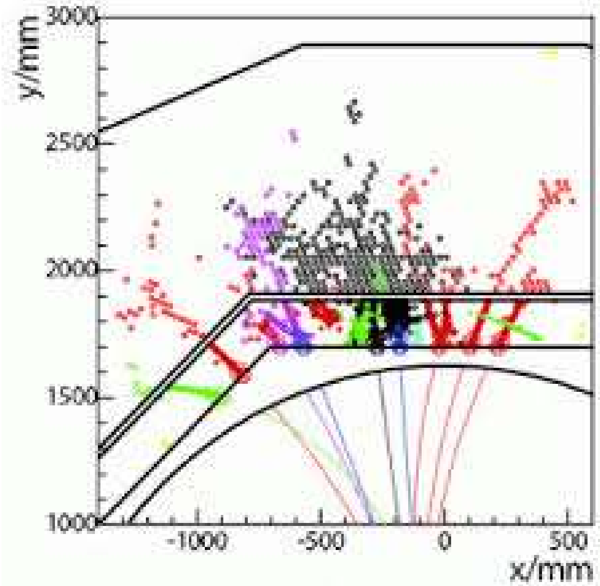
- Simulate impulse response
- Frequency response
- Input impedance
- Ballistic deficit
- Effect of amplifier gain
- Effect of resistive feedback
- Test pulse injection
- Effect of input capacitance
- Parasitic inductance
- Capacitive crosstalk
- Resistive/Inductive ground return

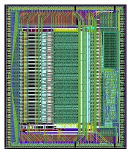


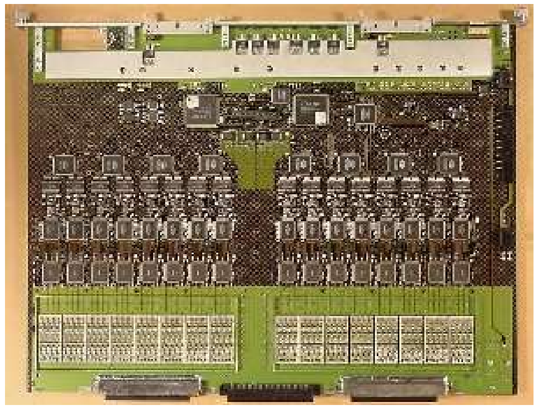
Evolution of calorimetry



- 3D calorimetry : eta, phi, Energy
- 4D calorimetry : x,y,z,E
- 5D calorimetry : x,y,z,E,t
  - High granularity=> Millions of channels = > Low power !
    - Power pulsing ~1% for ILC
    - Low power + C02 cooling for HL-LHC
  - Energy measurement : Large dynamic range
    - MIP sensitivity => low noise (~0.1 fC)
    - Up to thousands of MIPs (~10 pC)
  - Timing information
    - Nice addition for ILC for PID : few ns is enough
    - Crucial for HL-LHC : pileup mitigation, need few tens of ps
  - Embedded electronics vs data out
    - Daisy chain and low power busses for ILC
    - High speed e/optical links for HL-LHC
  - Radiation levels
    - Negligible at an ILC
    - Daunting at HL-LHC : >100 Mrad $1^{E}16N$



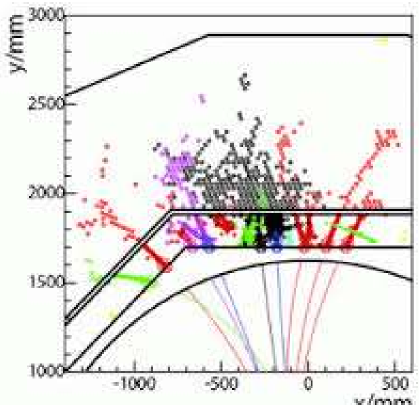




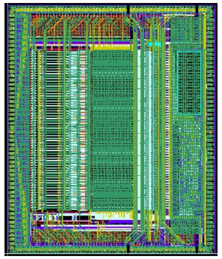
CALICE technological prototypes

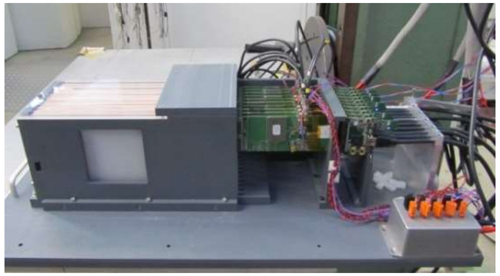
Omega

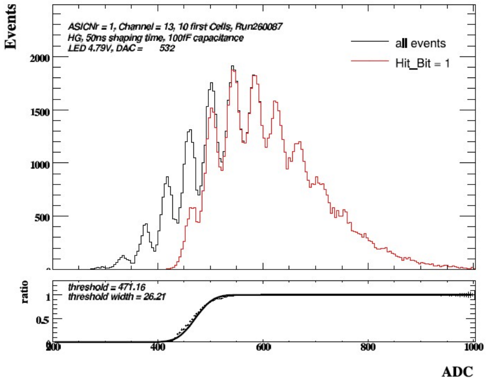
- R&D on imaging calorimetry
  - Particle Flow Algorithms [
  - Electronics crucial (low noise, low power, fully integrated)
  - Several innovative features (power pulsing, SiPM…)
  - Validation of technological prototypes
  - Common R/O features
  - Worldwide collaboration



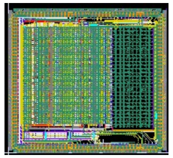
SKIROC2



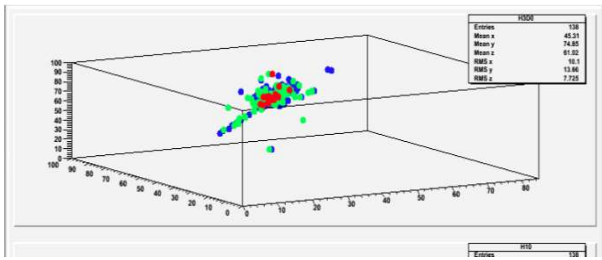




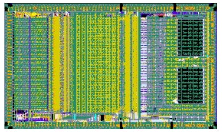
SPIROC2



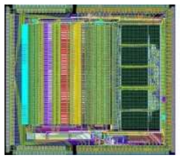
AIDA



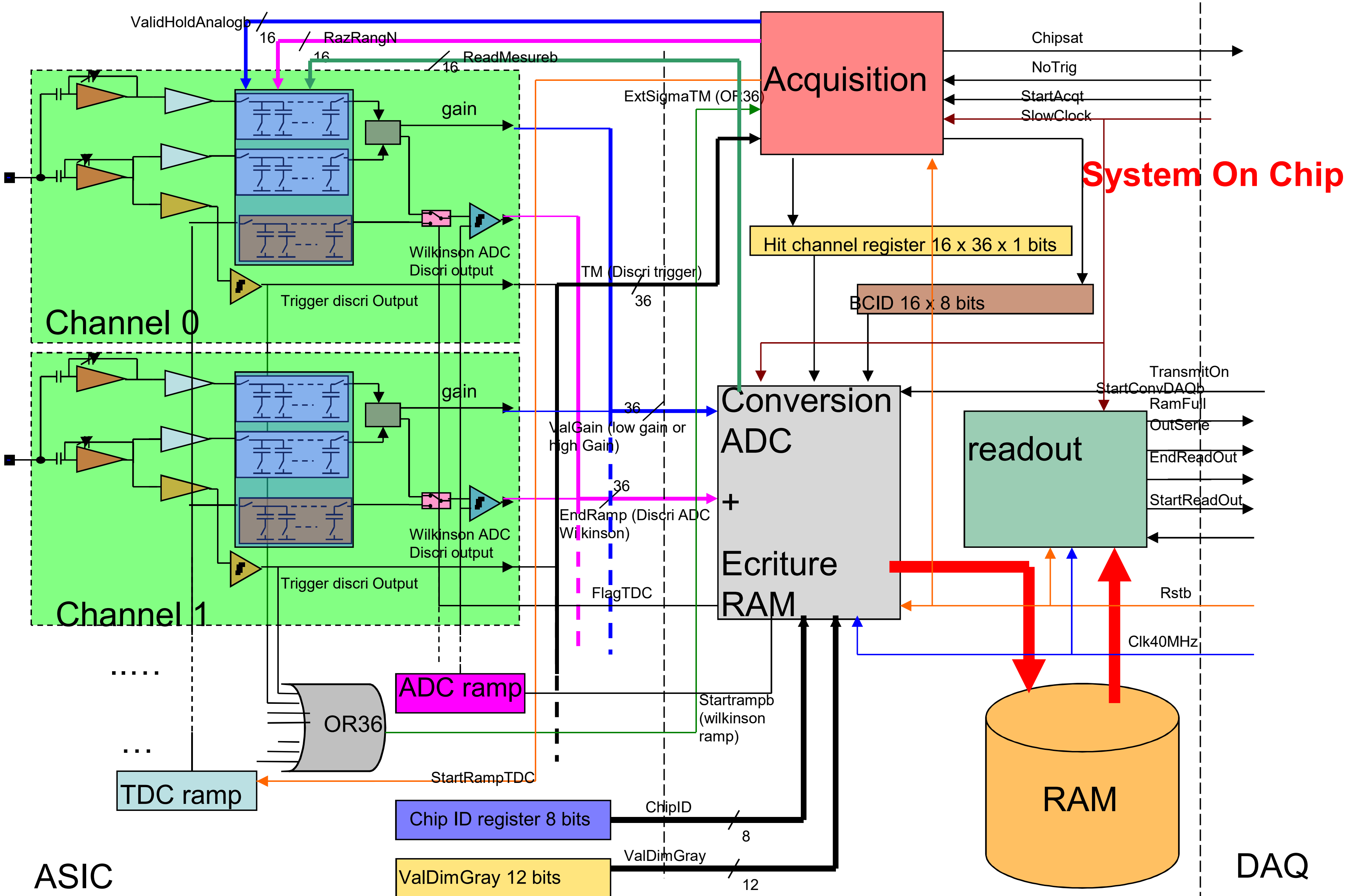
HARDROC2



MICROROC

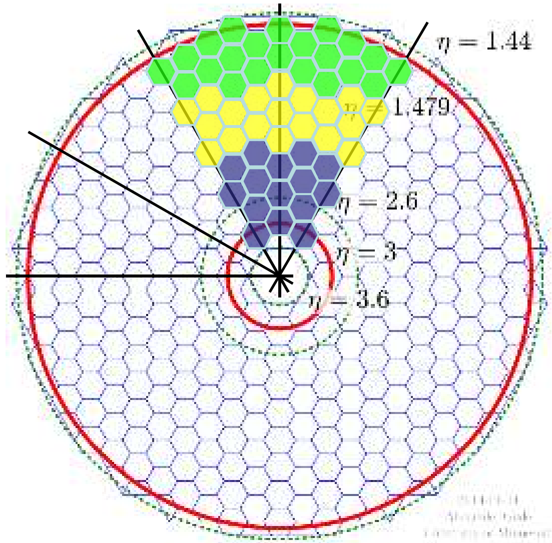


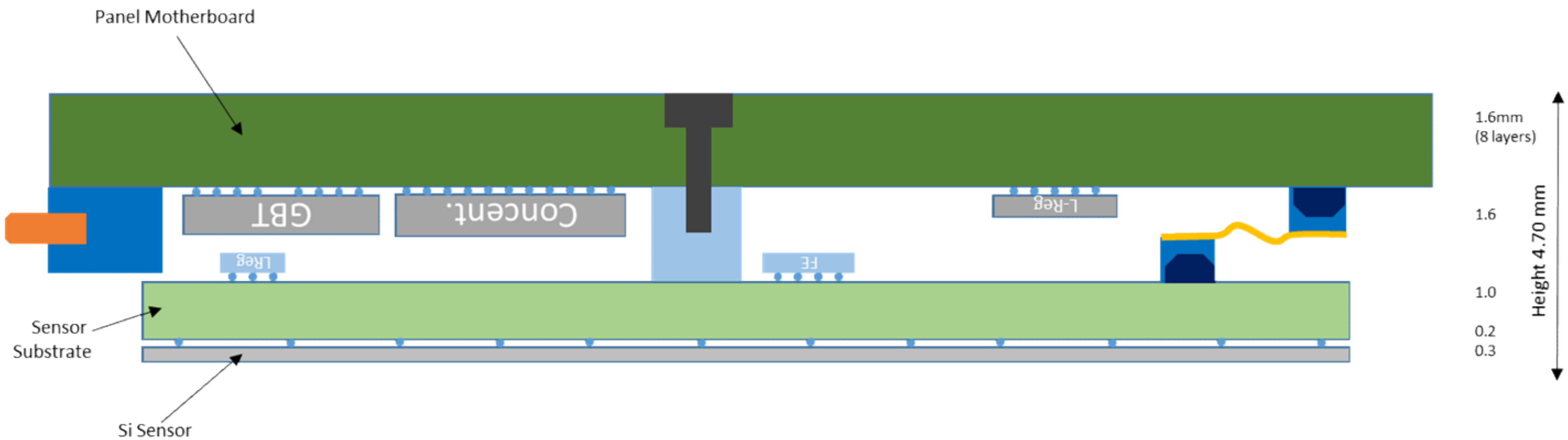
SPIROC : System On Chip



CMS HGCAL Detector overview

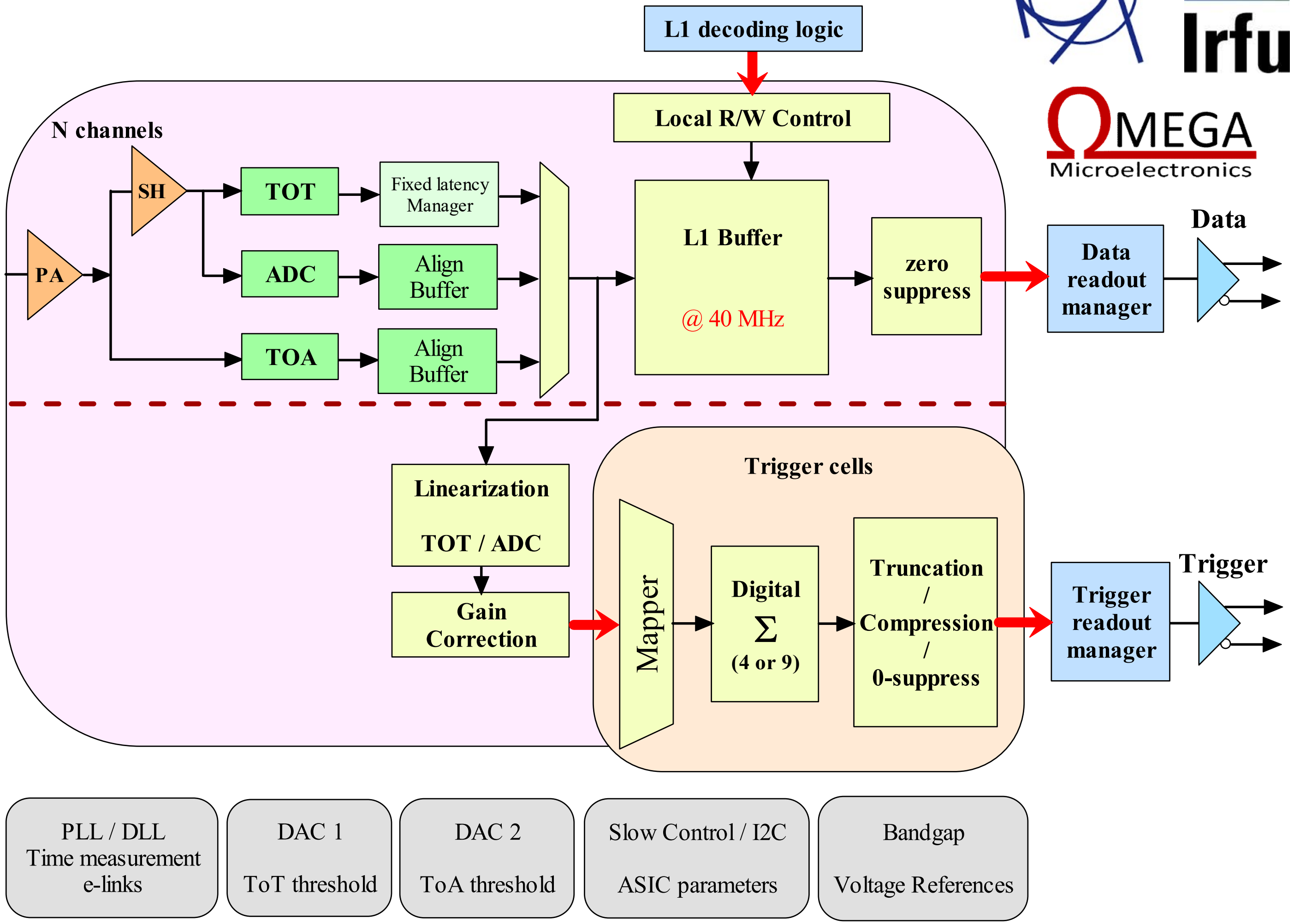
- Stringent requirements for Front-End Electronics
  - Low power (< 10 mW),
  - low noise (< 2000 e-) MIP ~ 1-4 fC
  - High radiation (200 Mrad, 10^E16 N)
  - System on chip (digitization, processing…)
  - High speed readout (5-10 Gb/s)
  - ~ 10 million channels





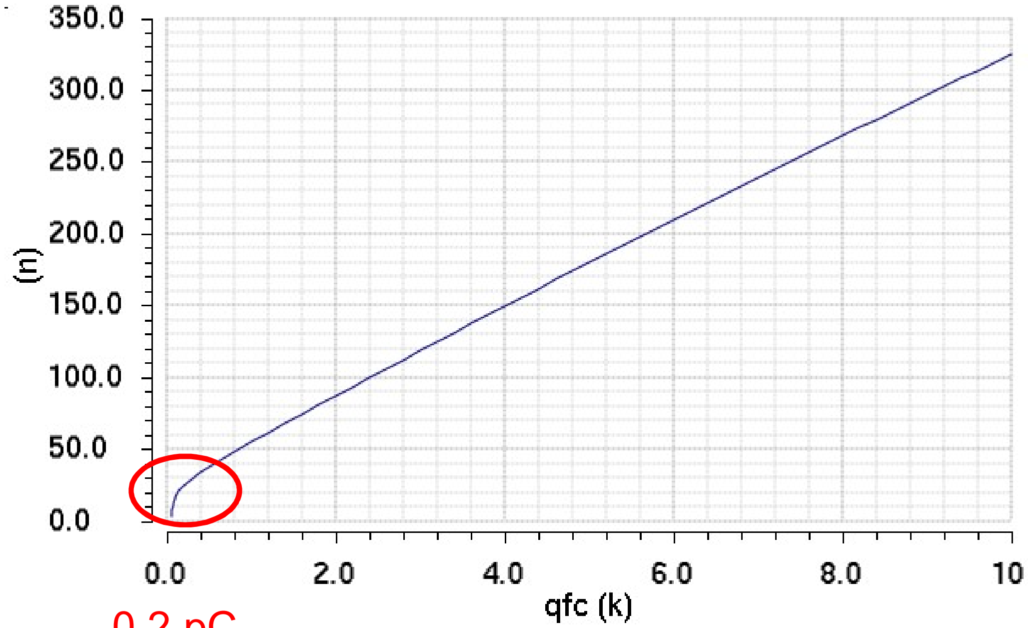
HGCAL readout ASIC : HGCROC

- 72 channels dual polarity
- 10bit 40 MHz ADC 0-100 MIPs
- TOT above with 60 ps TDC
- Timing down to 25 ps
- Trigger sums at 40 MHz
- 1.28 Gb/s elink outputs

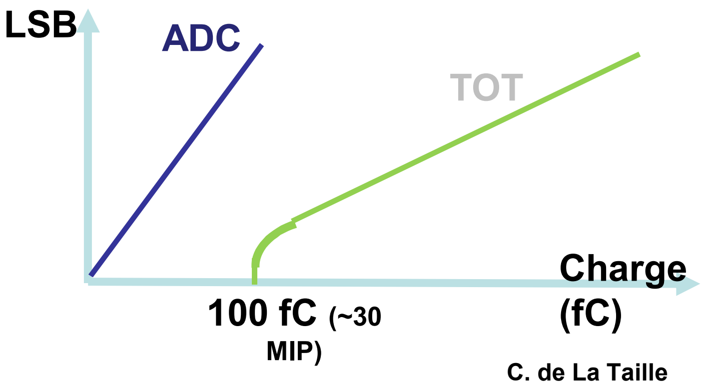


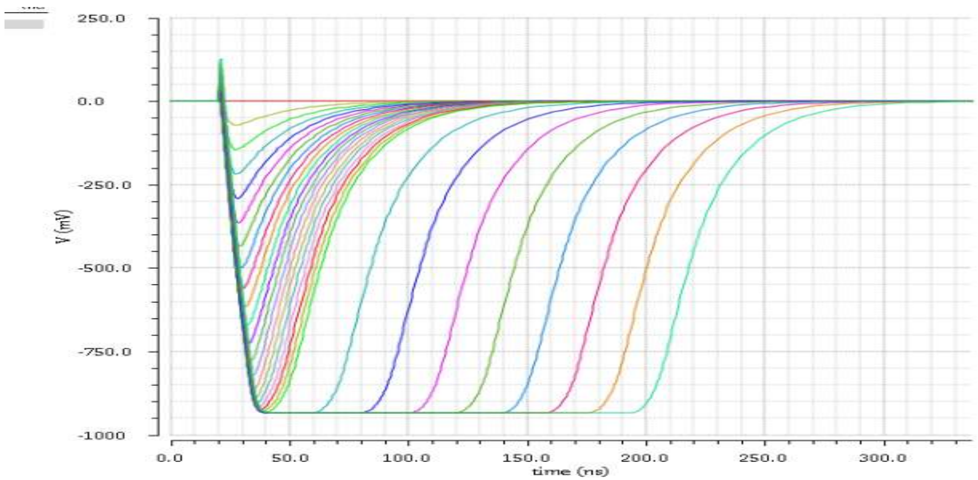
VFE architectural issues

- key issues to be studied :
  - Noise
  - Resolution
  - Stability
  - Linearity
  - Accuracy
  - Calibration
  - crosstalk
  - Radiation
  - Timing
  - Systematic effects



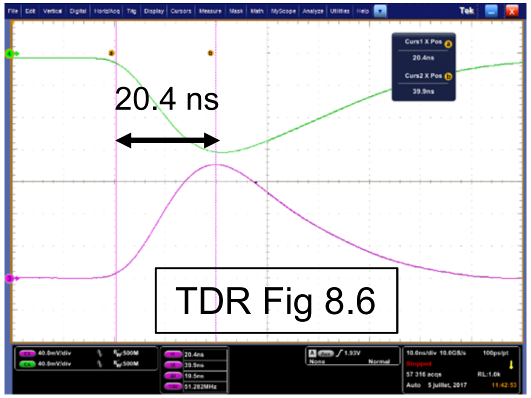
0.2 pC
~100 MIPS





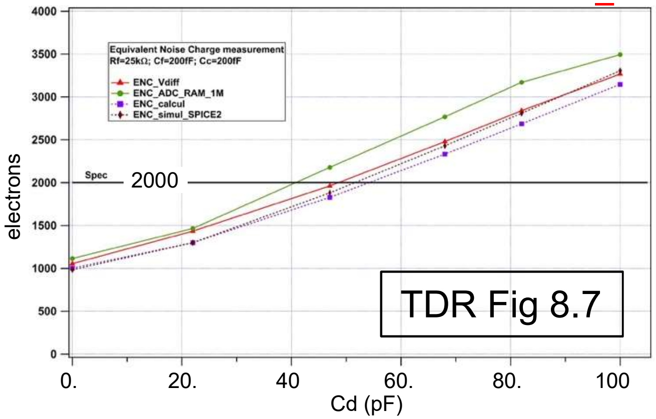
HGCROC: status

Test Vehicles 1 & 2 (2016)

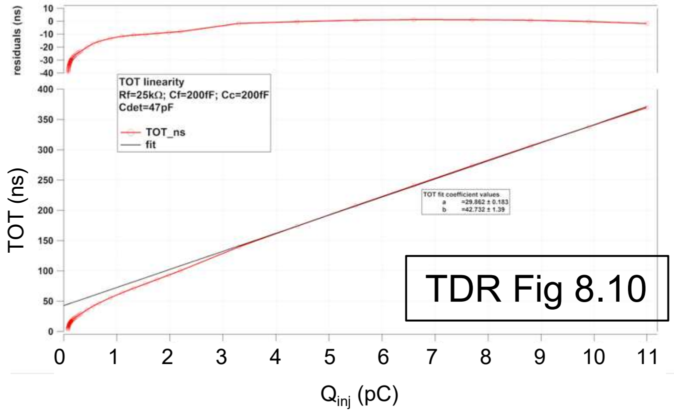


✓ Peaking time 20 ns

Measured Noise= red ENC_Vdiff



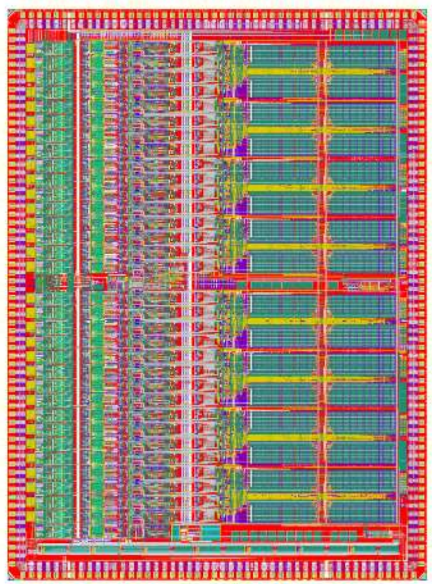
✓ Noise in agreement with simulation



✓ ToT linearity

HGCROC1 (submitted July 2017)

- Missing some digital functionalities
- 32 channels instead of 78
- 2 variants for ToT TDCs
- SAR Omega ADC
- 1.28 Gb/s E-links
- L1 Buffer: provisional SRAM (too high power, new one being designed)
- Now under test



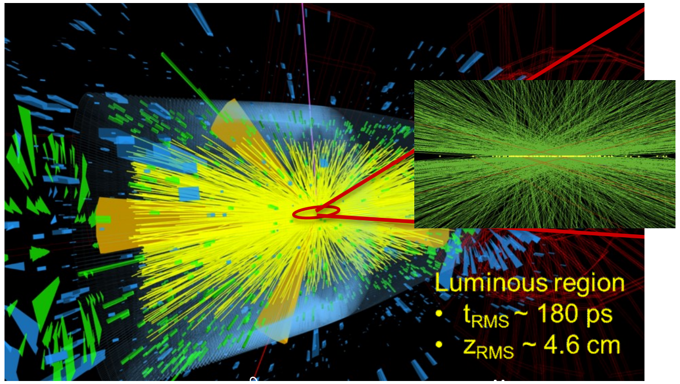
OMEGA Microelectronics · Irfu · CERN · Imperial College London

Need for timing

- Time resolution <50ps required by many experiments/applications keeping low power, large dynamic range ….

- **PET/ Time of Flight** measurements (SiPM)
  - Dynamic range : 1 pe (100fC) up to 3000 pe (300 pC)
  - Time resolution <100ps

- **CMS High Granularity CALorimeter**: (Si pin diodes)
  - Large dynamic range : few fC up to ~10 pC
  - Calorimetry => Precision /linearity < 1%
  - Fast timing ability ~50ps (for > 10 mips desirable)
  - Peaking time 15-20 ns (minimize noise, minimise Out of Time pileup)
  - Power on detector < ~10 mW/channel all included



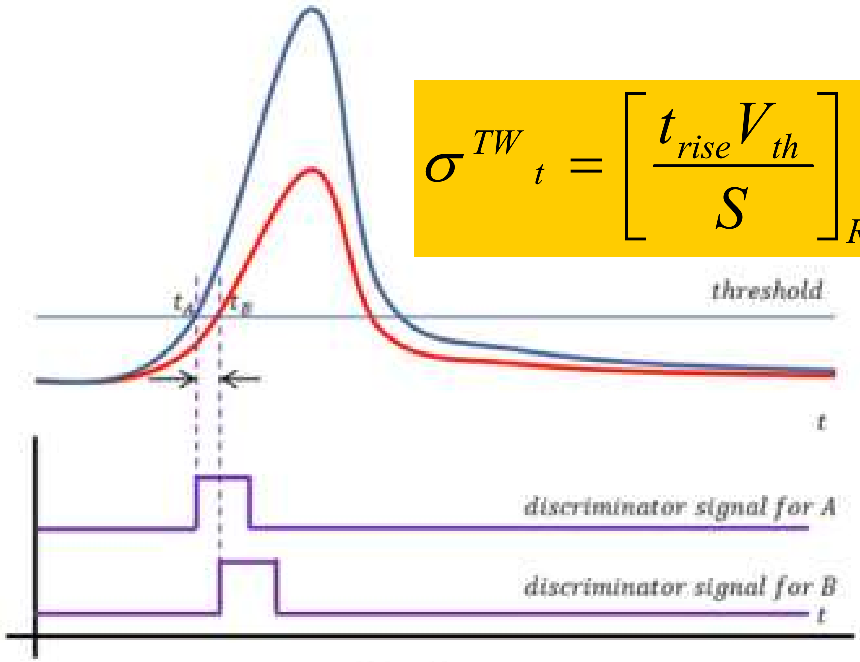
- **ATLAS High Granularity Timing Detector** (LGAD)
  - Time performance ~30 ps : To reject Time Pile up events => better particle identification

Time walk and time jitter (see talk by A. Rivetti)

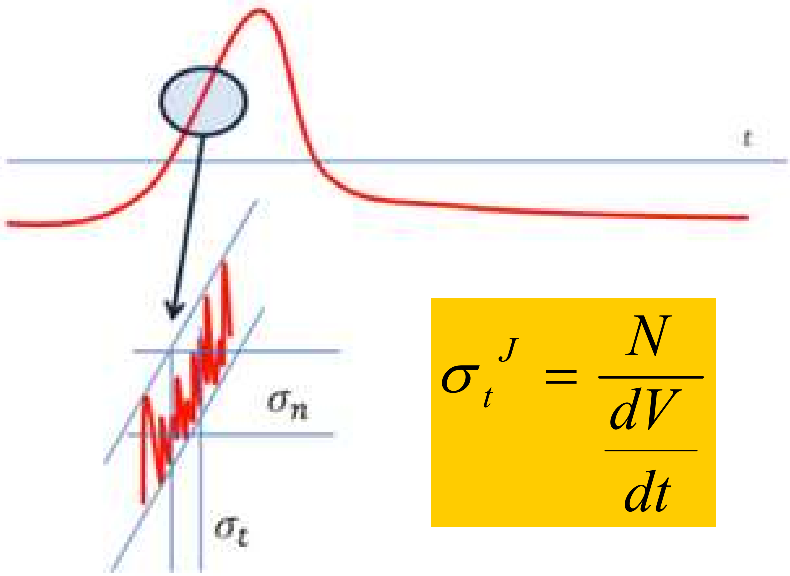
Time walk: the voltage value Vo is reached at different time for signal of different

Jitter: the noise is summed to the signal, causing amplitude variations

$$\sigma^{TW}_{t} = \left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}$$



Time walk effect



$$\sigma_t^{J} = \frac{N}{\frac{dV}{dt}}$$

Jitter effect

Due to the physics of signal formation

Mostly due to electronic noise

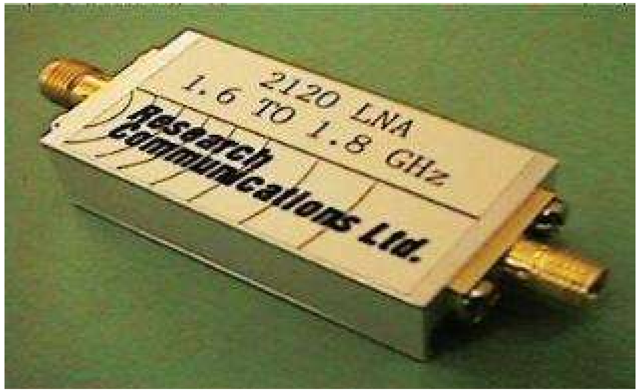
$$\sigma_t^2 = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

Jitter

Time Walk

TDC

© N. Cartiglia Trento workshop 2016
https://indico.cern.ch/event/485239/overview/


2120 LNA
1.6 TO 1.8 GHz
Research Communications Ltd.

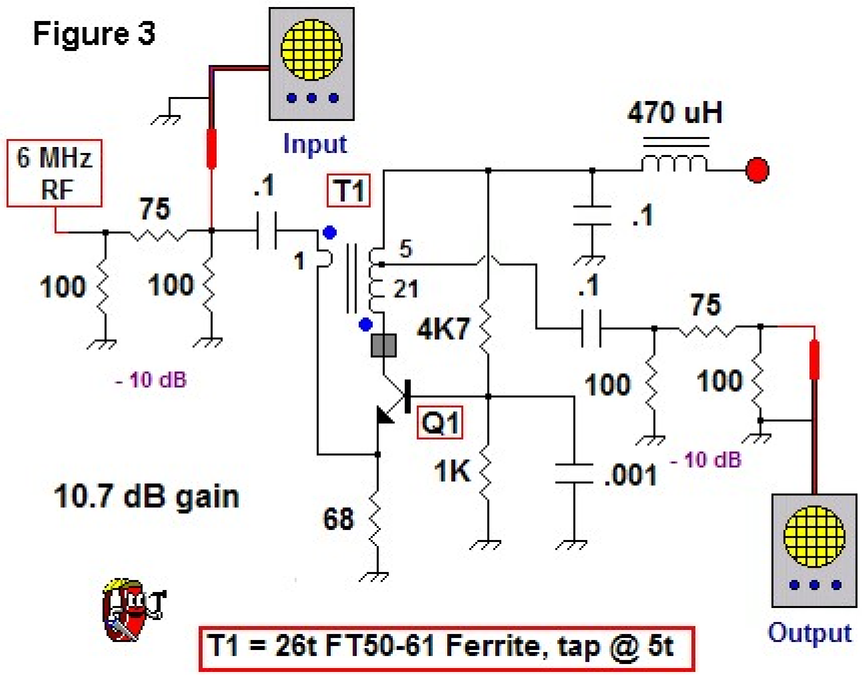
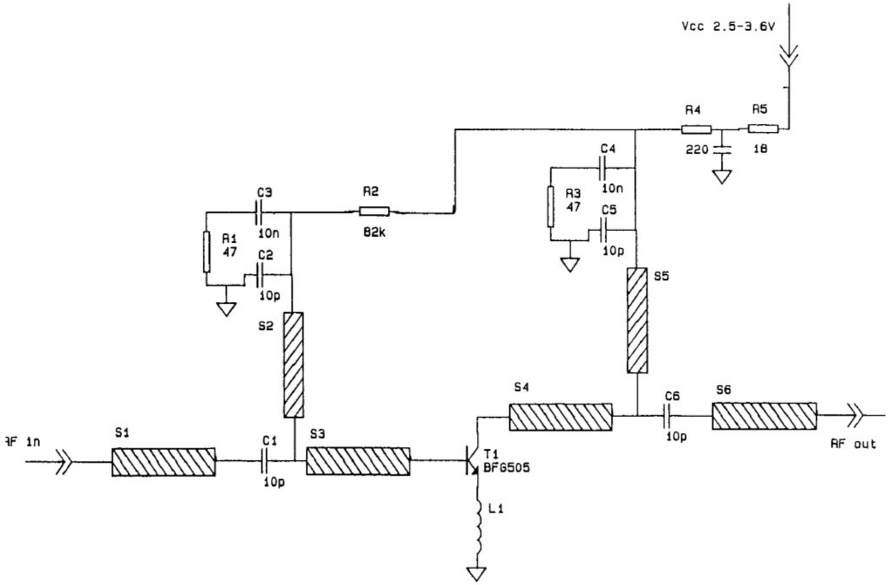
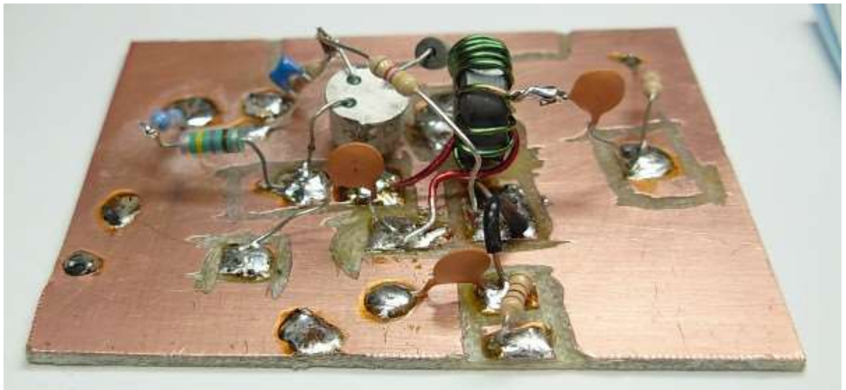


Figure 3
Input
6 MHz RF
75
.1
T1
470 uH
.1
5
1
21
100
100
4K7
.1
75
- 10 dB
100
100
Q1
1K
.001
- 10 dB
10.7 dB gain
68
T1 = 26t FT50-61 Ferrite, tap @ 5t
Output


Vcc 2.5-3.6V
R4
R5
220
18
C4
10n
R3
47
C5
10p
C3
R2
10n
82k
R1
47
C2
10p
S2
S5
S4
C6
S6
10p
RF in
S1
C1
S3
10p
T1
BFG505
L1
RF out



Timing optimization : common view

- Jitter due to electronics noise:

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}}$$

- also presented as j = tr / (S/N)
- dV/dt prop to BW, N prop to √ BW => jitter prop to 1/√BW

⇒ « the faster the amplifier the better the jitter ? »

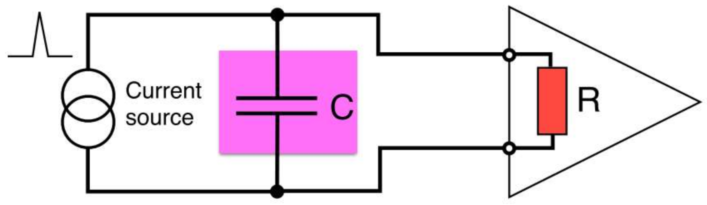
⇒ « High speed preamps need to be low impedance (50 Ω or less) »

NB : tr = $t_{10\text{-}90\%}$ = 2.2 tau.

f_{-3dB} = 1/2πtau = 0. 35 / $t_{10\text{-}90}$

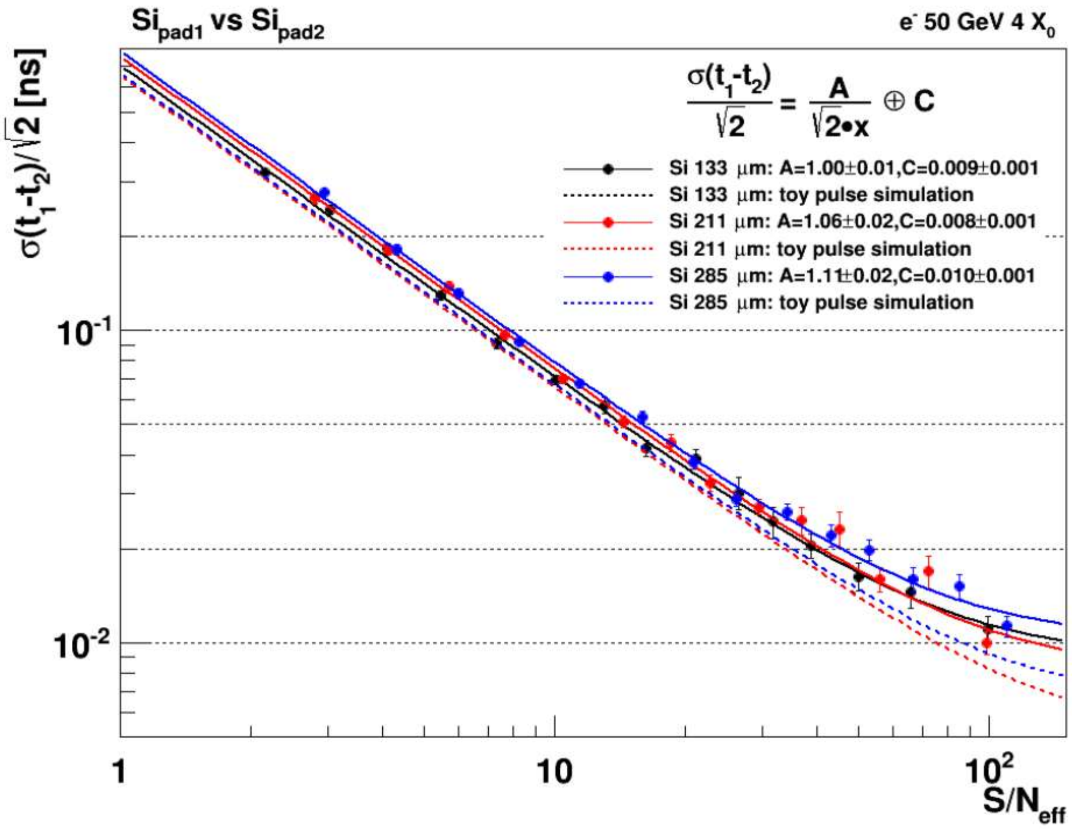
f_{-3dB} = 1 GHz <-> $t_{10\text{-}90\%}$ = 300 ps

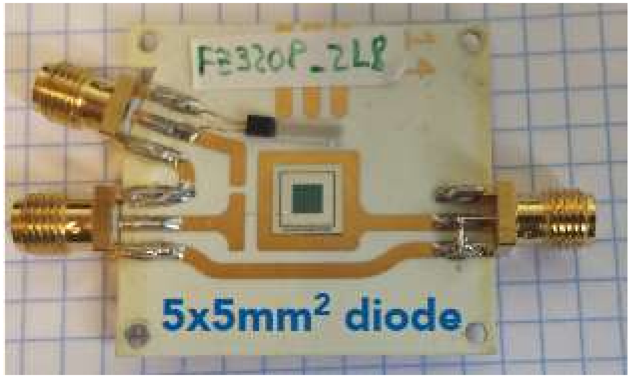
1 ps = 300 µm in vaccum

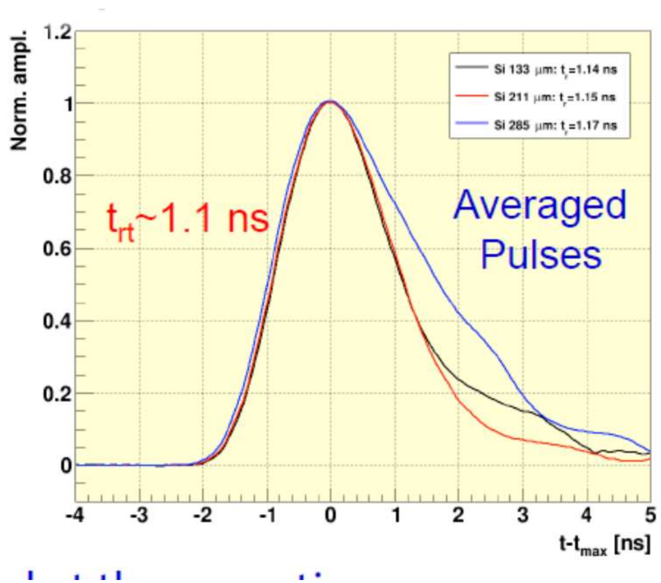


HGCAL timing performance

- CMS HGCAL testbeam measurements
- Jitter : j ~1 ns / S/N
  - But S and N depend on BW…
  - Parts come from detector and from electronics



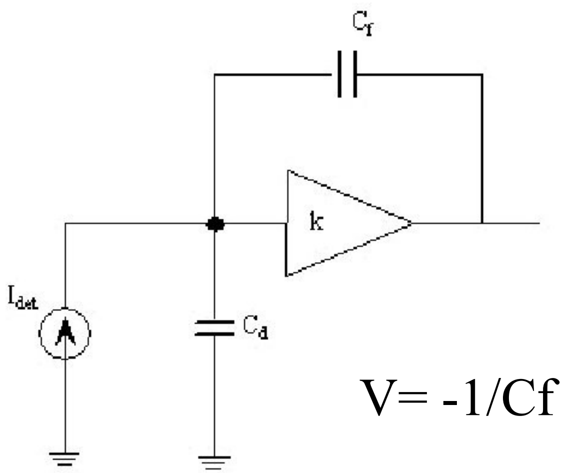




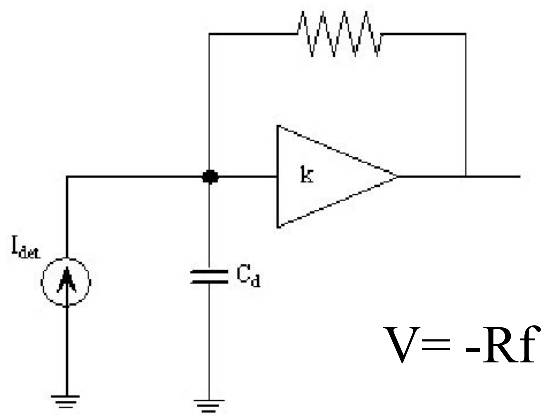
© M. Mannelli et al. ACES 2016
https://indico.cern.ch/event/468486

- Charge preamp
- Capacitive feedback Cf
- Vout/Iin = - 1/jωCf
- Perfect integrator : vout=-Q/Cf∫
- Difficult to accomodate large SiPM signals (200 pC)
- Lowest noise configuration
- Need Rf to empty Cf

- Current preamp
- Resistive feedback Rf
- Vout/Iin = - Rf
- Keeps signal shape
- Need Cf for stability



$V = -1/Cf \int i(t)dt$



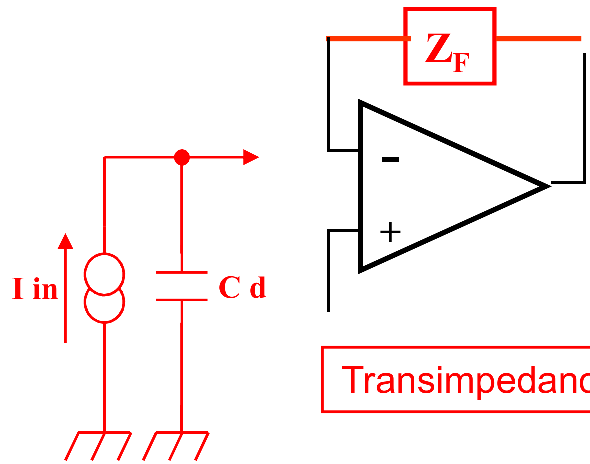
$V = -Rf\ i(t)$

Transimpedance configuration

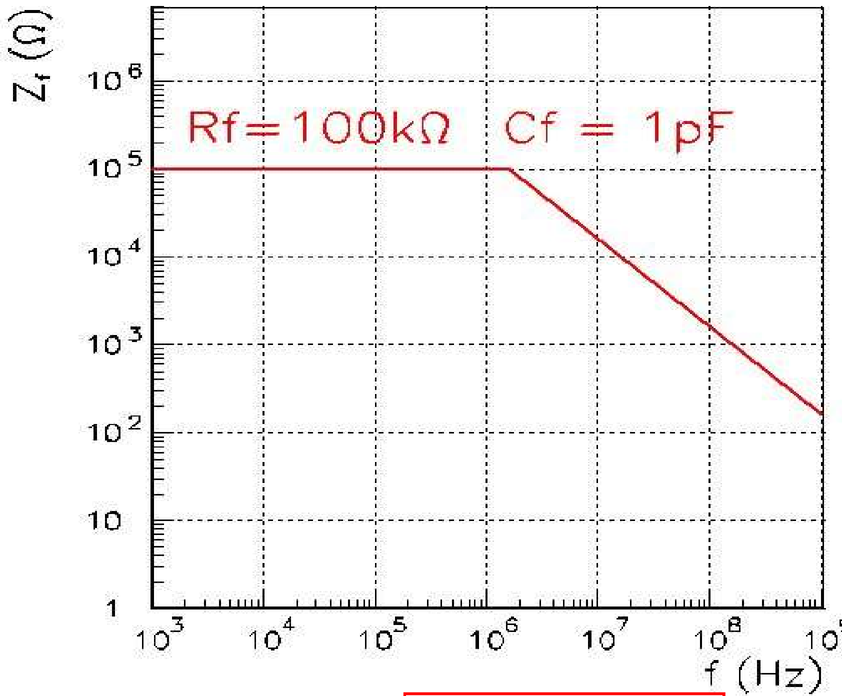
- Transfer function
  - Using a VFOA with gain G
    - $V_{out} - v_{in} = - Z_f\, i_f$
    - $V_{in} = Z_d\,(i_{in} - i_f) = - v_{out}/G$
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f\, /\, (1 + Z_f\, /GZ_d)$

- $Zf = Rf\, /\, (1 + j\omega\, RfCf)$
  - At $f << 1/2\pi RfCf$:
    $V_{out}(\omega)/i_{in}(\omega) = - R_f$
    current preamp
  - At $f << 1/2\pi RfCf$:
    $V_{out}(\omega)/i_{in}(\omega) = - 1/j\omega C_f$
    charge preamp

- Ballistic deficit with charge preamp
  - Effect of finite gain : G_0
  - Output voltage «only» Q C_d/G_0C_f



Transimpedance amplifier



Transfer function

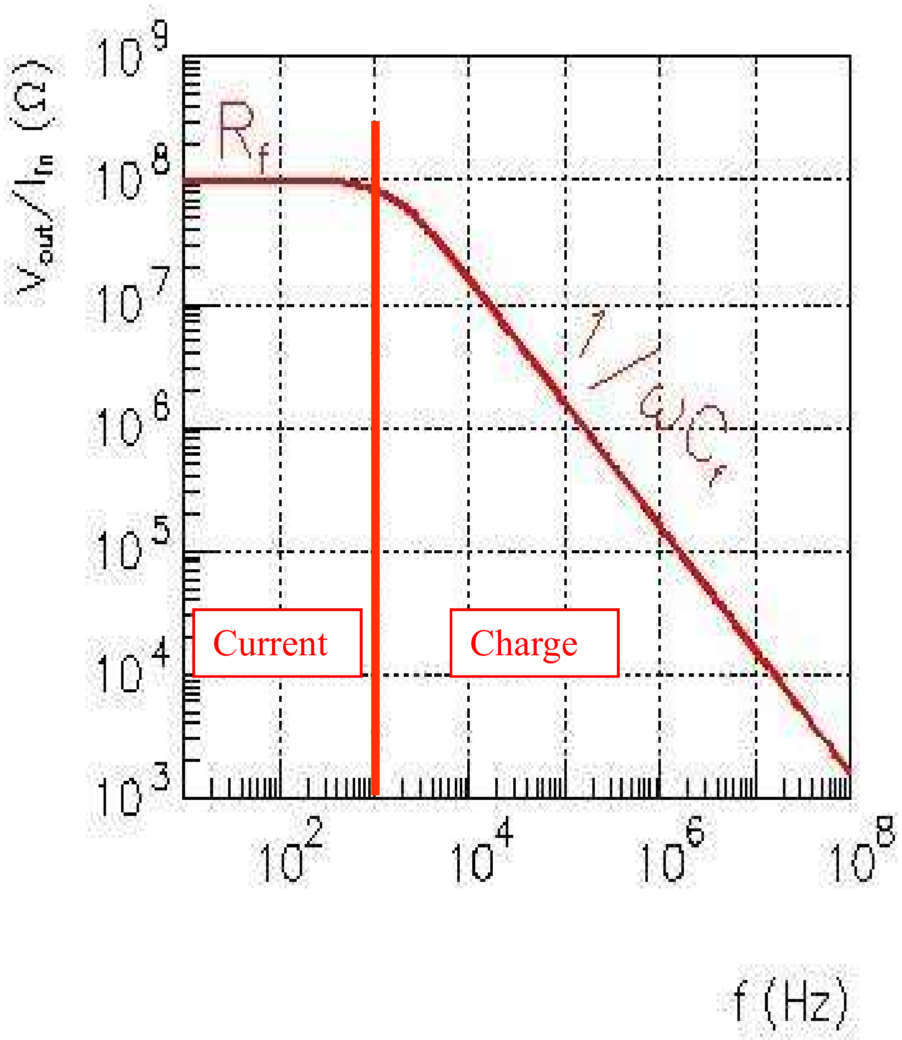
Charge vs Current preamps

- Charge preamps
  - Best noise performance
  - Best with short signals
  - Best with small capacitance

- Current preamps
  - Best for long signals
  - Best for high counting rate
  - Significant parallel noise

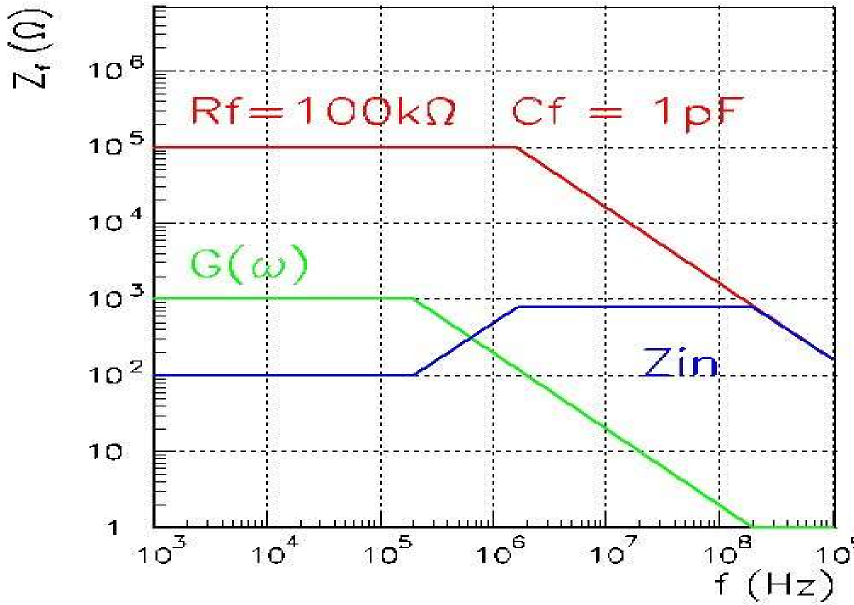
- Charge preamps are <u>not slow</u>, they are <u>long</u>

- Current preamps are <u>not faster</u>, they are <u>shorter</u> (but easily unstable)

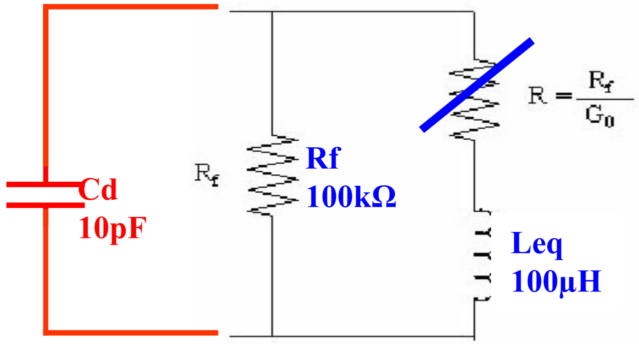


- Input impedance
  - Zin = Zf / G+1
  - Zin->0 virtual ground
  - Minimizes sensitivity to detector impedance
  - Minimizes crosstalk

- Equivalent model
  - $G(\omega) = G_0/(1 + j\,\omega/\omega_0)$
- Terms due to Cf
  - $Zin = 1/j\omega\, G_0C_f + 1/\, G_0\omega_0\, C_f$
  - Virtual resistance : $Req = 1/\, G_0\omega_0\, C_f$
- Terms due to Rf
  - $Zin = R_f/\, G_0 + j\,\omega\, R_f/\, G_0\omega_0$
  - Virtual inductance : $Leq = R_f/\, G_0\omega_0$
- Possible oscillatory behaviour with capacitive source



Input impedance or TZA



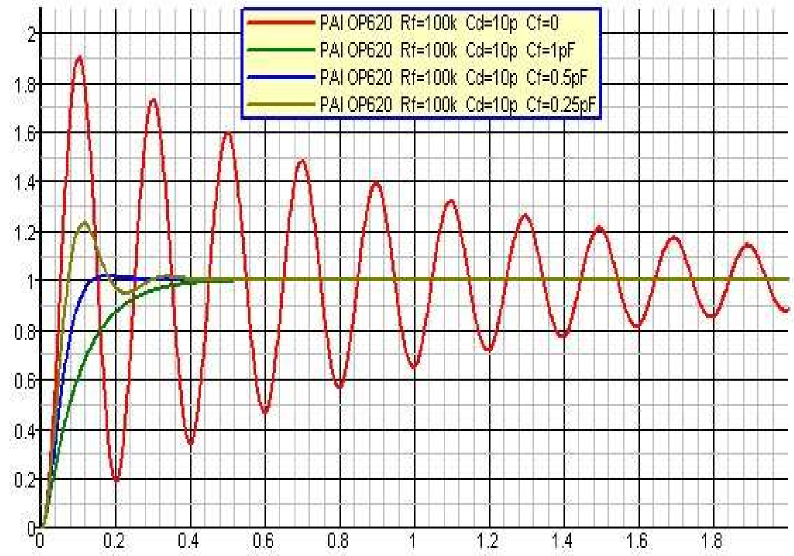
Equivalent circuit at the input

Current preamplifiers :

- Easily oscillatory
  - Unstable with capacitive detector
  - Inductive input impedance : $= R_f / \omega_C$
  - Resonance at : $f_{res} = 1/2\pi \sqrt{L_{eq} C_d}$
  - Quality factor : $Q = R / \sqrt{L_{eq}/C_d}$
    - $Q > 1/2$ -> ringing
  - Damping with capacitance C_f
    - $C_f = 2 \sqrt{(C_d / R_f G_0 \omega_0)}$
    - Easier with fast amplifiers

L_e

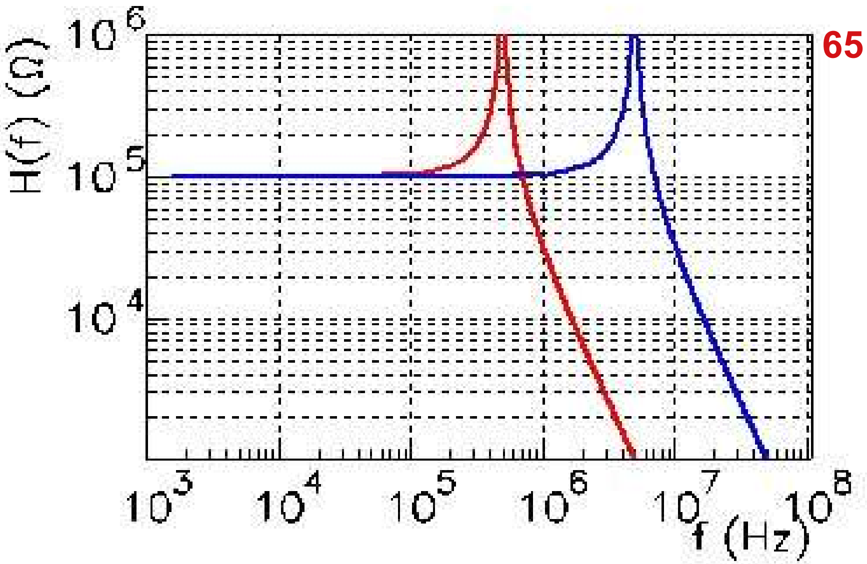
>



Step response of current sensitive preamp

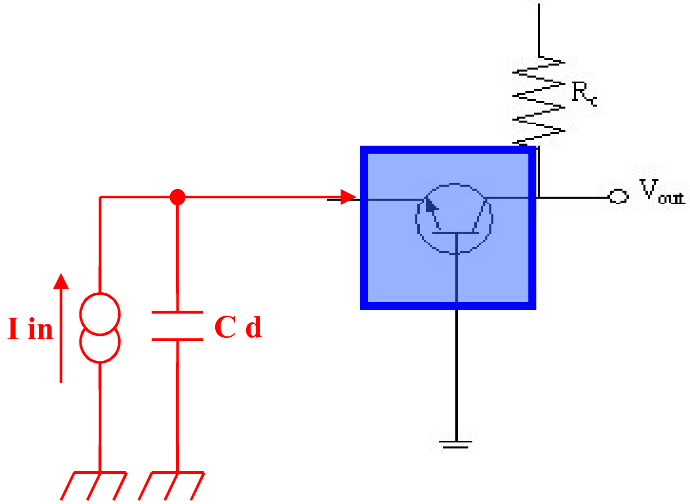
- In frequency domain
  - $H(j\omega) = -Rf / (1 + j\omega RfC_d/))$
  - $G(\omega) = G_0 / (1 + j\omega/\omega_0)$

  $H = - Rf / (1 + j\omega R_f C_d / G_0 - \omega^2 R_f C_d / G_0 \omega_0)$

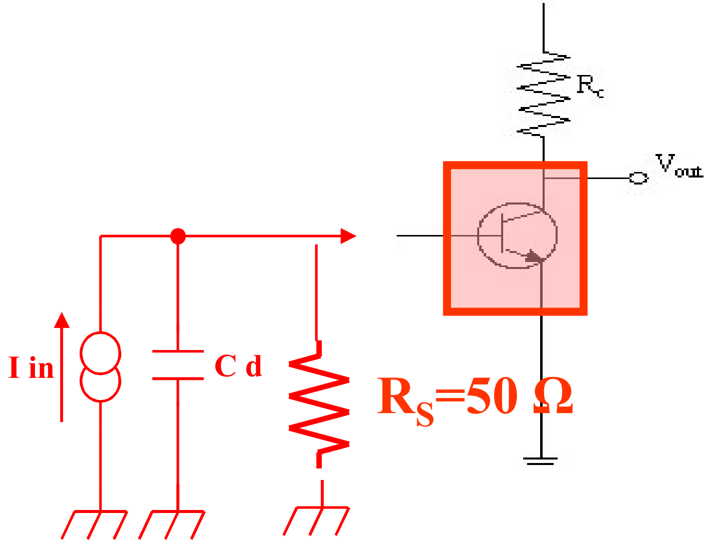


- Open loop configurations : current conveyors, RF amplifiers
- Usually designed at transistor level MOS or SiGe

- **Current conveyors**
- Small Zin : current sensitive input
- Large Zout : current driven output
- Unity gain current conveyor
- E.g. : (super) common-base configuration
- Low input impedance : Rin=1/gm
- Transimpedance : Rc
- Bandwitdth : 1/2πRcCu > 1 GHz



- **RF amplifiers**
- Large Zin : voltage sensitive input
- Large Zout : current driven output
- Current conversion with resistor R_S
- E.g. common-emitter configuration
- Transimpedance : -gmRcRs
- Bandwitdth : 1/2πRsCt

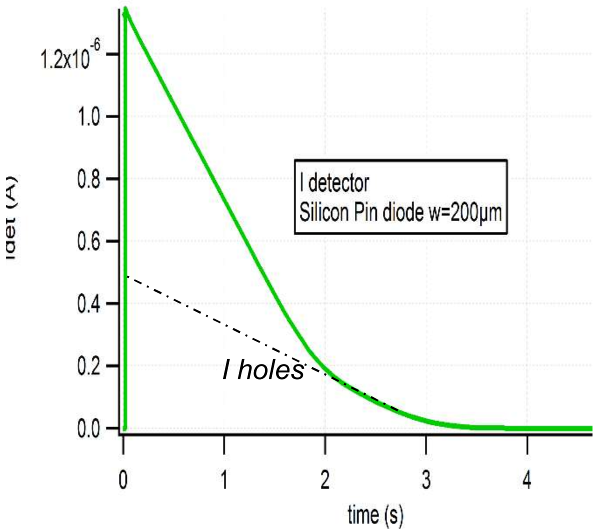


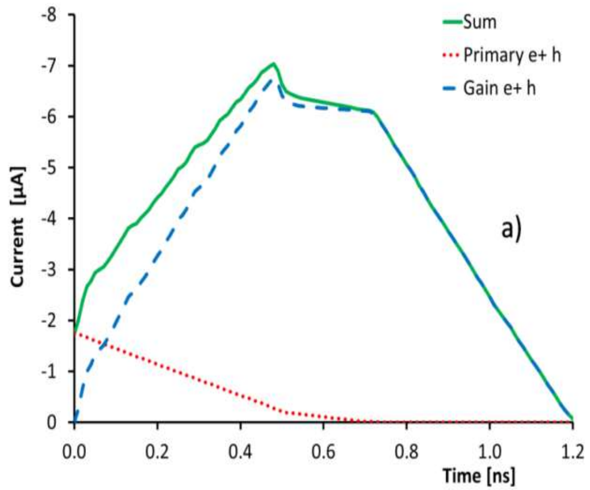
Signal : detector current

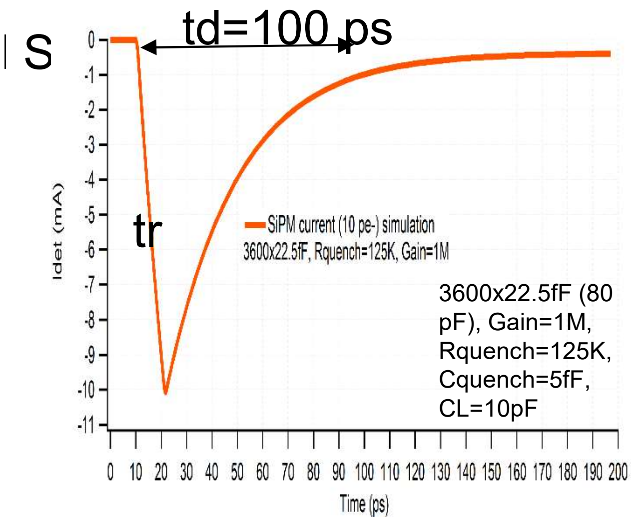
- PN diode w =200µm
- Very short rise time : tr~10ps
- Relatively long «drift time» : td~2ns

- LGAD sensor w =50µm
- rise time : tr~500ps
- Decay time» : td~700ps

- SiPM detector (10pe-)
- very short rise time : tr~10 ps
- Short duration : td~100ps),



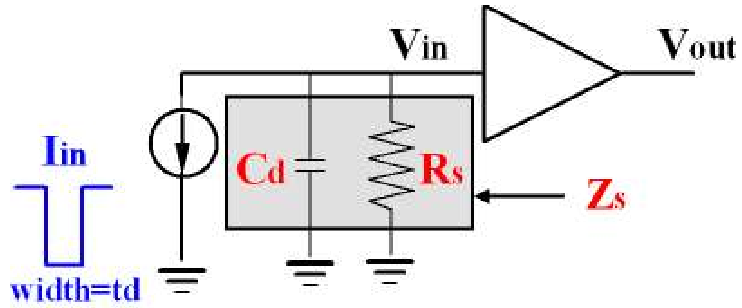




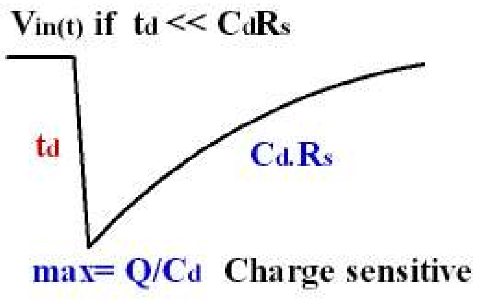
© Harmut Sadrozinski (Santa Cruz) “the beautiful risetime of the detector is spoilt by the electronics”

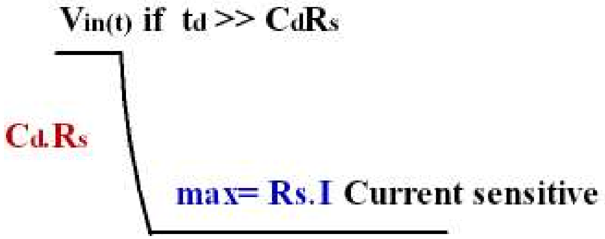
Detector impedance and input voltage

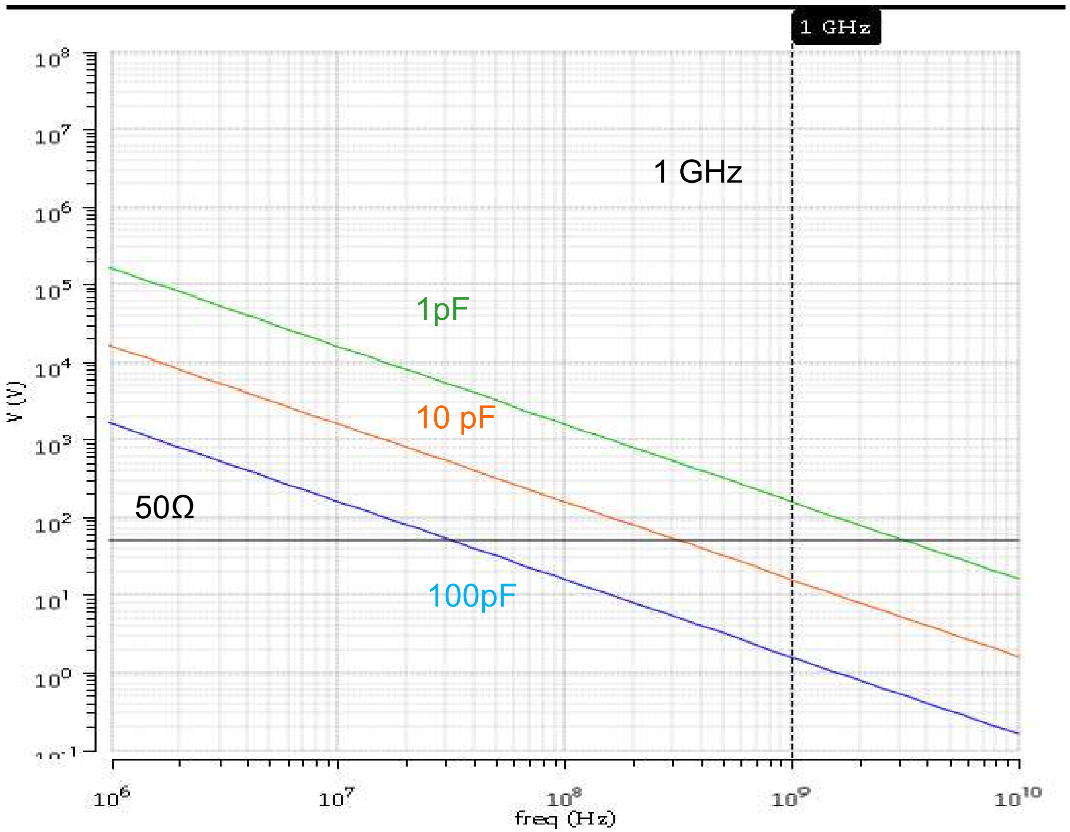
- 1 GHz, Cd=few tens of pF, input signal width <1ns
- Cd>1 pF, Zs@1GHz dominated by Cd
- Rise time: tr= td when td<< $R_S C_d$ and tr= $R_S C_d$ when td>> $R_S C_d$



At HF : difficult to beat the capacitance => signal integrated on Cd

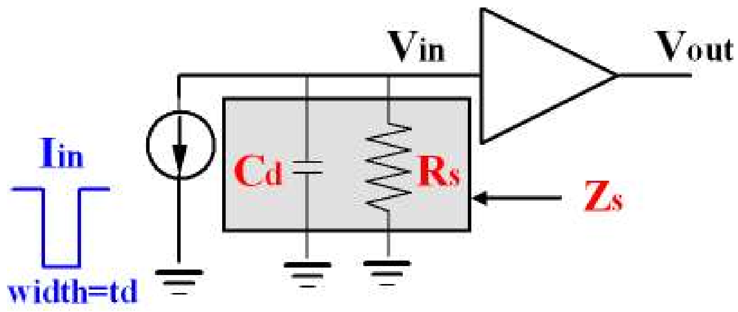


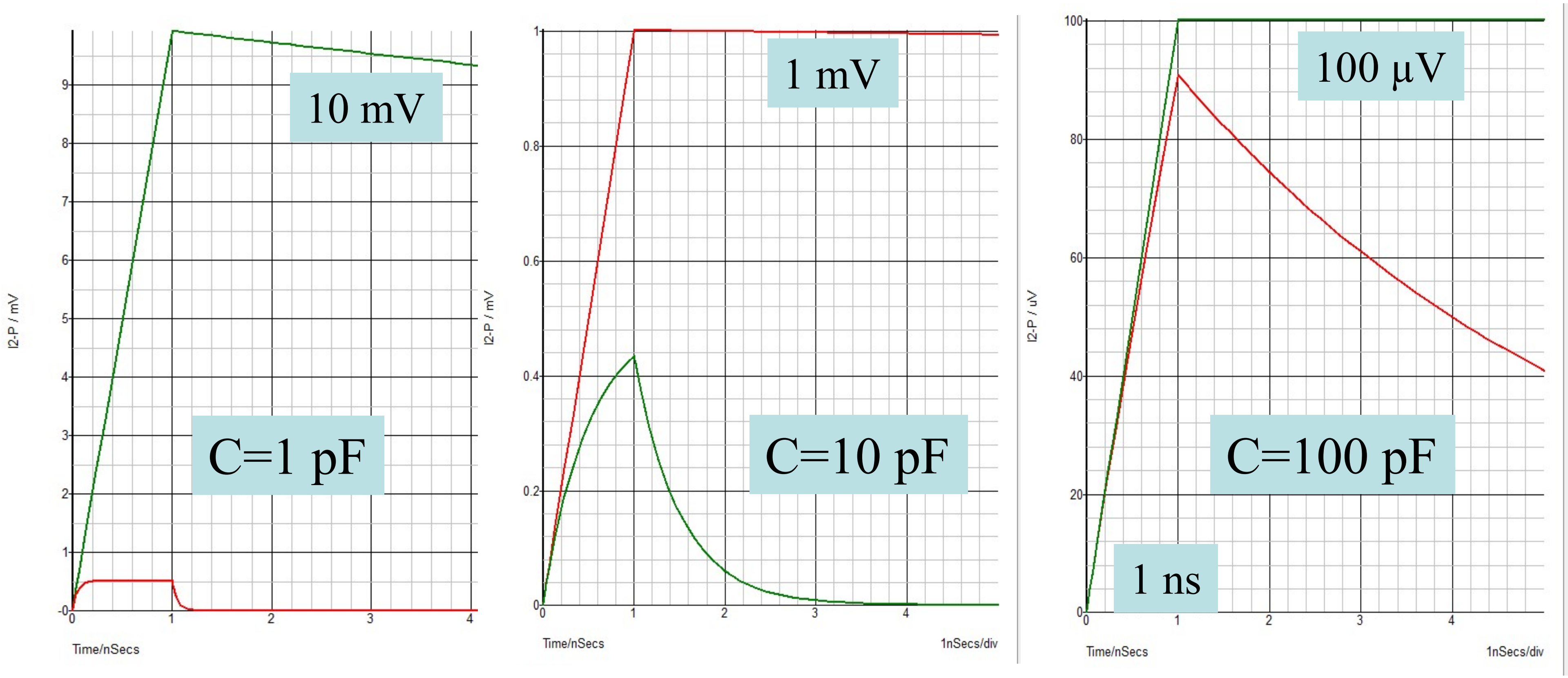




voltage vs current sensitive

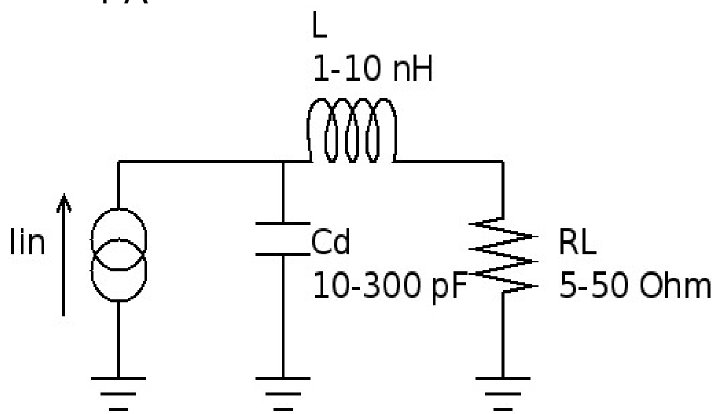
- *Example* : 10 fC – 1 ns signal from 1-10-100 pF sensors into 50 Ω (current) or 50k (voltage) preamp

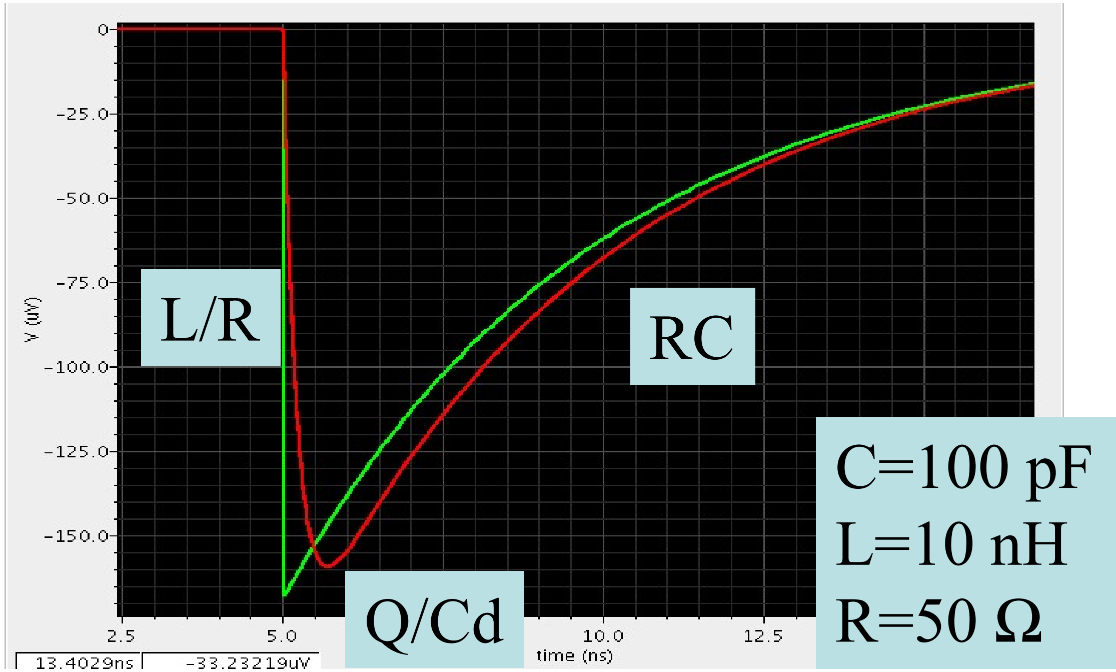


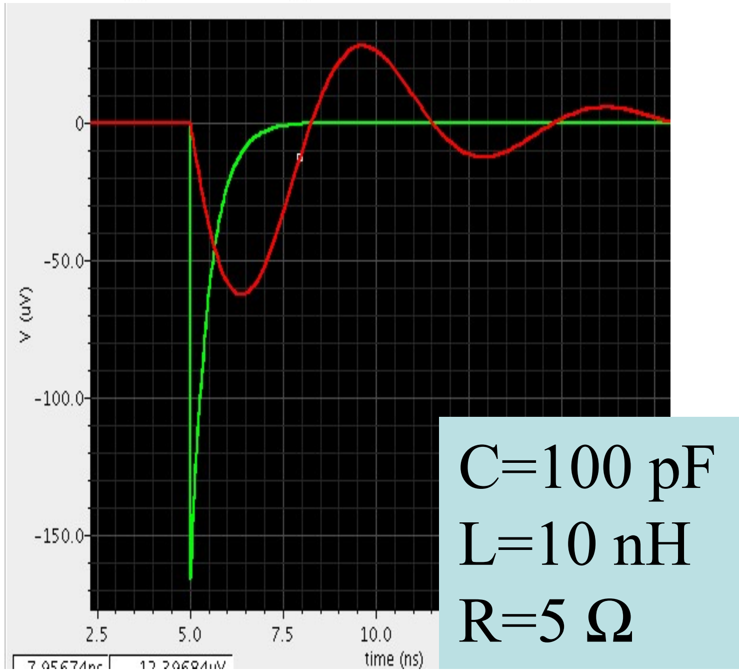


Examples of pulse shapes

- SiPM pulse : Q=160 fC, Cd=100 pF, L=0-10 nH, R_{PA}=5-50 Ω
- Sensitivity to parasitic inductance
- Choice of R_{PA} : decay time, stability
- Small R_{PA} not necessarily the fastest
- Convolve with current shape… (here delta)

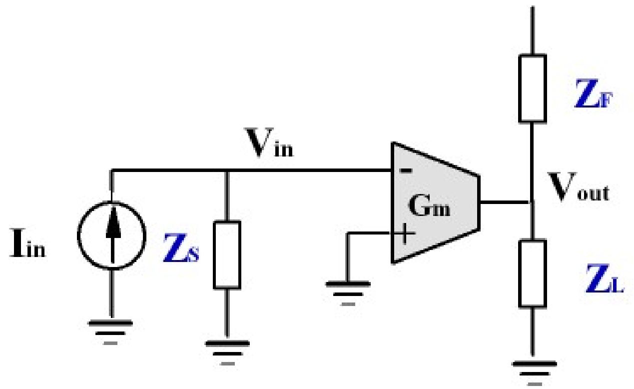




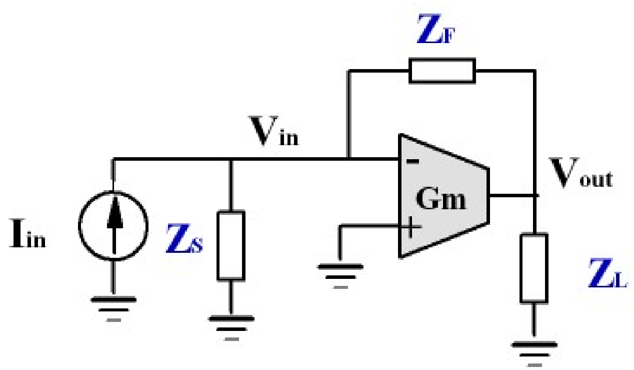


High speed amplifiers

- Response to very short pulse
- Broadband
  - Zin=Rs (50 Ohm)
  - Vin = Q/Cin
  - $V_{OUT} = -G_m R_F \frac{Q_{IN}}{C_d}$



- Transimpedance
  - Zin ~ Zf/G ~ 1/gm
  - $V_{OUT} = \frac{\frac{1}{G_m} - R_F}{1 + j\omega \frac{C_d}{G_m}} I_{IN} \approx -G_m R_F \frac{Q_{IN}}{C_d}$

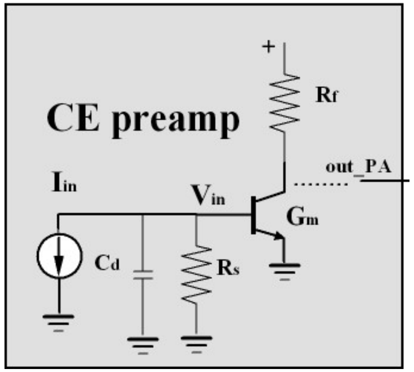


- Same response at High Frequency
- For highest speed : go to broadband. Faster, less stability issues

High speed amplifiers

- Jitter is given by [details in backup] :

$$\sigma_t^J = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$



- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

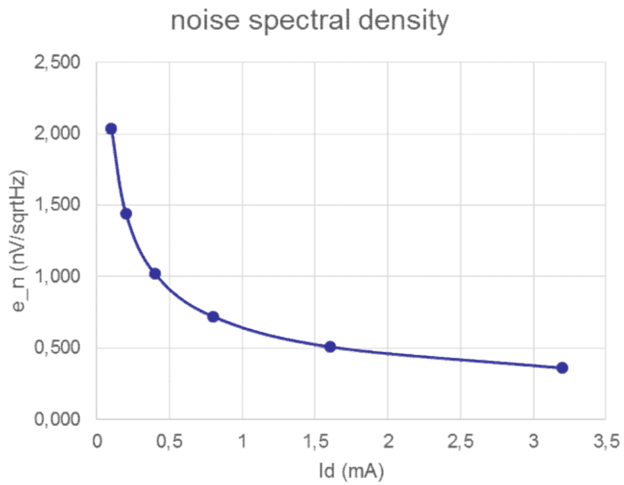
Cd: detector capacitance
$t_{10\_10\_PA}$: rise time of the PA
t_d= drift time of the detector
e_n preamp noise density

Dominated by sensor
Electronics only gives the spectral density of the input transistor e_n

- Gives ps/fC as scales with 1/Qin

- Electronics noise e_n given by the input transistor transconductance g_m:

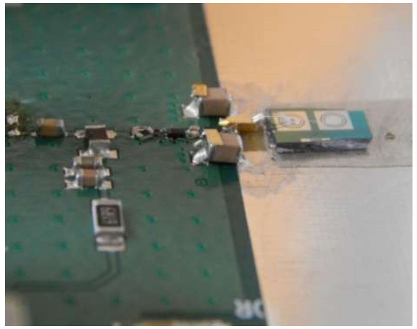
$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$



Examples [measurements from testbeam studies]

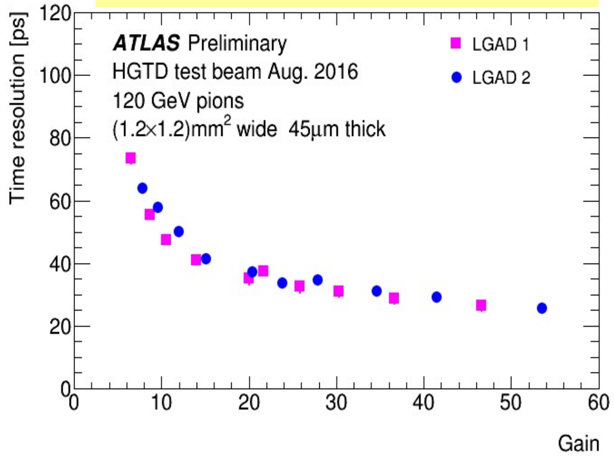
$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

- NA62 tracker : PIN diode thickness 300 µm A=0.09 mm²
  - C_d = 0.1 pF e_n = 11 nV/√Hz t_d = 3 ns σ = 60 ps/Q(fC)
  - 1 MIP = 3 fC => σ = 20 ps/#MIP (~60-200 ps measured)



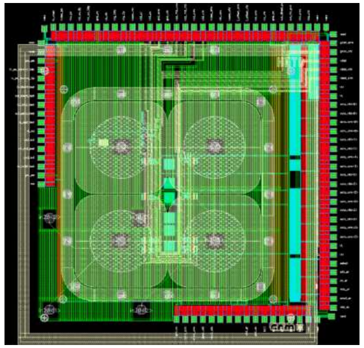
SiGe preamp © N. Spencer (UCSC)

- CMS HGCAL : PIN diode thickness 300 µm A=25 mm²
  - C_d = 8 pF e_n = 1 nV/√Hz t_d = 3 ns σ = 420 ps/Q(fC)
  - 1 MIP = 3.8 fC => σ = 110 ps/#MIP (~200 ps measured)
- ATLAS HGTD : LGAD diode thickness 50 µm A= 2 mm² G = 10
  - C_d = 2 pF e_n = 2 nV/√Hz t_d = 0.5 ns σ = 50 ps/Q(fC)
  - 1 MIP = 5 fC (G=10) => σ = 10 ps/#MIP (~40 ps measured

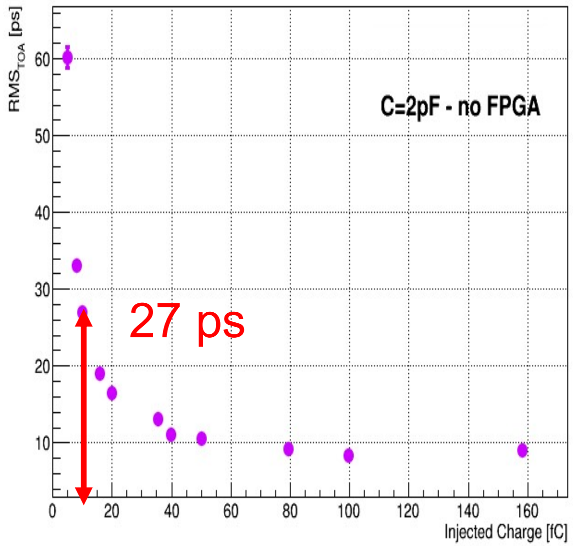


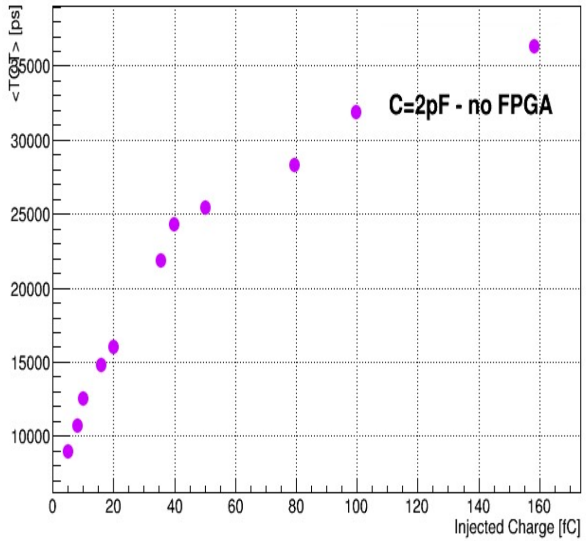
- SiPM G = 1E6
  - C_d = 300 pF e_n = 1 nV/√Hz t_d = 100 ps σ = 3 ns/Q(fC)
  - 1 pe = 160 fC => σ = 20 ps/#pe (~60 ps measured)

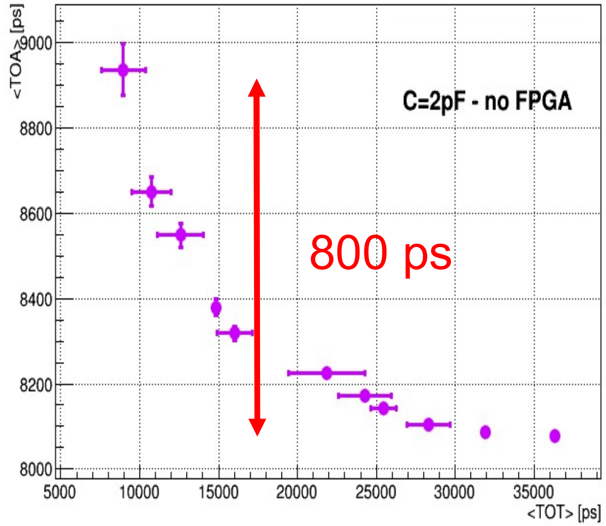
Example : HGTD measurements



- ALTIROC ASIC designed for HGTD (Atlas LGAD Timing Read-Out Chip)
  - Broadband amplifier + high speed discriminator Pd = 1 mW
  - Optimized for 1 mm² 50 µm LGAD (Cd=2 pF)
- TOA and TOT vs injected charge with additionnal Cd= 2 pF
- Preamp and testboard capacitance : ~1.3 pF
- Jitter = 27 ps @ 10 fC
- Time walk = 800 ps

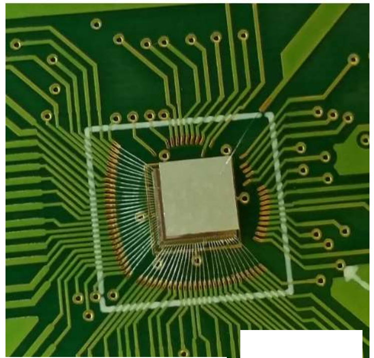




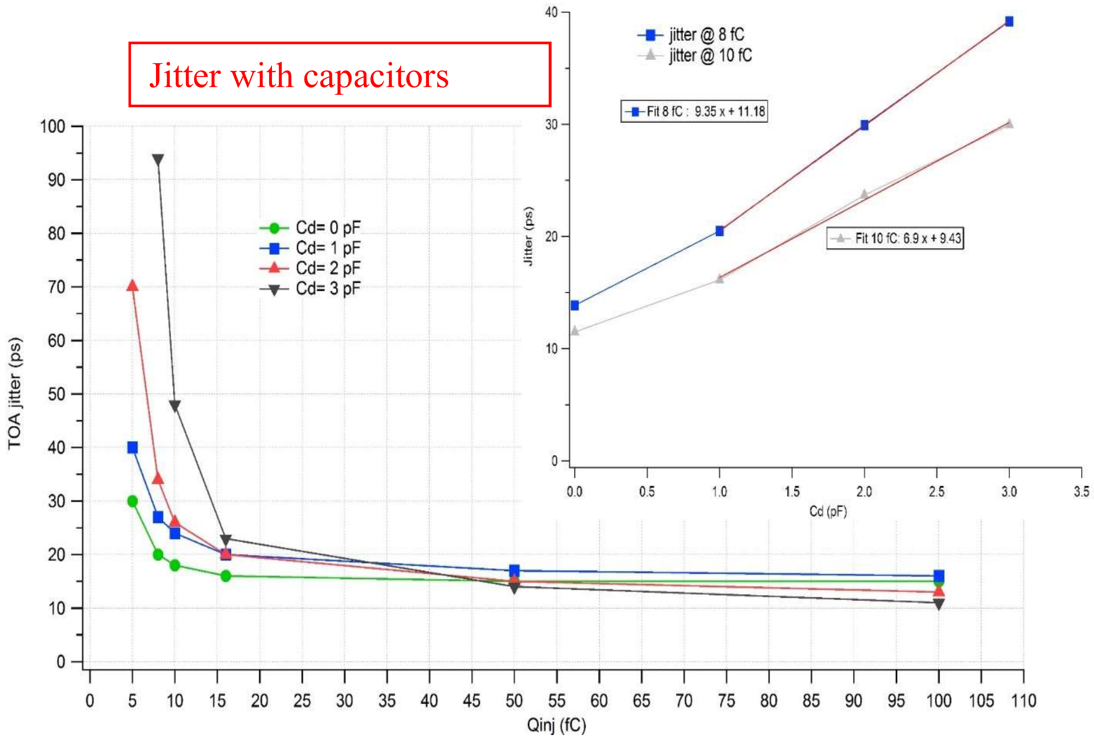


Testpulse injection with sensor

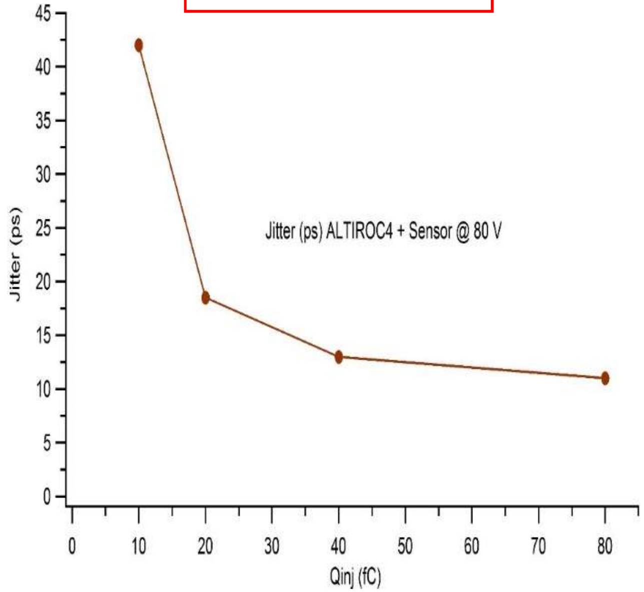
- 1x1 mm² sensors fabricated by CNM/IFAE Barcelona
- Bump-bonded to ALTIROC0 at Barcelona
- Sensor connected, biased at 80 V to have the actual capacitance
- Testpulse injection with Cinj=0.1 pF
- Jitter = 40 ps @ 10 fC
- Corresponds to Cd ~ 3 pF



Jitter with capacitors



Jitter with sensor



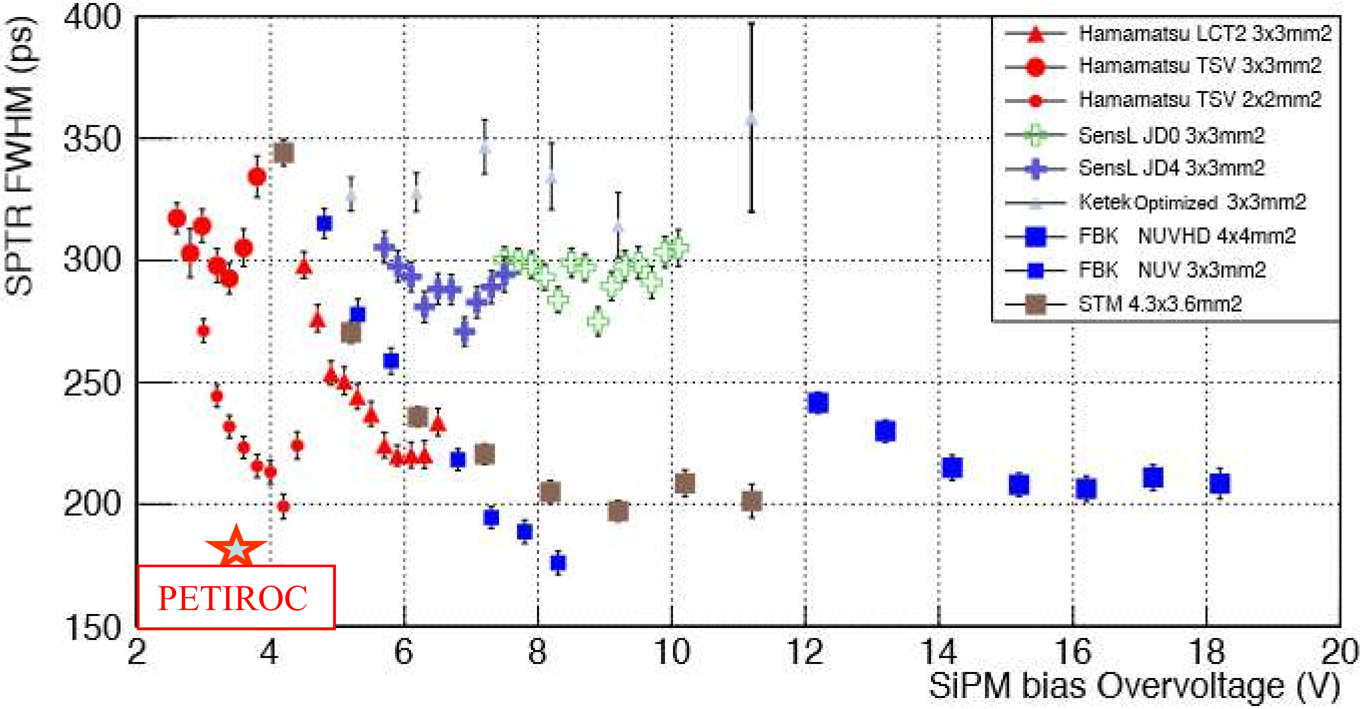
With SiPMs : SPTR [JINST 11 P10016]

- SPTR
  - FWHM ~200 ps
  - Rms ~ 80 ps

Single photon time resolution of state of the art SiPMs

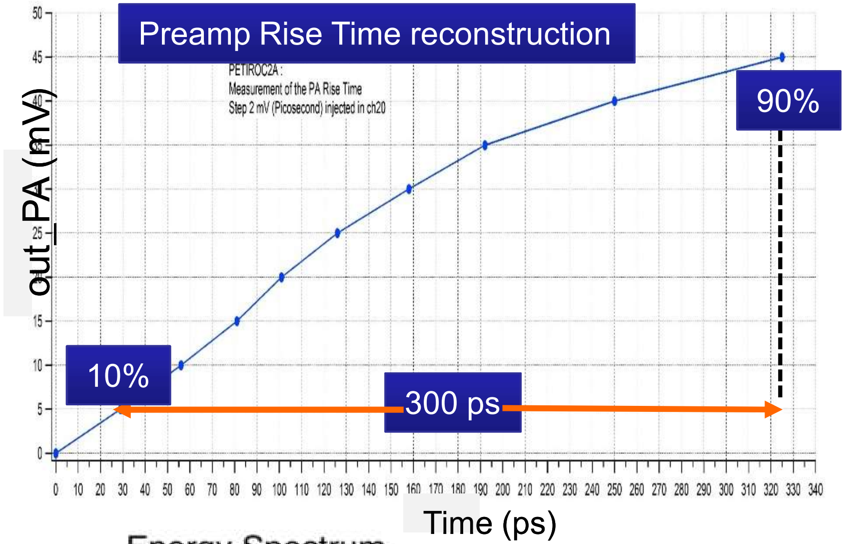
M.V. Nemallapudi,[1] S. Gundacker, P. Lecoq and E. Auffray

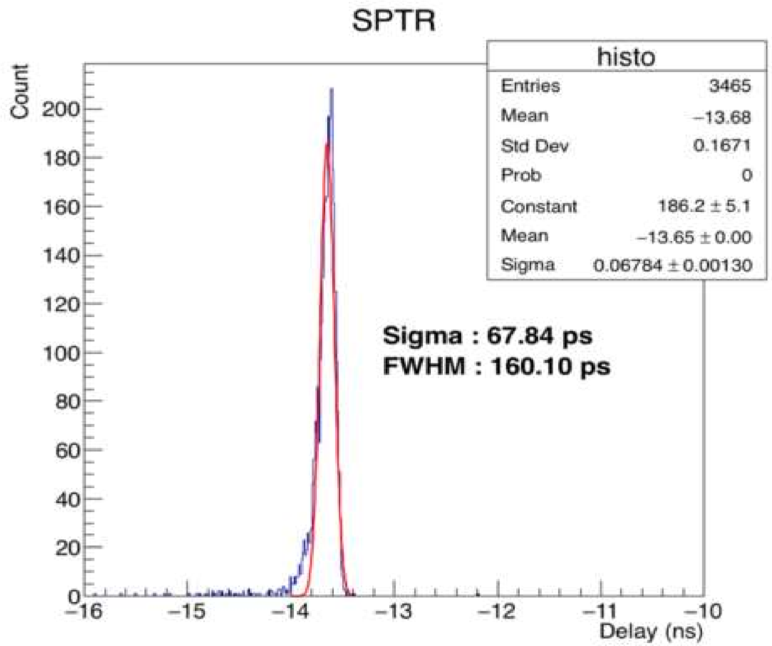
CERN,
23 Rue de Meyrin, Geneva, 1211-CH

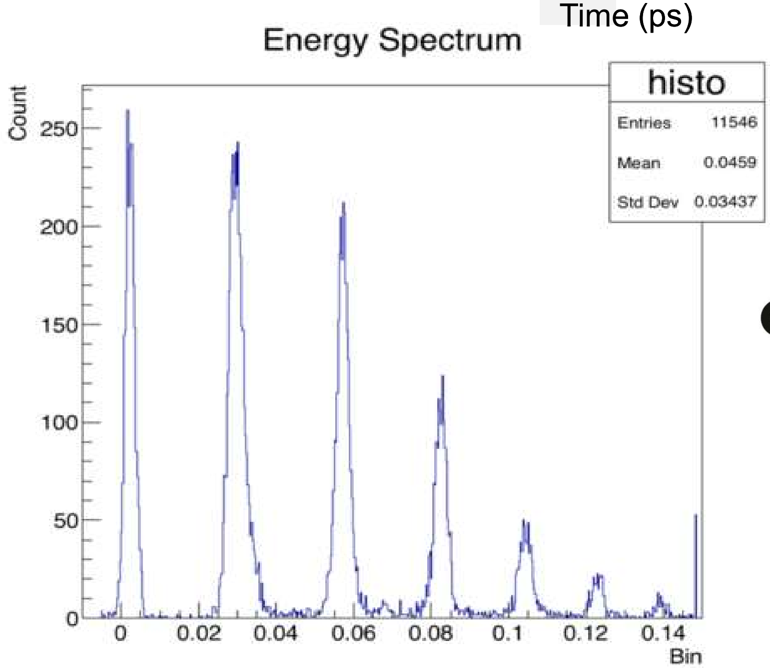


Going to lower SPTR

- Expect ~ 20 ps/pe
- NINO risetime ~1 ns
- Test with PETIROC2 (tr = 300 ps)
  - SPTR = 67 ps rms (180 ps FWHM)
- Possible effect of stray inductance
- Furhter studies in FAST framework







weeroc

© *J. Fleury TIPP17*

Summary

- Imaging calorimeters ramping up !
  - Require highly integrated R/O electronics : System On Chip
  - Low power, low noise, high speed, large dynamic range
  - Timing capability down to a few tens of ps
  - Lots of system issues

- Timing performance dominated by sensor characteristics
  - Capacitance, duration, MIP charge
  - Theory predicts :
  - Electronics affects only $g_m \sim Id/2U_T$

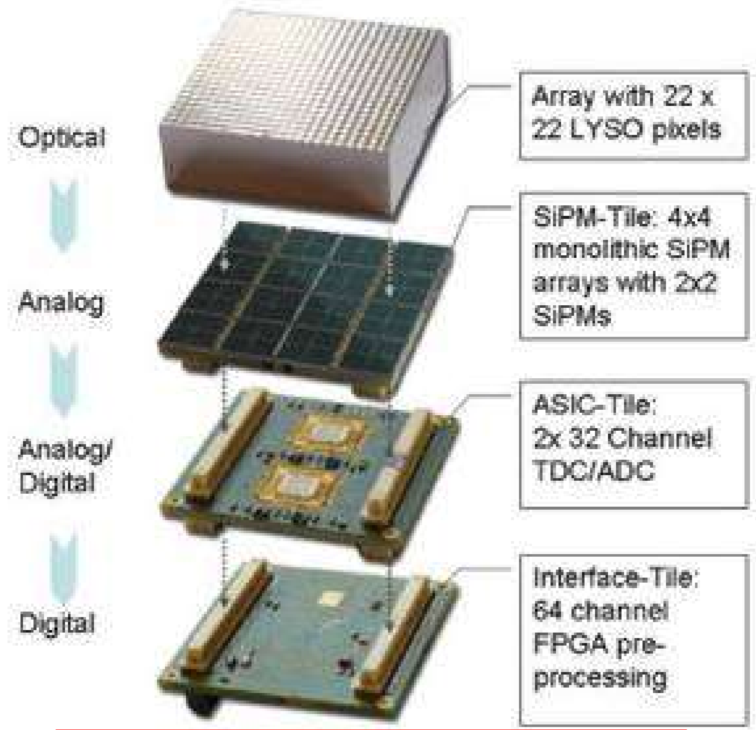
$$\sigma_t^{J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

- Work getting organized towards 10 ps (1 ps ?) timing

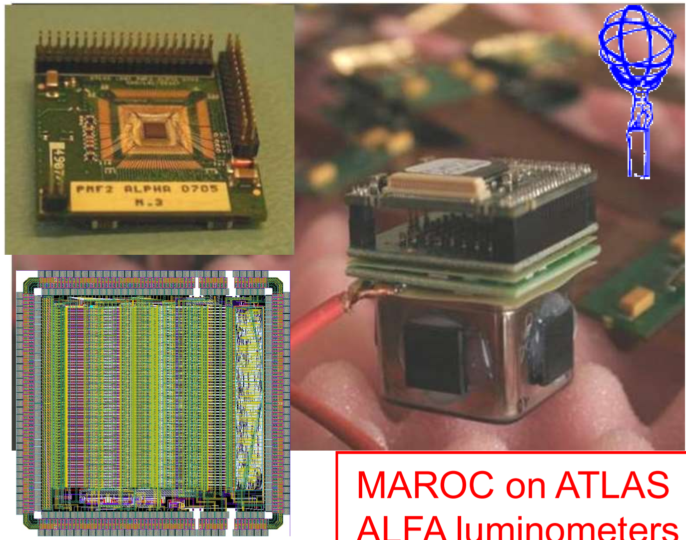
A few (personal) comments

- Strong push for high speed front-end > GHz
  - Essential for timing measurements
  - Several configurations to get GBW > 10 GHz
  - Optimum use of SiGe bipolar transiistors
- Voltage sensitive front-end
  - Easiest : 50Ω termination, many commercial amplifiers (mini circuit…)
  - Beware of power dissipation
  - Easy multi-gain (time and charge)
- Current sensitive front-end
  - Potentially lower noise, lower input impdance
  - Largest GBW product
- In all cases, importance of reducing stray inductance

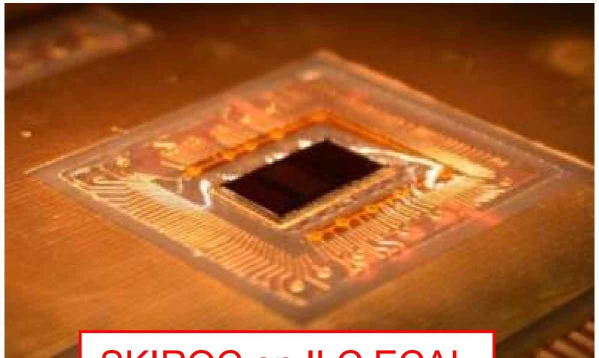
Electronics moves onto detectors



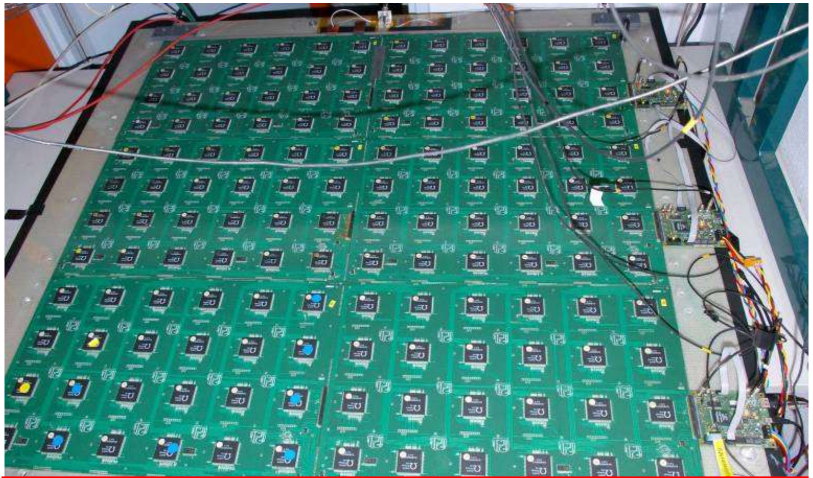
PET hyperimage project [P. Fisher]



MAROC on ATLAS ALFA luminometers



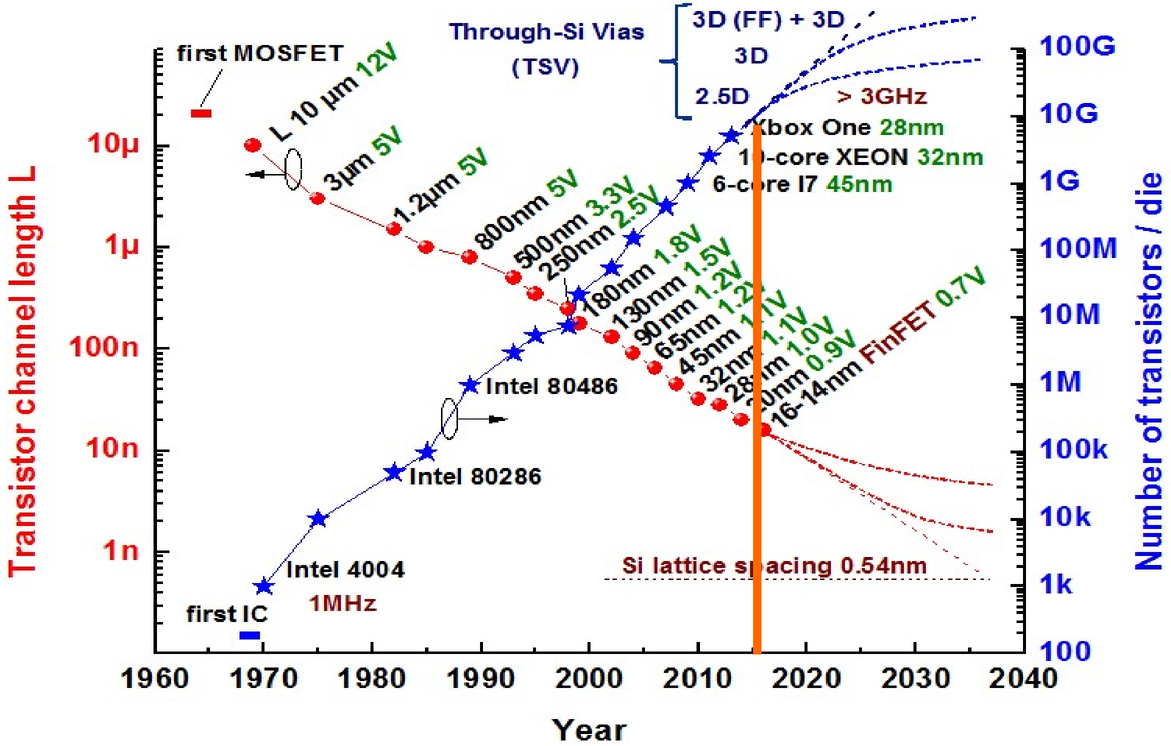
SKIROC on ILC ECAL



1m² RPC detector for ILC DHCAL [I. Laktineh]

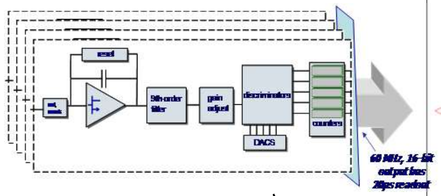
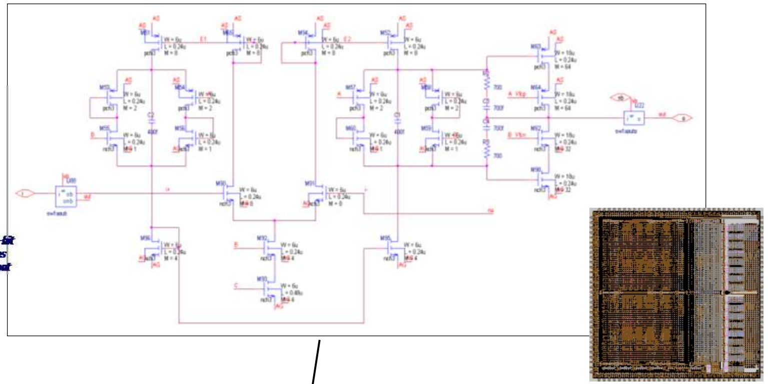
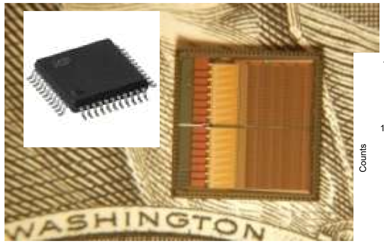
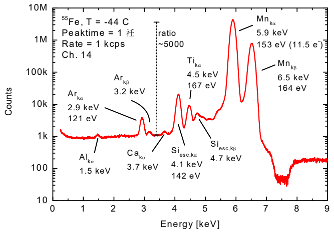
Evolution of technologies

- Performant design is at transistor level
- More and more functions are integrated inside chips (ASICs)
- Evolution of technologies make them more and more performant but more and more complex
- Cost increases …
  - MPW costs :
  - 350 nm : 1 k€/mm²
  - 130 nm : 2 k€/mm²
  - 65 nm : 6 k€/mm²
- Chip size also…
- PP a few M$/400G$



10 ans d'évolution des spécifications techniques pour la réalisation d' ASIC

ASIC Design Flow [V. Radeka BNL]

design phase	system level design	transistor level design	masks layout	fabrication	tests
months	~ 2	~ 6	~ 2	~ 3	~ 2

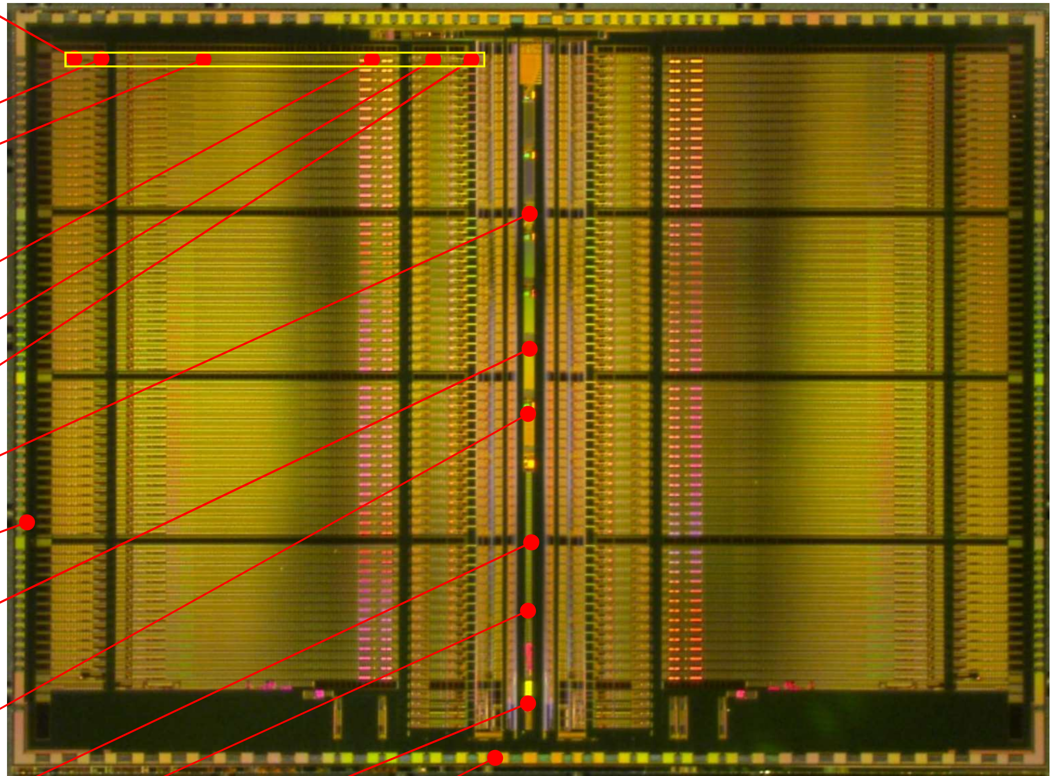
revision cycle

From concept to ready-for-production:
1 - 2 cycles, 2 - 3 years, 3-6 FTE (depending on complexity)

Higher functionality and complexity means more resources and expertise , higher risk, longer development time

Subcircuits

- Low-noise, low-power **charge amplifiers**
  - gas, liquid, solid state detectors
  - capacitances from 10^{-14} to 10^{-8} F
- Switched and continuous **adaptive reset**
- **High-order filters**, stabilizers, drivers
  - peak time / gain adjustment
- Single- and multi-level **discriminators**
- **Peak and time detectors**, derandomizers
- **Analog memories and multiplexers**
- **Counters** and digital memories
- Configuration registers
- **ESD protections**
- **Calibration pulse generators**
- **Analog-to-digital** converters
- **Digital-to-analog** converters
- Precision **band-gap references**
- **Temperature sensors**
- Readout control logic
- Low-voltage **differential signaling**
- **Current-mode** analog and digital interface

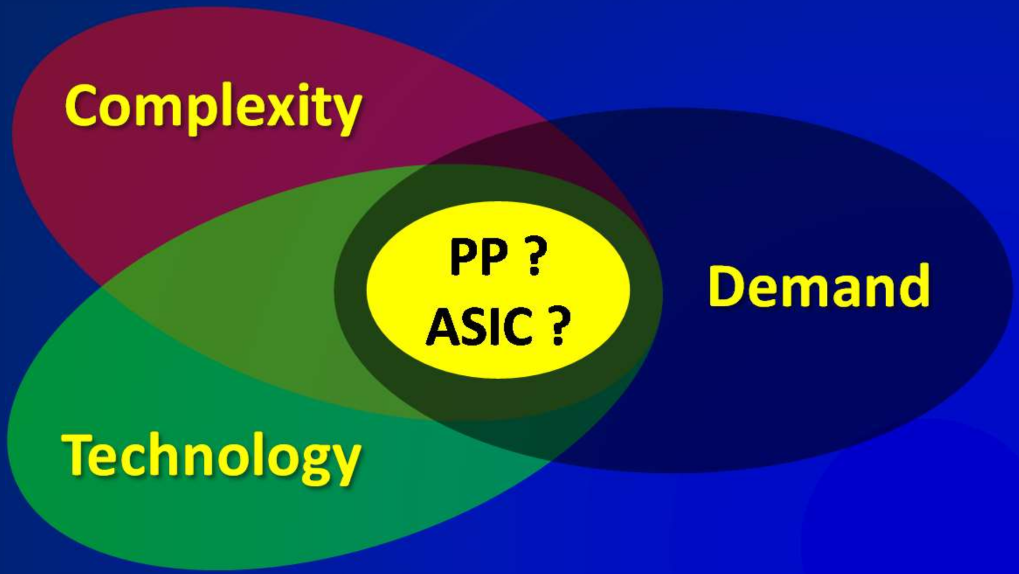


ASIC for 3D CZT 3D CZT Position Sensitive Detectors

- **128 channels**
- **2 mW/channel**
- **13 x 10 mm²**
- **300,000 transistors**
- **CMOS 250 nm**

Functionality and complexity increase by the years

The PP-ASIC Paradigm



Collaborations ?

- only part of the solution
- communication
- overhead
- lead of large group

The number of ASIC designers has to increase !

involve non-PP ASIC groups

<u>increase size of PP ASIC groups</u>

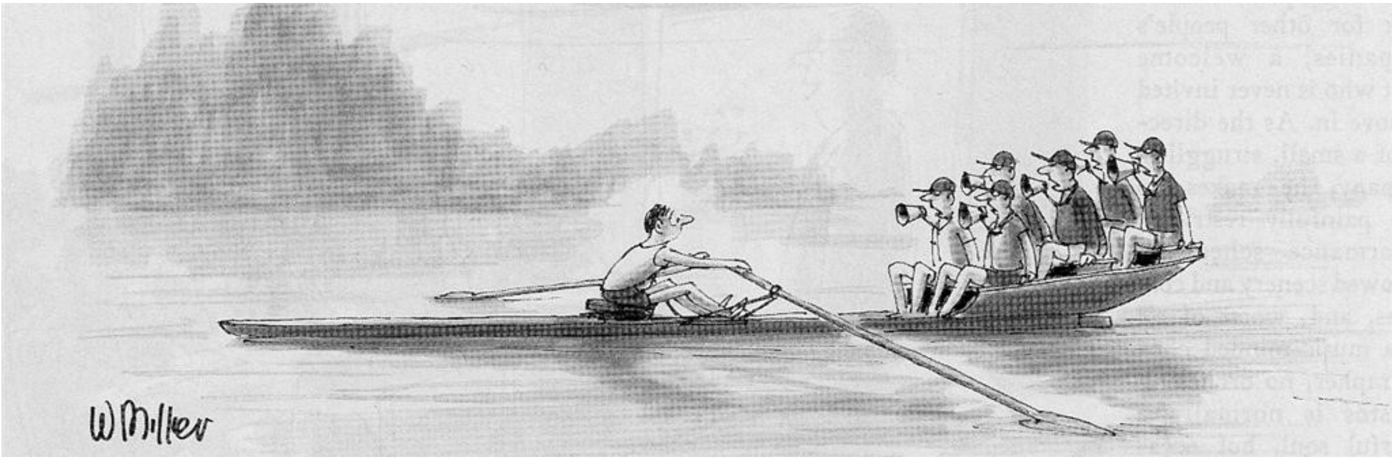
A note on ASICs in detectors:

ASIC developments are complex and require concentration of expertise and resources. For an ASIC to be successful, adequate infrastructure and collaboration on integral design of detectors and signal processing electronics is critical.

•

Microelectronics design teams

- Importance of team building



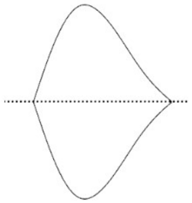
Conclusion

- enjoy designing electronics for future detectors !
- Profit from the nice location to foster collaborations
- 谢谢大家倾听我的报告

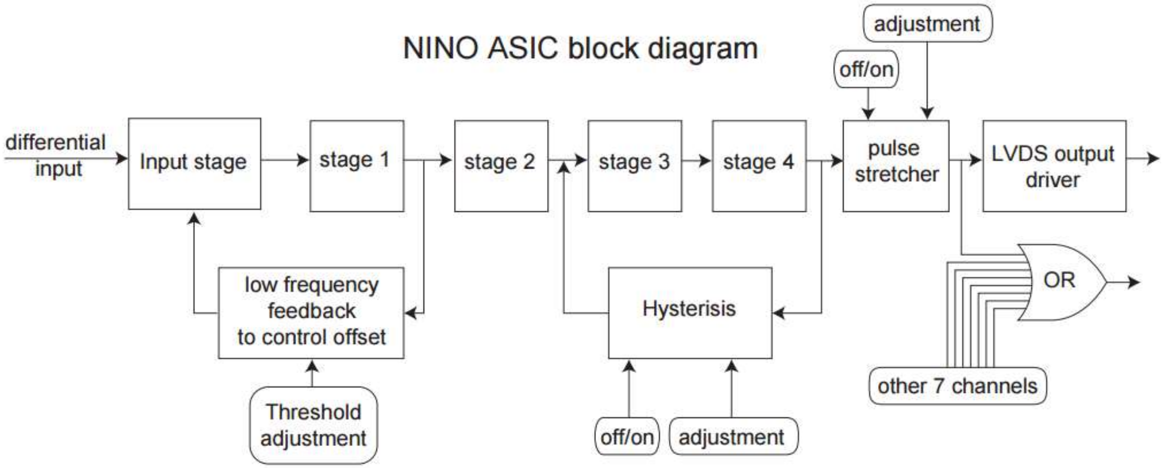
backup

NINO architecture

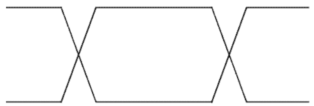
- Current conveyor and discriminator
- Time over threshold for time walk correction

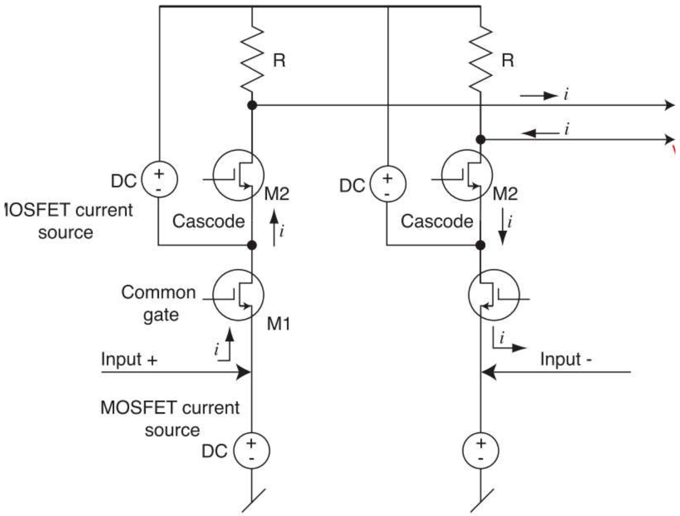


Diff. signal

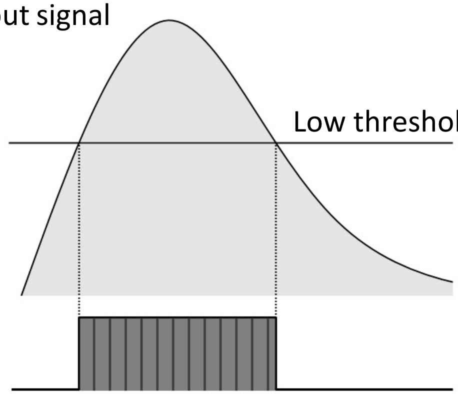


LVDS



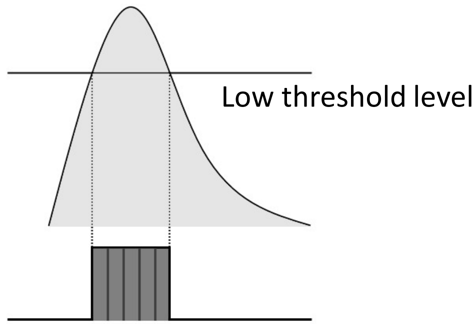


Input signal



Time-Over-Threshold

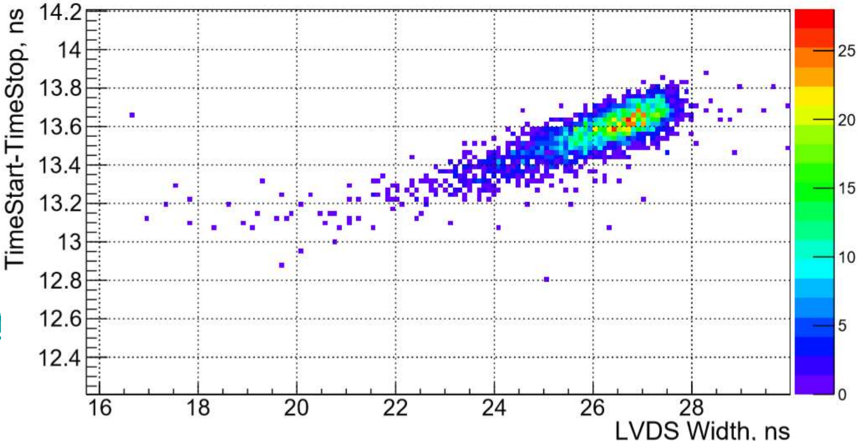
Input signal



Time-Over-Threshold

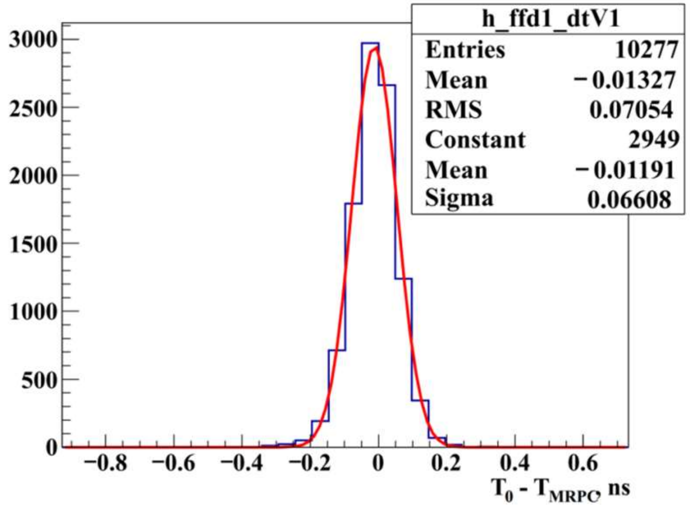
performance

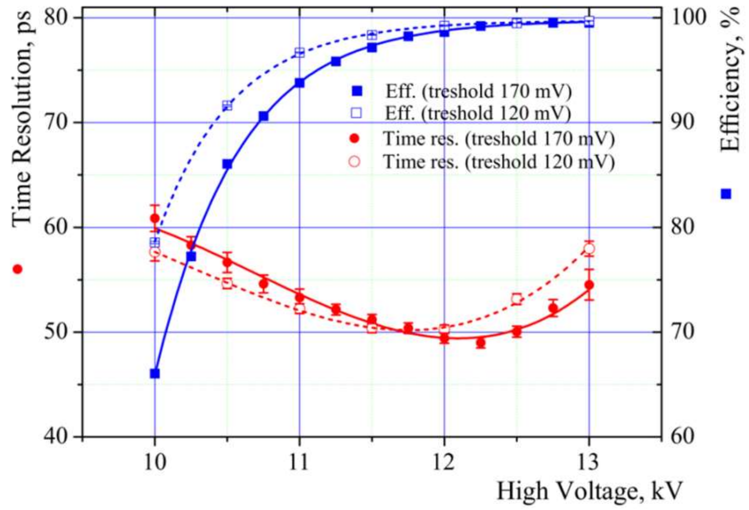
- 60 ps jitter on detector
- Evolving to SUPER-NINO
  - Lower input impedance (5 ohm)
  - Targetting SiPM readout
  - Coupled to pico-TDC
  - https://indico.cern.ch/event/609917/contributio ernino-status.pdf



Time-width distribution without correction.

Distribution of the LVDS widths.



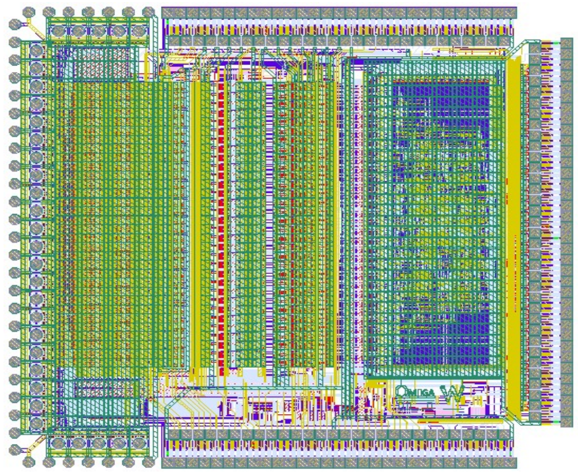


Distribution of the LVDS widths.

PETIROC2 DESCRIPTION

- Time of Flight read-out chip with embedded TDC (25 ps bin) and ADC
- Dynamic range: 160 fC up to 400 pC
- 32 channels (negative input)
  - 32 trigger outputs
  - NOR32_chrage
  - NOR32 time
  - Charge measurement over 10 bits
  - Time measurement over 10 bits
  - One multiplexed charge output
- Common trigger threshold adjustment and 6bit-dac/channel for individual adjustment
- Variable shaping time of the charge shaper
- 32 8bit-input dac for SiPM HV adjustment
- Power consumption 6 mW/ch
- Front-end
  - Broad Band SiGe fast amplifier
  - Fast SiGe discriminator
  - 1 GHz overall bandwidth, gain = 25

AMS 0,35µm SiGe



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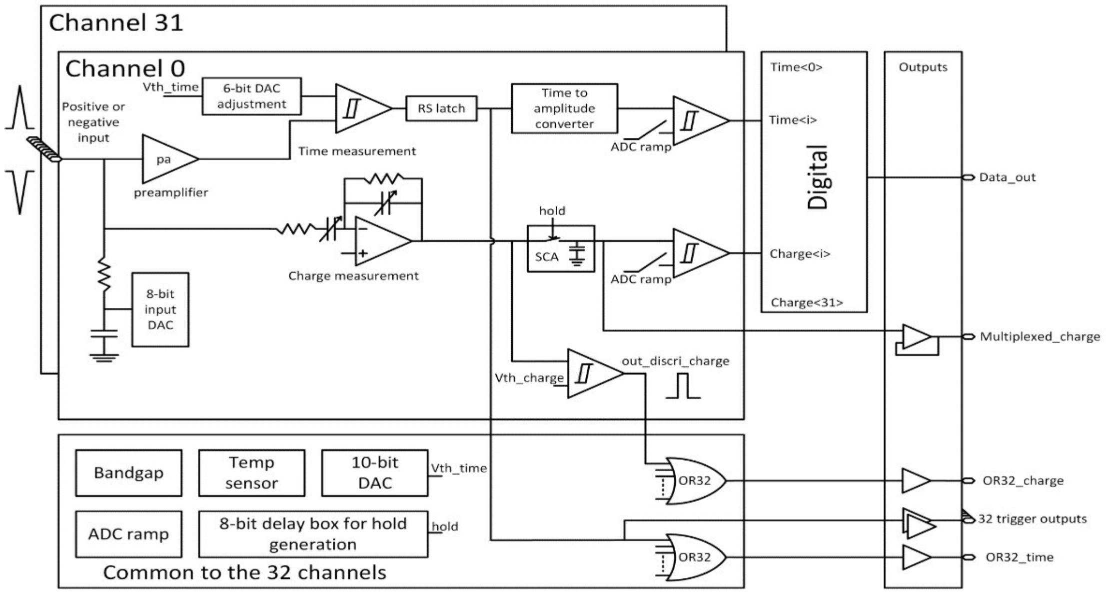

PETIROC2A: performance