CMOS Monolithic Active Pixel Sensors (MAPS)
CMOS Pixel Sensors (CPS)

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- *General introduction – Vertex detector*
- *Introduction of hybrid pixels & CCD*
- *MAPS HR, HV, Twin-well, Quadruple-well*
- *Examples of Pixel Sensor Architectures*
  - *Twin-well circuits*
  - *Quadruple-well circuits*
  - *Towards More Demanding applications ?*
  - *CPS R&D for e+ e- Colliders*

Monolithic Active Pixel Sensors: A Long Term R&D

Ultimate objective: ILC, with staged performances

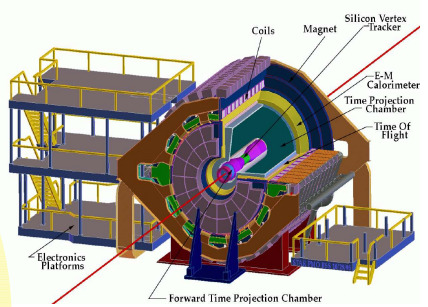
MAPS applied to other experiments with intermediate requirements

EUDET 2006/2010

Beam Telescope

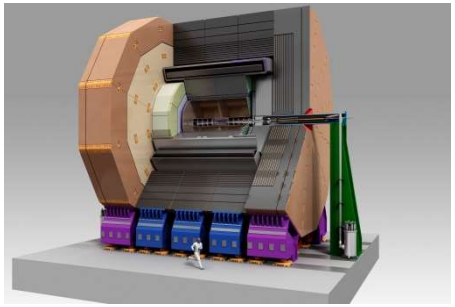
STAR 2013

Solenoidal Tracker at RHIC



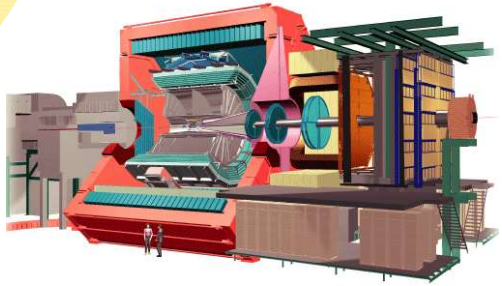
ILC >2025

International Linear Collider



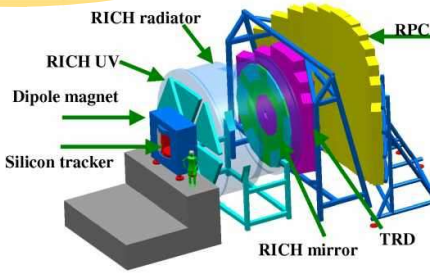
ALICE 2018

A Large Ion Collider Experiment



CBM >2020

Compressed Baryonic Matter



Monolithic Active Pixel Sensors: A Long Term R&D

Ultimate objective: ILC, with staged performances

MAPS applied to other experiments with intermediate requirements

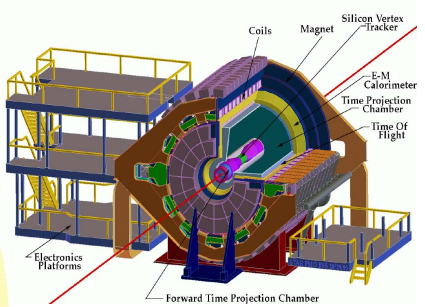
EUDET 2006/2010

Beam Telescope

- ✓ EUDET (R&D for ILC, EU project)
- ✓ STAR (Heavy Ion physics)
- ✓ HadronPhysics2 (generic R&D, EU project)
- ✓ AIDA (generic R&D, EU project)
- ✓ FIRST (Hadron therapy)
- ALICE/LHC (Heavy Ion physics)
- CBM (Heavy Ion physics)
- ATLAS ITK (Particle physics)
- LHCb Tk (Particle physics)
- ILC (Particle physics)
- EIC (Hadron physics)
- CLIC (Particle physics)
- CEPC (Particle physics)
- …

STAR 2013

Solenoidal Tracker at RHIC



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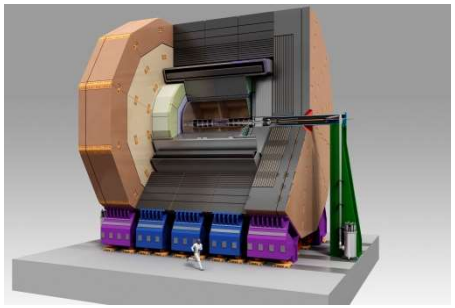

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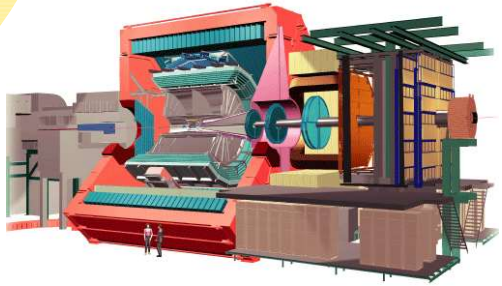

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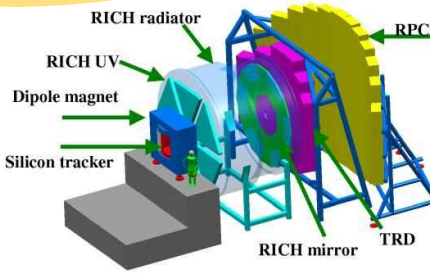
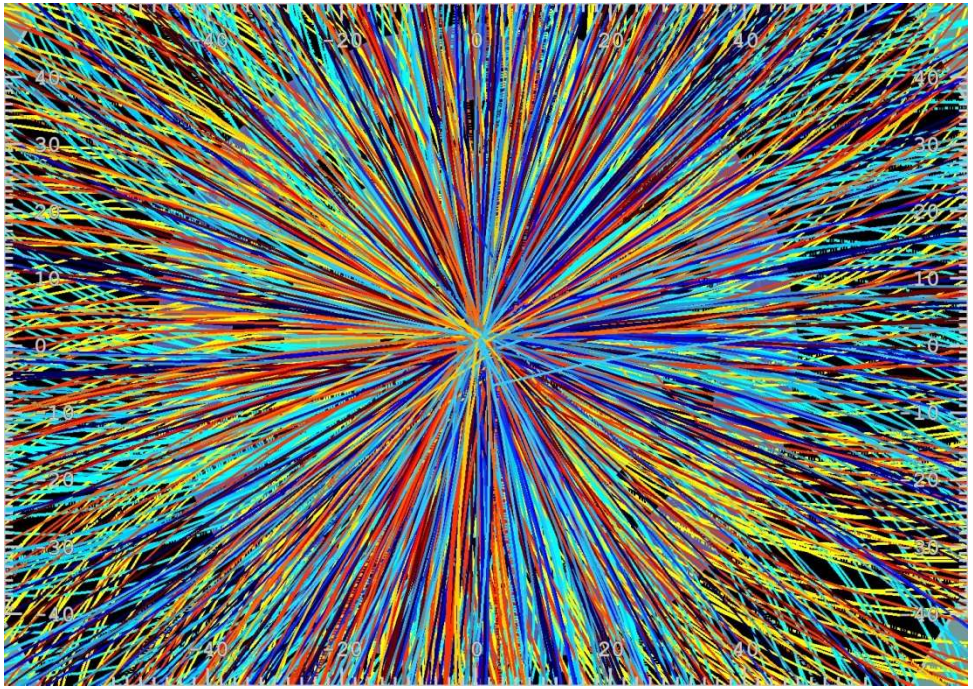


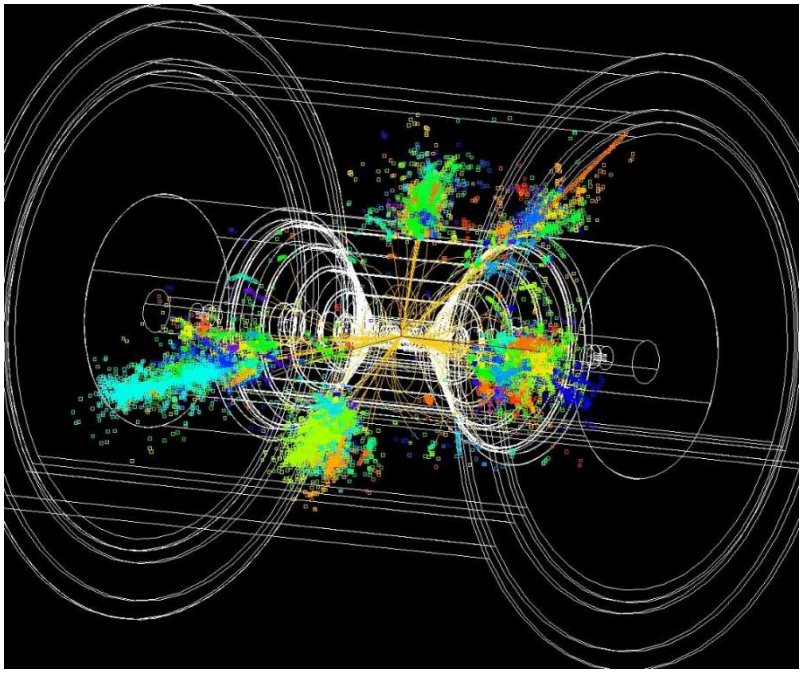
Nowdays …



How do we see the collisions?

- We need highly granular detectors that take pictures quickly, and manipulate the resulting data on board and store it before shipping to a farm of computers

Nowdays …



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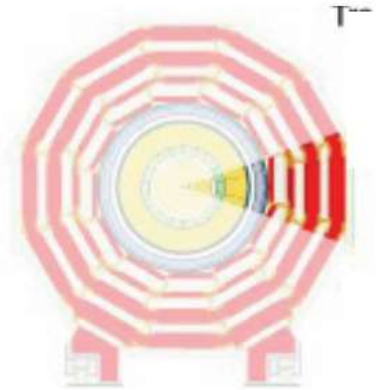
Particle Physics Detector Overview

Tracker: Precise measurement of track and momentum of charged particles due to magnetic field.

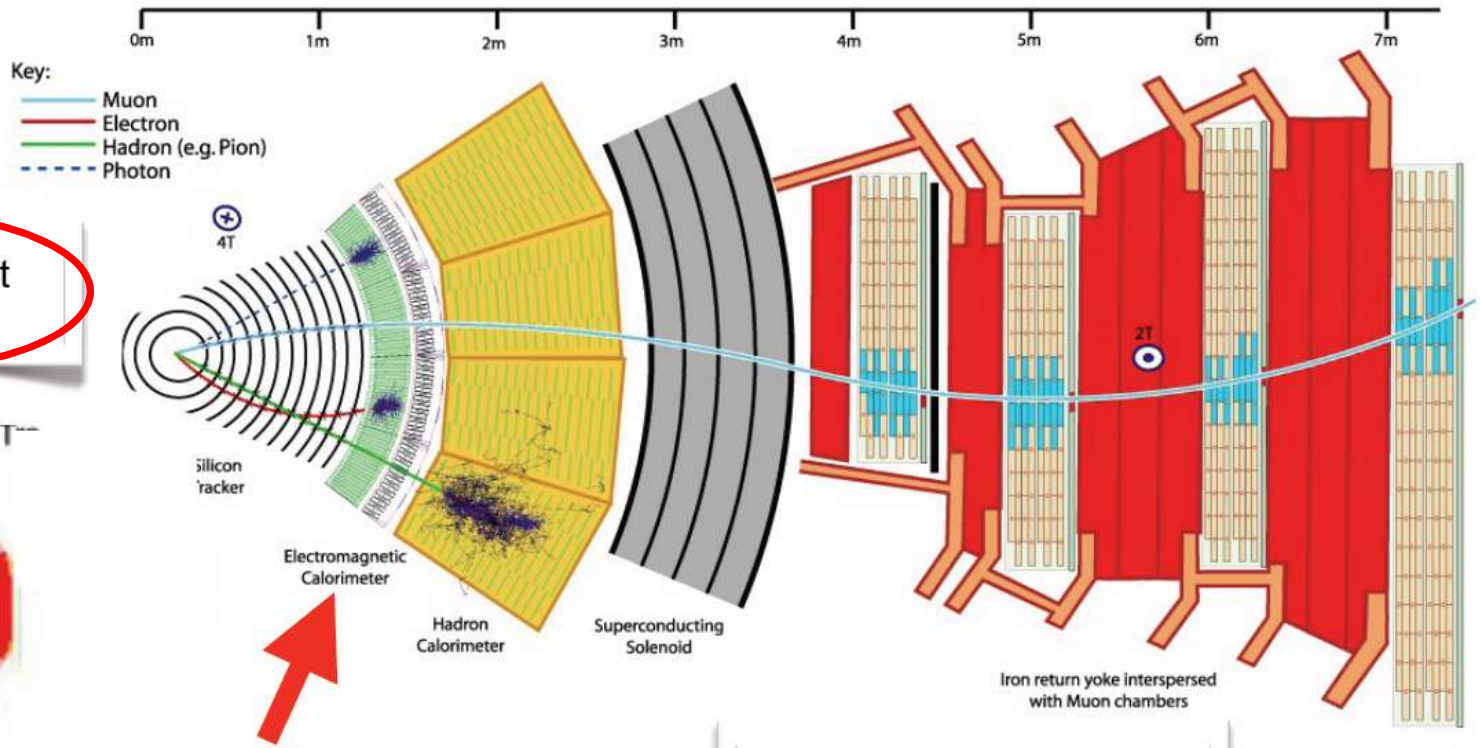
Calorimeter: Energy measurement of photons, electrons and hadrons through total absorption

Muon-Detectors: Identification and precise momentum measurement of muons outside of the magnet

Vertex: Innermost tracking detector



Transverse slice through CMS



picture: CMS@CERN

Good energy resolution up to highest energies

Radiation hard (hadron collider)

Vertex Detectors

- Figure of merit for the VXD: Impact Parameter Resolution

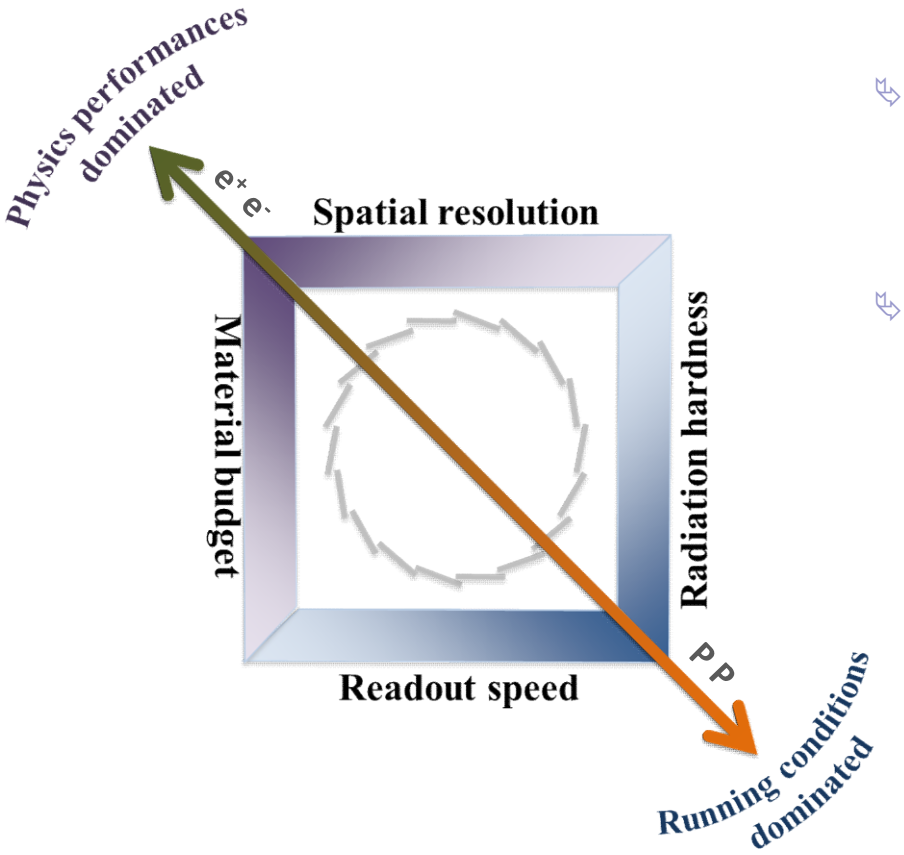
$$\sigma_{ip} = \boldsymbol{a} \oplus \frac{\boldsymbol{b}}{\boldsymbol{p}(GeV)sin^{3/2}\theta} \ (\mu m)$$

  - **a** depends on the single point resolution of the sensor and the lever arm, which is equal to R_{ext} - R_{int}
  - **b** depends on the distance of the innermost layer to IP and the material budget
  - **P** and θ are the particle momentum and polar angle

Accelerator	a (µm)	b (µm.GeV/c)
LEP	25	70
Tevatron	10	40
LHC	<12	<70
RHIC-II	12	19
ILC/CLIC	**<5**	**<10**

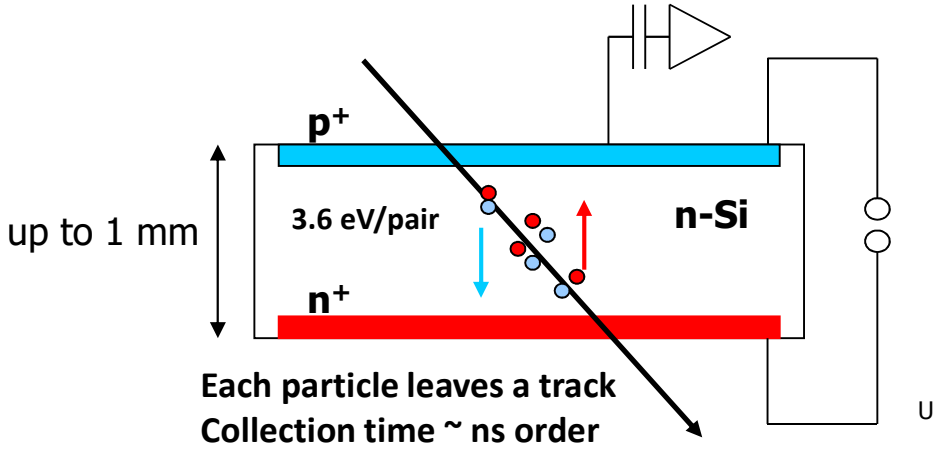
The Challenges of a Vertex Detector

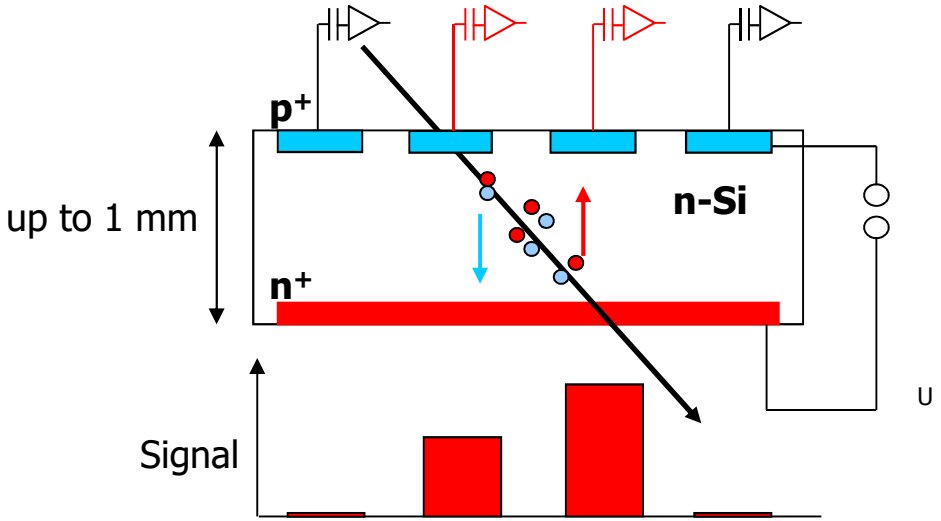
- Precision (resolution)
- Material budget
- Readout speed
- Radiation hardness
- + Power consumption



- **Conflict** between physics performance driven parameters and running condition constraints:
  - Physics performance: spatial resolution (small pixel) and material budget (thin sensors) + distance to IR
  - Running conditions: read-out speed and radiation tolerance (HL-LHC: 10 times LHC)
  - Moreover:
    - ⋆ limitations from maximum power dissipation compatible
    - ⋆ limitations from highest data flow acceptable by DAQ
  - Ultimate performance on all specifications cannot be reached simultaneously
    - ⋆ There is no single technology best suited to all applications
    - ⋆ Motivation for continuous R&D (optimum is stronly time dependent)

Particle Tracking in Si



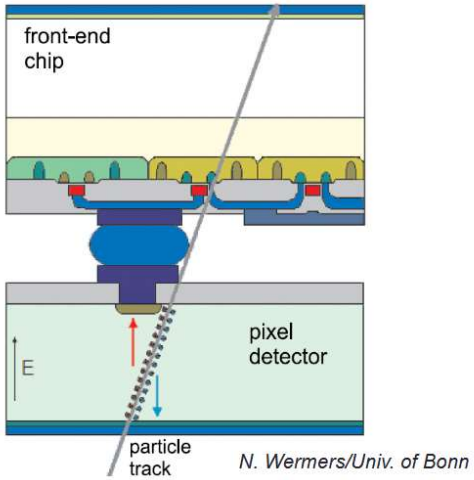


- The generated charge Q is given by:
  $Q = Sub_{th} * x$
  - sub_{th} is the substrate thickness
  - x is a continuous random variable distributed according to the Landau distribution with MPV = e-h/µm

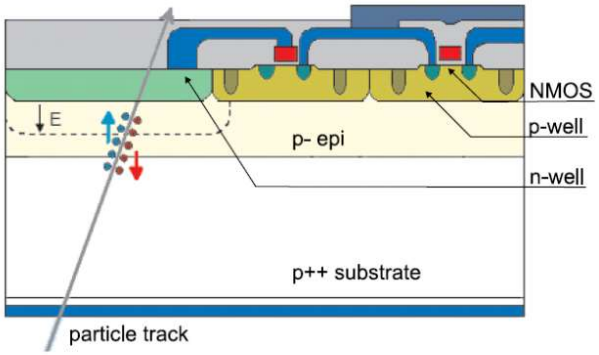
Position can be determined → centre of gravity

To obtain good position resolution → high S/N ratio

Pixel Detectors: Hybrid versus Monolithic



N. Wermers/Univ. of Bonn



Hybrid

- Used in large majority of installed systems
- 100% fill factor easily obtained
- Sensor and readout circuit can be optimized separately
  - Other materials for the sensor
  - Standard ASIC CMOS (often denser than imaging processes)

Monolithic

- Easier integration, lower cost
- Promising not only for pixels but also for trackers
- Potentially a significant impact on the material budget
- MAPS are installed in STAR and adopted for the upgrade of the ALICE ITS

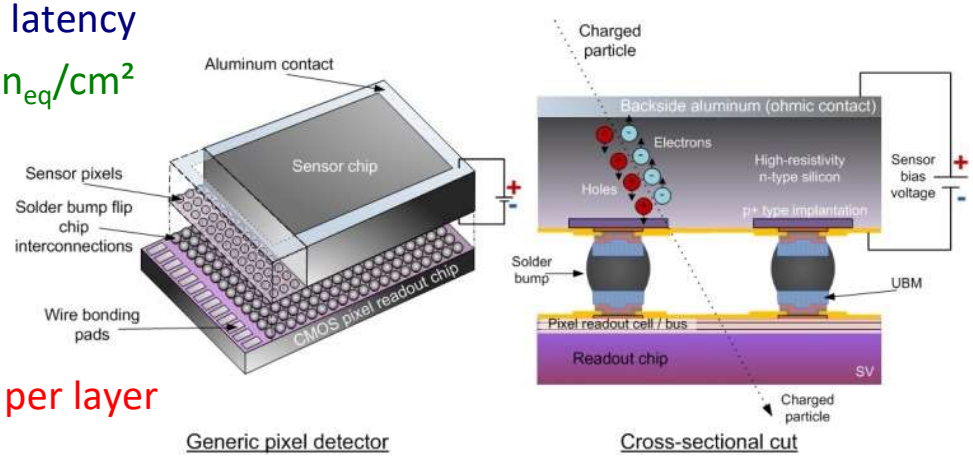
- *New technologies (Through-Silicon-Vias, microbumping, etc.) make that the distinction is more vague*
- *Stacked CMOS imagers are available in the industry but often not with an individual connection for each pixel*

https://www-group.slac.stanford.edu/ais/publicDocs/presentation127.pdf

https://indico.cern.ch/event/452781/contributions/2297515/attachments/1346032/2030268/Re_Vertex_2016.pdf

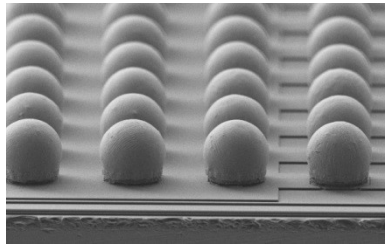
Hybrid Pixels

- Offer a number of advantages due to the split functionality of sensor and readout:
  - Complex signal processing in readout chip
  - Zero suppression and hit storage during L1 latency
  - Radiation hard chips and sensors to > 10^{15} n_{eq}/cm^2
  - High rate capability (~MHz/mm2)
  - Spatial resolution ≈ 10-15 µm



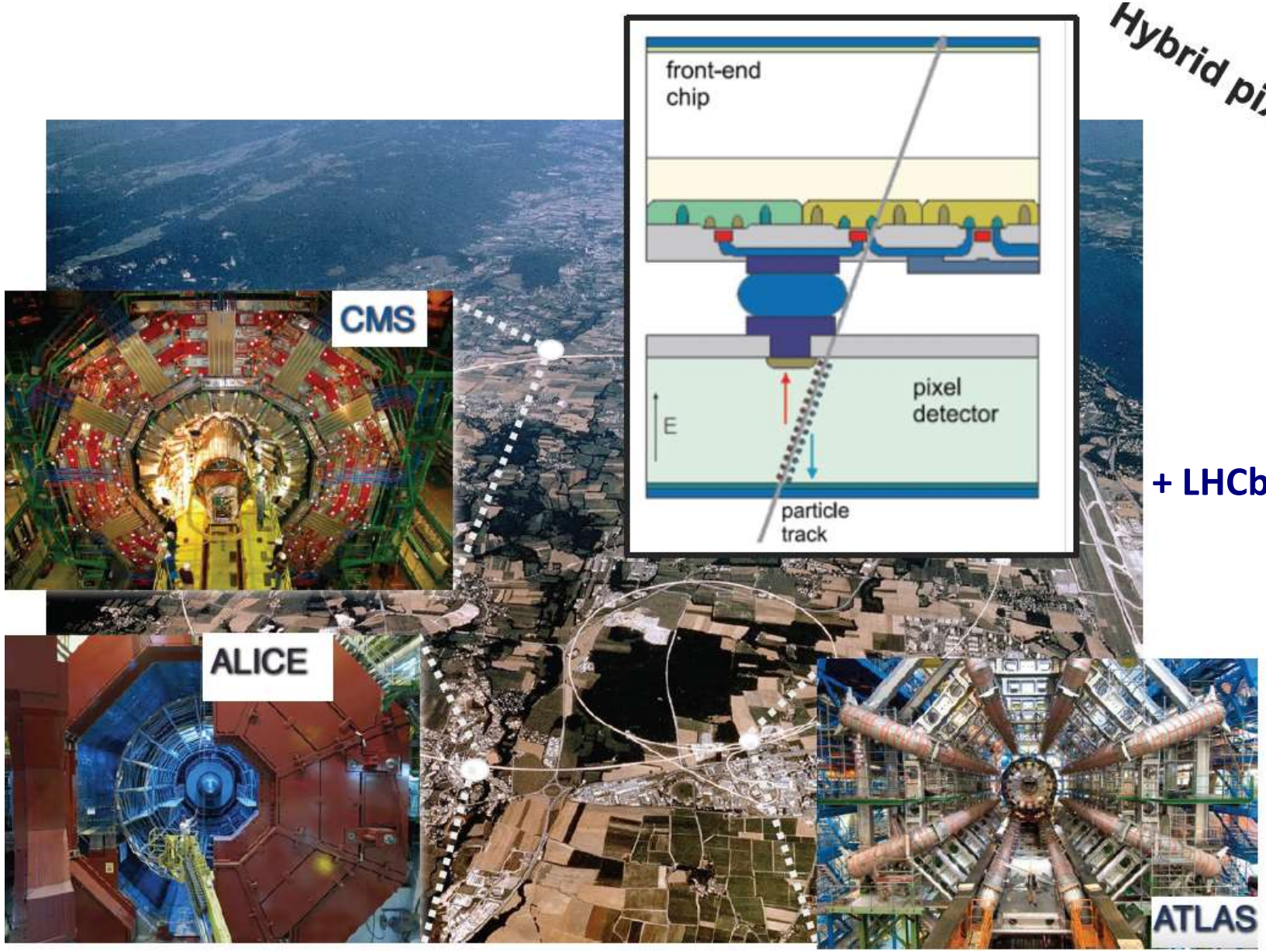
Generic pixel detector | Cross-sectional cut

- There are also some other aspects:
  - Relatively large material budget: >1.5% X0 per layer
  - Resolution could be better
  - Complex and laborious module production
    - ⋆ bump-bonding / flip-chip
    - ⋆ many production steps
  - Expensive



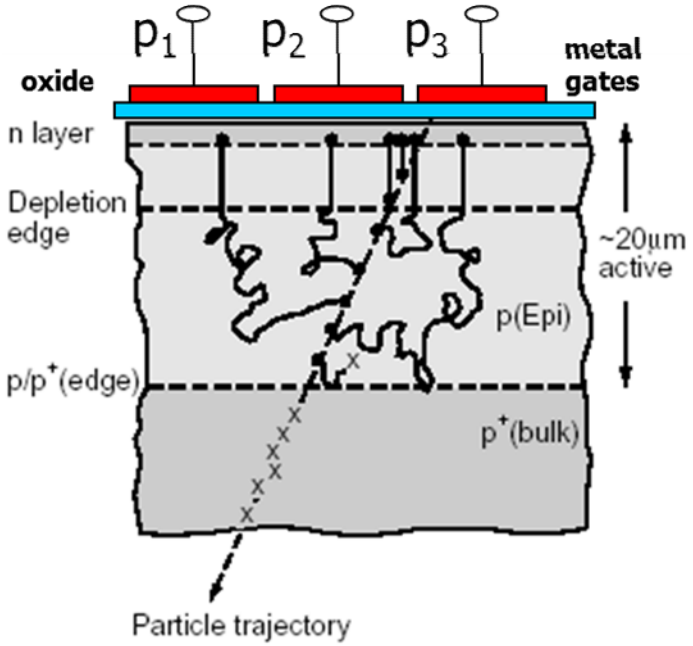
- But hybrid pixels are extremely successful and if you look at today's LHC experiments...

Pixel Detectors at LHC



CCD (Charge Coupled Devices)

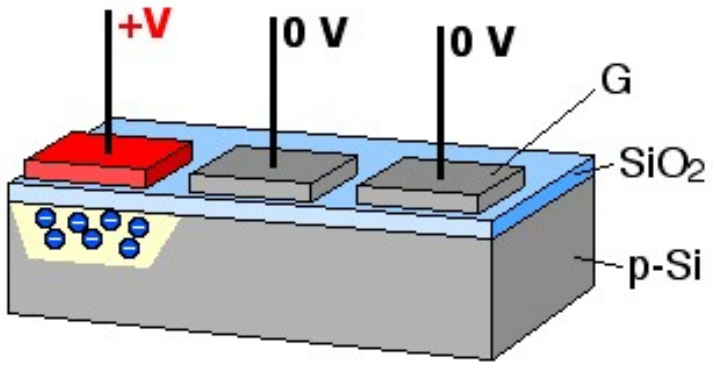
- History
  - First CCD was designed in AT&T Bell Lab in 1969 by Willard S. Boyle and George E. Smith (Awarded with the Nobel Prize in Physics for 2009)



Step 1 - Charge Generation
Step 2 - Charge Collection
Step 3 - Charges Transfer
Step 4 - Charge-to-Voltage Conversion
Step 5 - Digitization

Buried channel CDD:

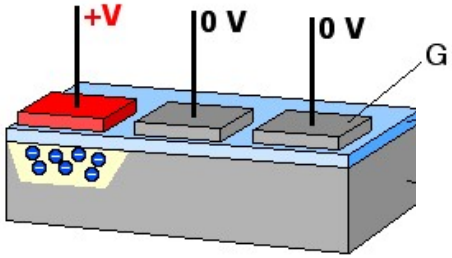
- Potential minimum moved from the surface by n^+
- Collected charge is a combination of drift and diffusion (drift much faster – high resistive epi-Si)
- p/p^+ edge works as a reflection layer
- MOS gate is superimposed on top of the n^+ layer
- Depleted region is controlled by the voltage applied to the electrodes (p_1,p_2,p_3)

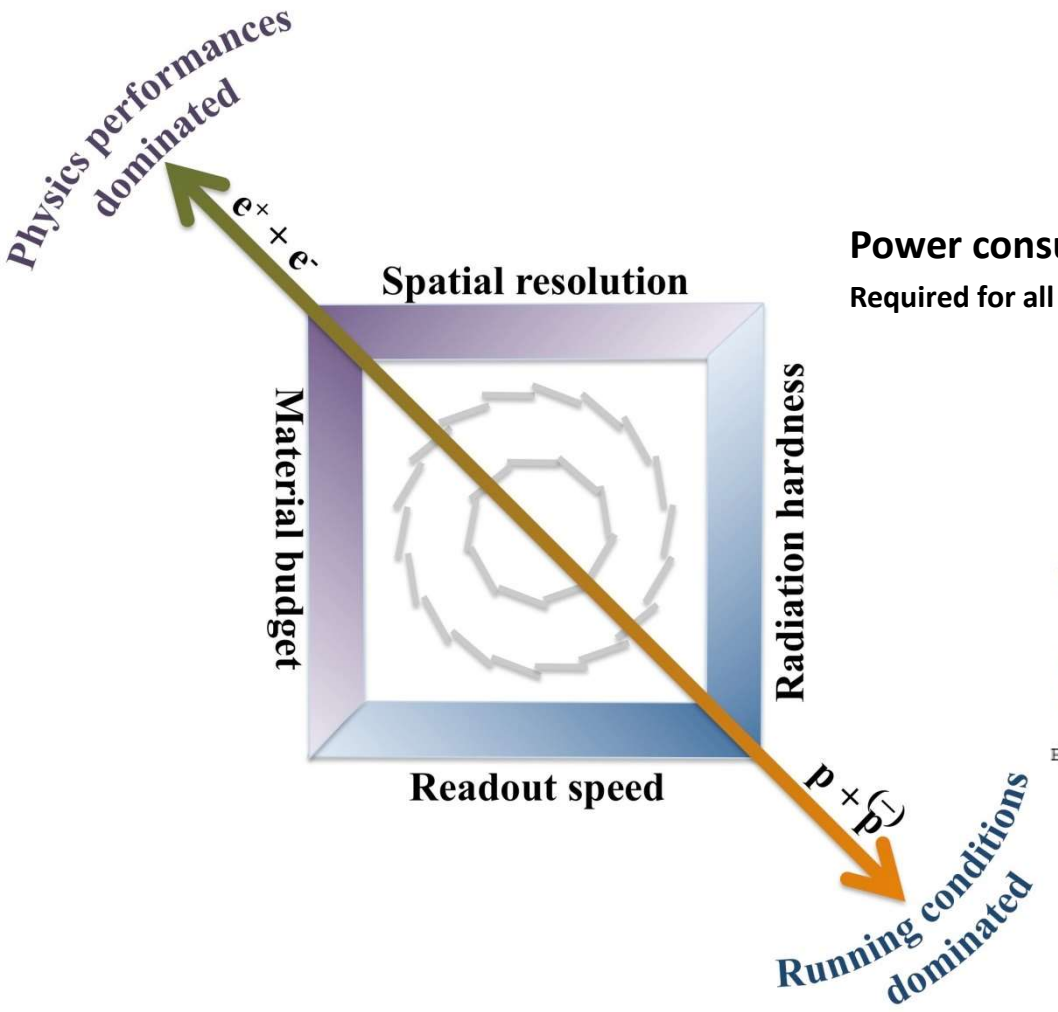


SLD CCD Vertex Detector (SLAC Linear Collider)
Pixels of 22 x 22 µm²

Trends for Pixel Sensor Development

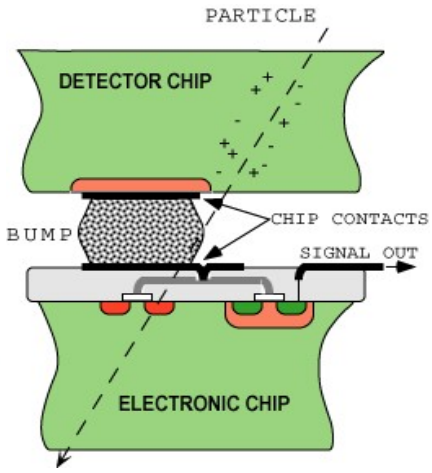
CCD (Charge Coupled Device)





Power consumption

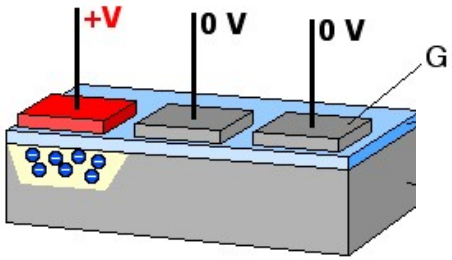
Required for all experiments



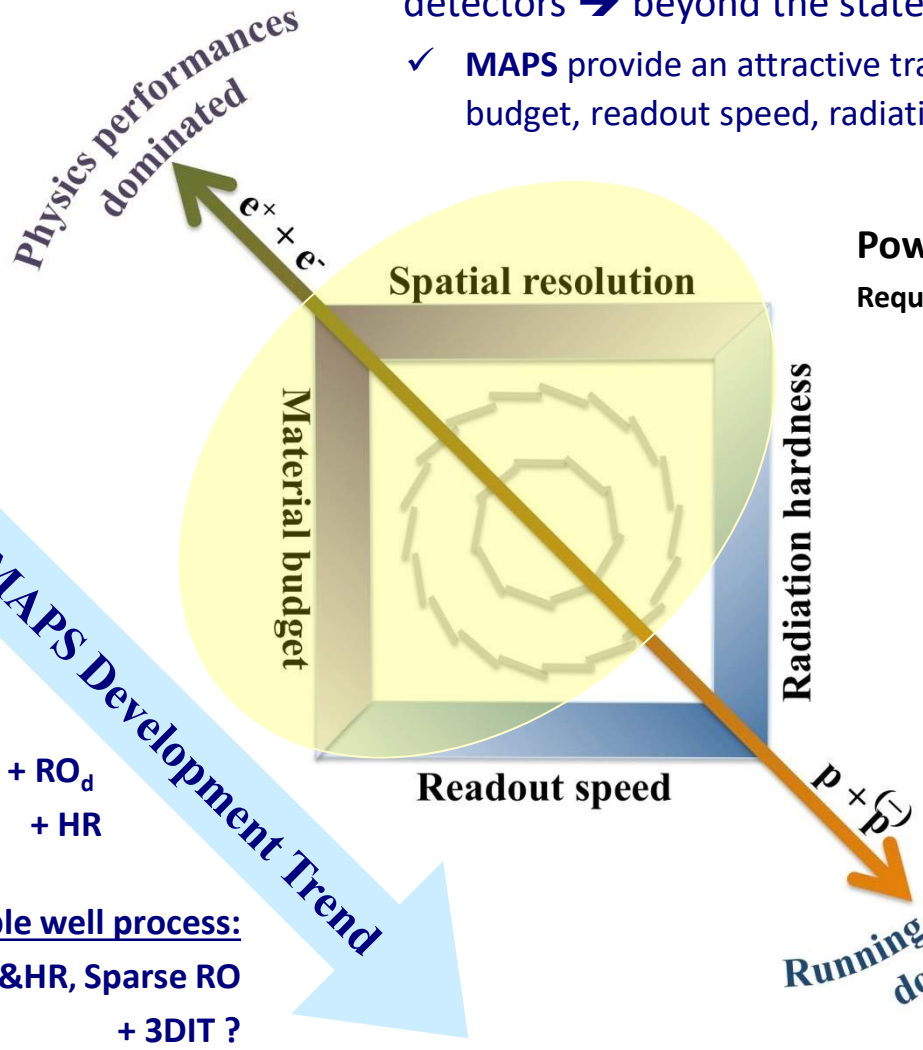
Hybrid Pixel Detector

Trends for Pixel Sensor Development

CCD (Charge Coupled Device)



- CPS triggered by the need of very granular and low material budget sensors. Future subatomic physics experiments need detectors ➔ beyond the state of the art
  - ✓ **MAPS** provide an attractive trade-off between granularity, material budget, readout speed, radiation tolerance and power dissipation



Power consumption

Required for all experiments

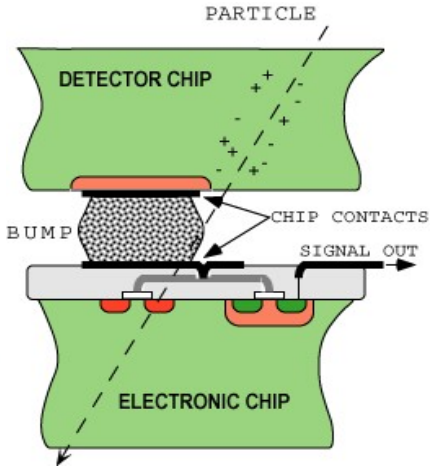
Twin well process:

Pixels: 2/3 T + RO_a

In-pixel signal processing + RO_d + HR

Quadruple well process:

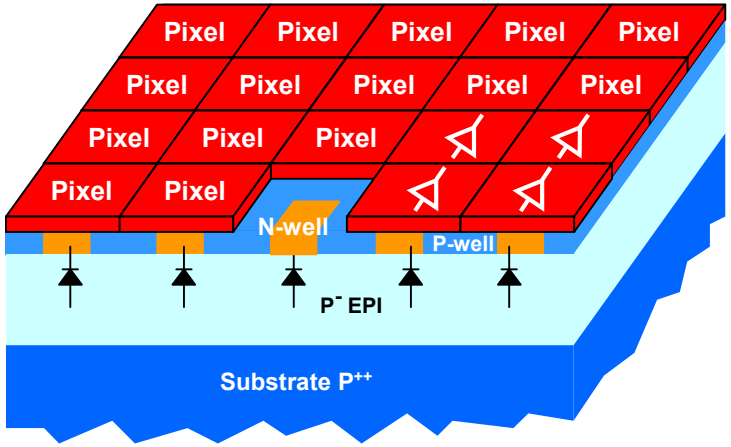
HV&HR, Sparse RO + 3DIT ?

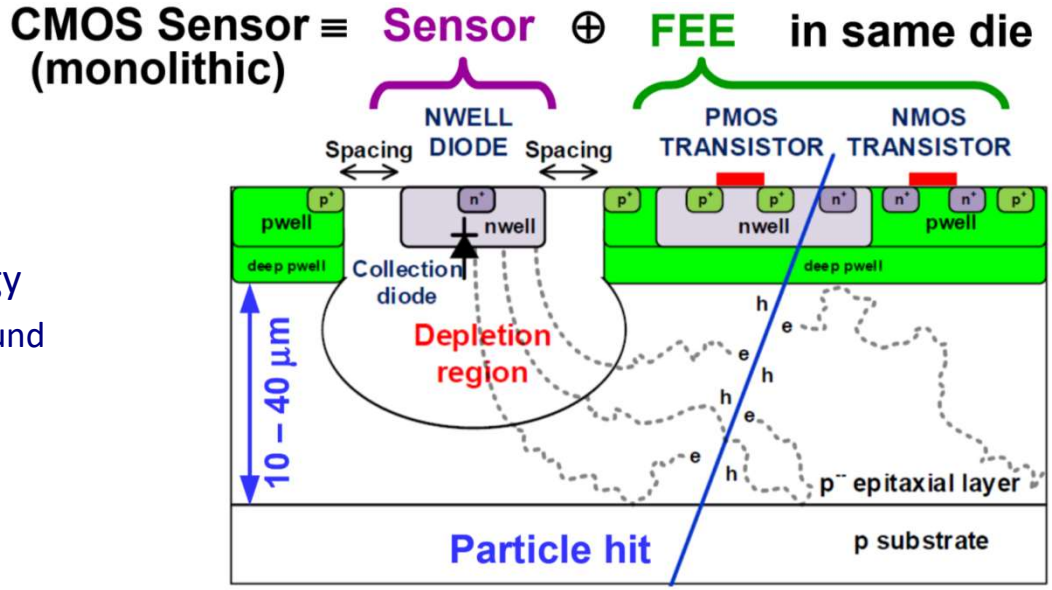


Hybrid Pixel Detector

Principle of CMOS Pixel Sensor

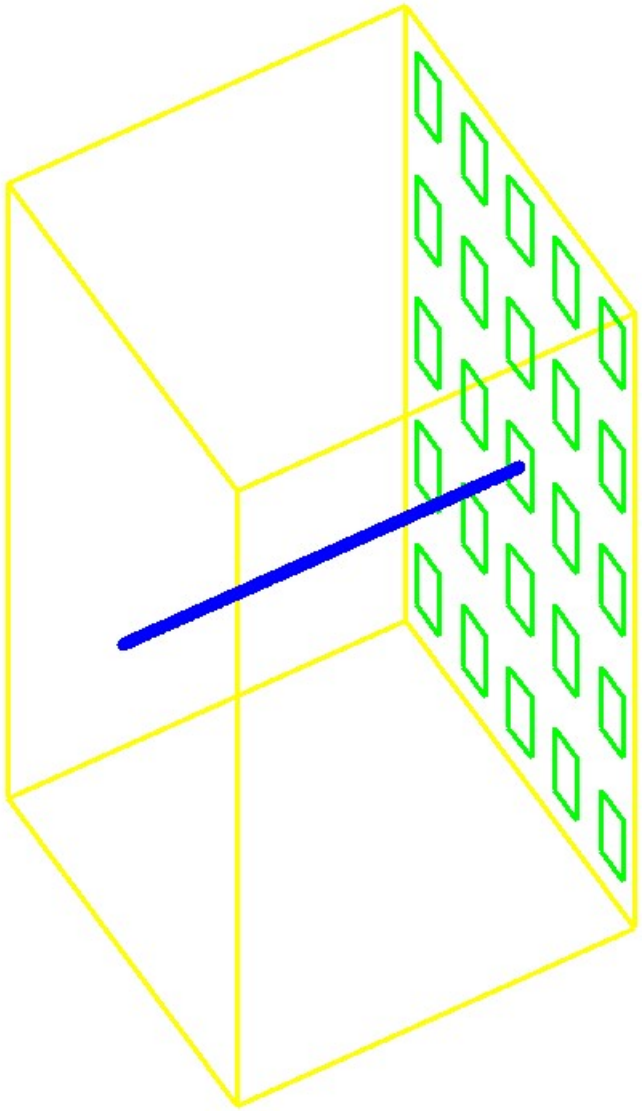
- **Original aspect:**
  Integration of sensitive volume (EPI: epitaxial layer) and front-end read-out electronics on the same substrate
  - Charge created in EPI layer, excess carries propagate thermally, collected by N_{WELL}/P_{EPI} diodes, with help of reflection on boundaries with P-well and substrate (high doping)
  - Q = 80 e^-h / µm ➔ signal < 1000 e^-
  - High granularity, compact, flexible
  - EPI layer ~O(10) µm thick
  - Thinning to ~30-40 µm permitted
  - Standard CMOS fabrication technology
    - ⋆ Cheap, fast multi-project run turnaround
  - Room temperature operation
    - ⋆ ~35 °C





- Attractive balance between granularity, material budget, radiation tolerance, read out speed and power dissipation

Principle of Operation

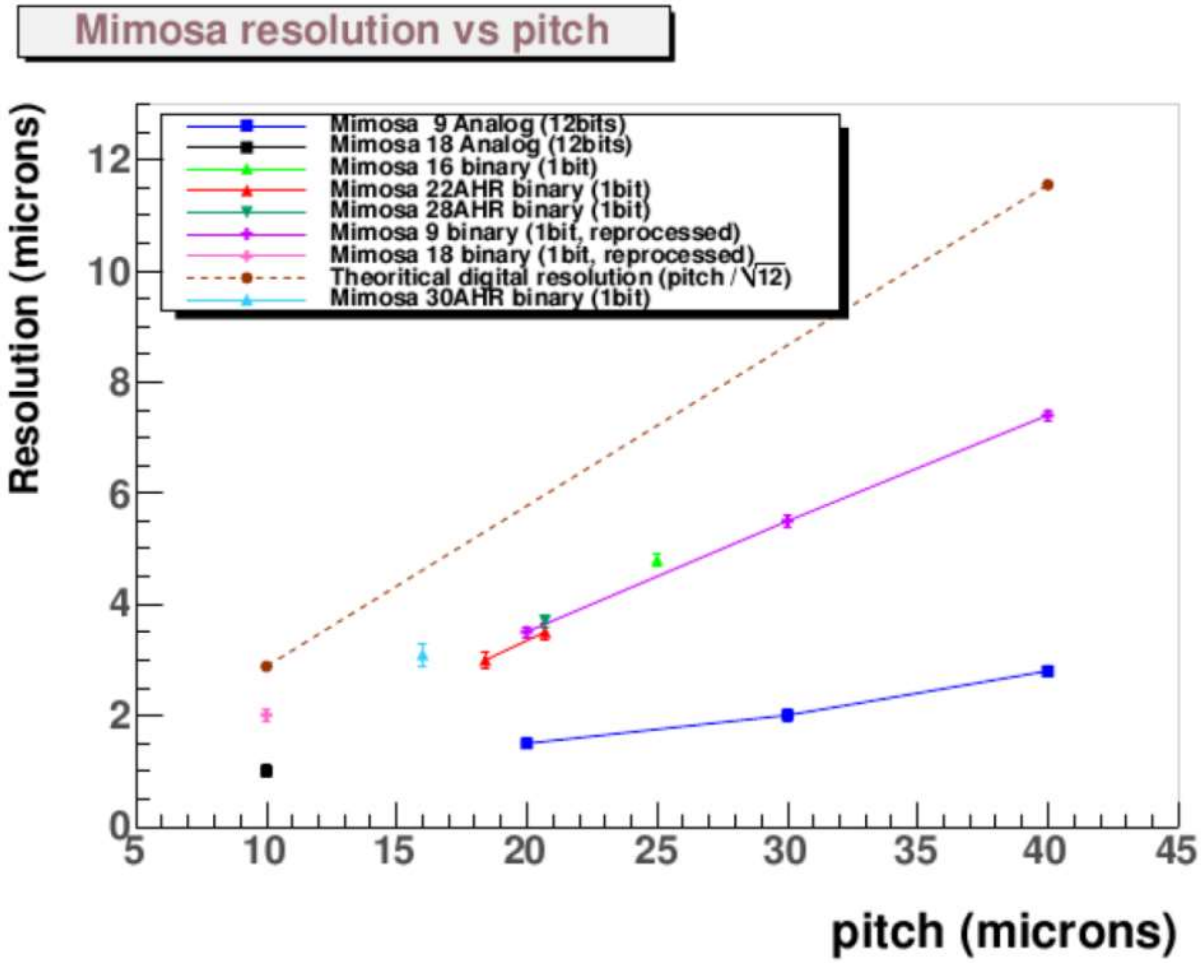


- Energy of a particle transferred to creation of $e^{-}h$ pairs in silicon bulk (p-type epitaxial layer)
- Moving electrons and holes induce current on sensing electrodes (Nwells)
- Current is converted to voltage on Nwell/Pepi diode capacitance

- Physics processes describing the charge collection are very complex
  - Device simulation is needed to understand them and to verify new ideas…

Single Point Resolution

- Driven by pixel pitch
- Benefits from large cluster: Exploit charge centre of gravity



Single Point Resolution vs Electric Field

- Low electric field:
  - Charge sharing (charge centre of gravity) → resolution improved
    - Low-level signals may be lost
  - Charge collection time longer
    - Charges recombination increase
  - Radiation tolerance degraded

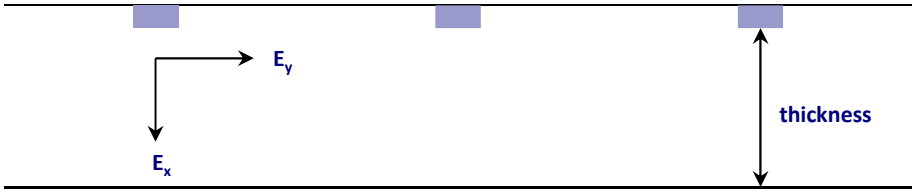
- High electric field:
  - Charge collection time short
    - radiation tolerance enhance
  - Less charge sharing → resolution reduced
    - Less signals loss

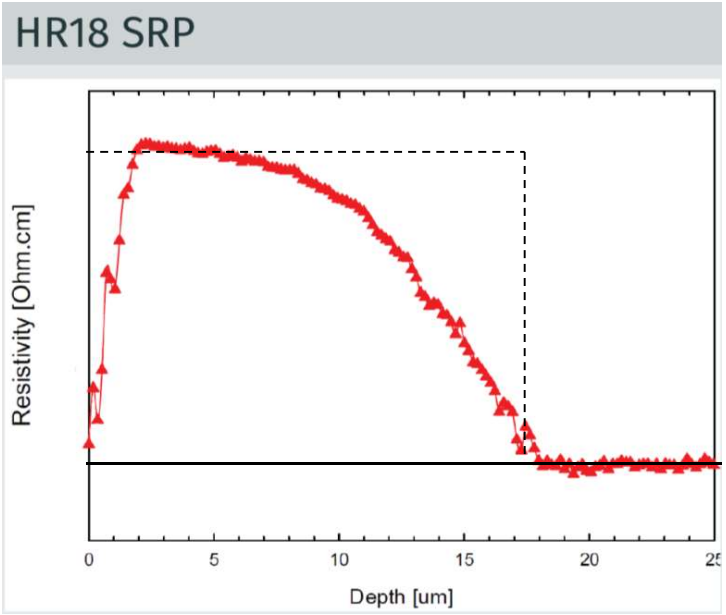
Electric Field on Function of Multi-parameters

$$E_{x,y} \propto f\,(\rho, V, Diode\ geometry, Diode\ density, Doping\ profile,\ \ Thickenss, \ldots)$$

ρ: resistivity

V: bias voltage (front-side or back-side)





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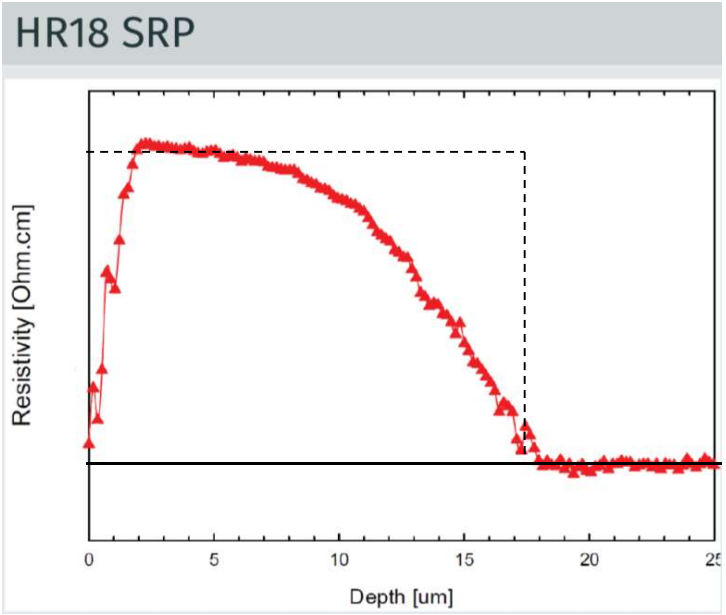
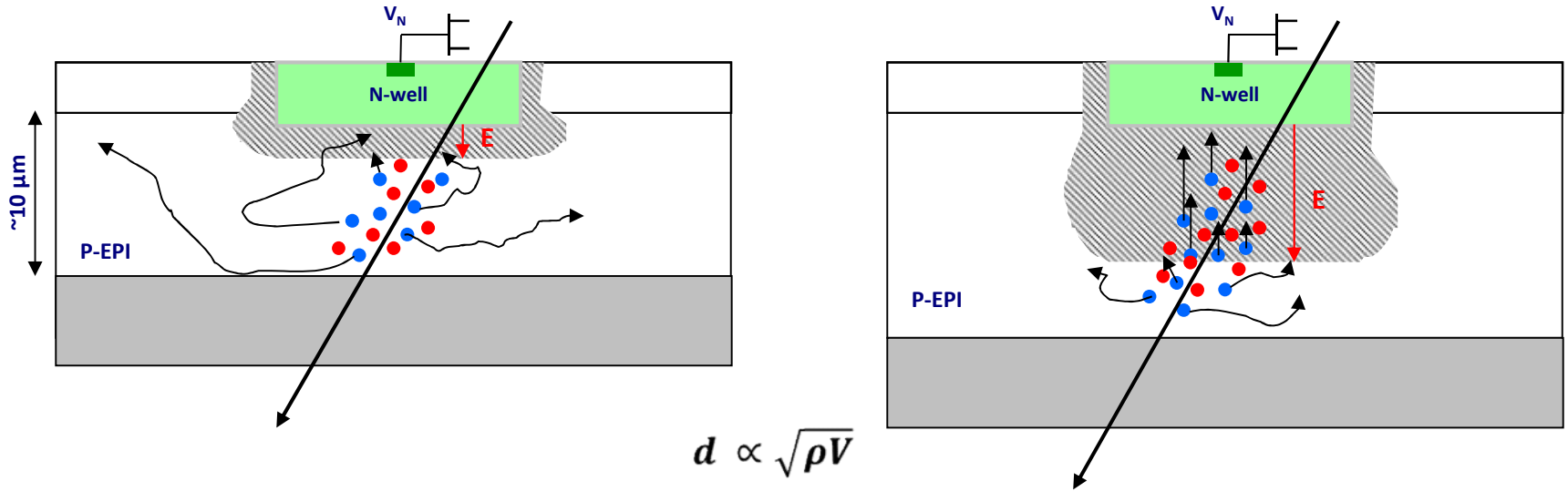


CMOS Pixel Sensors: EPI Layer



$$d \propto \sqrt{\rho V}$$

Standard Epitaxial Layer

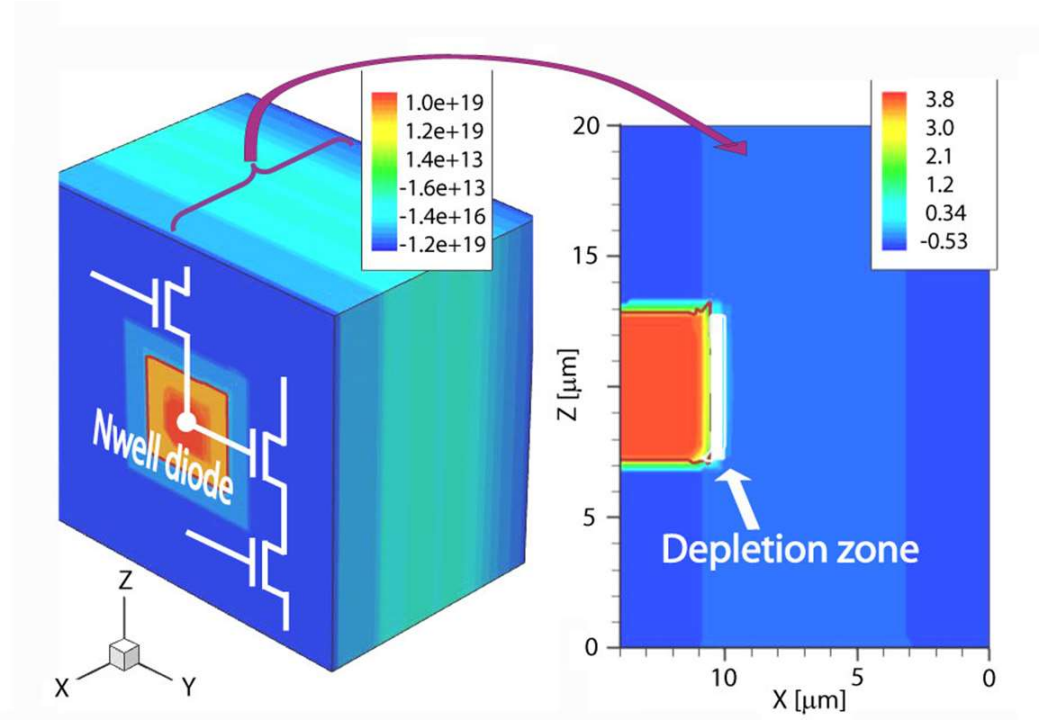
- *Standard CMOS OPTO Process: EPI ~10 Ω*cm*
- *Charge collection: thermal diffusion*
- *Collection time: O(100 ns)*

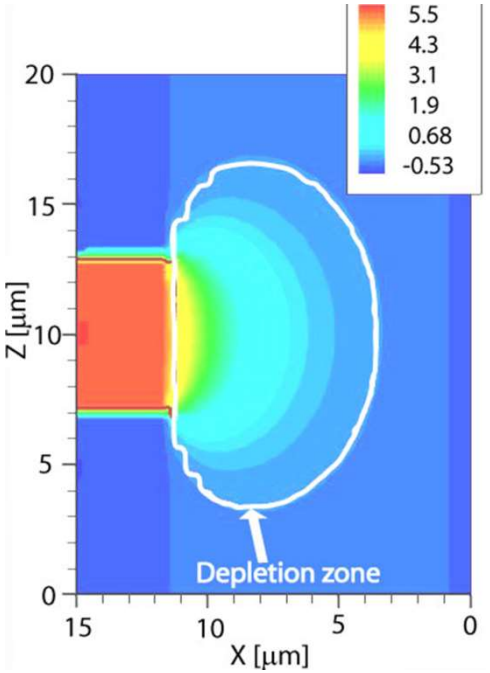
High resistivity (HV) Epitaxial Layer

- *High resistivity >1 kΩ*cm & thicker (up to 40 µm) EPI*
- *Charge collection: drift/thermal diffusion*
- *Collection time faster, less recombination ➔ radtol.*
- *Depletion depth depends on bias*

Standard EPI Layer vs. HR EPI Layer

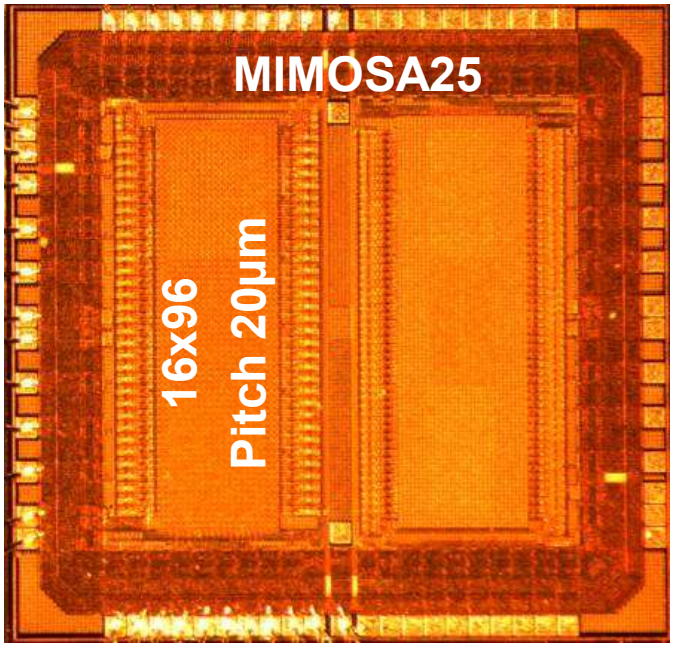
- Standard CMOS technology p-epitaxial layer has low resistivity ~10 Ω•cm
  - Charge collection time ~> 100 ns due to non depleted layer
- "High" resistivity p-epitaxial layer has resistivity:
  - ~400 Ω•cm (Mimosa28-Ultimate - 2010) and > 1 k Ω•cm (ALPIDE - 2016)

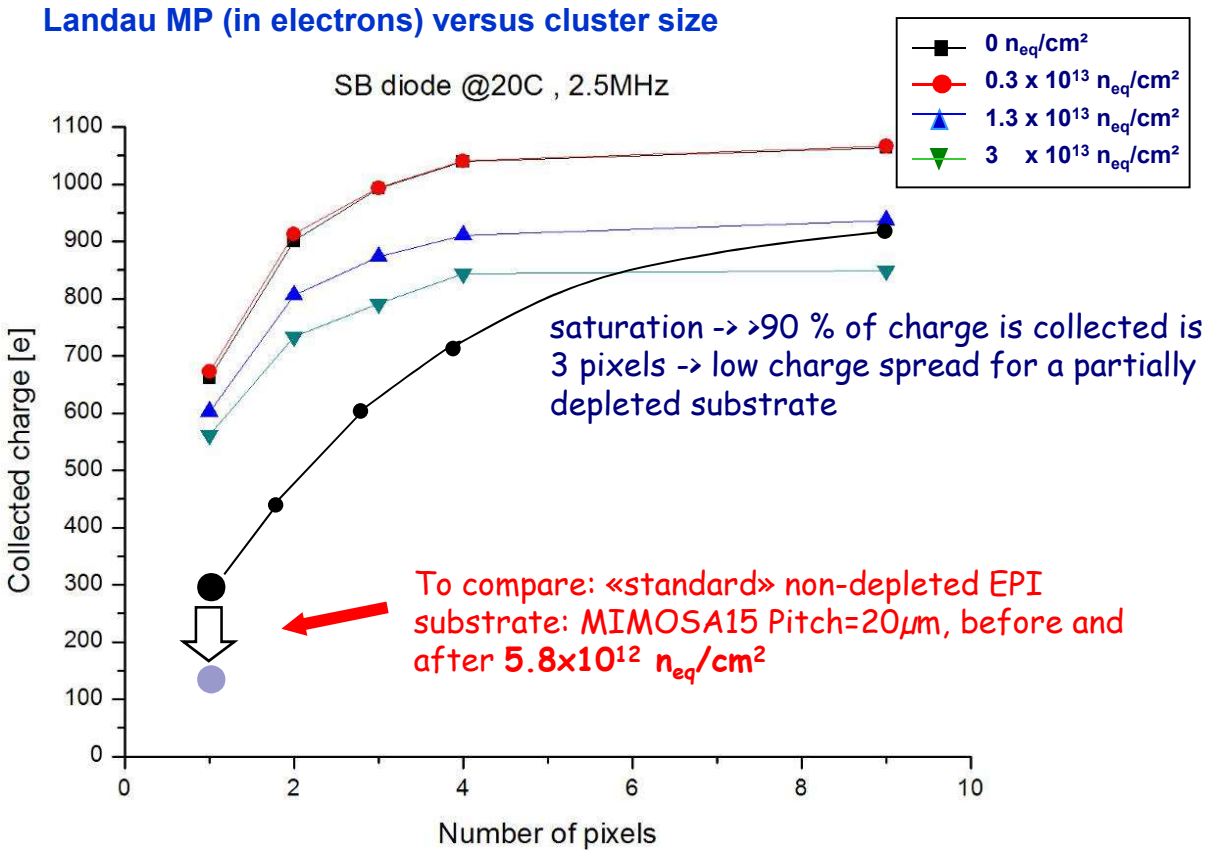




Courtesy of Andrei DOROKHOV

MIMOSA25 (2009) in High Resistivity (HR) Epitaxial Layer

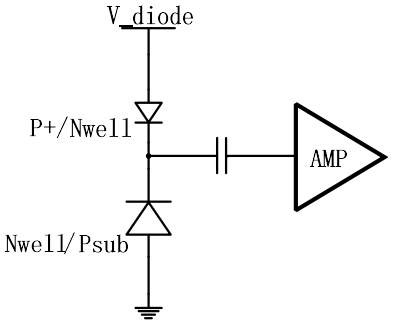


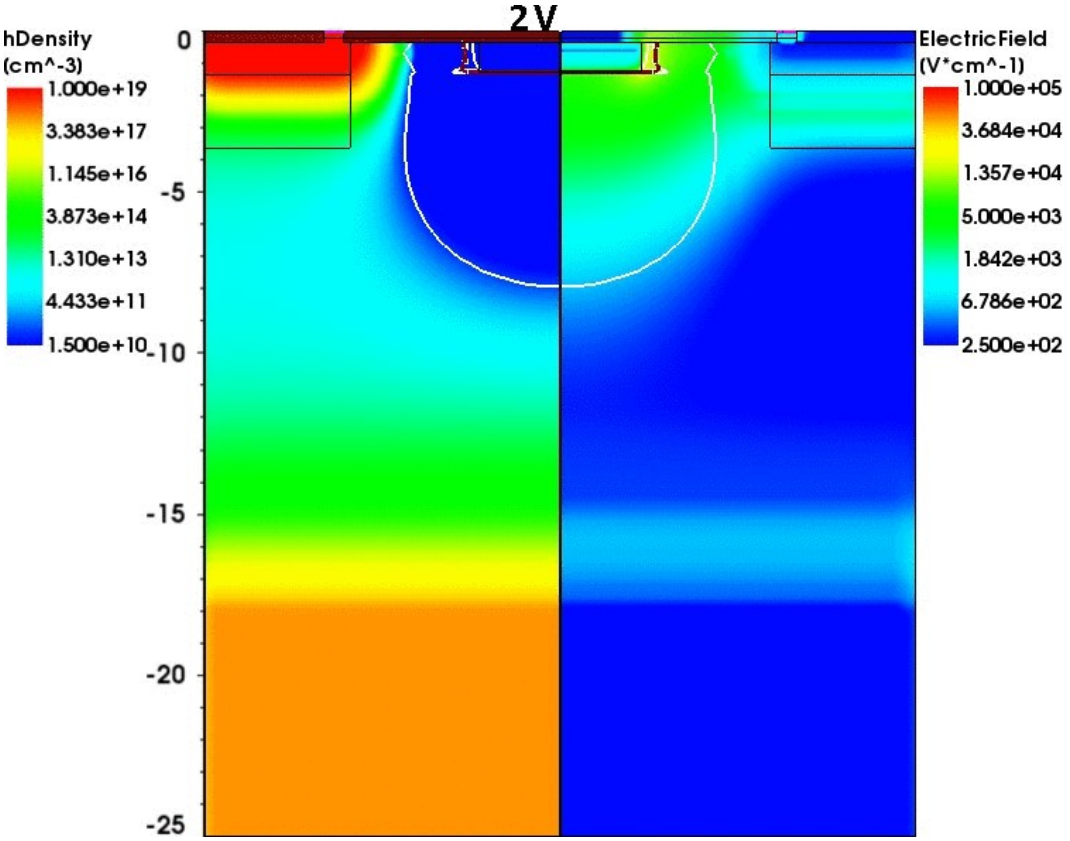


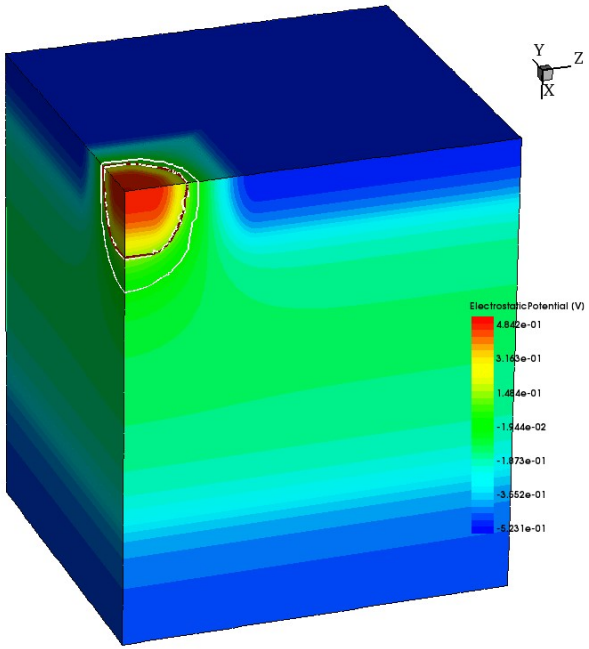
- Resistivity of the EPI layer: ~400 Ω•cm
- 20 µm pitch, + 20°C, self-bias diode @ 4.5 V, 160 µs read-out time
- Fluence ~ (0.3 / 1.3 / 3) • 10^{13} n_{eq}/cm^2
- Tolerance improved by > 1 order of mag.

High Voltage (HV) in MAPS

- Simulation result: (TJ HR18: ρ > 1 kΩ•cm, EPI_{th} ~ 18 µm)



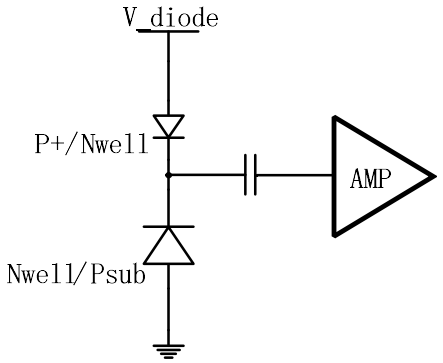




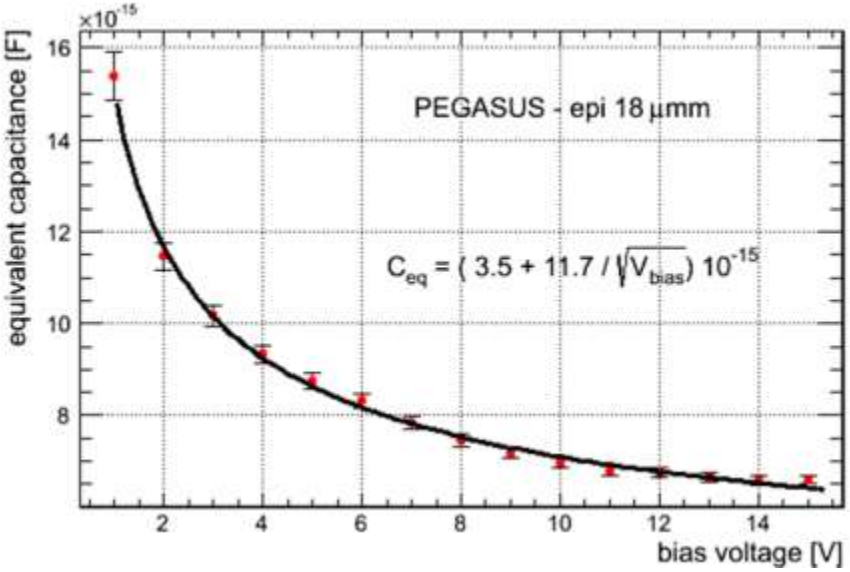
Effects of High Voltage (HV)

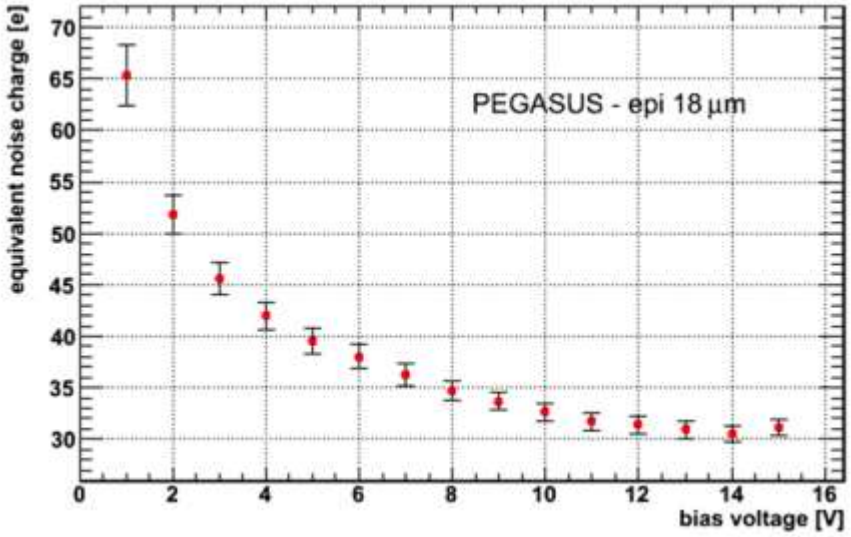
- Input equivalent capacitor C_{eq}
  - Expected behaviour

$$C_{eq} \propto \frac{1}{\sqrt{V_{bias}}}$$



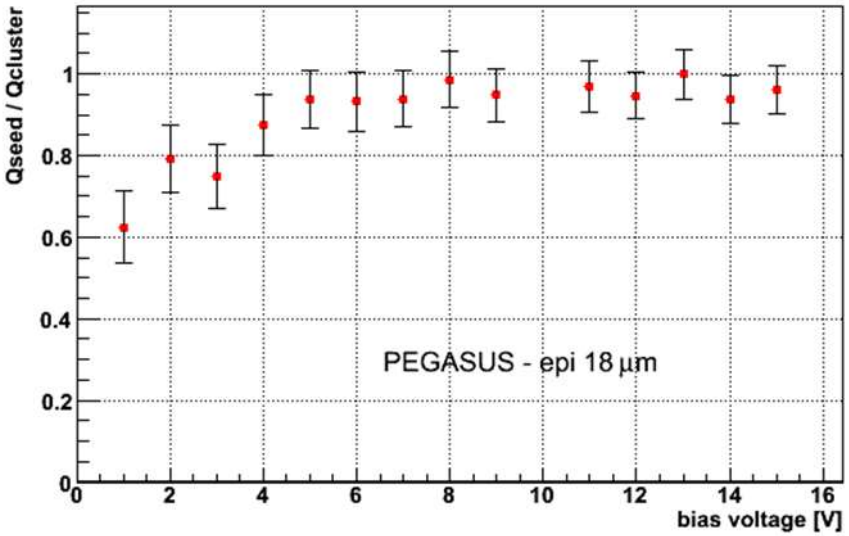
- Equivalent noise charge ENC
  - Interplay C_{eq} & leakage current

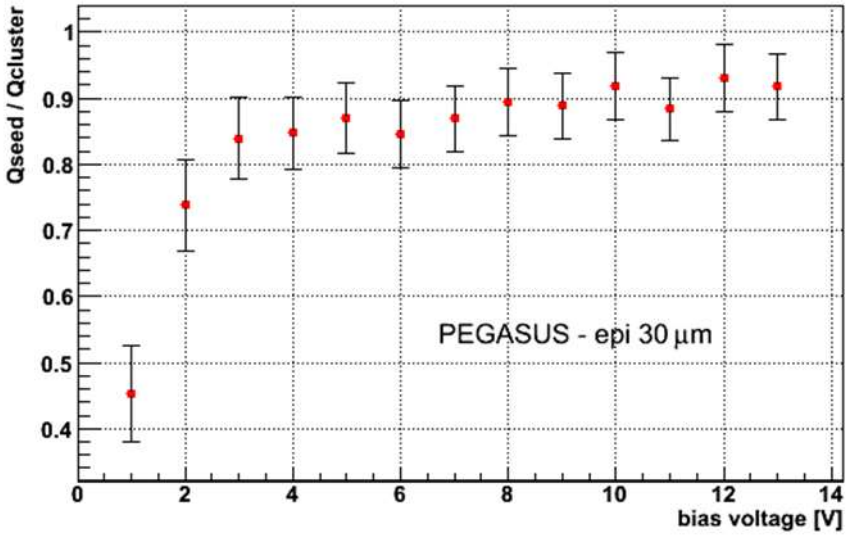




Effects of High Voltage (HV) - (2)

- Cluster size is impacted by depletion ➔ ratio $\frac{Q_{seed}}{Q_{cluster}}$





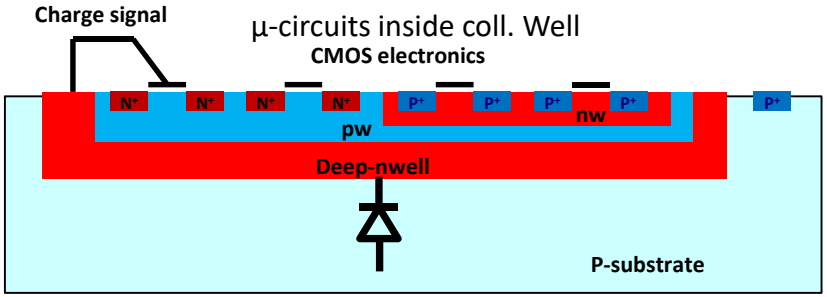
➔ **Clear evolution with bias voltage**

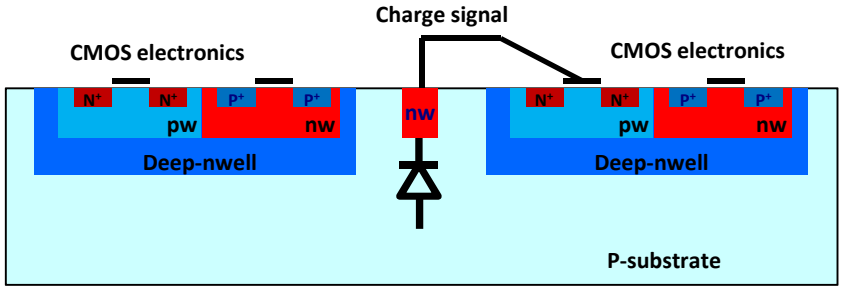
↳ Saturation effect <~ 8 V

Large Electrodes vs. Small Electrodes

$$E_{x,y} \propto f\,(\rho, V, \textit{Diode geometry}, \textit{Diode density}, \textit{Doping profile}, \textit{Thickenss}, \ldots)$$

- Sensing node = key element → SPECIFIC GLOBAL OPTIMISATION for each dedicated application
  - Pixel pitch, nw dimensions, spacing between nw & dnw, voltage





Large electrodes (HVCMOS)

+ *No low field regions*
+ *On average short(er) drift distances → radiation hard*
− *Large sensing node capacitance (~200 fF) → ENC, gain, rise time, power*

$$ENC^2_{thermal} = \frac{4}{3}\frac{kT}{g_m}\frac{C_d^2}{\tau} \qquad \tau_{CSA} \propto \frac{1}{g_m}\frac{C_d}{C_f}$$

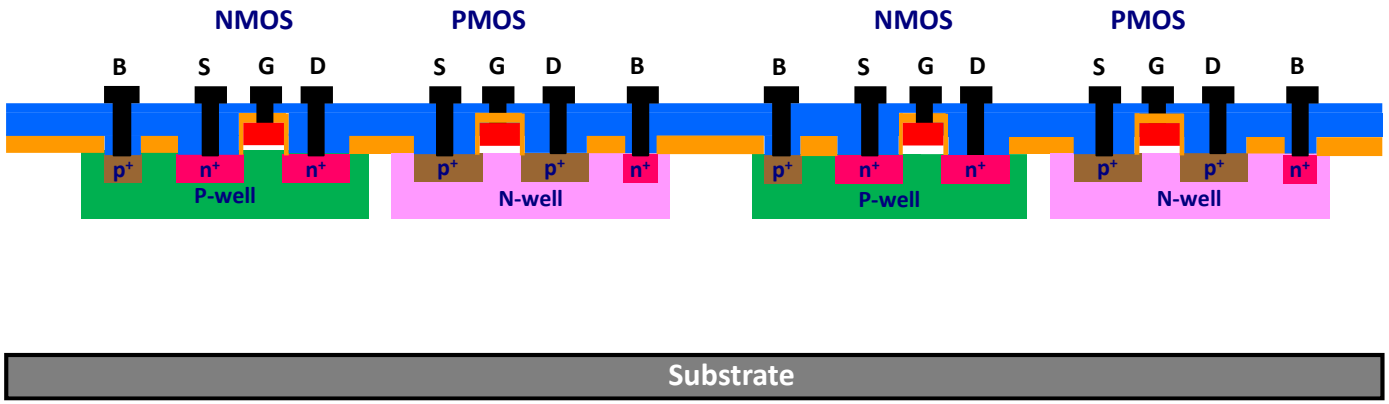
− *Risk of X-talks between Dig. & Ana. µC*

Small electrodes

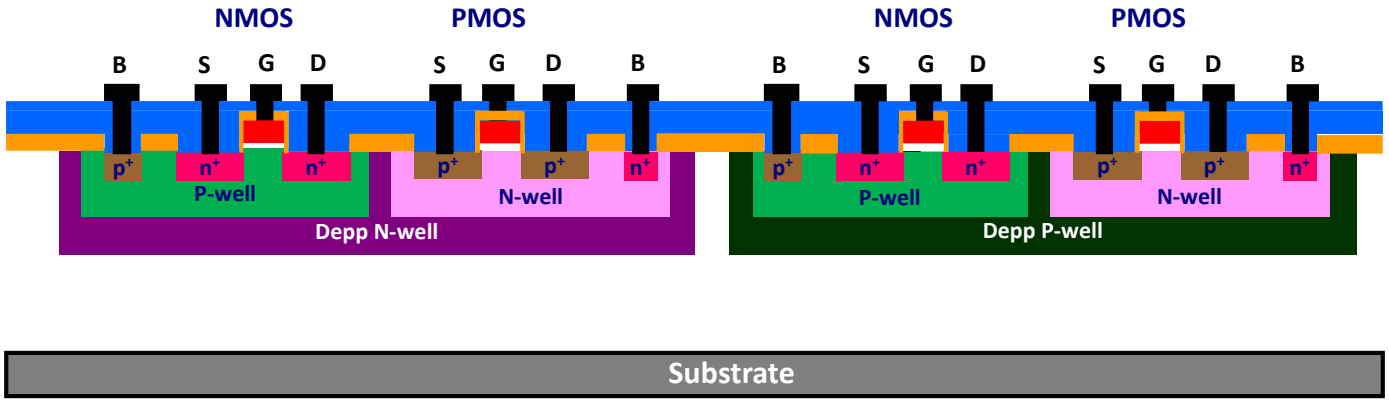
+ *µ-circuits outside coll. Well*
+ *Small capa. (~5 fF) → high SNR, fast signal*
+ *Separate Ana. & Dig µ circuits*
− *On average longer drift distances and low field regions → radiation hardness more diffcult?*

CMOS Fabrication Process

- Twin-well process:
  - Separate optimization of the n-type and p-type transistors is provided. The independent optimization of Vt, body effect and gain of the P-devices, N-devices is made

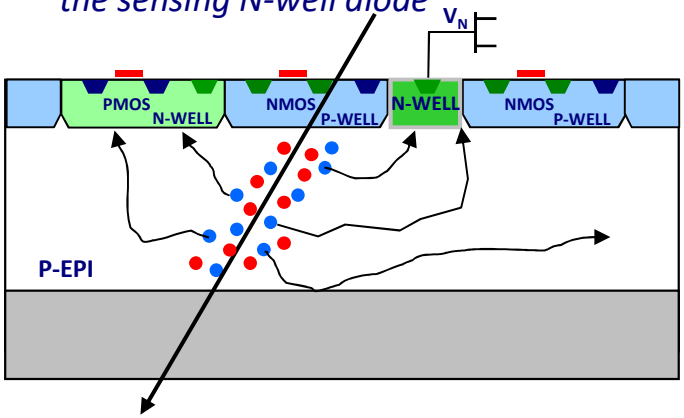


- Triple & quadruple well process:



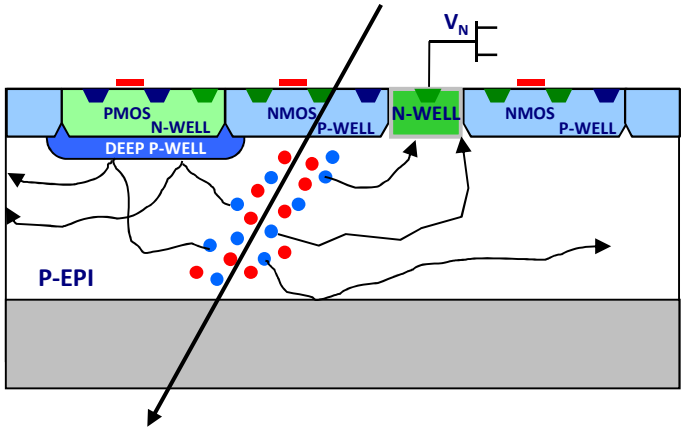
MAPS Process Evolution

- *Twin well process: 0.6-0.35 µm*
  - *Use of PMOS in pixel array is not allowed because any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode*

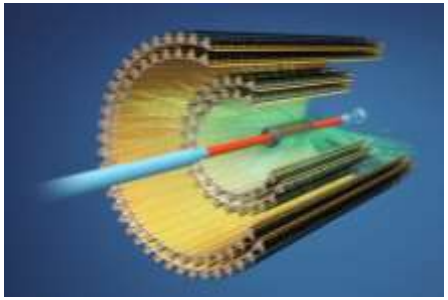


  - *Limits choice of readout architecture strategy*
  - *Already demonstrate excellent performances*
    - ⋆ *STAR PXL detector: MIMOSA28 are designed in this AMS-0.35 µm process*
      - ✓ $\varepsilon_{eff} > 99.5\%$, $\sigma < 4$ µm
    - ⋆ *1st MAPS based VX detector at a collider experiment*

- *Quadruple well process (deep P-well): 0.18 µm*
  - *N-well used to host PMOS transistors is shielded by deep P-well*
  - *Both types of transistors can be used*



  - *Widens choice of readout architecture strategies*
    - ⋆ *ALICE ITS upgrade:*
      - Data driven Readout



MAPS Design: Optimisation Process

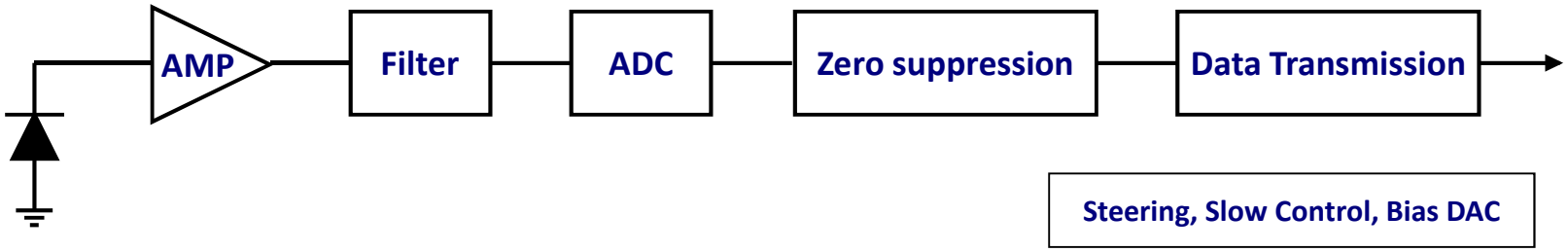
- Sensor performance are evaluated in terms of:
  - Noise ⟷ Dark hit noise
  - Charge Collection & Signal/Noise ⟷ Detection efficiency (ε_{det})
    Radiation tolerance
  - Cluster multiplicity (CM) ⟷ Spatial resolution (σ_{sp})

  } **Depend on construction parameters**

- E.g.: Role of epitaxial layer
  - Q_{signal}: thickness & doping profile
  - ε_{det} & NIEL tolerance: depletion depth vs thickness
  - CM & σ_{sp} : pixel pitch / thickness, depletion depth, ...

- Application-specific multi-parametric trade-off to be found, based on exploratory prototypes rather than on simulations

Main Components of the Signal Processing Chain



- Typical components of read-out chain
  - AMP: in-pixel low noise pre-amplifier
    - Low signal value: ~ 80 e-h+ pairs/µm ➔ signal O(1 Ke^-) collected by a cluster of ~3-5 pixels➔ low noise
  - Filter: in-pixel filter ➔ low noise
  - ADC: analog-to digital converter (1 bit = discriminator)
  - Zero suppression: only hit pixel information is retained and transferred
  - Data transmission: O(Gbits/s) link implemented on sensor periphery
- Read-out in general data-driven
  - Synchronous: clock distribution over pixel array ➔ power consumption
  - Asynchronous: no clock running over pixel array ➔ increased design complexity?
- Trade-off between conflicting parameters

Figure of Merit S/N vs Design Optimisation

- **Signal:** $S(\mathrm{v}) = \frac{Q}{C}$ $\qquad C = C_{diode} + C_{Tin} + C_{connection}$
  - *Small collection electrode, small input transistor, short inter connection for low C*
  - *BUT too small diode does not favour the charge collection*
- **Noise:**
  - *Sensing Diode:*
    - ⋆ *Shot noise due to leakage current, especially after irradiation*
      - ✓ I_{leak} *is proportional to diode dimensions*
      - ✓ *Shot noise is proportional to integration time, negligible for short integration time O(1 µs)*
    - ⋆ *RTS (Random Telegraph Signal) noise*
  - *Input Transistor: in* ***W****eak inversion:* $dv_{eq}^2 = \left(\frac{K_F}{WLC_{ox}^2 f^{\alpha}} + \frac{2K_B T n}{g_m}\right) df, \quad g_m \sim I$

    S*trong inversion:* $dv_{eq}^2 = \left(\frac{K_F}{WLC_{ox}^2 f^{\alpha}} + \frac{4K_B T \gamma}{g_m}\right) df, \quad g_m \sim \sqrt{I}$

    Flicker noise (1/f) *Thermal noise*
    - ⋆ *To minimise*
      - ✓ *Flicker noise: large input transistor → large* C_{tin} *& area*
      - ✓ *Thermal noise Large* g_m *, → high power*
      - ✓ *Both of two noise: Use a filter (band-pass)*

    → 1. *trade-off between Noise & Power*
    2. *trade-off between MOS in very weak inversion & dispersion*
    3. *need a filter*

K_F	*Technology dependent constant*
W, L	*MOS transistor width and length*
C_{ox}	*Gate oxide capacitance per unit area*
g_m	*Transistor transconductance*
K_B	*Boltzmann constant*
T	*Absolute temperature*
n	*Weak inversion slope*
γ	*Often around ½ - 2/3 in strong inversion*

Figure of Merit S/N vs Design Optimisation (2)

- *In-pixel transistors RTS noise:* *increases as the feature size of the devices is scaled down*
  - *Impact on dimensions (W and L) of the in-pixel transistors*
  - *PMOS has better performance than NMOS*
  - *Negligible if integration time small enough*
- *Reset noise:* $v_N^{\,2} = \frac{kT}{C}$
- *Contributions from:*
  - *Other transistors in pre-amplifier stage is not negligible*
  - *Next stages* $N_{total} = N_1 + \frac{N_2}{G_1} + \frac{N_3}{G_1 G_2} + \ldots$
  - ➔ *High gain in the first stage (G1) tends to mitigate the total noise*

- *Maximise the figure of merit is the design guideline*

Analog Power vs. Q/C

- Signal over noise ratio: $\frac{S}{N} \sim \frac{Q}{C}\sqrt{g_m} \sim \frac{Q}{C}\sqrt[m]{I} \sim \frac{Q}{C}\sqrt[m]{P} \quad with\ 2 \leq m \leq 4$

- Power consumption for constant S/N at a certain bandwidth:

$$P \sim \left\{\frac{Q}{C}\right\}^{-m} \quad with\ 2 \leq m \leq 4$$

  - Q/C: key parameter to reduce analog power consumption
    - ⋆ To gain Q/C by a factor of 2, P reduction of a factor 4 (to 16)
  - Operating the transistor in or near weak inversion region to maximize the g_m (m = 2)
  - … speed?

- Example of an open-loop circuit:
  - A transistor biased at 100 nA in weak inversion has thermal noise ~480 µV (40 MHz BW), high-resistivity (~1 KΩcm) 20 µm thick EPI, small electrode ~5 fF, 30 µm pitch ➔ ≤ 10 mA/cm²

$$\frac{Q}{C} = \frac{80 \times 20 \times q}{5\ fF} = 51\ mV \qquad \frac{S}{N} = \frac{51\ mV}{450\ \mu V} \sim 100$$

- ATLAS hybrid pixel (50x400 µm²):
  - 24 µA/pixel ➔ 120 mA/cm², 285 µm thick sensor, C_f ~400f F, Q/C < 10 mV

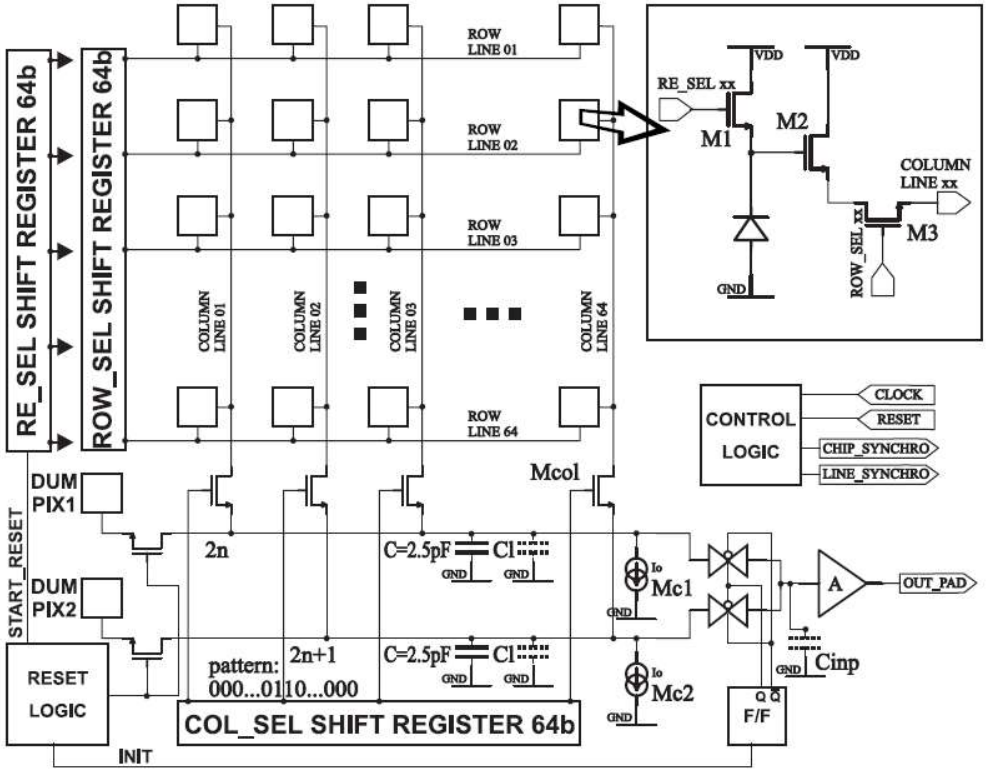
- Strip detector: Q/C < 1mV

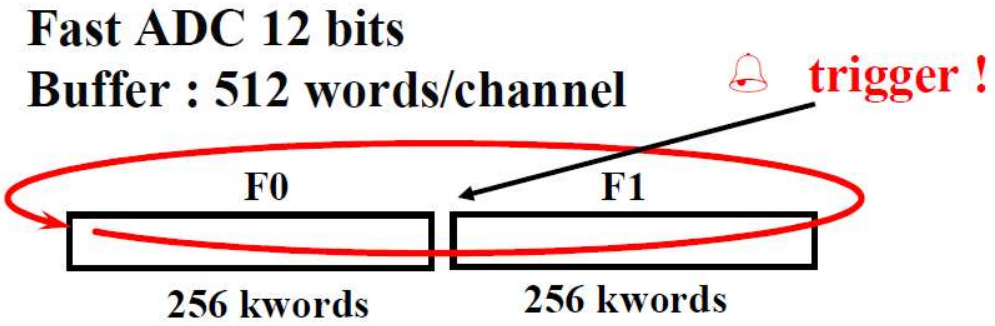
Ref. Monolithic pixel detectors for high energy physics, W. Snoeys, Nuclear Instruments and Methods in Physics Research A 731 (2013) 125-130

First Generation MAPS
Twin-well circuits

1st Generation MAPS

- The simplest readout electronics: diode + 3 transistors/pixel

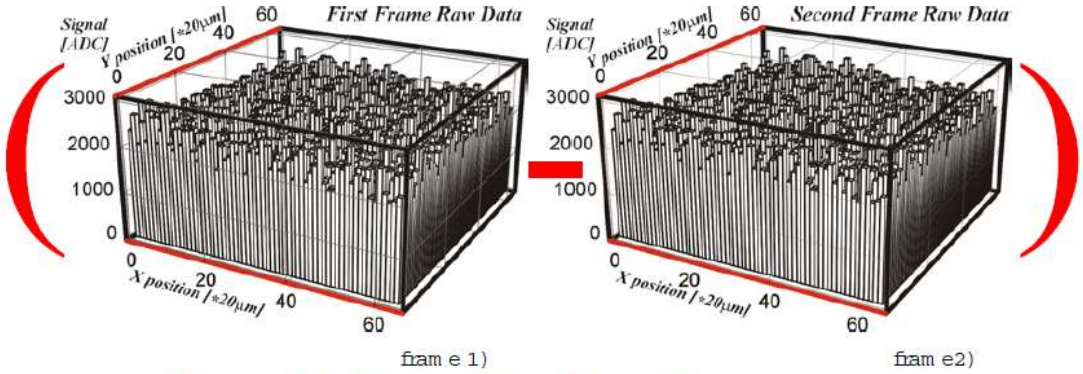




$$V = \frac{Q}{C}$$ (~O(10) mV)

1. Reset in order to inverse bias
2. Continuous serial addressing and readout (digitisation) of all pixels
3. Keeping two successive frames in external circular buffer
4. Following reset when needed (removing integrated dark current)
5. After trigger (or in a real time), simple data processing in order to recognise hits

Data Processing: (Off Line) Correlated Double Sampling

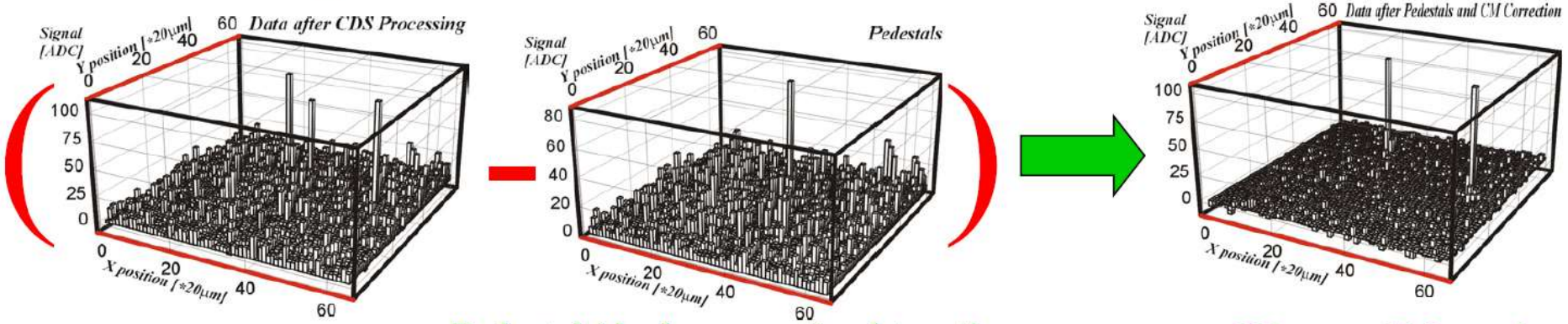


Useful signal on top of Fixed Pattern DC level

Fixed Pattern dispersion: ~100 mV

Typical signal amplitude: ~1mV

(frame2 - frame1) subtraction **Why?** **1. high gain amplifier**



Pedestal (dark current) subtraction

Hit candidates!

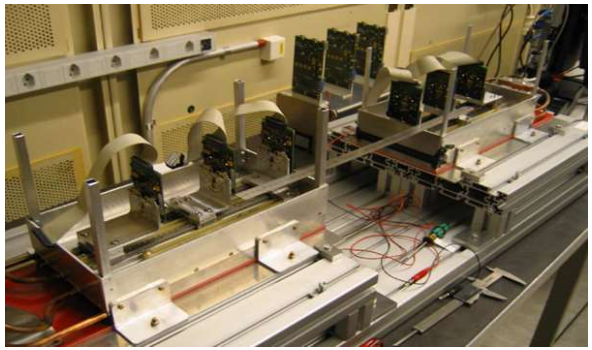
➔ **1. Very long integration time ~ms** **2. fast readout time**

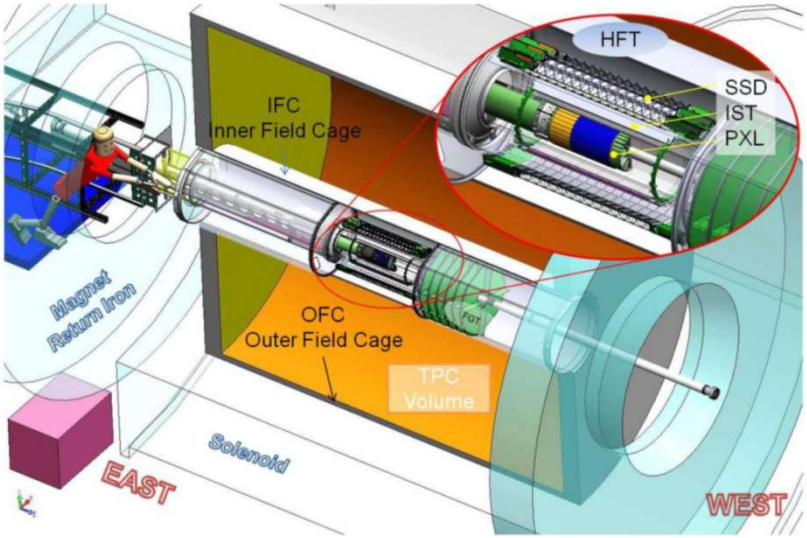
2. Off-line processing

Examples of Pixel Sensor Architectures
Twin-well circuits

The First Two MAPS with Integrated Ø

- Mimosa26: EUDET telescope, provide an infrastructure exploiting detector R&D for the ILC
  - Construct a 6-MAPS planes beam telescope ➔ Extrapolated resolution < 2 µm
- Mimosa28: PXL detector in STAR Heavy Flavor Tracker (HFT) upgrade ➔ Extend the measurement capabilities in the heavy flavor domain, good probe to QGP



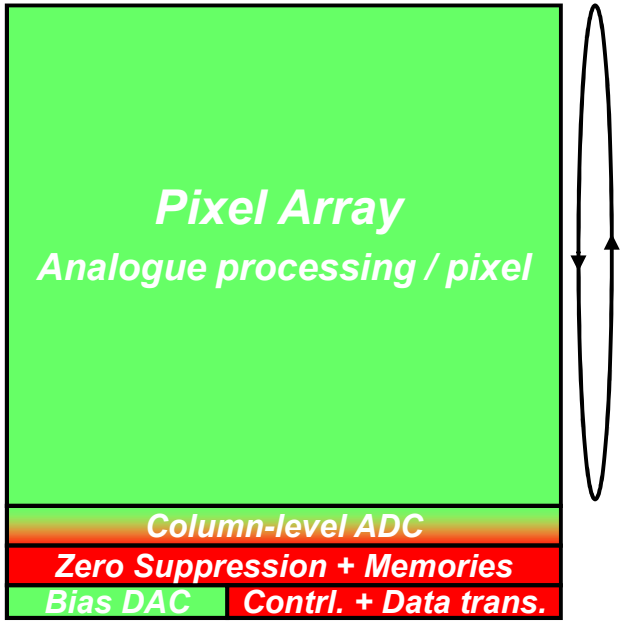


- Two sensors have similar spec.
  - STAR final sensors (M28/Ultimat) spec.:
    - ⋆ Active surface: ~2x2 cm² (EUDET: ~1x2 cm²)
    - ⋆ Total ionizing dose: 150-300 kRad per year
    - ⋆ Non-ionizing radiation dose: charged pions <~ O(10^{13}) / year
    - ⋆ Hit density: 10^6 hits/s/cm²
    - ⋆ Readout (integration) time: < 200 µs (EUDET: 115.2 µs)
    - ⋆ Power consumption: ~100 mW/cm²
- Designed in a 0.35 µm **Twin-well** process

Twin-Well: High Readout Speed Sensors Architecture

- ***Design according to 3 main issues:***
  - *Increasing S/N at pixel-level*
    - ⋆ *Pre-amp and cDS in each pixel*
  - *A to D Conversion at column-level*
    - ⋆ *1 discriminator / column*
    - ⋆ *Offset + FPN compensations*
  - *Zero suppression at chip edge level*
    - ⋆ *Reduce the raw data flow of MAPS*
    - ⋆ *Data compression factor ranging from 10 to1000, depending on the hit density per frame*
  - *On-chip bias DAC, voltage regulators*
  - *Remote and programmable controller*

Implemented in chip periphery

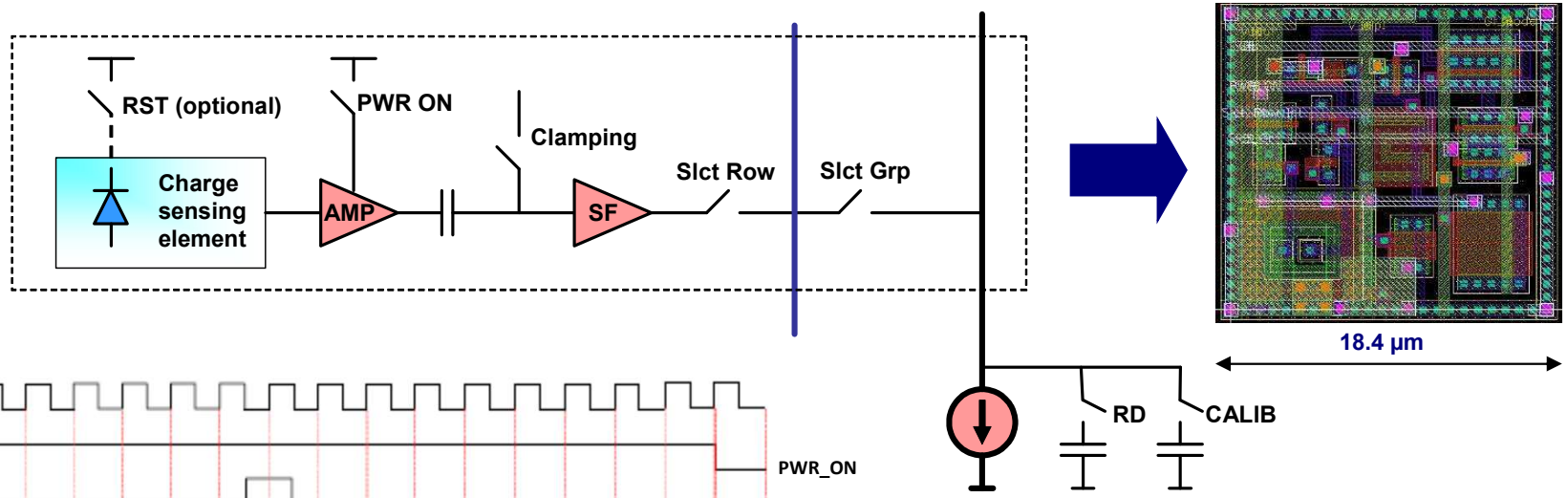


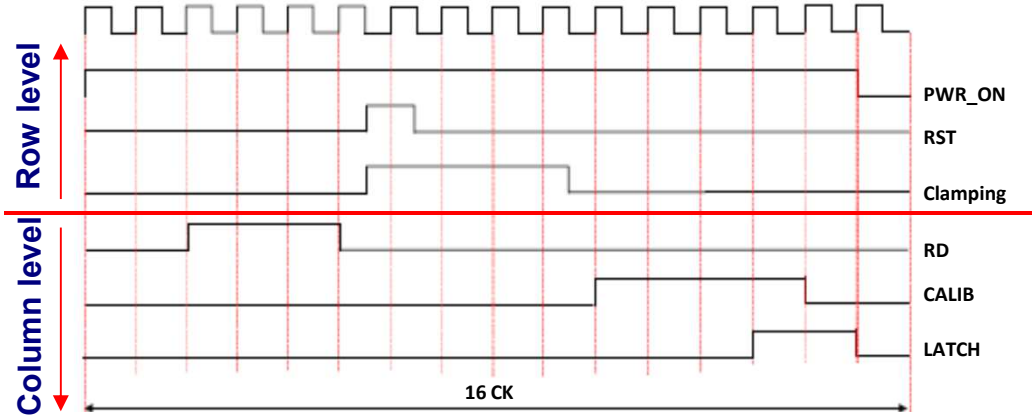
- ***Low Power vs. High Speed***
  - *Power ➔ only the selected rows to be read out are powered ON*
  - *Speed ➔ Pixels belonging 1 row are read out simultaneously*
    - ⋆ *Integration time = frame readout time*

$$t_{int} = \text{(row readout time) x (No. Of rows)}$$

Twin-Well: In Pixel amplification & Signal Processing

- Pixel design:
  - Optimize diode size: charge collection, S/N
  - Amplification in pixel: improve S/N
  - Correlated double sampling (CDS) in 2 levels: pixel, discriminator





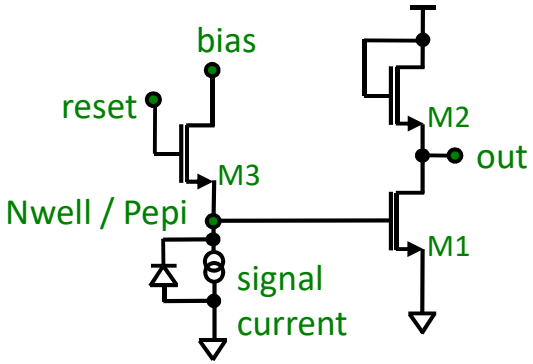
RO: 16 clock cycles per row
CK: 80-160 MHz
RO time: 100-200ns/row depending on the size of pixel array

Digital commands common for 1 row up to 1152 pixels per row

Twin-Well: In Pixel amplification & Signal Processing (2)

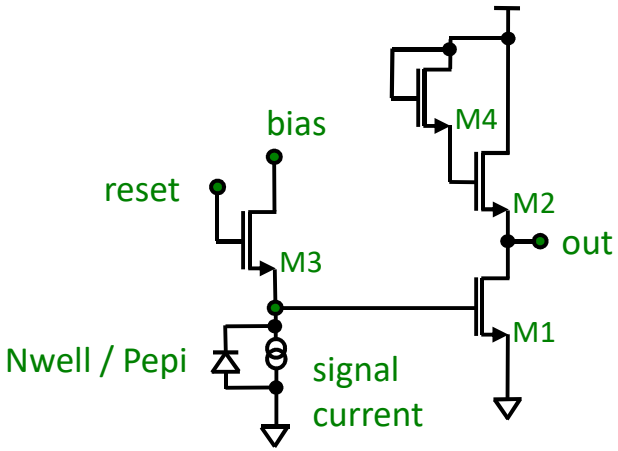
- Common Source (CS) amplification in pixel
  - Only NMOS transistors can be used

1 CS + Reset



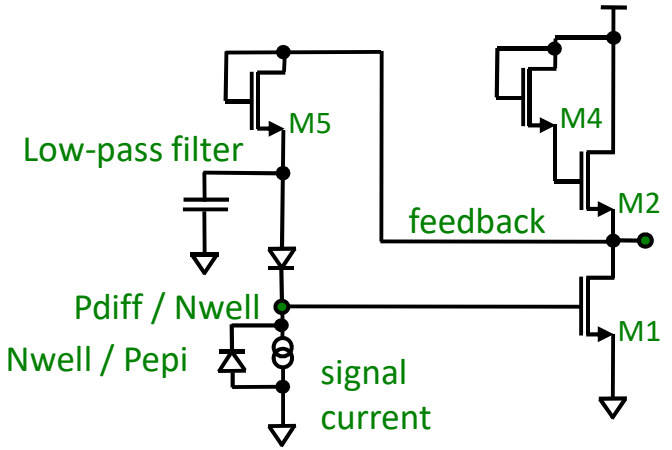
$$Gain = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{(g_{m2}+g_{mb2}+g_{ds1}+g_{ds2})}$$

2 Improved CS + Reset



$$Gain = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{(g_{mb2}+g_{ds1}+g_{ds2})}$$

3 Improved CS + Feedback + Self biased

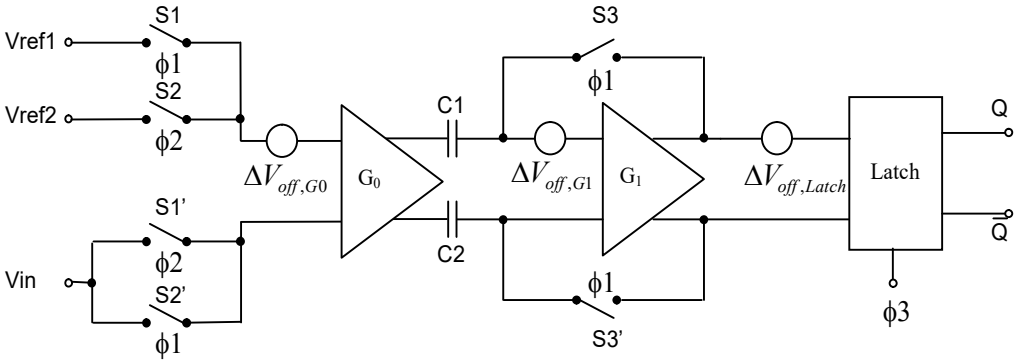


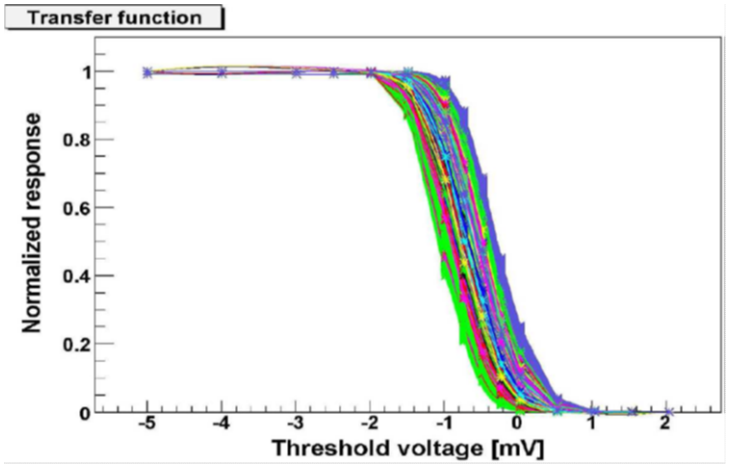
- A negative low frequency feedback was introduced to decrease the gain variations due to process variations

Twin-Well: A/D conversion: Column-level discriminators

- Choice of number of bits depends on the required spatial resolution and on the pixel pitch
  - These applications ➔ 1 bit ➔ discriminator

- Discriminator design considerations:
  - Small input signal ➔ Offset compensated amplifier stage
  - Dim: 16.4 x 430 µm^2
  - Conversion time = row read out time (~200 ns)
  - Consumption ~230 µW

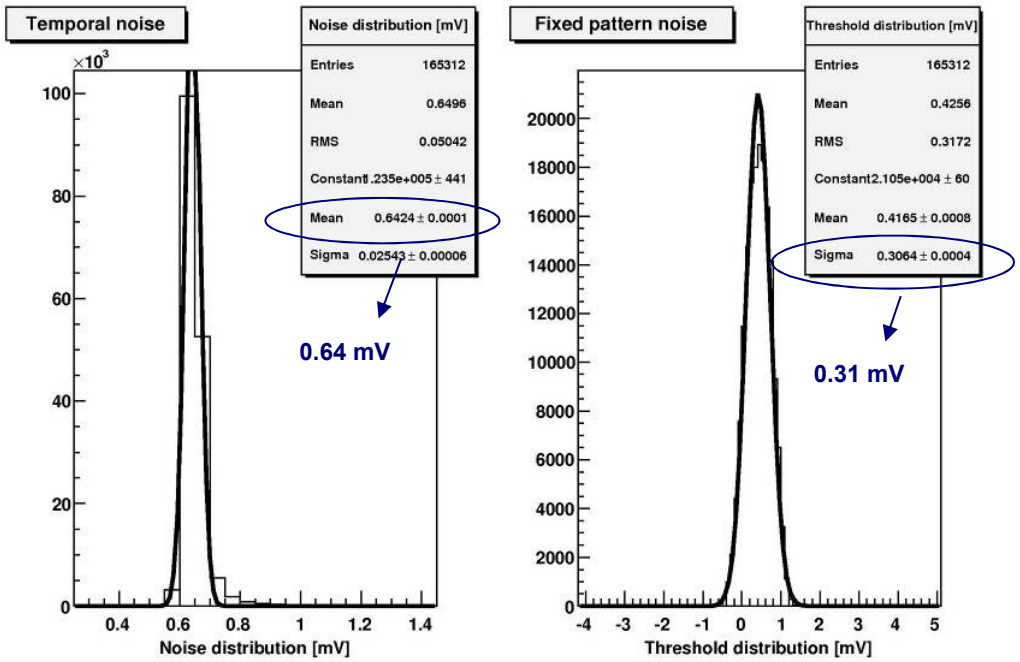




- Measurement results of 1152 column-level discriminators (Mimosa26):
  - Temporal Noise: 0.3-0.40 mV
  - Fixed Pattern Noise (FPN): 0.15 mV

Pixel Array + Discriminated Output Test Results

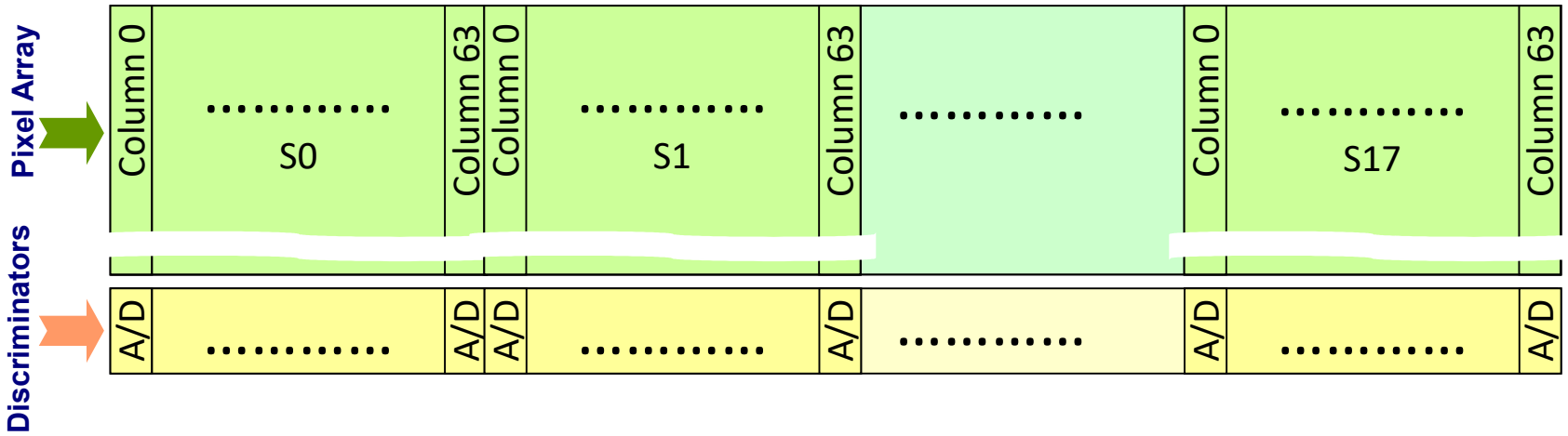
- **Array of 660,000 pixels coupled to 1152 discriminators**



- Typical value of total temporal noise ~ 0.6 - 0.7 mV
- Typical value of total FPN noise ~ 0.3 - 0.4 mV
- N <~12 - 13 e^- ENC

Twin-Well: Readout path: zero suppression + memories

- *Connected to column-level discriminators outputs*
- *Zero suppression is based on row by row sparse data scan readout*



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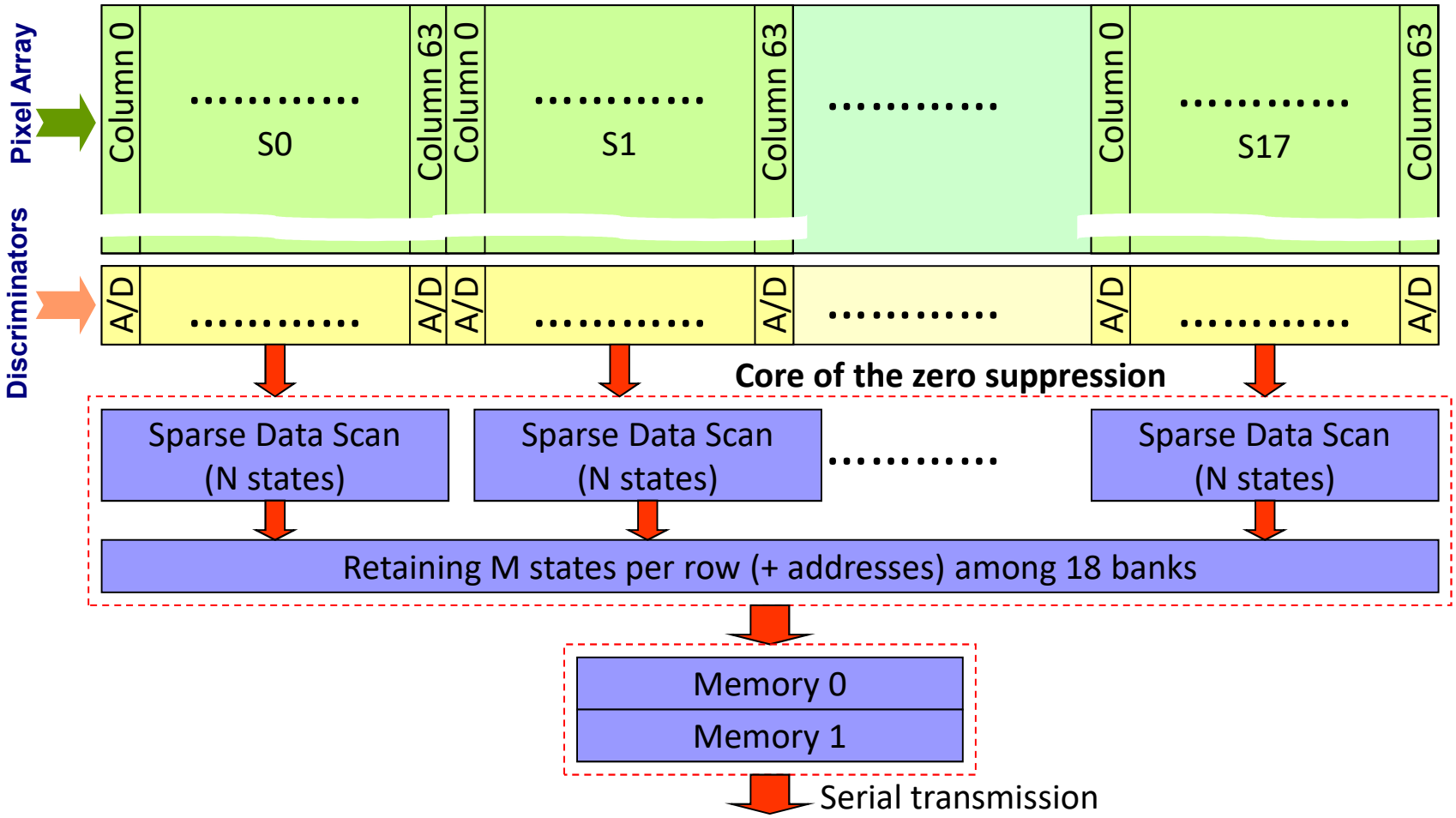
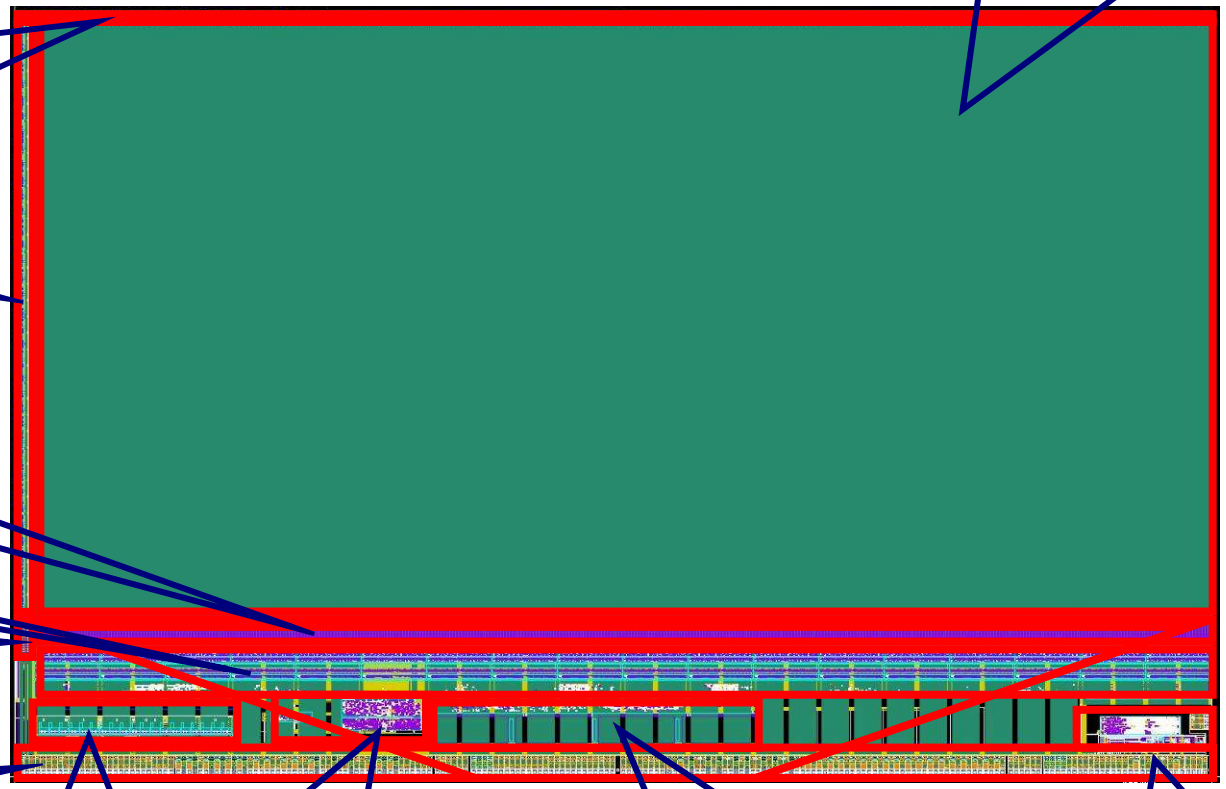


MIMOSA26: 1st MAPS with Integrated Ø

CMOS 0.35 µm OPTO technology
Chip size : 13.7 x 21.5 mm²

Pixel array: 576 x 1152, pitch: 18.4 µm
Active area: ~10.6 x 21.2 mm²
In each pixel:
- Amplification
- CDS (Correlated Double Sampling)

Testability: several test points implemented all along readout path
- Pixels out (analogue)
- Discriminators
- Zero suppression
- Data transmission



Row sequencer
Width: ~350 µm

1152 column-level discriminators
- offset compensated high gain preamplifier followed by latch

Zero suppression logic

Reference Voltages
Buffering for 1152 discriminators

I/O Pads
Power supply Pads
Circuit control Pads
LVDS Tx & Rx

Current Ref.
Bias DACs

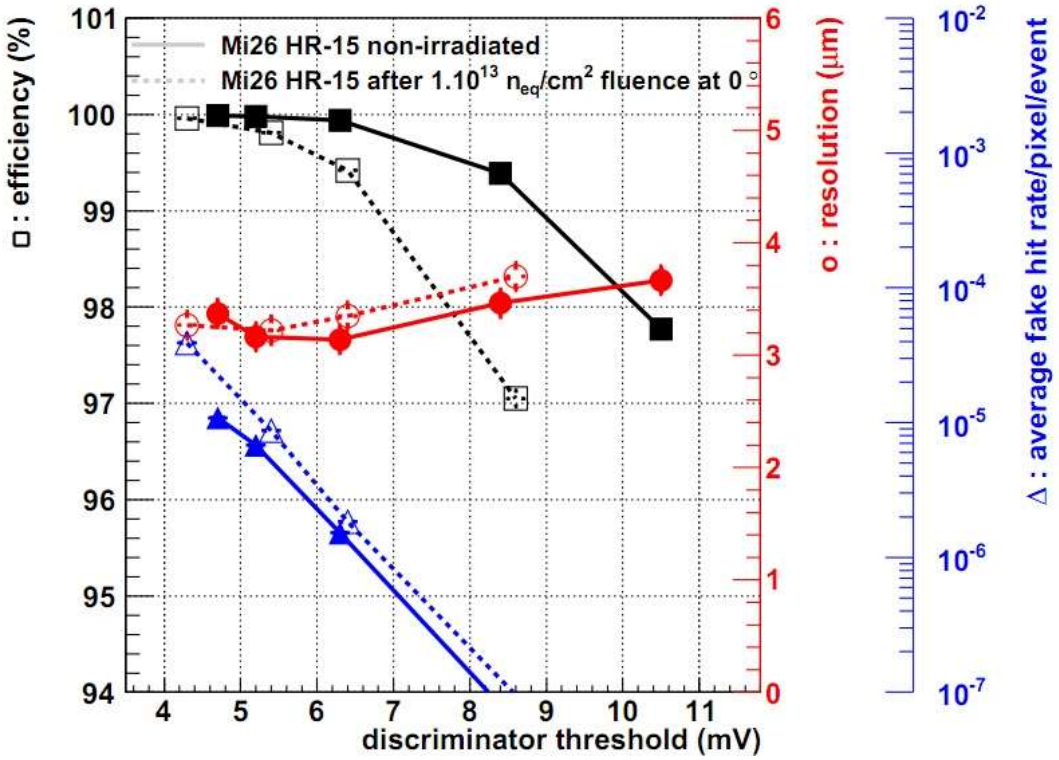
Readout controller
JTAG controller

Memory management
Memory IP blocks

PLL, 8b/10b optional

MIMOSA26 with high resistivity EPI layer

- Beam test at CERN SPS (120 GeV pions)
  - Test conditions: 35 °C temperature



- Main features:
  - In-pixel amplification & CDS, comparator for each column
  - data sparsification
  - pitch: 18.4 µm~ 0.7 million pixels
  - read-out time 110 µs nominal (80 µs achieved)

Examples of Pixel Sensor Architectures
Quadruple-well circuits

ALICE Inner Tracking System Upgrade Objectives

- Improve impact parameter resolution by a factor ~3
  - Get closer to IP (radius of first layer): 39 mm -> 23 mm
  - Reduce pixel size: currently 50 x 425 μm^2 -> O(30 x 30 μm^2)
  - Reduce x/X_0/layer from ~1.14% -> ~0.3% (inner layers)

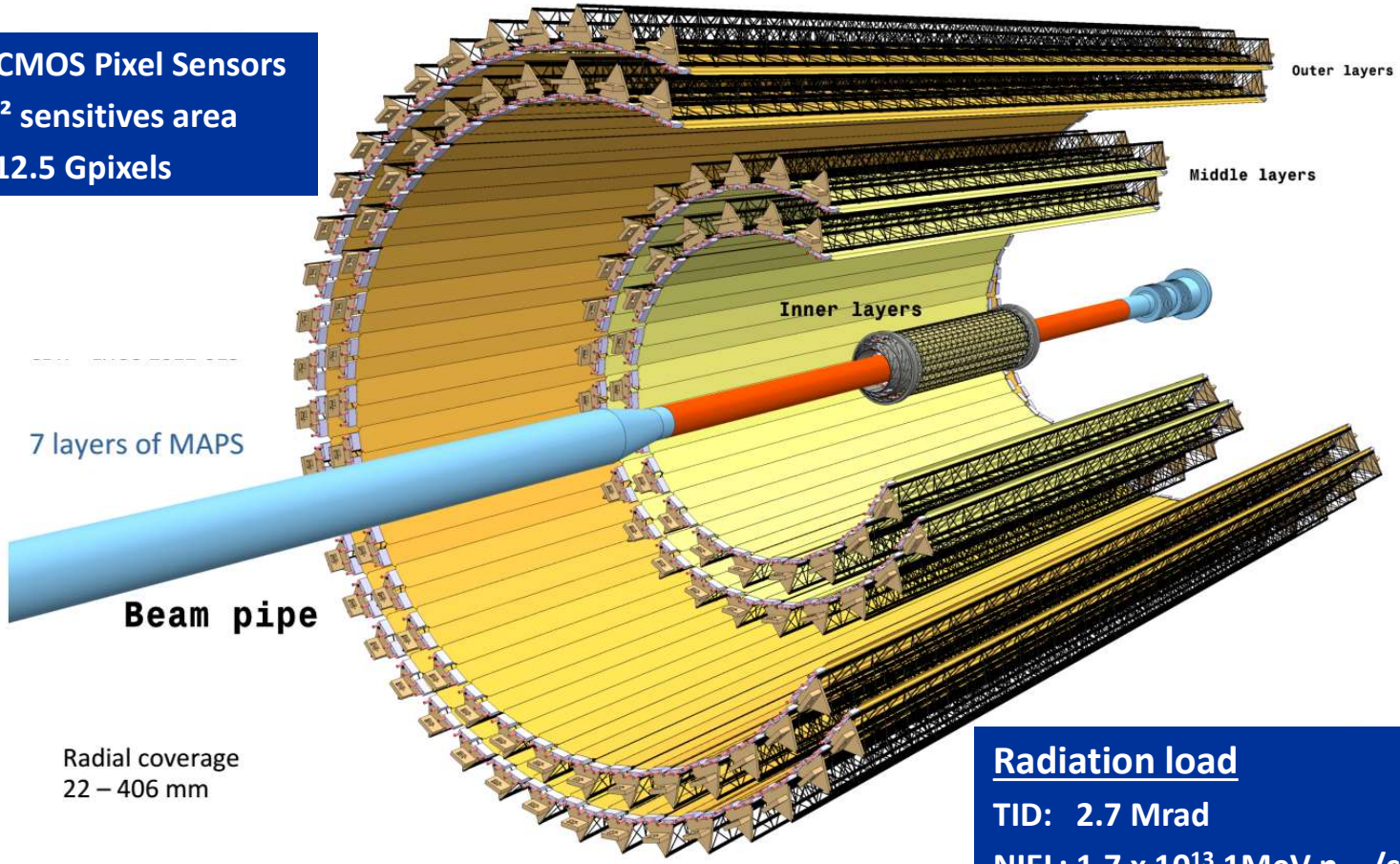
$$\sigma_{ip} = a \oplus \frac{b}{p(GeV) sin^{3/2}\theta} \ (\mu m)$$

- Better tracking efficiency and p_T resolution at low p_T
  - Finer granularity: from 6 to 7 layers and all layers with pixels
- Fast readout
  - Readout Pb-Pbinteractions at 100 kHz
  - Readout pp interactions at >200 kHz (current ITS limited at 1 kHz)
- Design for fast removal and insertion
  - Maintenance during yearly shutdown

Installation of the new detector during LHC Long Shutdown 2 (2019-2020)

New ALICE ITS Layout

~24000 CMOS Pixel Sensors
10 m² sensitives area
12.5 Gpixels



Radiation load
TID: 2.7 Mrad
NIEL: 1.7 x 10^{13} 1MeV n_{eq} /cm²

Barrel geometry

3 Inner Barrel layer (IB) 0.3% X_o
4 Outer Barrel layer (OB) 1% X_o

Coverage

23 mm < r < 400 mm, $|\eta| < 1.22$
Layers z-length: 27 – 150 cm

ITS Chip General Requirements

Parameter	Inner Barrel	Outer Barrel
Chip size (mm x mm)	15 x 30	
Chip thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	> 99%	
Fake hit rate	$< 10^{-5}$ evt^{-1} pixel^{-1} (ALPIDE $<< 10^{-5}$)	
Integration time (μs)	< 30 (< 10)	
Power density (mW/cm^2)	< 300 (~35)	< 100 (~20)
TID radiation hardness (krad) (**)	2700	100
NIEL radiation hardness (1 MeV n_{eq}/cm^2) (**)	1.7×10^{13}	1.7×10^{12}
Readout rate, Pb-Pb interactions (kHz)	100	
Hit Density, Pb-Pb interactions (cm^{-2})	18.6	2.8

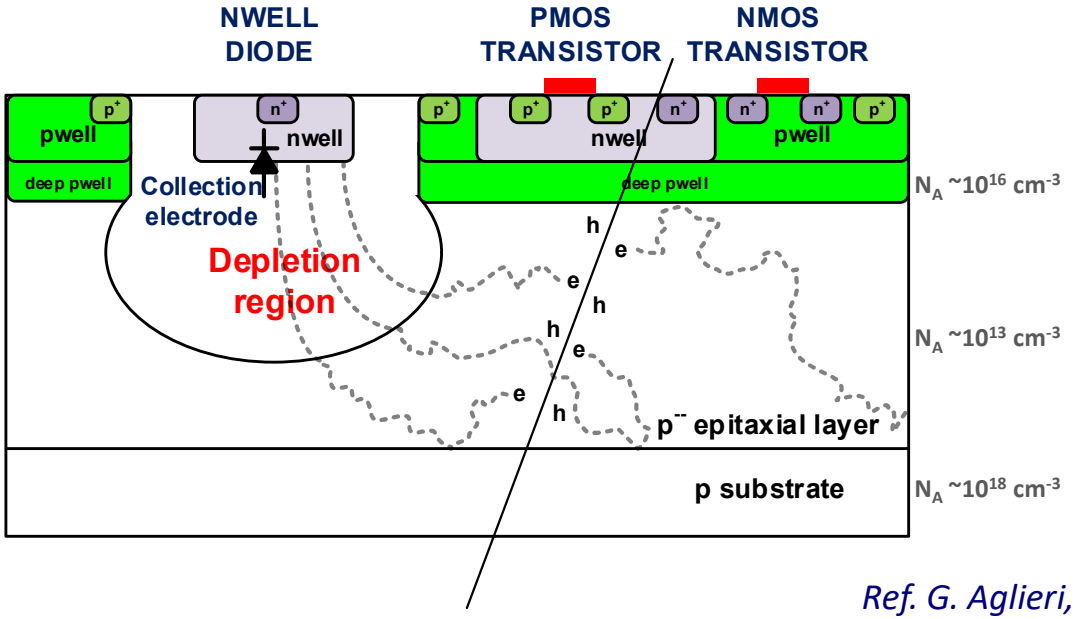
(*) In color: ALPIDE performance figure where above requirements

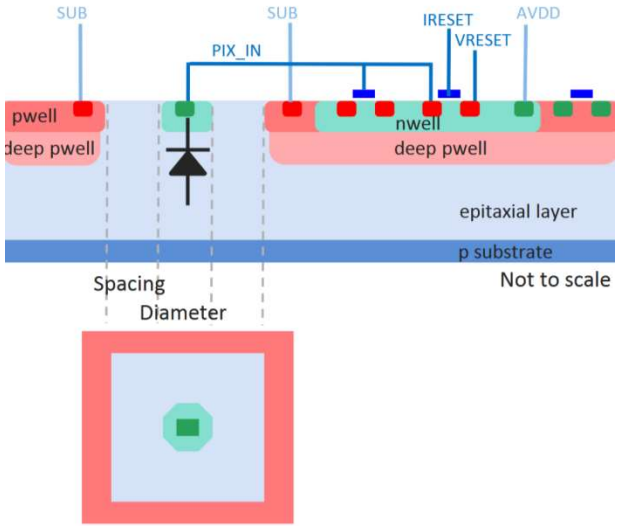
(**) 10x radiation load integrated over approved program (~ 6 years of operation)

Ref. G. Aglieri VCI2016

Small Electrodes: ALPIDE Technology

Pixel Sensor CMOS 180 nm Imaging Process (TowerJazz):3 nm thin gate oxide, 6 metal layers

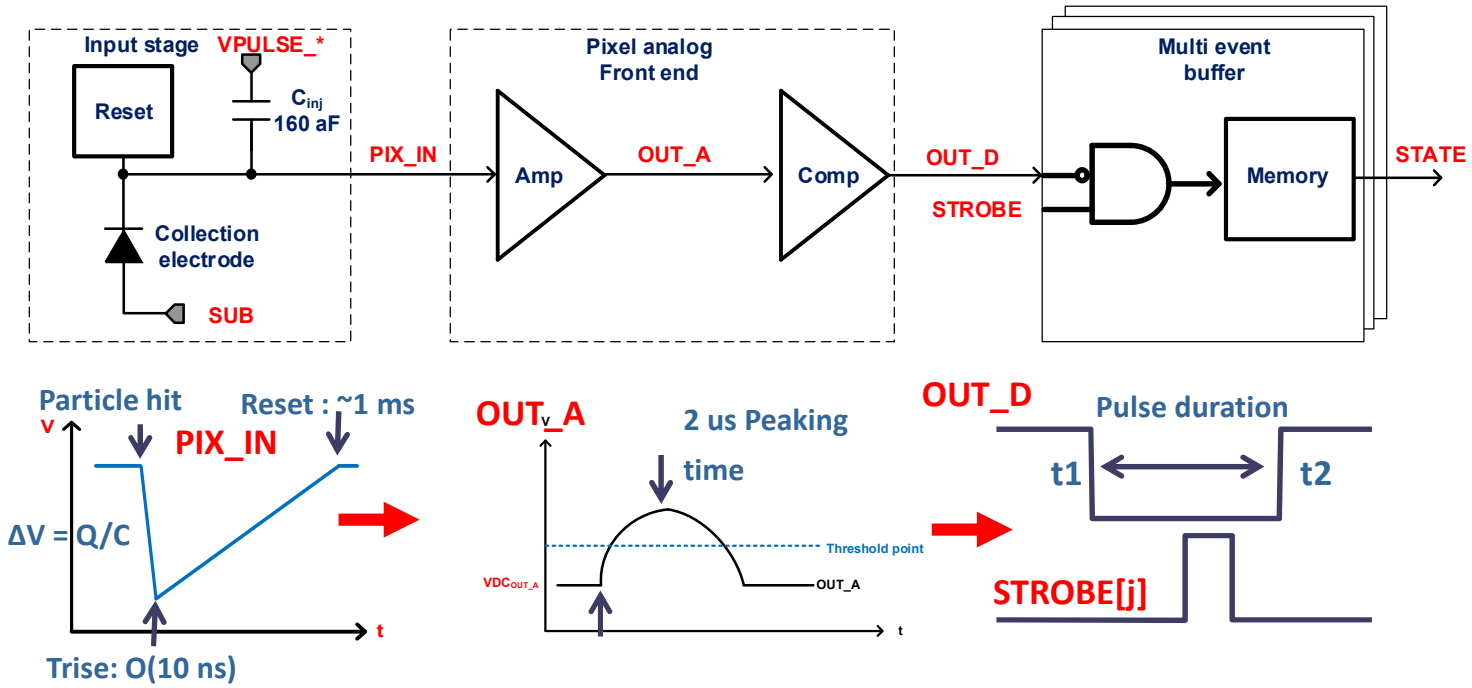




Ref. G. Aglieri, 2016 VCI

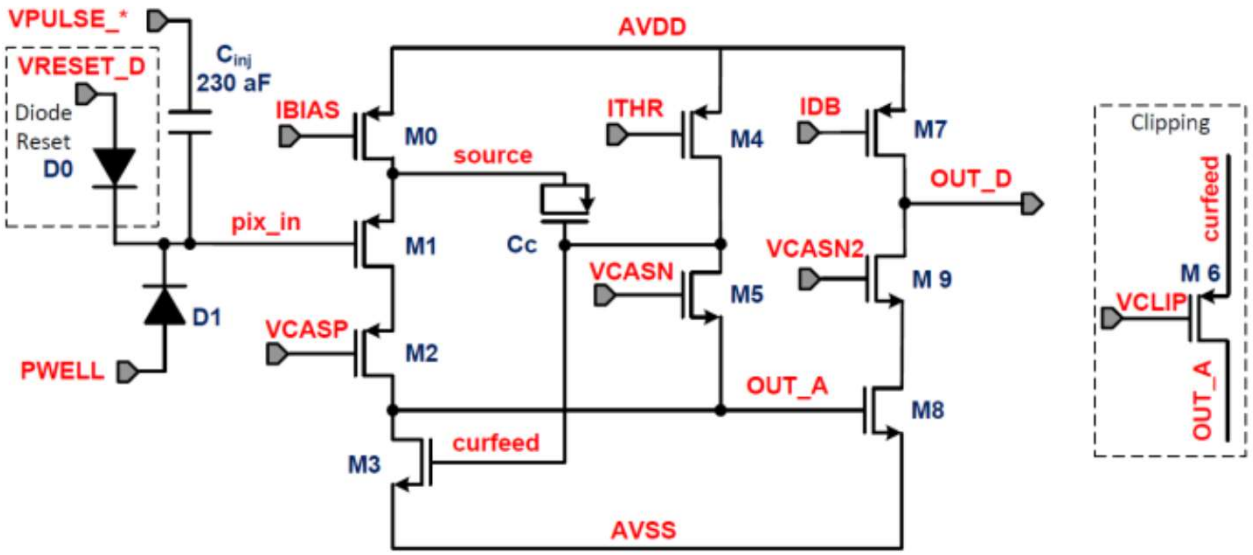
- Small collection electrodes:
  - High-resistivity (> 1kΩ cm) p-type epitaxial layer (18 - 30 µm) on p-type substrate
  - Deep Pwell shielding Nwell allowing PMOS transistors (full CMOS within active area)
  - **Reverse bias** can be applied to the substrate to increase the depletion volume around the Nwell collection diode
  - Higher gain and faster response due to smaller capacitance (<5 fF) and higher Q/C
    - Potentially lower power consumption

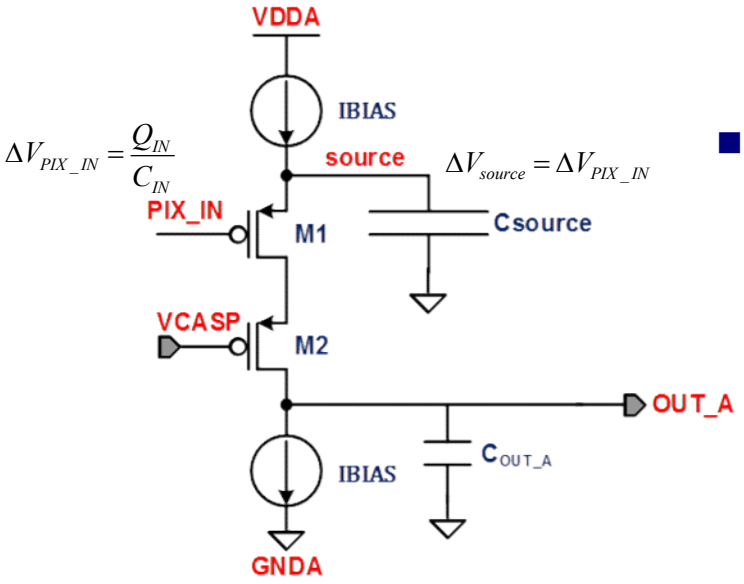
ALPIDE : In-pixel Front-end Electronics



- Analog front-end and discriminator continuously active
  - Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel
  - The front-end acts as analogue delay line
  - Test pulse charge injection circuitry
  - Global threshold for discrimination -> binary pulse OUT_D
- Digital pixel circuitry with three hit storage registers (multi event buffer)
  - Global shutter (STROBE) latches the discriminated hits in next available register
  - In-Pixel masking logic

ALPIDE: Pixel Front-end Circuit (1)





$\Delta V_{PIX\_IN} = \frac{Q_{IN}}{C_{IN}}$ $\Delta V_{source} = \Delta V_{PIX\_IN}$

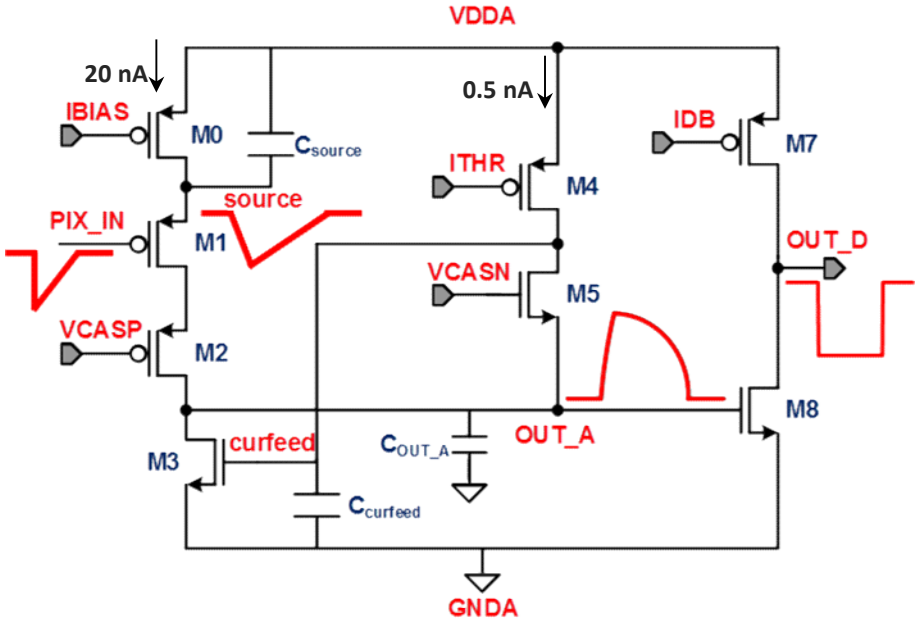
- Transfer of charge to generate voltage gain
  - Signal charge creates negative voltage step ΔVPIX_IN at the input PIX_IN
  - M1 (S Follower) and forces its source to follow its gate
  - This causes transfer of charge Q_{source} from C_{source} to C_{OUT_A}

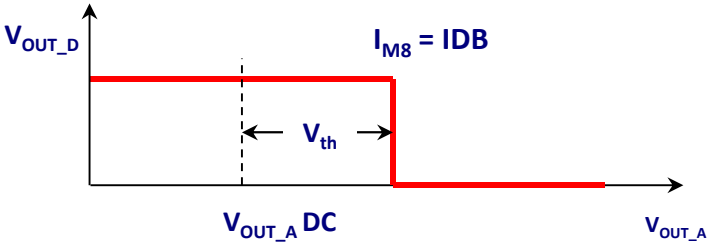
$$\Delta V_{OUT\_A} \approx \frac{Q_{source}}{C_{OUT\_A}} = \frac{C_{source} \times \Delta V_{PIX\_IN}}{C_{OUT\_A}} = \frac{C_{source}}{C_{OUT\_A}} \Delta V_{PIX\_IN} = \frac{C_{source}}{C_{OUT\_A}} \frac{Q_{IN}}{C_{IN}}$$

  - Voltage gain is obtained if $C_{source} >> C_{OUT\_A}$

Ref. D. Kim, 2016 JINST 11 C02042

ALPIDE: Pixel Front-end Circuit (2)

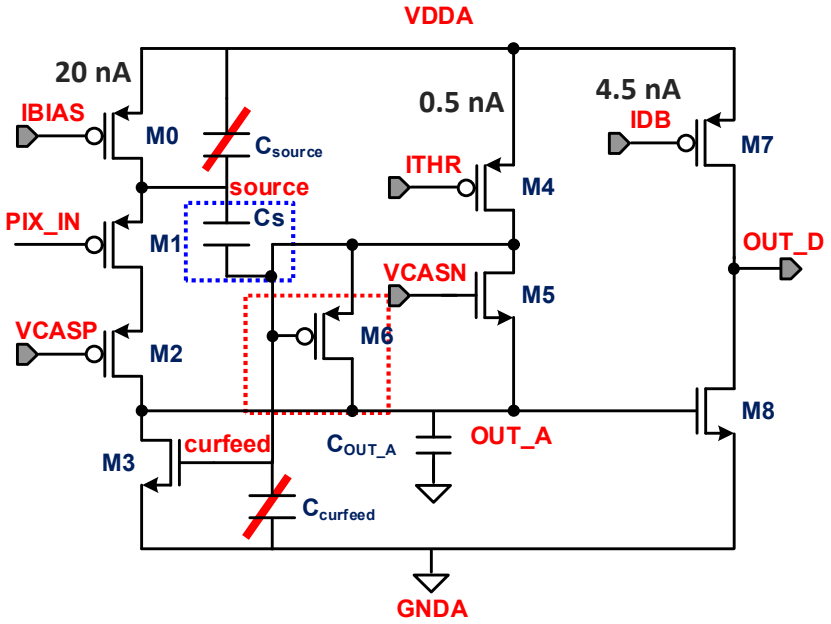


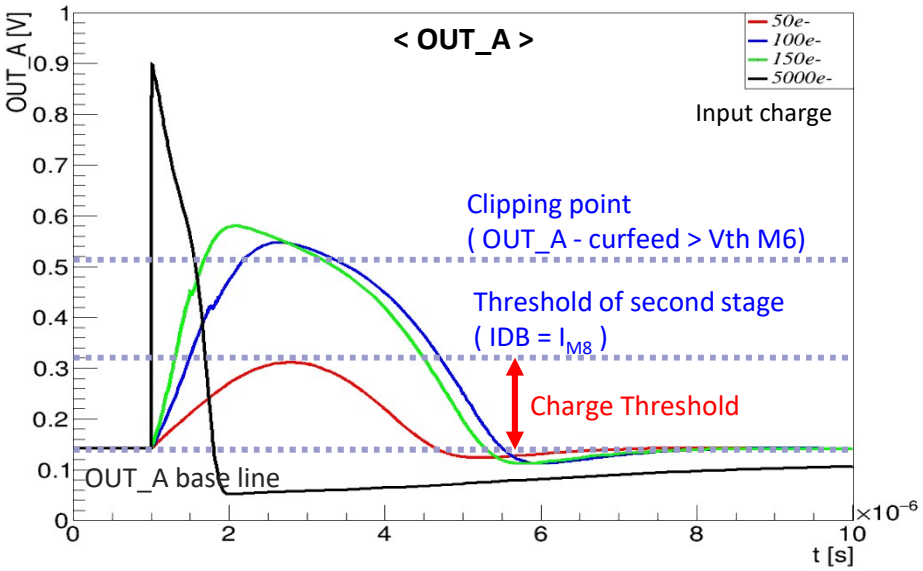


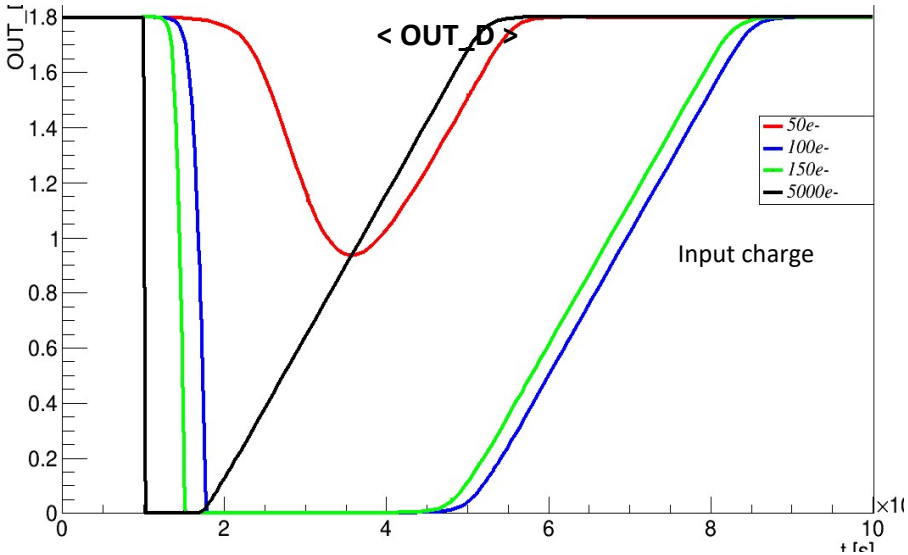
- M4, M5 ➔ low frequency feedback. ($V_{curfeed}$) is adjusted for M3 to to absorb IBIAS+ITHR
- ITHR, VCASN define V_{OUT_A} DC level and return to the steady state after a hit
- Baseline V_{OUT_A} is adjusted below the point where I_{M8} = IDB
- $V_{Threshold}$ is the difference between V_{OUT_A} baseline and the point where I_{M8} = IDB
- If V_{OUT_A} excursion is sufficiently large for i_{M8} > IDB ➔ pulldown the output$_{dig.}$ OUT_D

Ref. D. Kim, 2016 JINST 11 C02042

ALPIDE: Pixel Front-end Circuit (3)







- Combined capa. to reduce layout area
  - C_{source} and $C_{curfeed}$ ➔ C_s
- Charge threshold parameters
  - OUT_A baseline value : ITHR,VCASN
  - Threshold of second stage : IDB
- M6 is used to clip large signals and force OUT_A to quickly return to its DC value
- Keeping C_{OUT_A} << C_{source}

Ref. D. Kim, 2016 JINST 11 C02042

ALPIDE: Pixel Front-end Circuit Optimisations (1)

Q/C

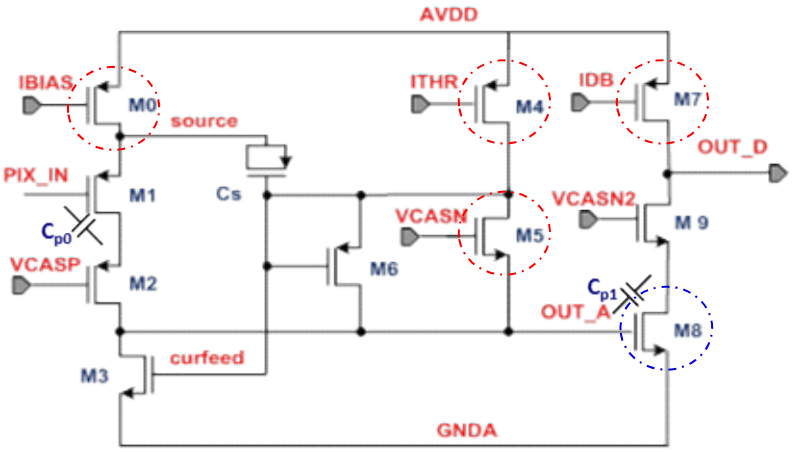
Input transistor optimisation

Charge threshold uniformity:

- Identify the influence of mismatch of each MOS
  - Monte-Carlo simulation
- Layout dimension vs. devices sizes

$$rms = \frac{rms_0}{\sqrt{Area}}$$

  - M0, M4, M5, M7 sizes are limited by the layout
  - M8 trade-off between large area for low mismatch and small area to reduce C_{out_A}

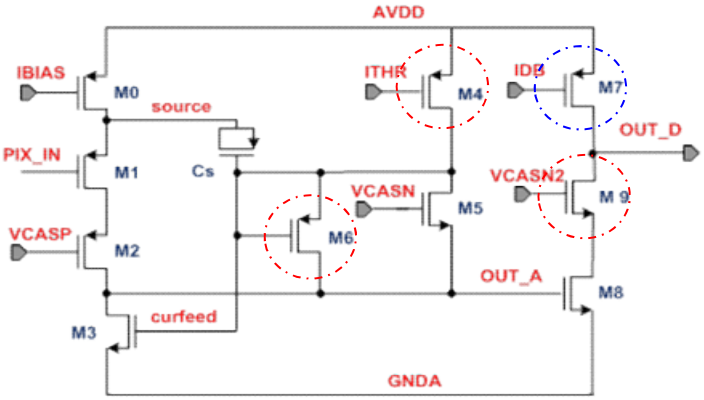


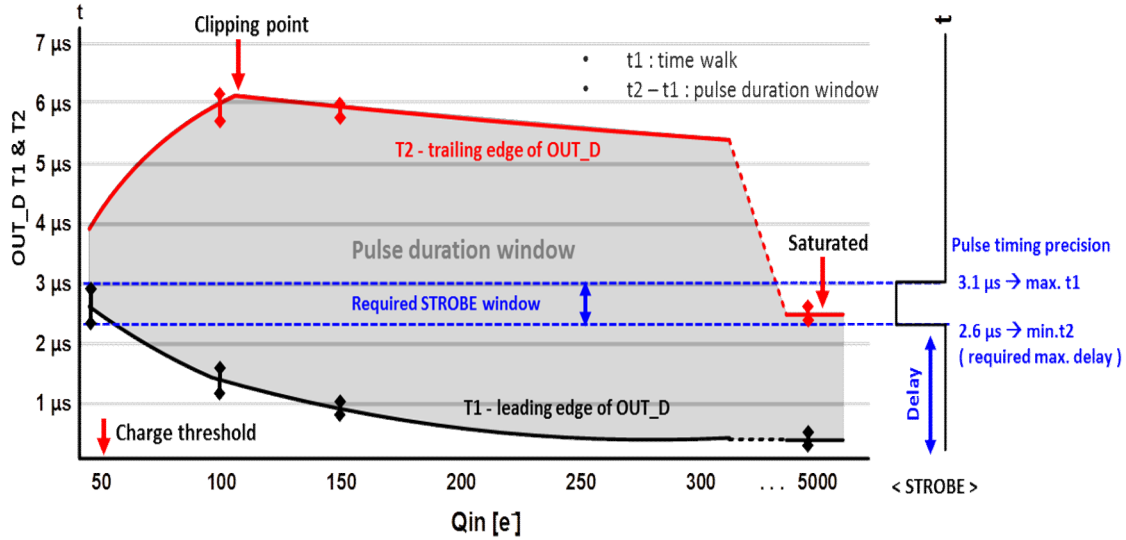
- Parasitic components
  - C_{p1} impacts threshold, M9 reduces Miller effect
  - C_{p0} impacts input capacitor (noise & gain), M2 reduces Miller effect

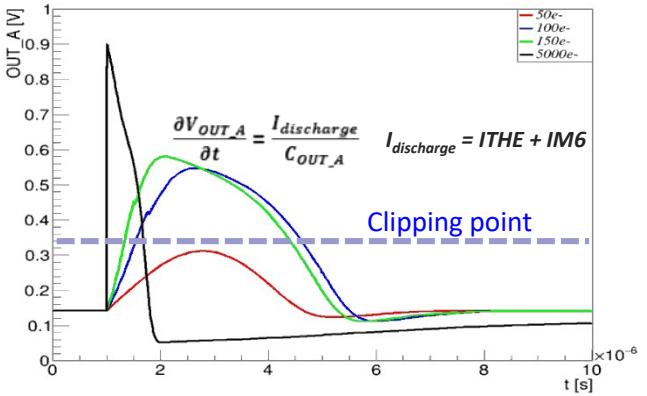
ALPIDE: Pixel Front-end Circuit Optimisations (2)

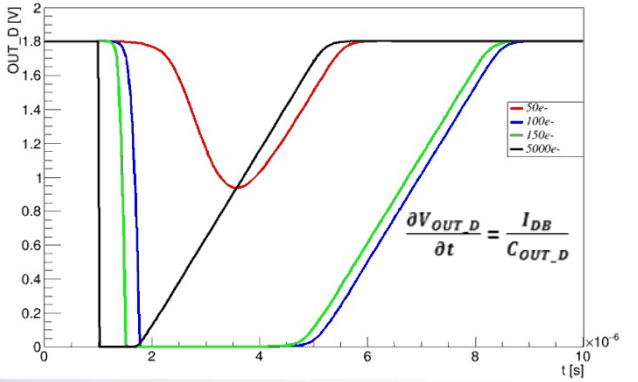
Time response uniformity:

- Trigger mode: important because the front end is used as analog memory
  - OUT_A
    - ★ Larger M4 to reduce ITHR variation
    - ★ Introducing M9 to reduce C_{OUT_A} variation
    - ★ Longer M6 to reduce the clipping point variation
  - OUT_D
    - ★ Longer M7 to reduce IDB variation





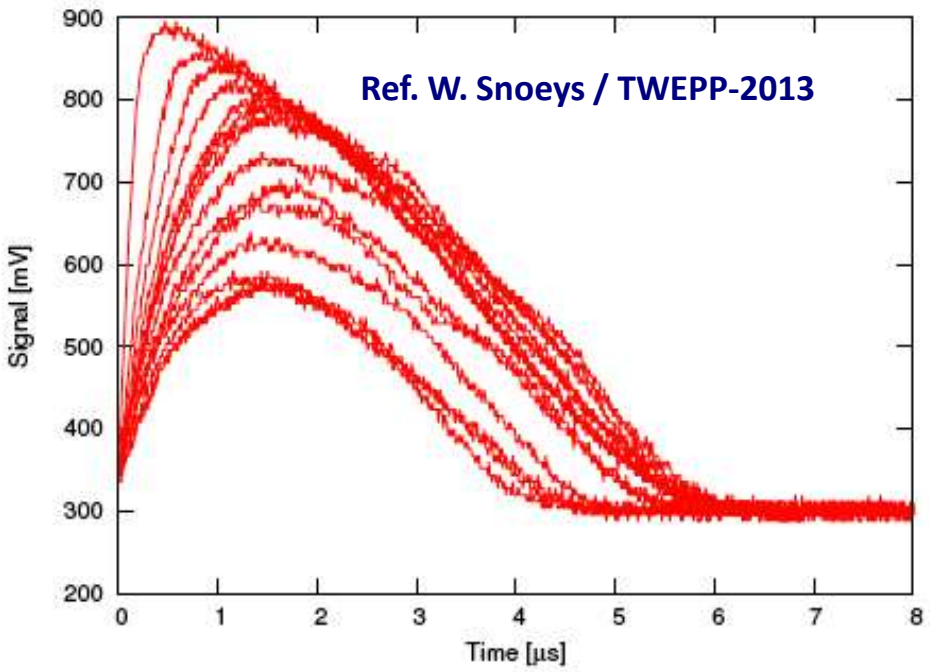


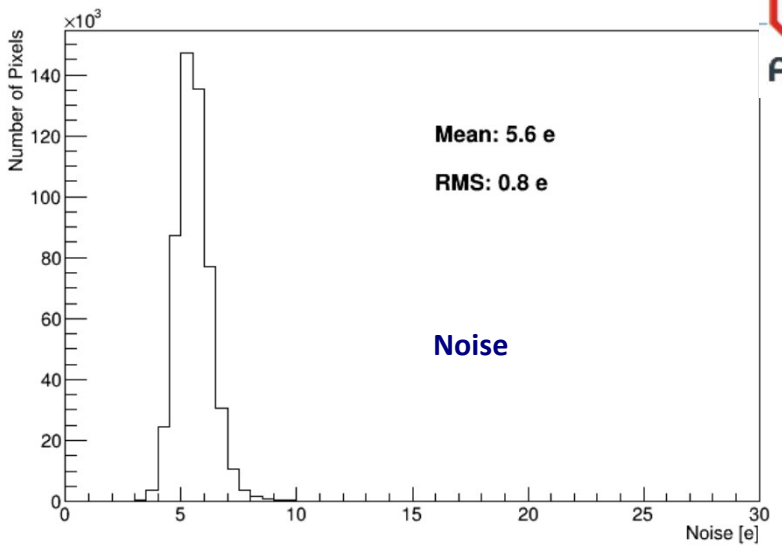


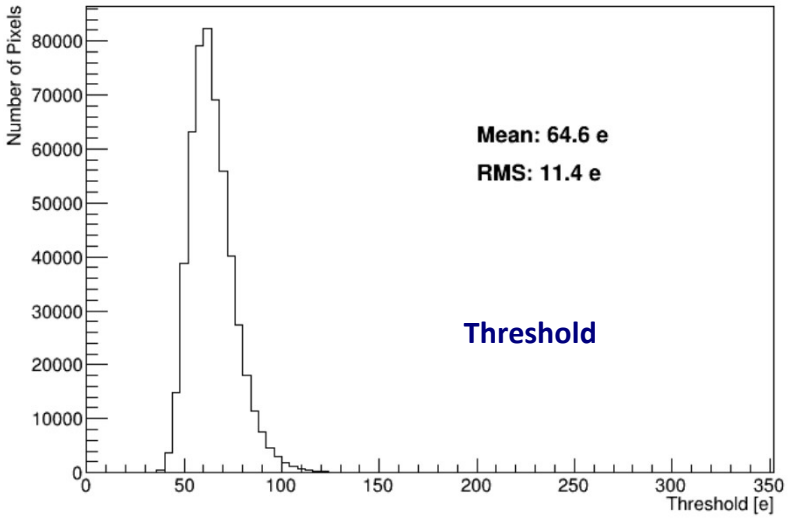
Ref. D. Kim, 2016 JINST 11 C02042

Analogue Response & Noise and Threshold Distributions

Analog output of one pixel under ^{55}Fe



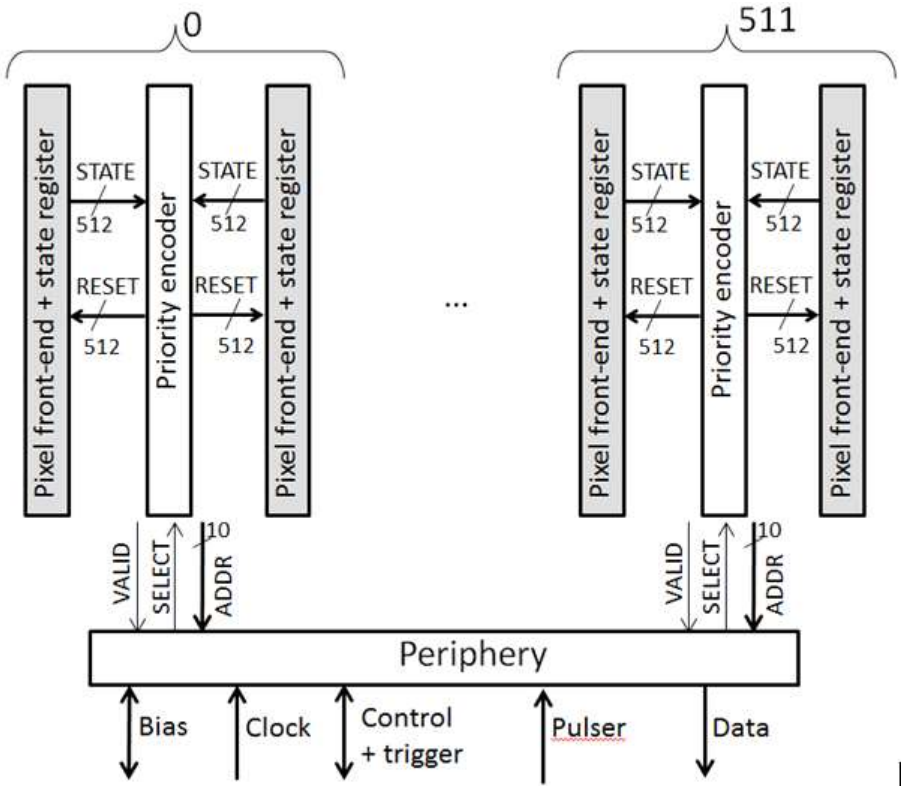




- Minimum detectable charges: ~130 e^-
- Threshold spread (FPN): 11.4 e^-
- Thermal noise: 5.6 e^-

Ref. W. Snoeys, HST 2017

ALPIDE: Matrix Readout



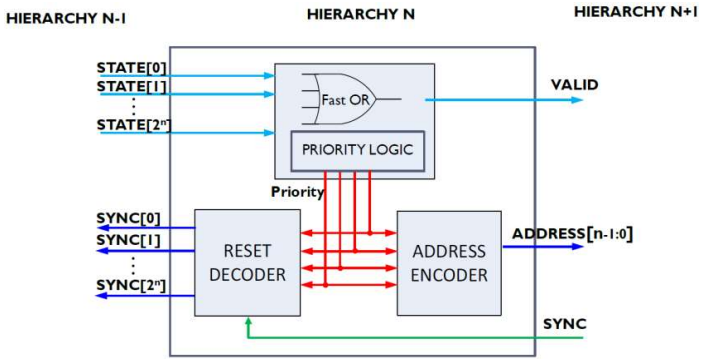
- Data driven readout: the Priority Encoder sequentially provides the addresses of all hit pixels in a double column
  - Combinatorial digital circuit steered by peripheral sequential circuits during readout of a frame
  - No free running clock over matrix. No activity if there are no hits
  - Energy per hit: E_{hit} ~= 100 pJ → ~3 mW for nominal occupancy and readout rate
  - Buffering and distribution of global signals (STROBE, MEMSEL, PIXEL RESET)

Column-Level Data Driven Readout

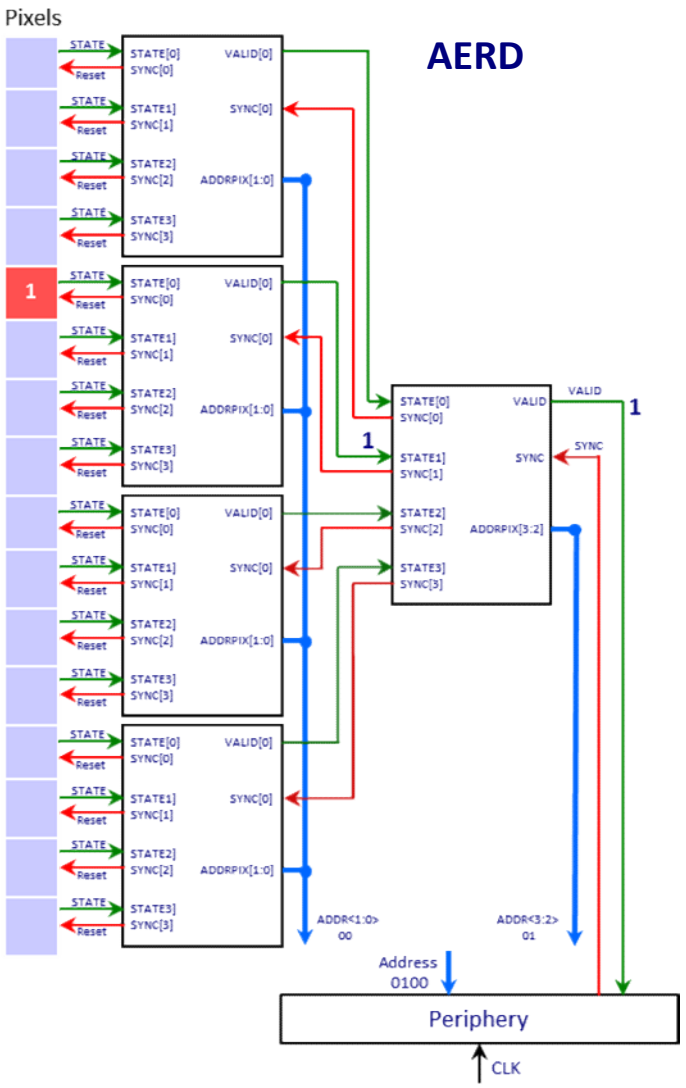
- *Data driven readout is based on an arbiter tree scheme with hierarchical address encoders and reset decoders*
- *An example of a single bit 4 to 2 encoder*

S0	S1	S2	S3	A1	A0	Valid
1	X	X	X	0	0	1
0	1	X	X	0	1	1
0	0	1	X	1	0	1
0	0	0	1	1	1	1
0	0	0	0	X	X	0

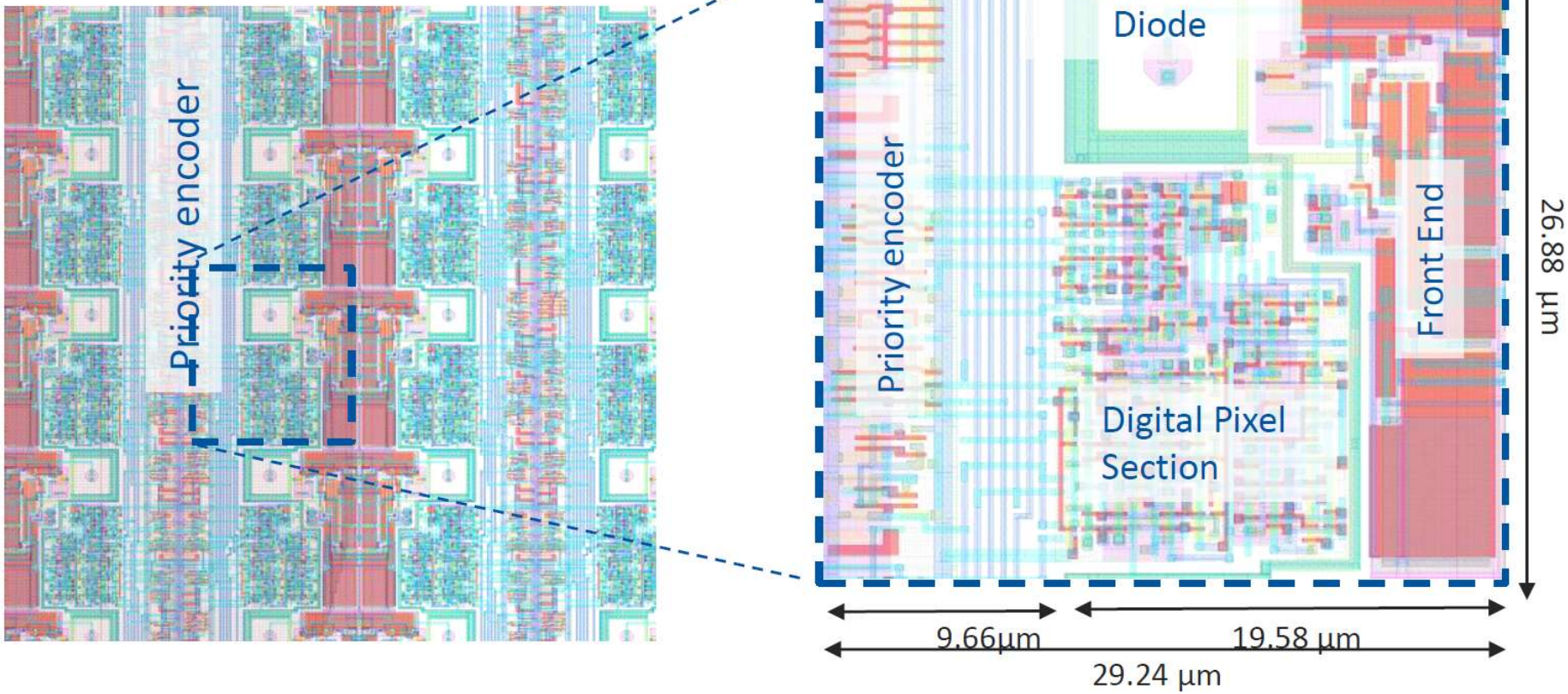
- *Basic logic contains three units:*
  - *Fast OR ➔ VALID*
  - *Address Encoder*
  - *Reset Decoder*



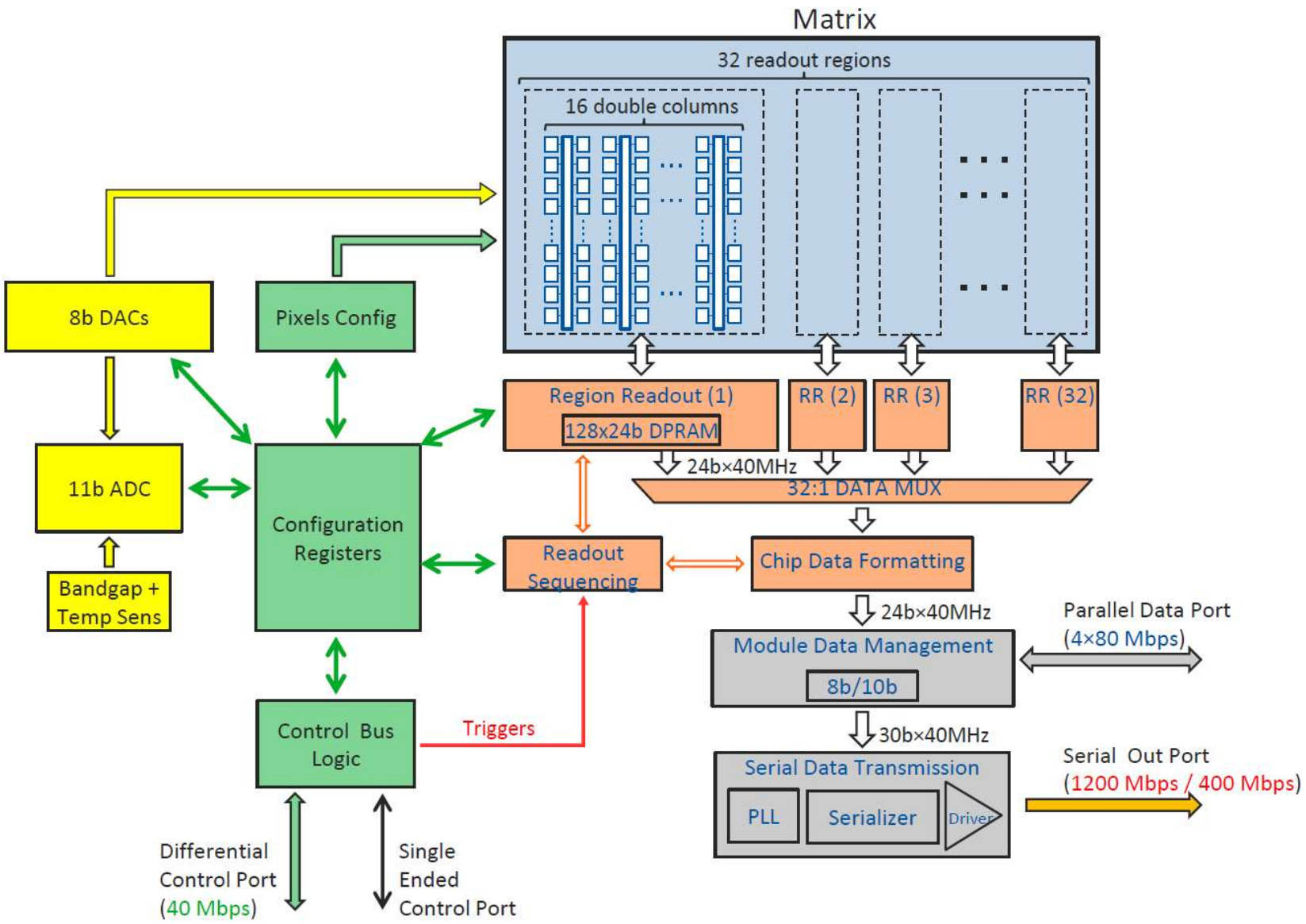
- *Repeated tree structure + buffering*



ALPIDE Pixel Layout

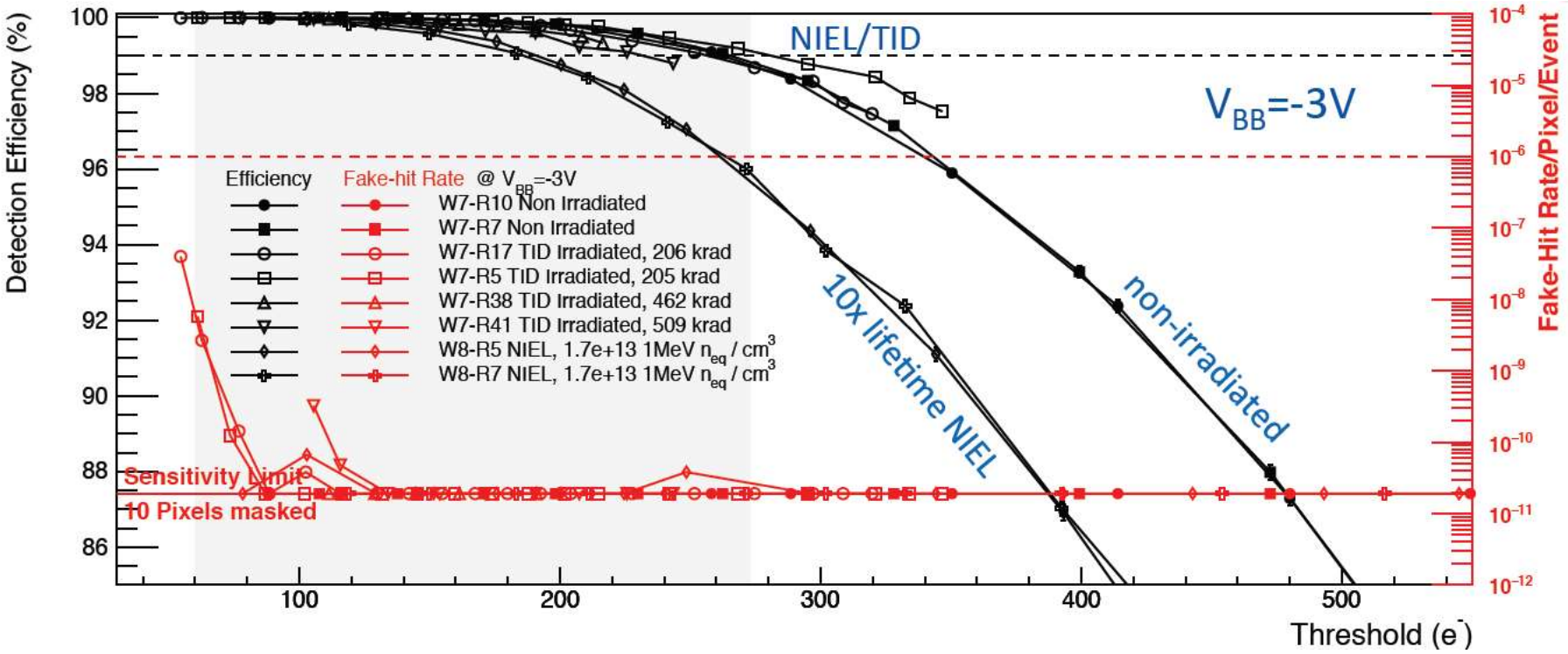


ALPIDE Architecture



Detection Efficiency and Fake Hit Rate

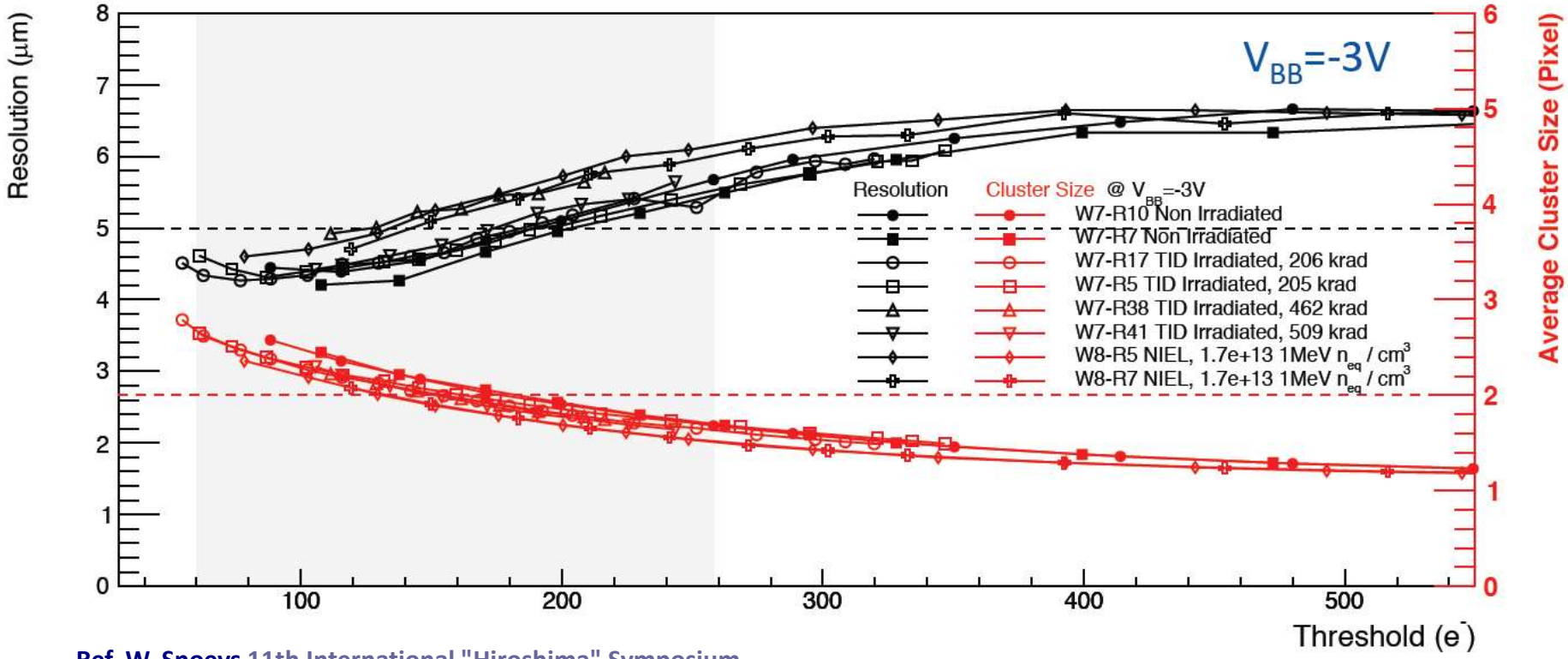
- Large operational margin with only 10 masked pixels (0.002%)
  - $\varepsilon_{det} > 99\%$ @ $\lambda_{fake} << 10^{-5}$ / event/pixel
- Chip-to-chip fluctuations negligible
- Sufficient operational margin after 10x lifetime NIEL dose



Ref. W. Snoeys 11th International "Hiroshima" Symposium

Position resolution and cluster size

- Chip-to-chip fluctuations negligible
- Non-irradiated and TID/NIEL chips show similar performance
- Resolution of about 6 µm at a threshold of 300 electrons
- Sufficient operational margin even after 10x lifetime NIEL dose

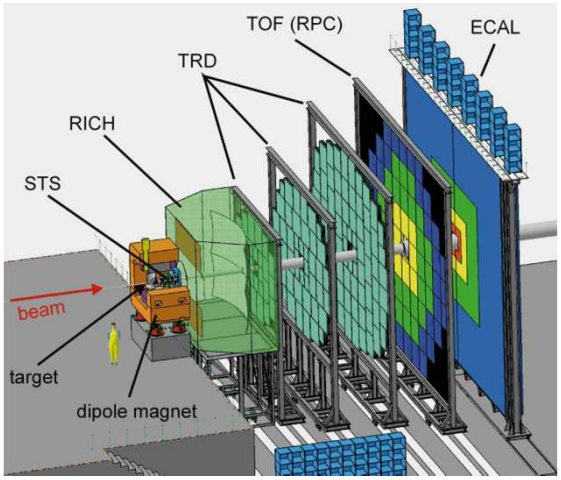


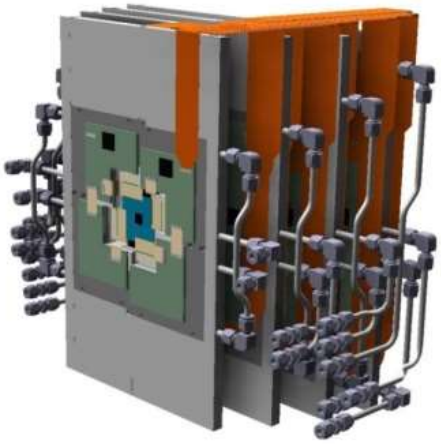
Ref. W. Snoeys 11th International "Hiroshima" Symposium

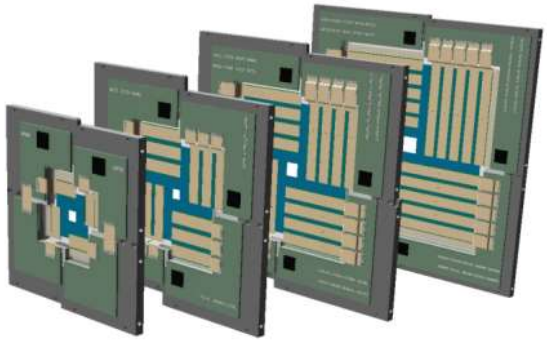
MIMOSIS

CBM-MVD required performance

- Improve secondary vertex resolution
- Low material budget (few 0.1% X0)
- Host highly granular silicon pixel sensors featuring
  - Fast read-out: <~10 µs
  - Excellent spatial resolution: ~5 µm
  - Robustness to radiation environment
    - ⋆ TID: 3 Mrad @ -20 °C & 1 Mrad @ + 30 °C
    - ⋆ NIEL: 3 x 10^{13} n_{eq}/cm² @ -20 °C & 1 x 10^{13} n_{eq}/cm² @ +30 °C
  - Hit rate capability (most exposed 4x4 mm²)
    - ⋆ Average: ~1.5 x 10^5/mm²/s
    - ⋆ Peak: ~7 x 10^5/mm²/s
  - Power consumption
    - ⋆ Station 2&3: <200 mW/cm²
    - ⋆ Station 0&1: <300 mW/cm²
  - Date rate capability:
    - ⋆ Average: ~160 Mbits/cm²/s
    - ⋆ Peak: ~1.6 Gbits/cm²/s

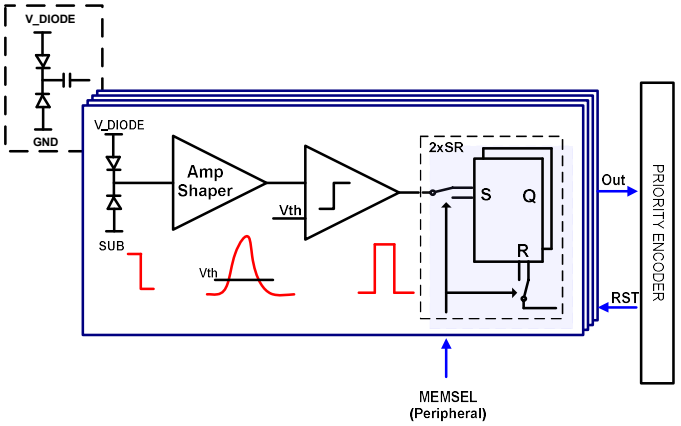


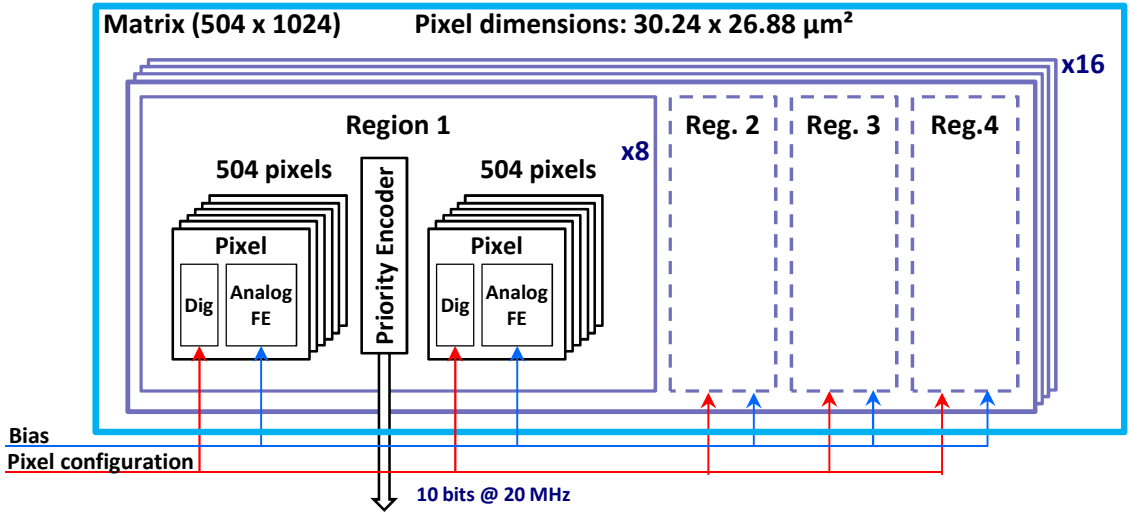




MVD detector

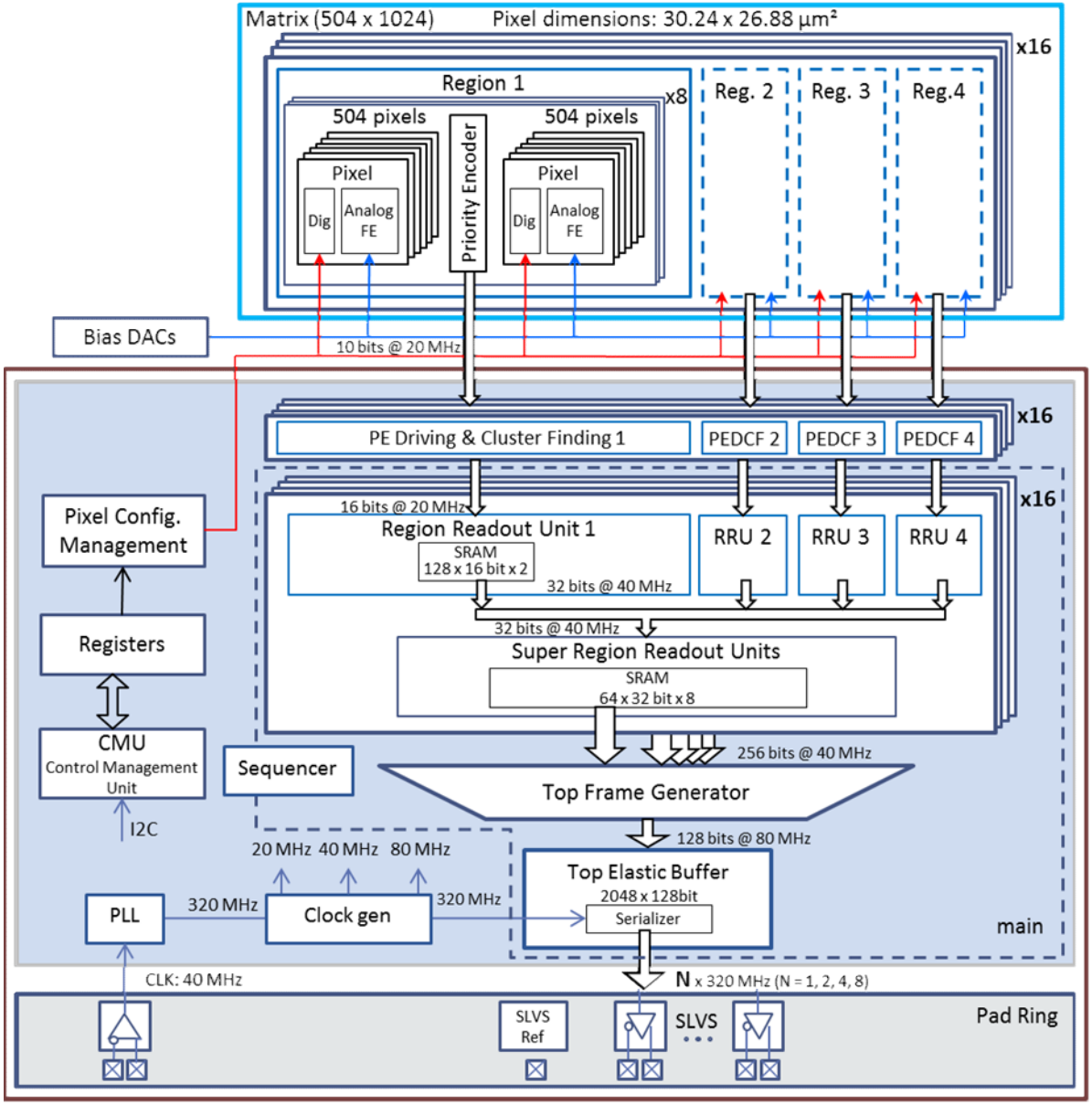
Pixel Array

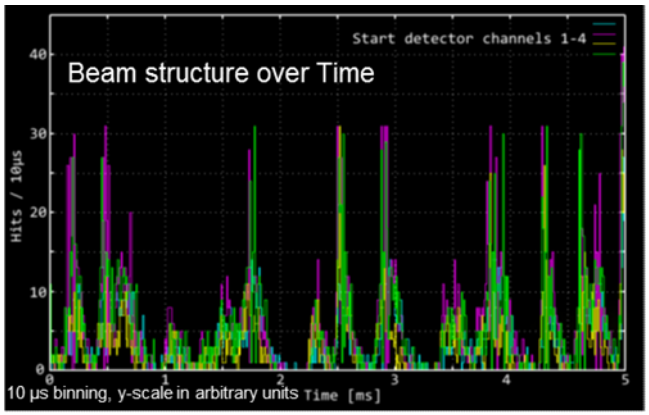


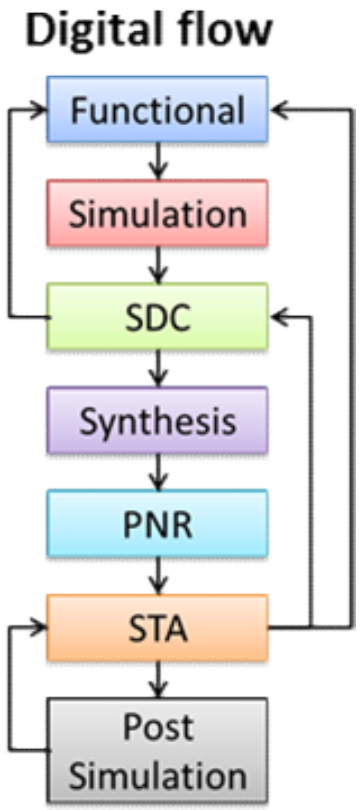


- Every pixel contains: a sensing element, a preamplifier/shaper, a discriminator, 2 digital buffers & a part of data driven readout encoder
- Priority encoder: 1 encoder per double column (2 x 504 pixels)
  - 504 rows chosen to allow including header & frame counter inside data within 16 bit words
- 1 region has 8 double columns, 64 regions are running in parallel
  - Increasing the ability to handle the higher event rate. The number of regions depends on the values of the peak hit rate, the probability and the Priority Encoder readout speed
- 8 Priority Encoders in a region are read-out in serial @ 20 MHz
- Readout frame per frame in 5 µs ➔ pipeline mode

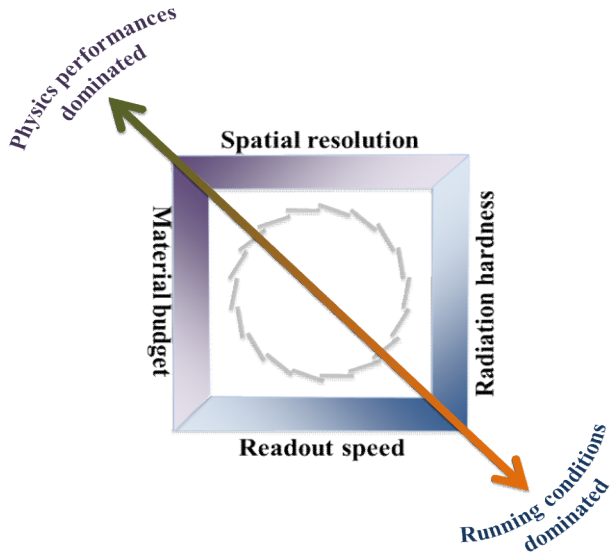
Overall Sensor Organisation







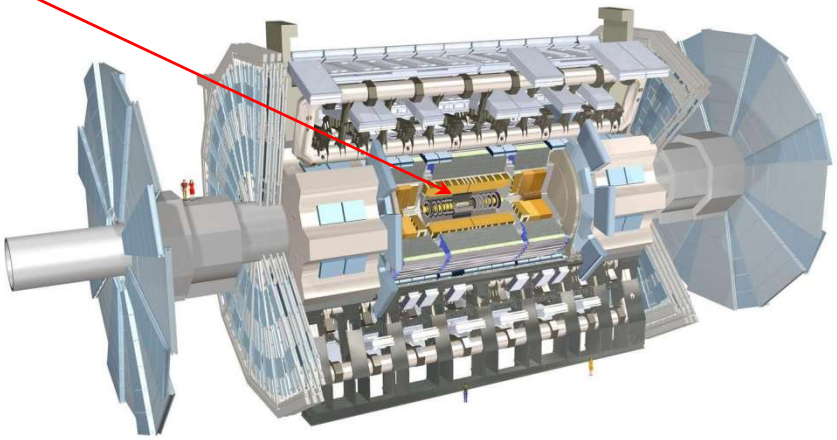
Examples of Pixel Sensor Architectures
Towards More Demanding applications ?



Towards More Demanding applications

- Specifications for the ATLAS Inner Tracker Upgrade Phase 2 (HL-LHC)

	ALICE-LHC	ATLAS-HL-LHC	
		Outer	Inner
Required Time Res. [ns]	20 000	**25**	
Particle Rate [kHz/mm^2]	10	**1000**	10 000
Fluence [n_{eq}/cm^2]	>10^{13}	**10^{15}**	10^{16}
Ion. Dose [Mrad]	0.7	**50**	1000

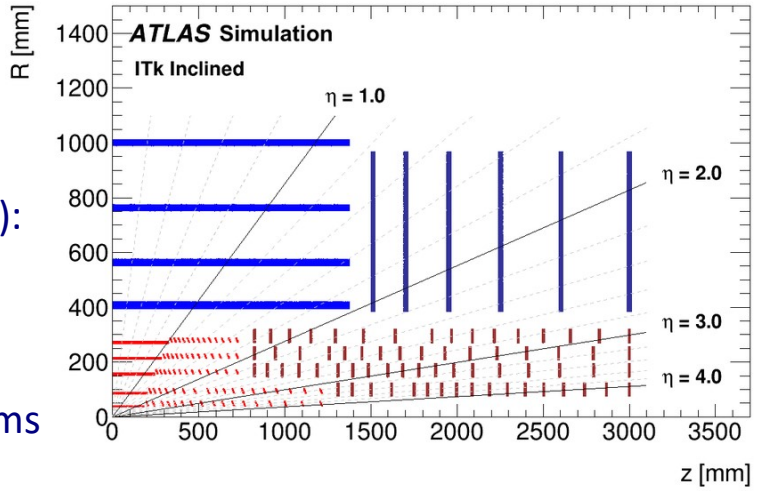


- Time resolution: fast collection by drift (<< 25 ns)
  ➔ larger depletion

$$E_{x,y} \propto f\,(\rho, V, Diode\ geometry, Diode\ density, Doping\ profile,\ \ Thickness, \ldots)$$

- High particle rate: short dead time (< 1 us)
- Tolerance to non-ionizing radiation (displacement damage): fast collection by drift to decrease signal charge trapping probability ➔ larger depletion

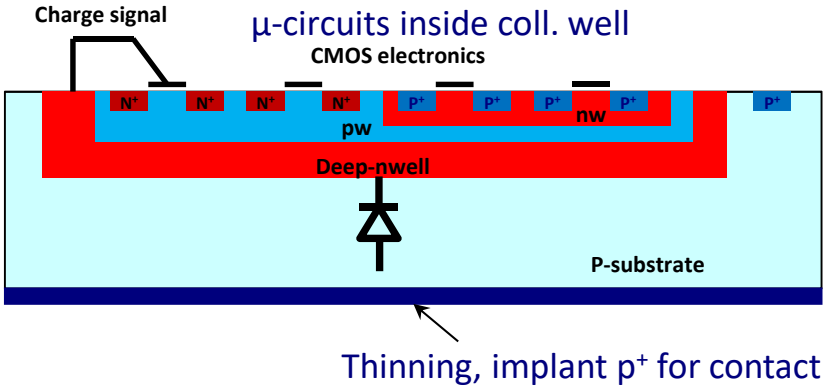
- ✓ CMOS development for the outer pixel layer benefit in terms of assembly and cost

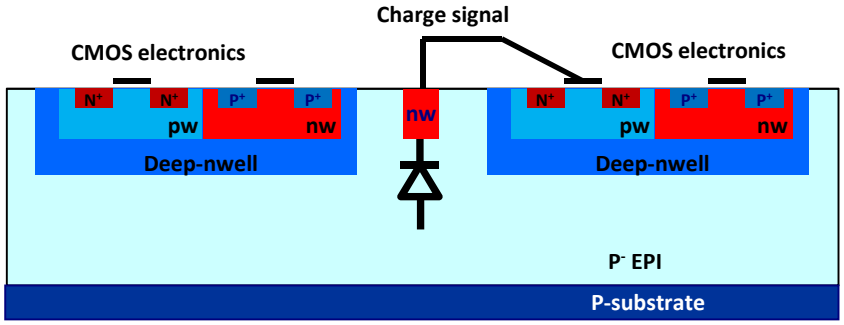


ATLAS ITk: Two Approaches

$$E_{x,y} \propto f(\rho, \text{V, diode geometry, diode density, doping profile, sub thickness, } \ldots)$$

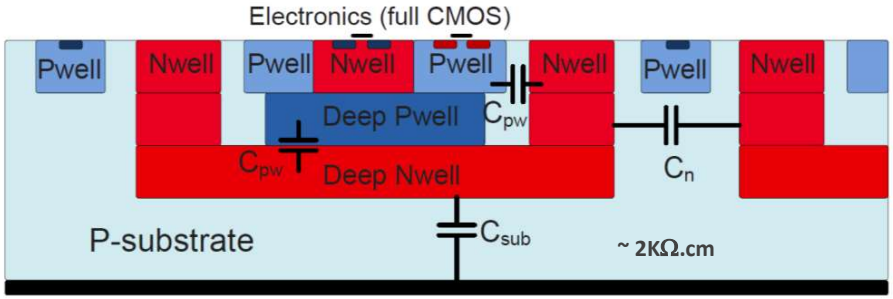
- Large collection electrode (HV-CMOS): Electronics in the collection electrode
  - Functional sensors, good radiation tolerance, power penalty due to large sensor capacitance (> 100 fF) and robust design to avoid cross talk
  - HV process, HR wafer, backside processing
- Small collection electrode (CMOS sensor **modified** process) for full depletion combined with low C (< 5 fF, circuit + sensor)
  - Good sensor performance after irradiation
  - Design of two large-scale demonstrators with low power front-end (< 25 ns, < 1 µW)
    - MALTA, asynchronous readout
    - TJ-Monopix, synchronous readout





LF-Monopix: In-pixel Front-end Electronics

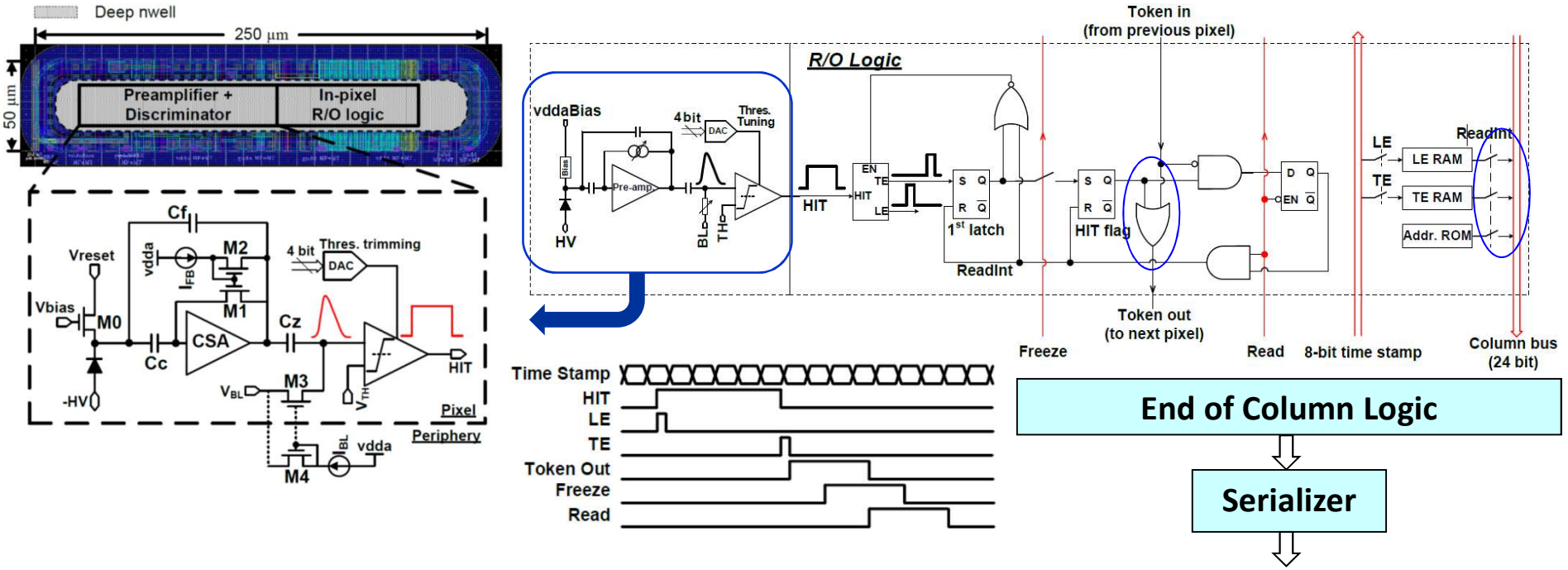
Ref. T. Wang, arXiv:1611.01206v1, 2016



LF-Monopix: 150 nm HV-CMOS, > 2kΩ.cm, Quadruple well process, up to 7 metal layers

- Chip size: 10 mm x 10 mm, Pixel size: 50 x 250 µm²
- Large detector capacitor degrades the noise performance, the speed of the front-end electronics and increases the power consumption
  - ✓ ENC ~ 200 e^-, threshold = 2500 e^-
- Large C_{pw} may introduce serious cross-talk

Pixel Design

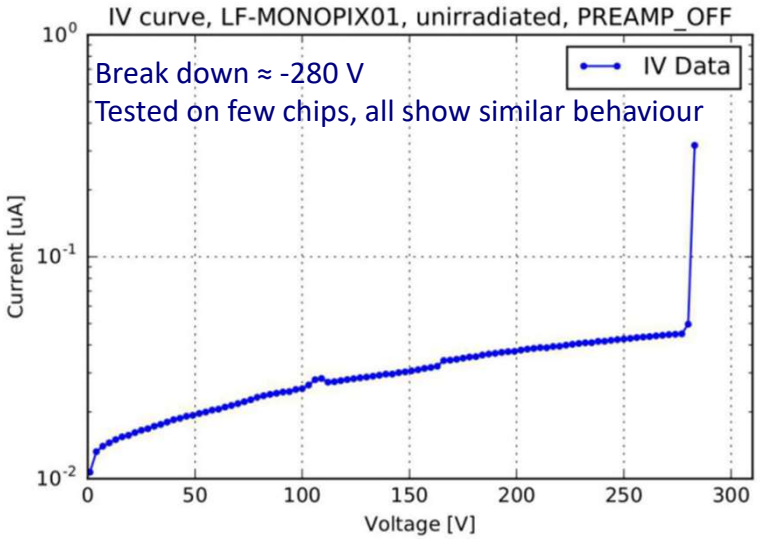


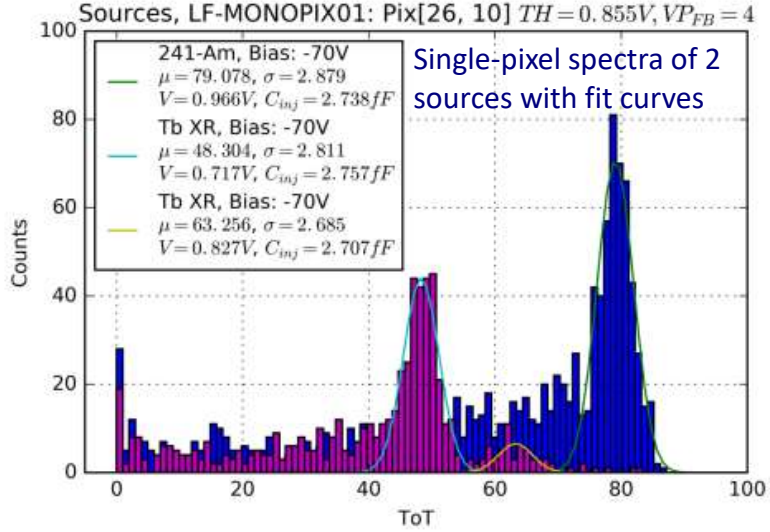
- Charge sensitive amplifier
- In-pixel 4 bit DAC for threshold trimming
- Hit register (1-bit)
- Time stamp is distributed in the matrix
- Hit information stored in the pixel
  - Time, charge of signal (TOT) (40MHz)
- Readout initiated by a token
  - Priority arbitration over the shared bus

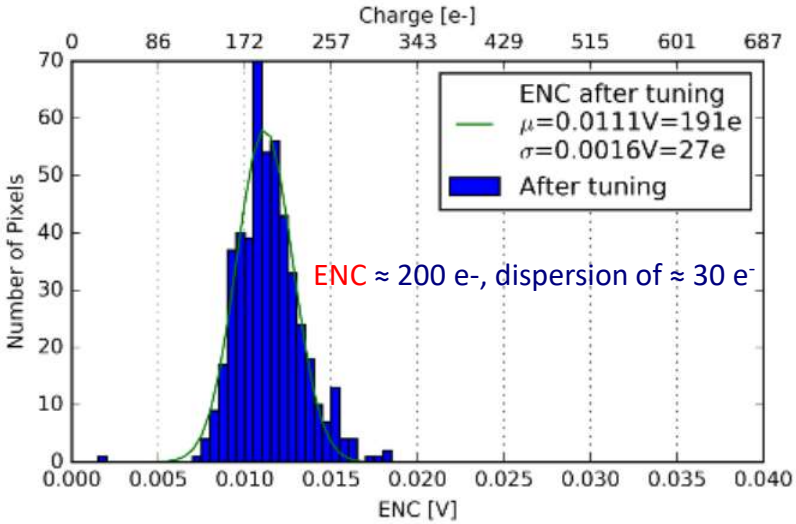
- Full-custom digital circuit
  - Minimised area ➔ for less C_d
  - Low noise circuit design for critical digital blocks
    - ⋆ a current steering logic is used for token propagation
    - ⋆ a source follower as the output stage is used for the readout of the memory

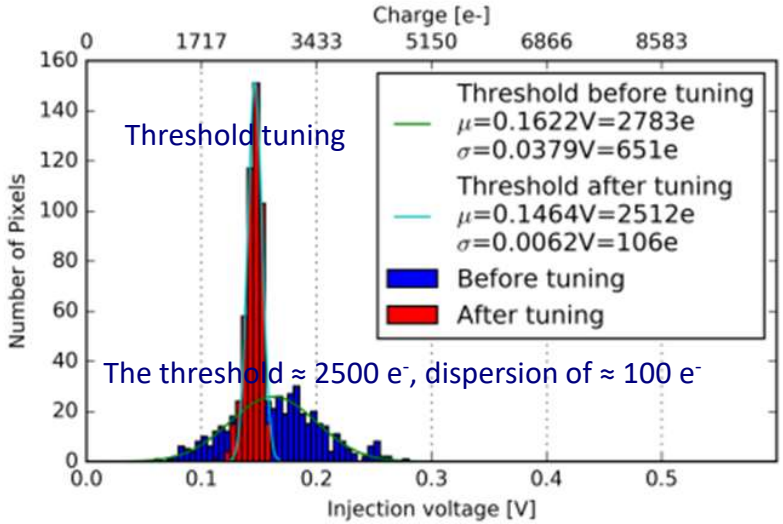
Some Test Results

^{241}Am source (59.5 keV) and ^{65}Tb (Kα: 44.5 keV, Kβ : 50.4 keV)

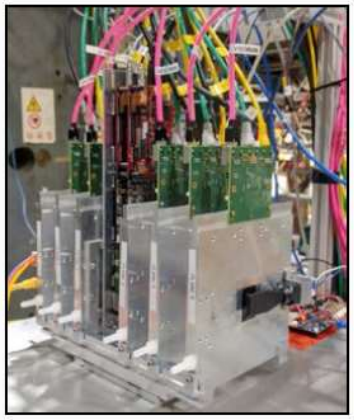


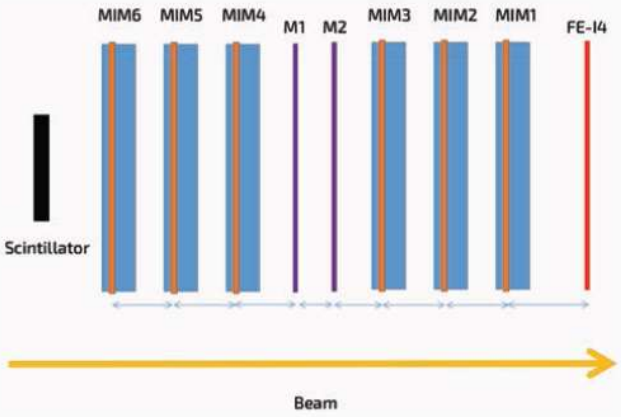






LF-Monopix in Test Beam

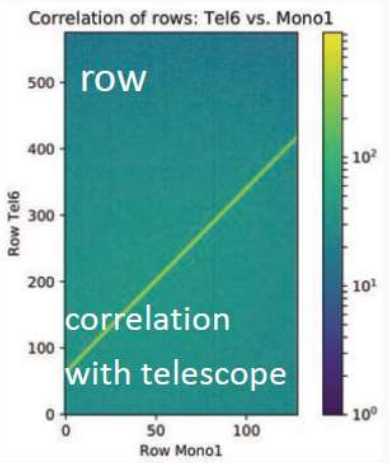


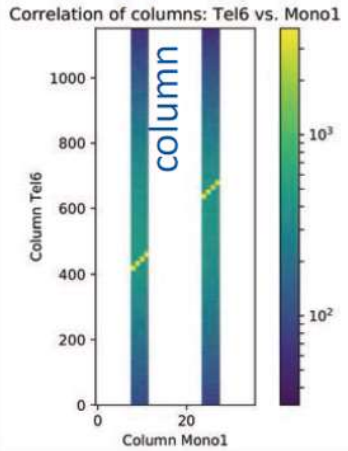


LF-MONOPIX (unirradiated and n-irradiated)
ELSA (2.5 GeV e-) CERN SPS H18 (180 GeV π)

- **MIMOSA26 x 6**
  - Pixel size: 18.4 µm x 18.4 µm
  - 115.2 µs/frame (rolling shutter)
- **FE-I4 x 1**
  - Pixel size: 250 µm x 50 µm
  - Timing resolution: 25ns (trig. by scintillator + TLU)

Sample of event correlation (@SPS)
MONOPIX <-> MIM26 (6)

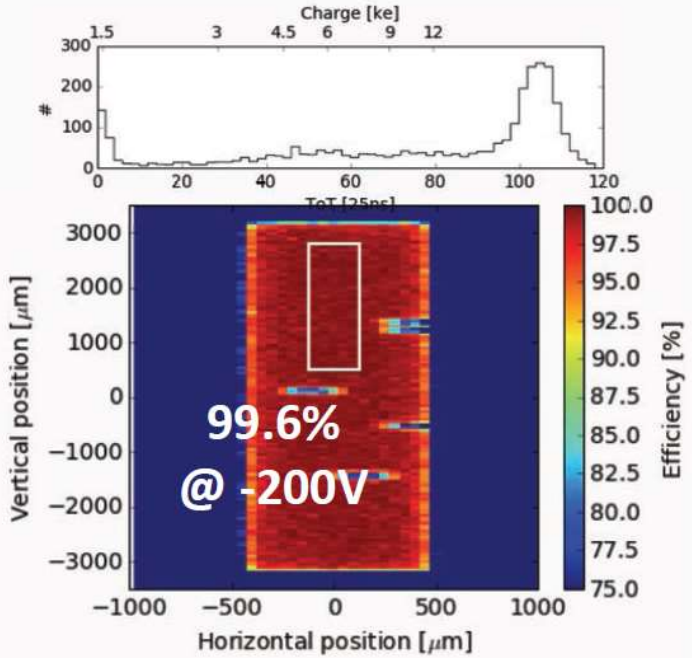




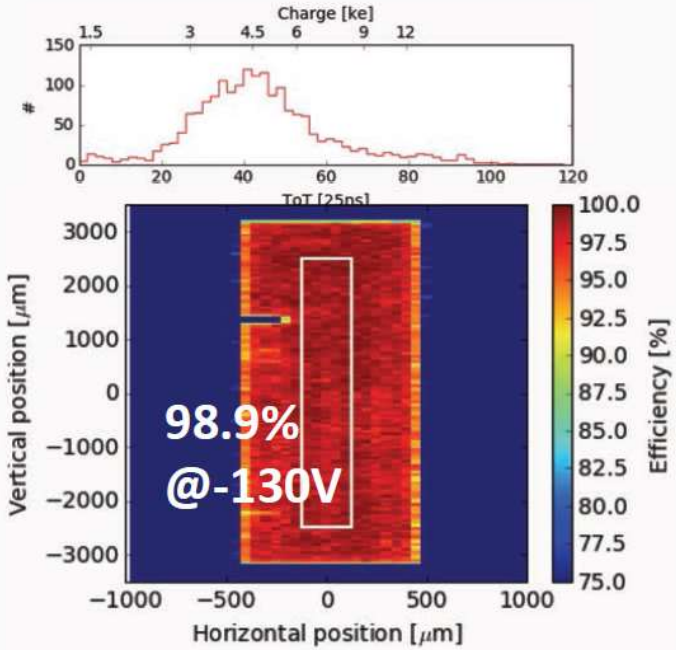
Ref. N. Wermes RD50-Hamburg 2018

Test Beam Results: Detection Efficiencies

- **un-irradiated**
  - Hit efficiency **@ Noise occ. << 10^{-7} , thr~1700e- (<10^{-7} @ 1400e-)**
  - 1% masked pixels from noise tuning



- **Neutron irradiated (1 x $10^{15}n_{eq}/cm^2$)**
  - Hit efficiency **@ Noise occ. < 10^{-8}, thr~1700e-**
  - < 0.2% masked pixels from noise tuning.



✓

Ref. N. Wermes RD50-Hamburg 2018

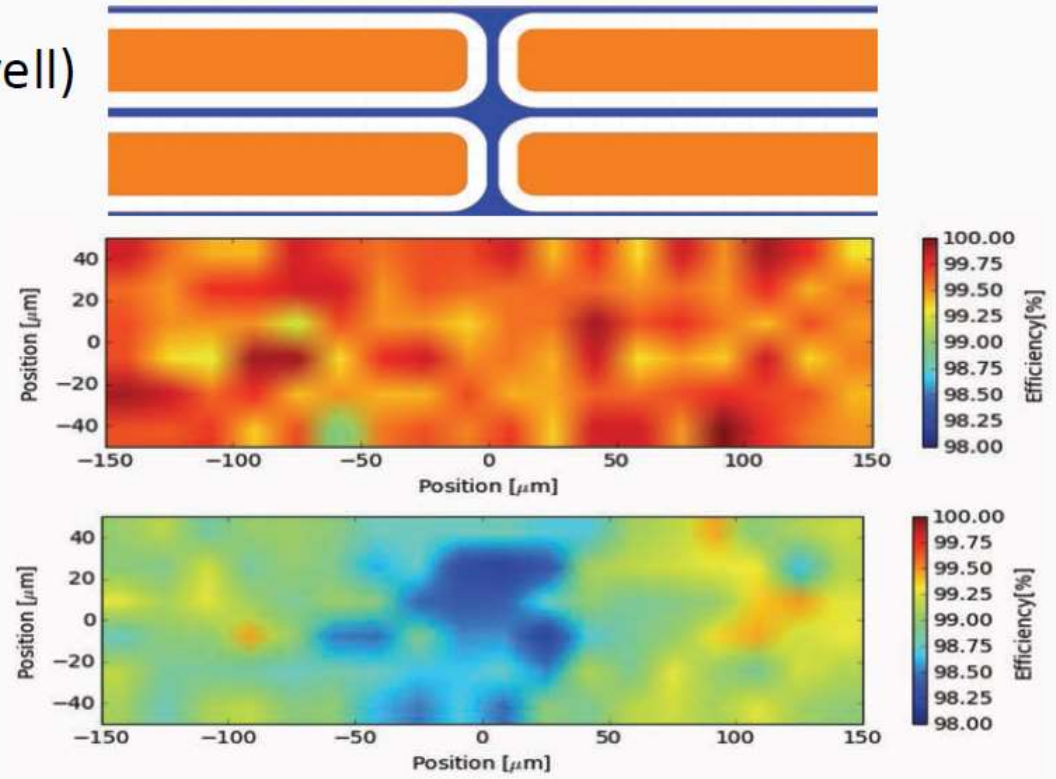
In-Pixel Efficiency

N-well (collection well)

P-well

Un-irradiated

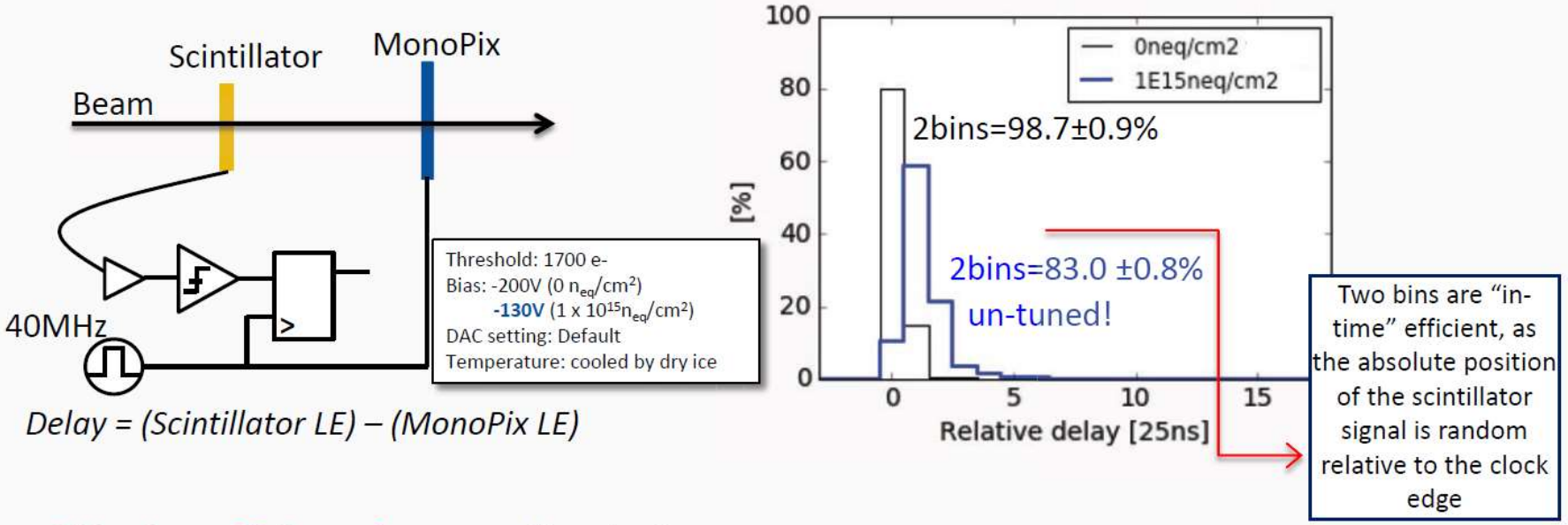
$1 \times 10^{15} n_{eq}/cm^2$



- In the irradiated sample, the degradation of the efficiency is observed not only at the corner of pixels but also in the middle of pixel → normal degradation

Ref. N. Wermes RD50-Hamburg 2018

Timing Performance



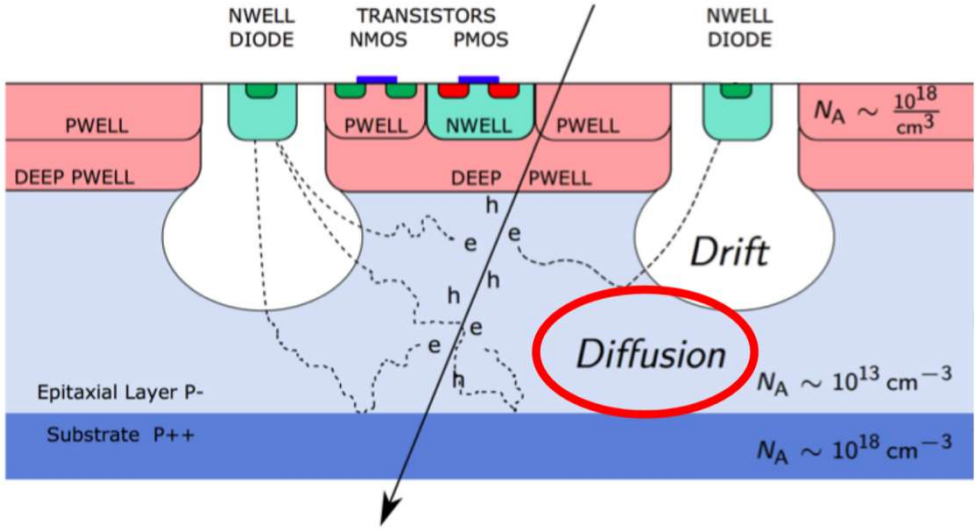
- **>80% in-time efficient after** 1 x $10^{15} n_{eq}/cm^2$.
  Remarkable for C_D ~ 400fF and promising for new design with smaller C_D (Optimized FF)
- **Note that there is still room for improvement by tuning:**
  Optimize: CSA, discriminator currents, etc., higher bias voltage, back side process.

Ref. N. Wermes RD50-Hamburg 2018

Small Electrode vs. Radiation Tolerance

- Present MAPS offer a number of very interesting advantages, but the diffusion is a limiting factor

- In a (very) high radiation environment (10^{15} – 10^{16} n_{eq}/cm^2)
  - The ionization charge is trapped/ recombined in the non-depleted part ➔ no more signal
  - Diffusion makes signal collection slower than typical requirements for pp – colliders



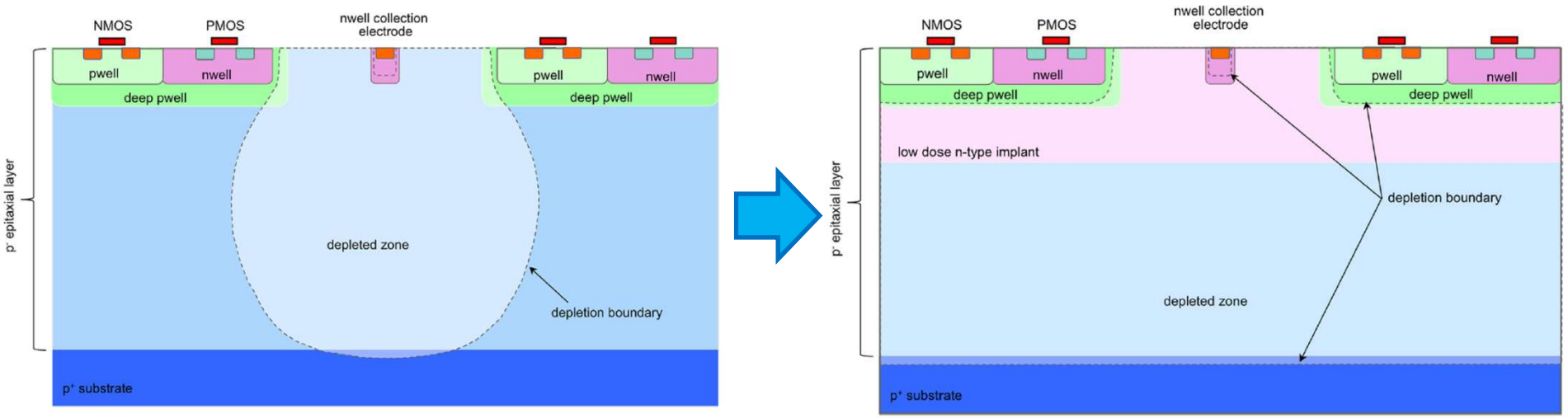
- Readout architectures (ALPIDE) are low power, but not designed for high rates like p-p at LHC

- Combine high resistivity and high voltage

$$d \propto \sqrt{\rho V}$$

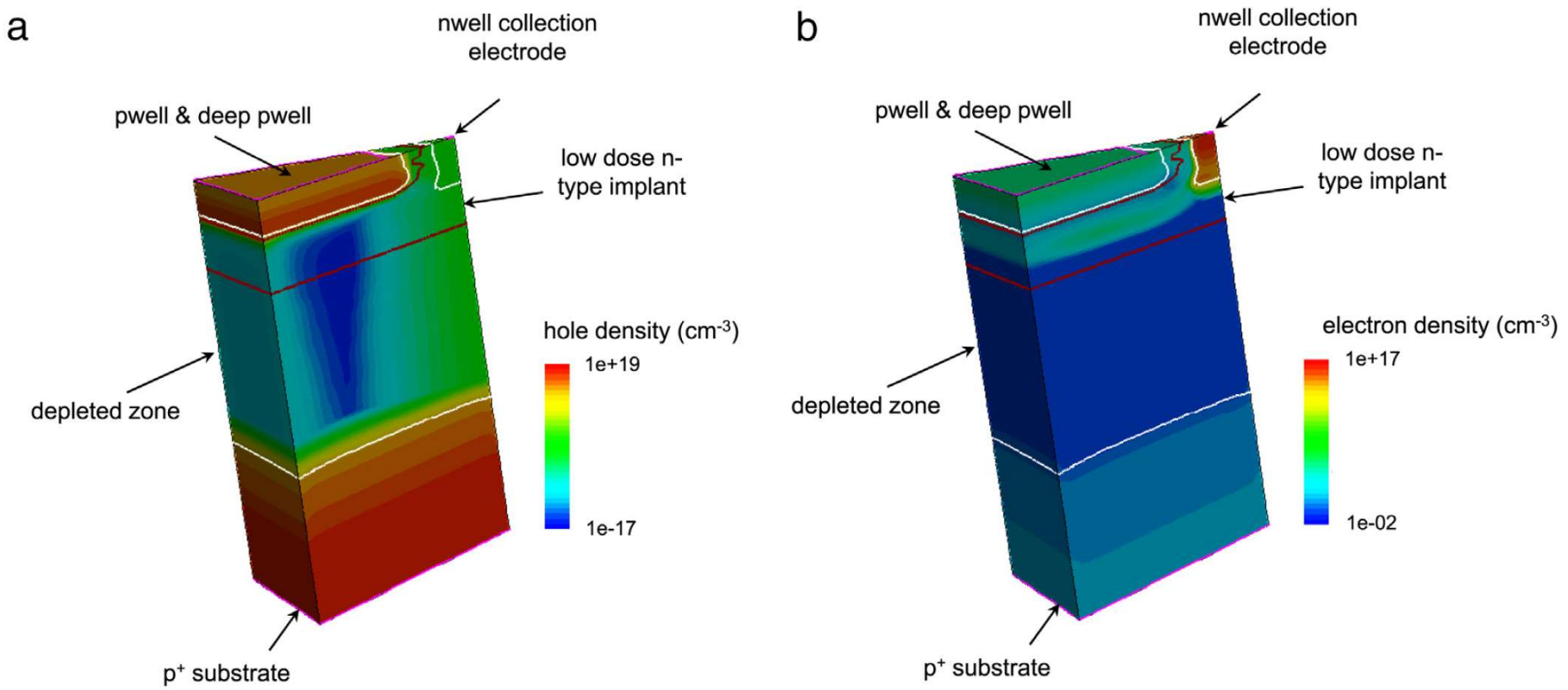
TowerJazz 180 nm Modified Process

- Modified process developed in collaboration of CERN with TJ foundry, originally developed in context of ALICE ITS
- Adding a planar n-type layer significantly improves depletion under deep PWELL
  - Increased depletion volume → fast charge collection by drift
  - better time resolution reduced probability of charge trapping (radiation hardness)
  - Possibility to fully deplete sensing volume with no significant circuit or layout changes



W. Snoeys et al., NIM A871 (2017) 90-96

Device Simulation

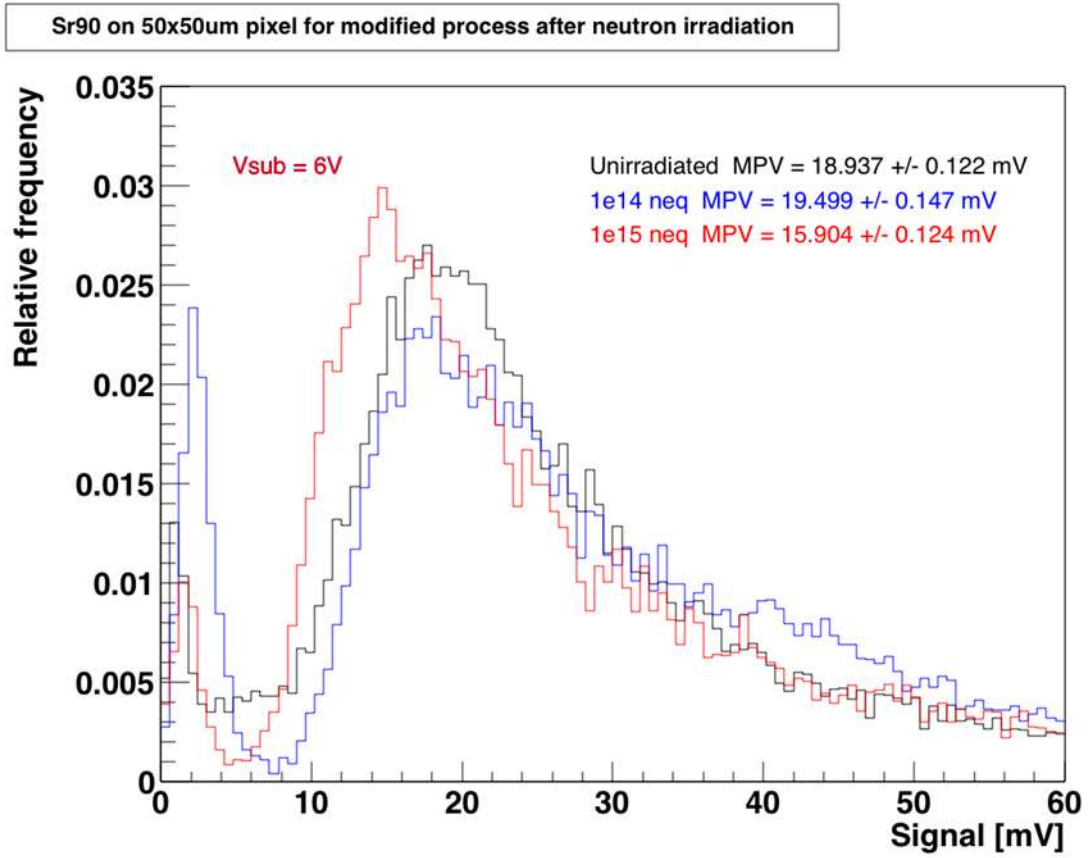


- Simulated hole (a) and electron (b) densities illustrate the depletion of the epitaxial layer and the low dose implant. The junctions are indicated with a red line and the edge of the depleted zone with white lines.
  - The pwell was grounded, the collection electrode and substrate are biased at + 5 V and −15 V respectively
  - similar depletion is already reached near zero substrate bias

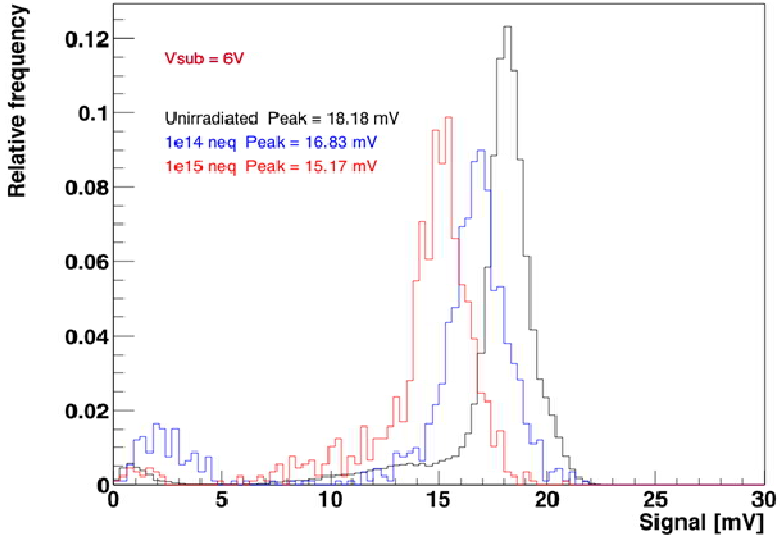
W. Snoeys et al., NIM A871 (2017) 90-96

Modified Process: Irradiation Results

- "Investigator" chip irradiated up to 10^{15} n_{eq}/cm^2 and 1 Mrad in several steps (temp =-15°C)
  - Little change in signal after irradiation
  - Signal well separated from noise



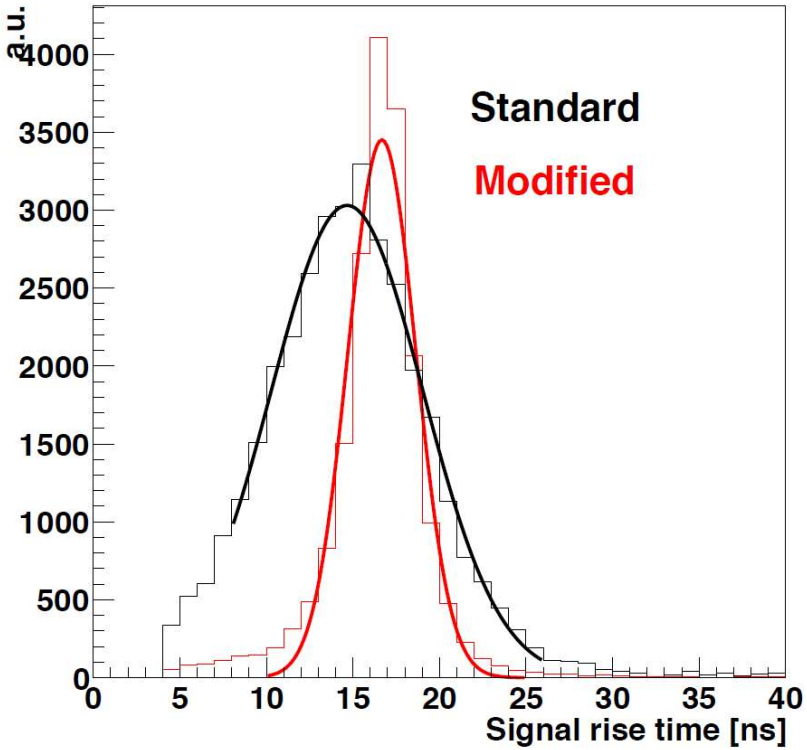
^{55}Fe signal response of 50x50 µm² pixel

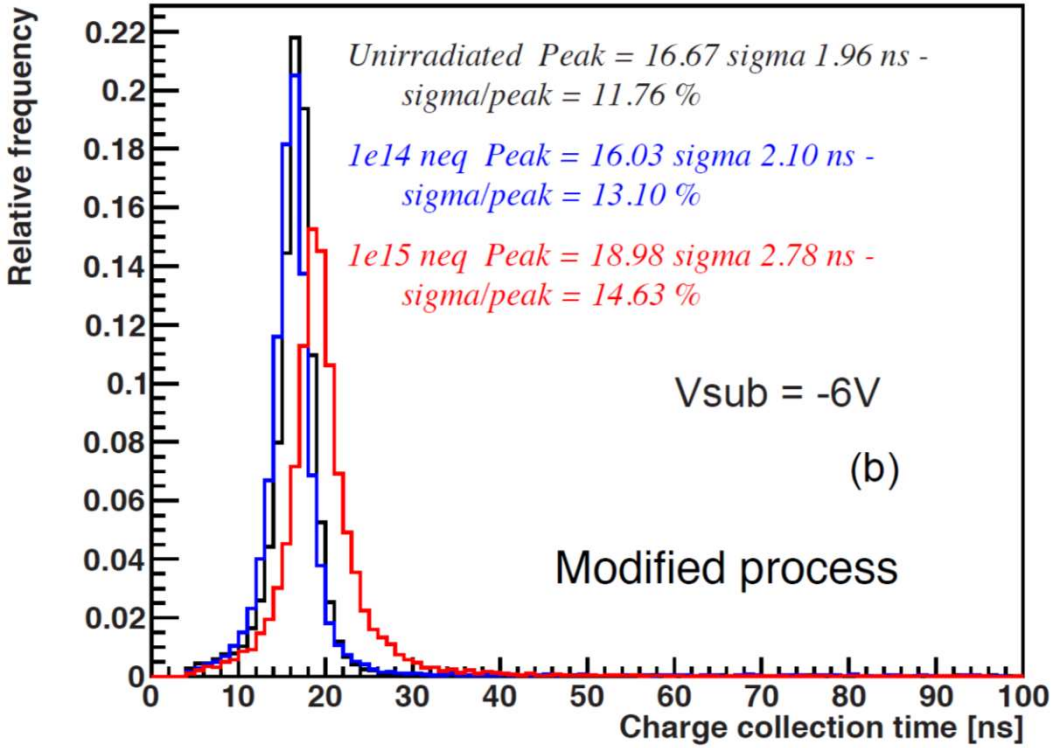


H. Pernegger et al., DOI 10.1088/1748-0221/12/06/P06008

Modified Process: Charge versus Collection Time

The signal collection time with 50x50 µm² pixel

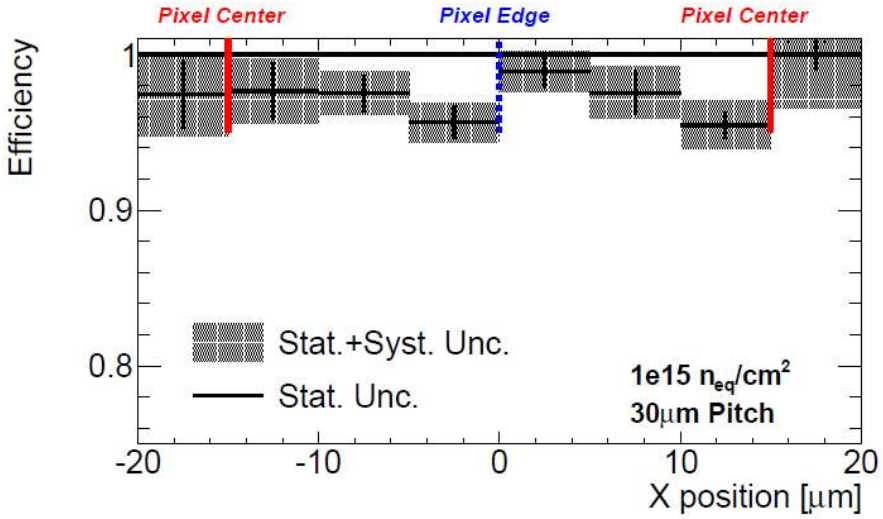


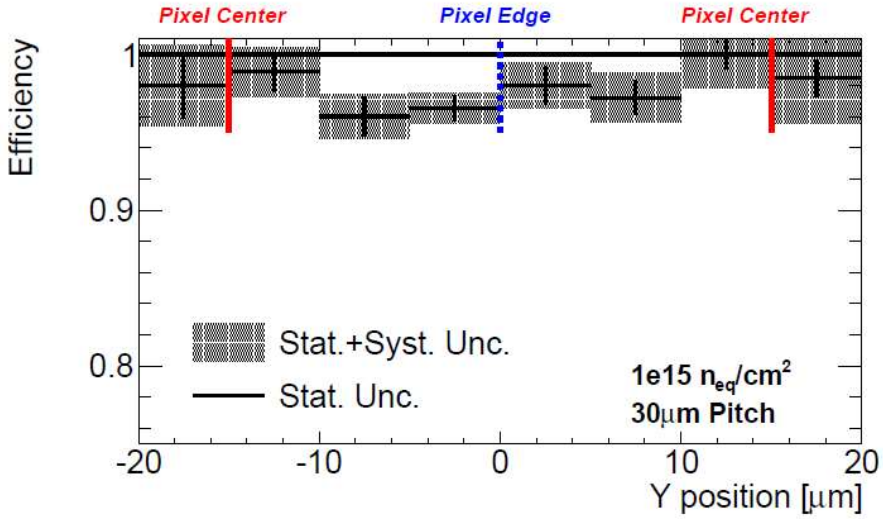


H. Pernegger et al., 11th International "Hiroshima" Symposium 2017

Beam Test: Detection Efficiency

- $10^{15} n_{eq}/cm^2$ irradiated modified process
- 30x30 µm² pixel sensor with 3 µm electrode and 3 µm spacing
- Efficiency projection between the pixel enters in X and Y direction

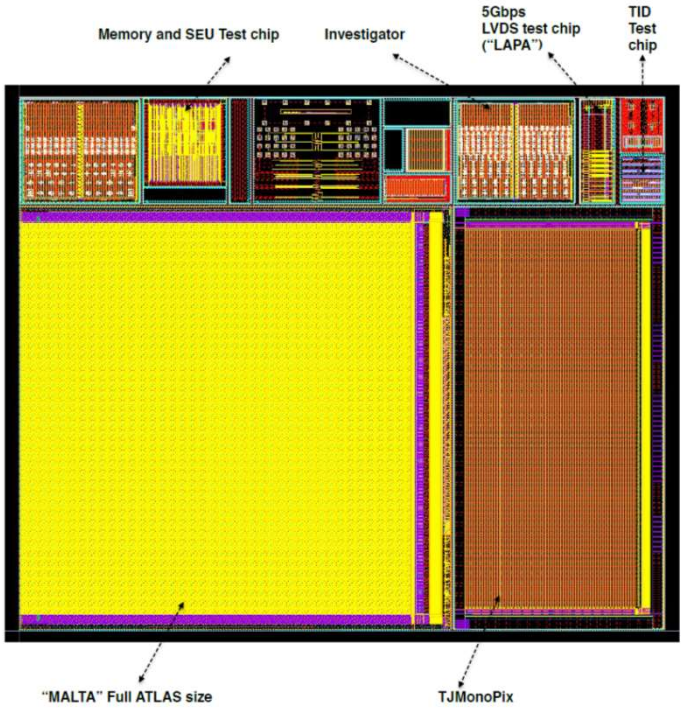


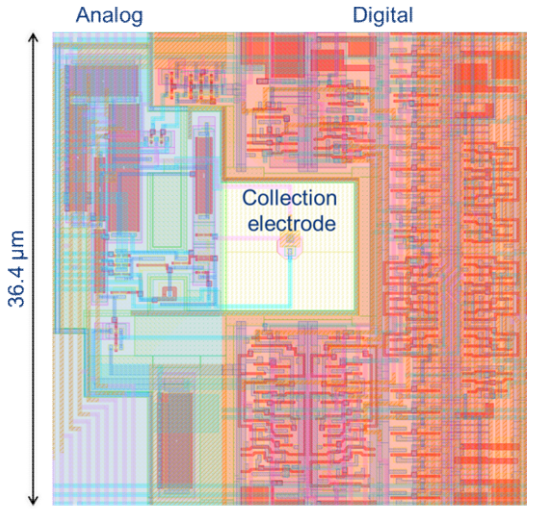


H. Pernegger et al., DOI 10.1088/1748-0221/12/06/P06008

TJ Submission: Design of Large-Scale Demonstrators

- Design of two full-scale demonstrators to match ATLAS specifications for outer pixel layers :MALTA & TJ-Monopix





Ref. Th. Kugathasan TWEPP 2017

- MALTA

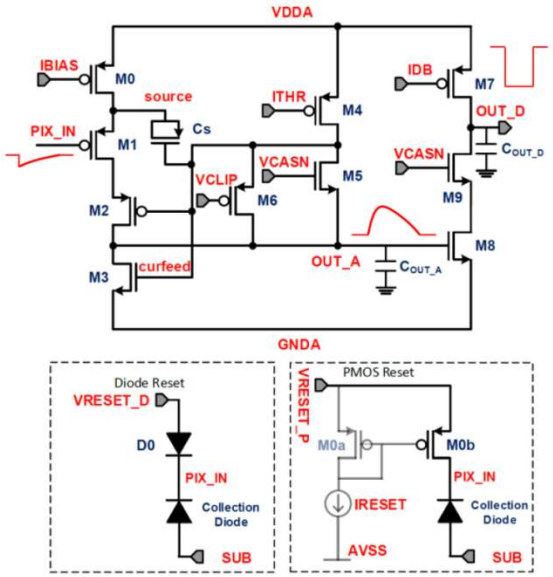
  Asynchronous readout architecture to reduce digital power consumption and increase hit rate capability in the matrix.
  No clock distribution over the pixel matrix - (power reduction)

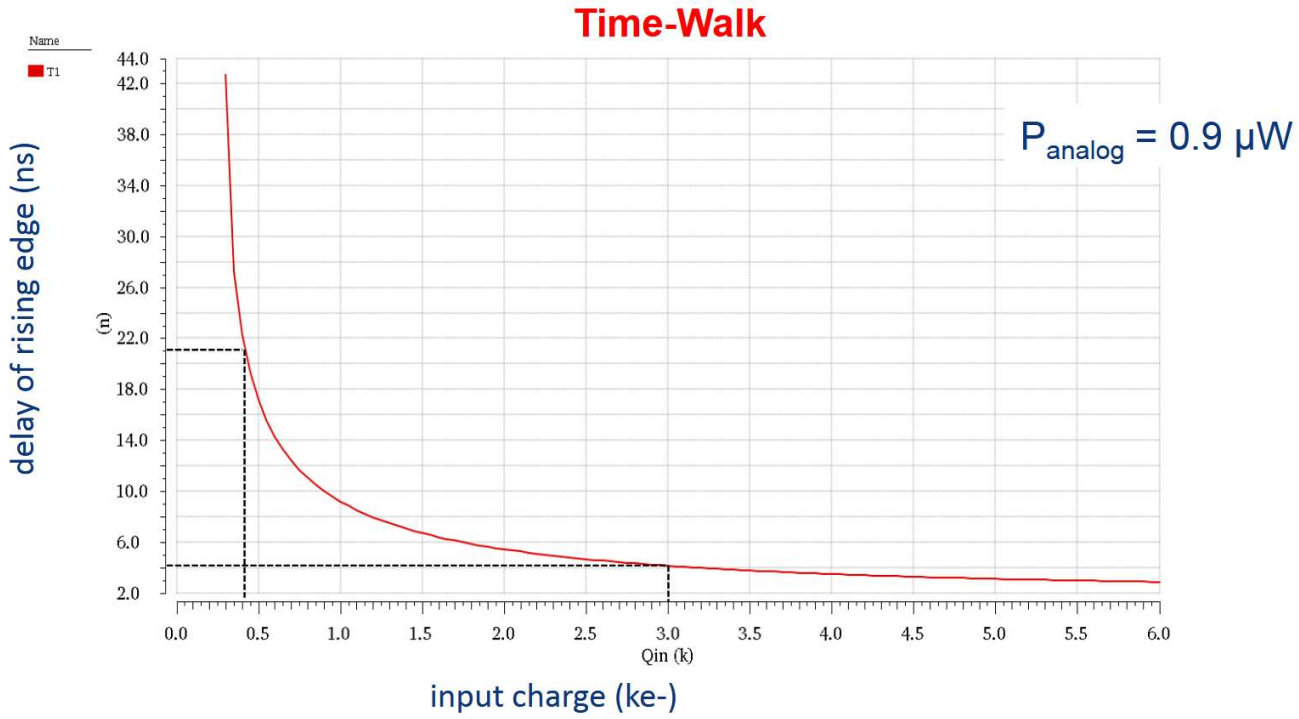
- TJ-Monopix

  Synchronous readout architecture. Uses the well-established column drain readout architecture (experience from LF-Monopix design)

Analog Front-End

- Based on the front-end of the ALPIDE chip (previously developed for the upgrade of the ALICE experiment)
- Improvement for fast timing (< 25 ns) and hit rate capability by increasing current consumption (250-500 nA/pixel, < 1 µW/pixel)

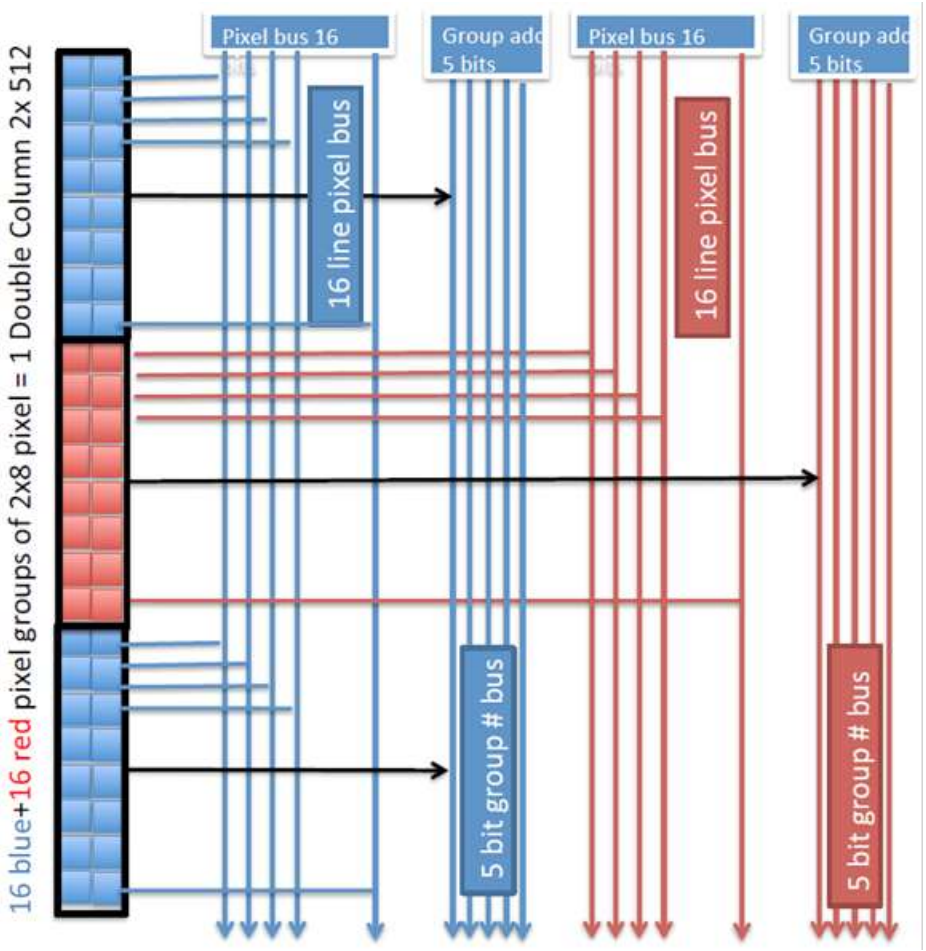




Ref. Th. Kugathasan TWEPP 2017

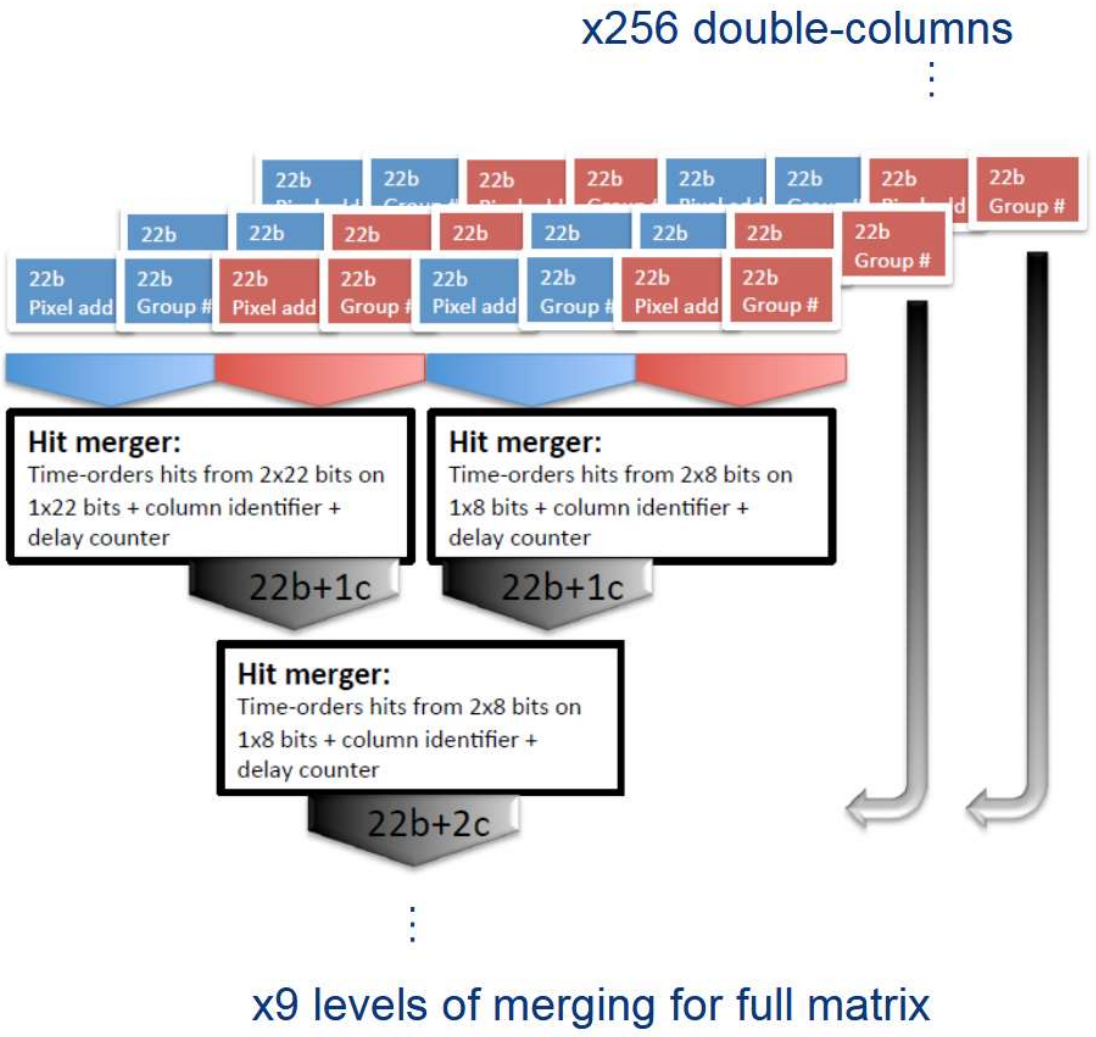
Asynchronous Matrix Readout

- No clock distribution over the pixel matrix – (power reduction)
- Hits are stored using in-pixel flip-flops and transmitted asynchronously over high-speed buses to the end-of-column logic (programmable pulse duration 0.5 ns to 2.0 ns)
- Double-column divided into groups of 2x8 pixels (“red” and “blue”)
- Buses shared by all groups of the same colour in the double-column
- Group number encoded on 5-bit group address bus



Digital End-Of-Column Logic

- At the periphery, signals of red and blue groups are merged together
- Addition of 4-bit bunch-cross ID (timing) and chip ID
- Simultaneous signals on two buses require additional arbitration logic (blue signal is given priority, red is delayed)
- Merging is repeated for all the double-columns and then continued until all outputs are merged into one parallel bus (40 bits)



Ref. Th. Kugathasan TWEPP 2017

Discussion on Power Consumption

- Assumptions: Matrix 2 cm x 2 cm, pitch 36.4 um
- Analog Power < 75 mW/cm2
- Matrix readout: asynchronous, depends on pixel hit rate
  - CMOS signals in the matrix (no noise issues, no need to use power consuming differential transmission)

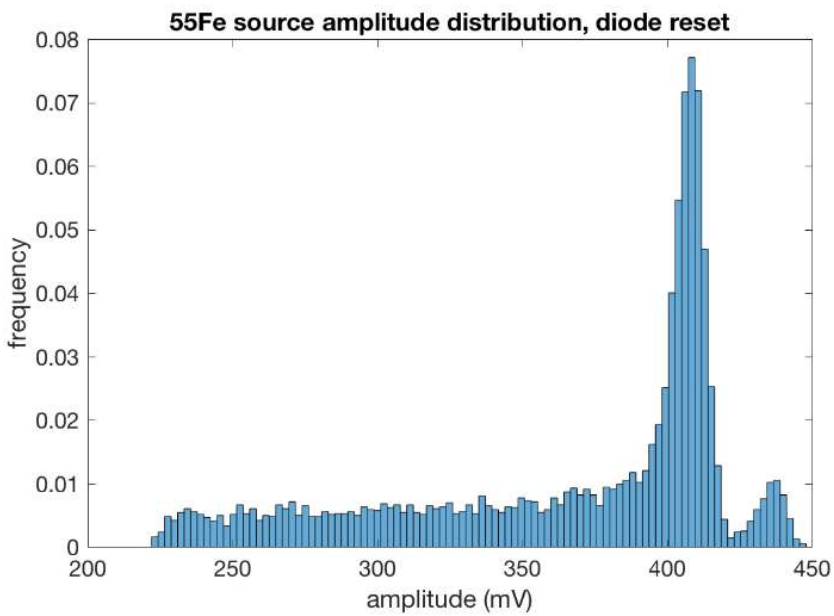
	pixel hit rate		Power/bit/cm^2 (H=2 cm)	Power (4.5 bit toggling)
Layer	hit/BC/mm^2	Mhit/mm^2/s	mW/cm^2	mW/cm^2
0	0.68	27.2	28.3	127.3
1	0.21	8.4	8.7	39.3
2	0.043	1.72	1.8	8.0
3	0.029	1.16	1.2	5.4
4	0.021	0.84	0.9	3.9

- Power for clock distribution (not used in the asynchronous readout)
  - Energy per 1 cm toggled line at 1.8 V = 3.2 pF/cm x (1.8 V)^2 = 10.4 pJ
  - 137 lines per cm (1 per double column) for 36.4 µm pixel pitch:
    - 137 x 10.4 pJ x 40 MHz = 57 mW/cm2

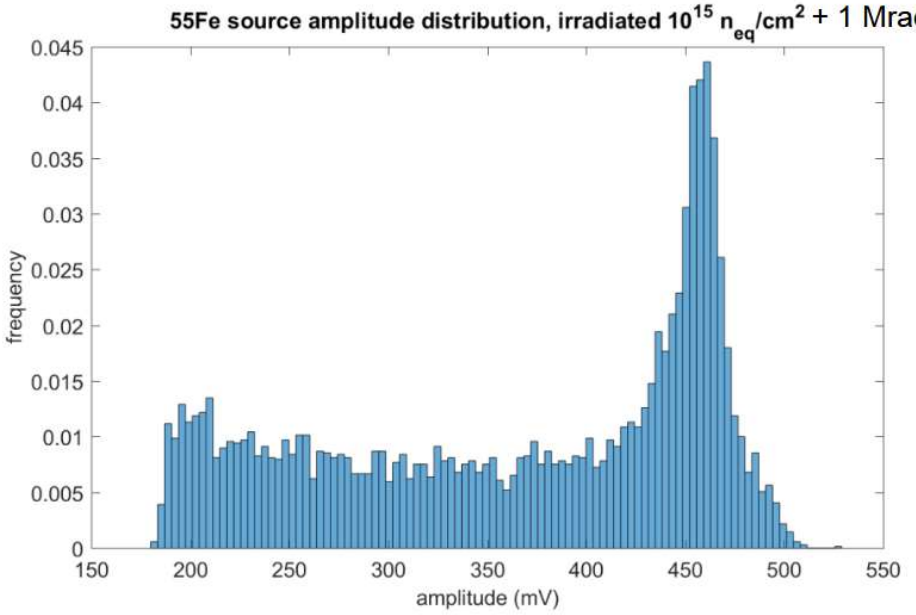
Ref. Th. Kugathasan TWEPP 2017

Test Results: ^{55}Fe Spectra

Before irradiation



After irradiation

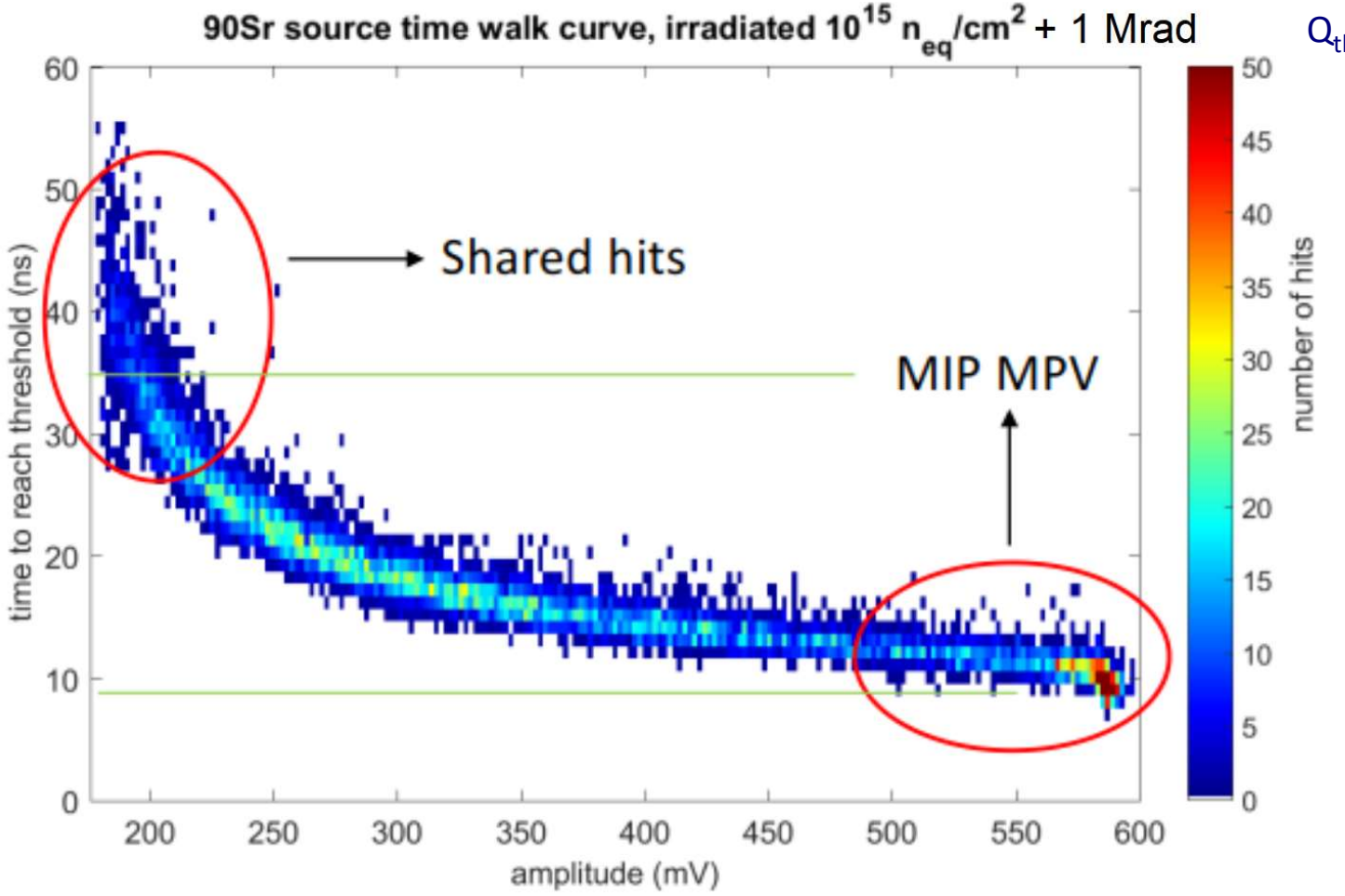


- Signal from analog monitoring pixel
  ➔ good response after irradiation

Ref. Kugathasan ACES 2018

MALTA: Front-End Time Walk

- Charge collection time and front-end timing (< 25 ns) good after irradiation
  P_{analog} = 0.9 µW/pixel

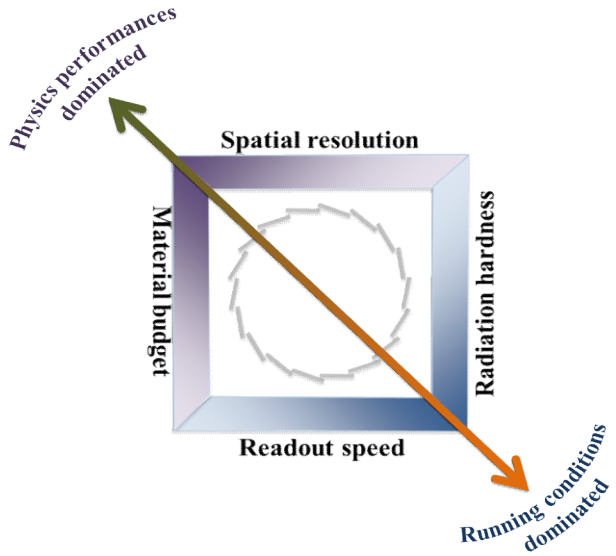


Q_{th} = 510 e^-

Ref. Kugathasan ACES 2018

CPS R&D for e^+ e^- Colliders

Initial motivation: the need of very granular and low material budget sensors



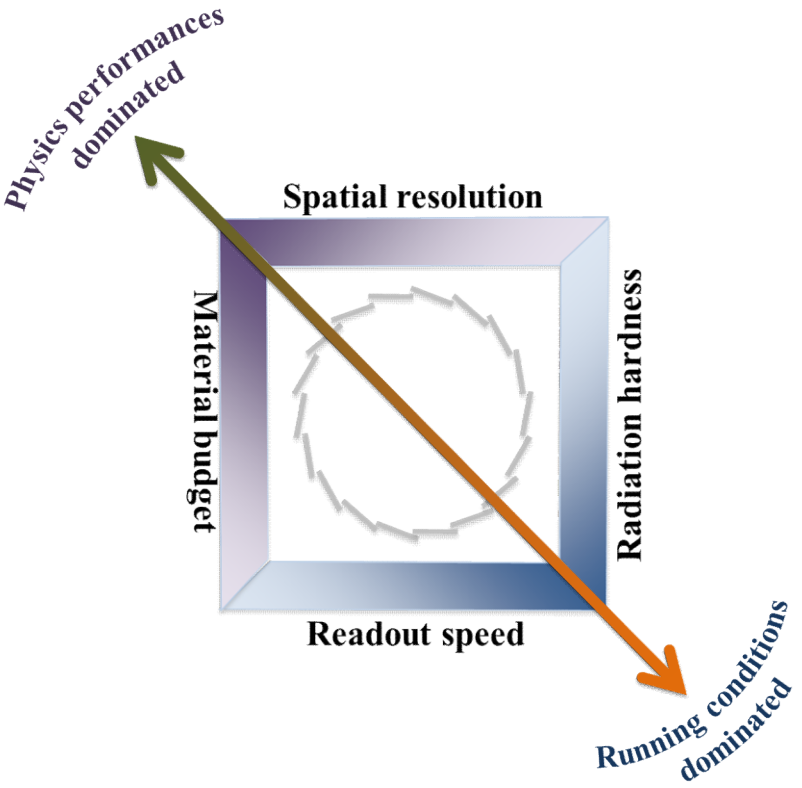
Discussion of MAPS Applications in e^+ e^- Colliders

- e^+ e^- colliders have very clean environment, moderate radiation compared to the LHC
- Physics driven:

  ILC: unprecedented precision detectors, with a highly granular calorimeter, excellent momentum resolution and vertexing capabilities

  - Compared to LHC detectors:
    - ⋆ Jet energy resolution (improve by a factor ~3)
    - ⋆ Momentum resolution (improve by a factor ~10)
    - ⋆ Vertex reconstruction (improve by a factor ~10)
- Vertex detector will play a crucial role, with:
  - A spatial resolution ~3 µm
  - A low material budget to minimize multiple scattering, typically 0.15% X_0/layer
  - A moderate/suppressed power consumption
  -

Radiation	ILC	CEPC
TID (kRad/year)	~100	~1000
NIEL (1 MeV n_{eq}/cm^2/year)	~10^{11}	~2 x 10^{12}



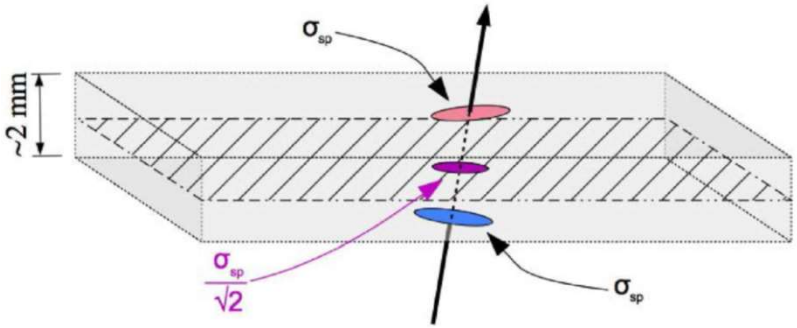
The sensor specifications necessitate negotiating the established conflict between the spatial resolution required by the physics objectives and the read-out speed imposed by the rate of the beam related background, while keeping the power consumption at an acceptable level

Improving the Spatial Resolution

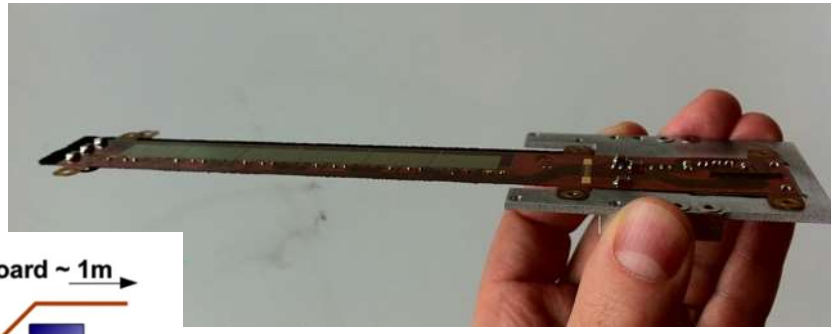
- Objectives:
  - Aim for $\sigma_{sp} \cong 4$ µm ➔ pitch $\cong 22$ µm
  - Double-sided layers:
    - ⋆ Combine impact positions observed on each ladder face to derive hit position in ladder "medium plane"

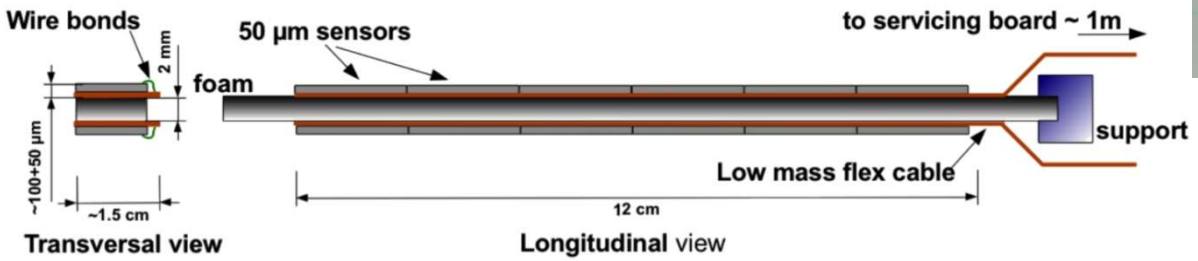
$$\sigma_{sp}^{layer} \cong \frac{\sigma_{sp}}{\sqrt{2}}$$

      - ✓ Based on straight line interpolation, exploiting low occupancy, proximity of impacts, low material budget



- PLUME (Pixelated Ladder with Ultra-low Material Embedding) Project
  - Study a double-sided detector ladder motivated by the R&D for ILD VD
  - Targeted material budget: <~0.3%XO
  - Correlated hits→ reconstruct mini-vector
  - Resolution/alignment/shallow angle tracks





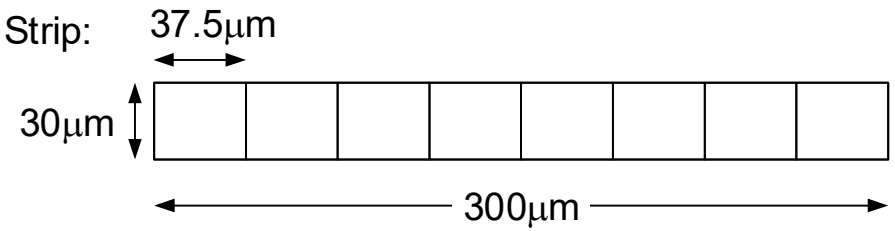
A Monolithic Chip for the CLIC Silicon Tracker

Requirements for a chip for the CLIC silicon tracker

- Channel dimensions:
  - Single point resolution in one dimension ≤7 μm (transverse plane)
  - Length of short strip/long pixel: 1 -10 mm
    (1 mm fulfils the requirements for the different barrels)
- Energy measurement (For time walk correction and improving spatial resolution)
  - 5-bit resolution
- Time measurement:
  - 10 ns bin, 8-bits
  - No multi-hit capability
- Material budget 1-1.5% X_0 (i.e. ~200 µm for silicon detector and readout)
- Power consumption < 150 mW/cm² (Power pulsing, duty cycle ~500 ns/20 ms (25×10^{-6}))
- Radiation hardness (NIEL< 10^{10} n_{eq}/cm²/yr, TID < 1 Gy/yr)
- Monolithic sensor in Tower Jazz 180nm CMOS imaging process (Expertise in design due to ALPIDE effort)

[1] D. Dannheim, A. Nürnberg: Requirements for the CLIC tracker readout (CLICdp-Note-2017-002)

The Detector Channel



- The detector unit cell consists of a strip of 30 x 300 mm²
- It is segmented in 8 pixels
  - To ensure prompt charge collection in the diodes
- Measurement
  - Pixel hit within strip (8 bits)
  - Time of arrival of the signal at the strip (10 ns bin, 8 bits) (first hit)
  - Energy deposit (TOT: Time over Threshold): 5 bits (pixel with largest deposition)
- Considered other architectures (e.g. analog summing but penalty in minimum threshold)

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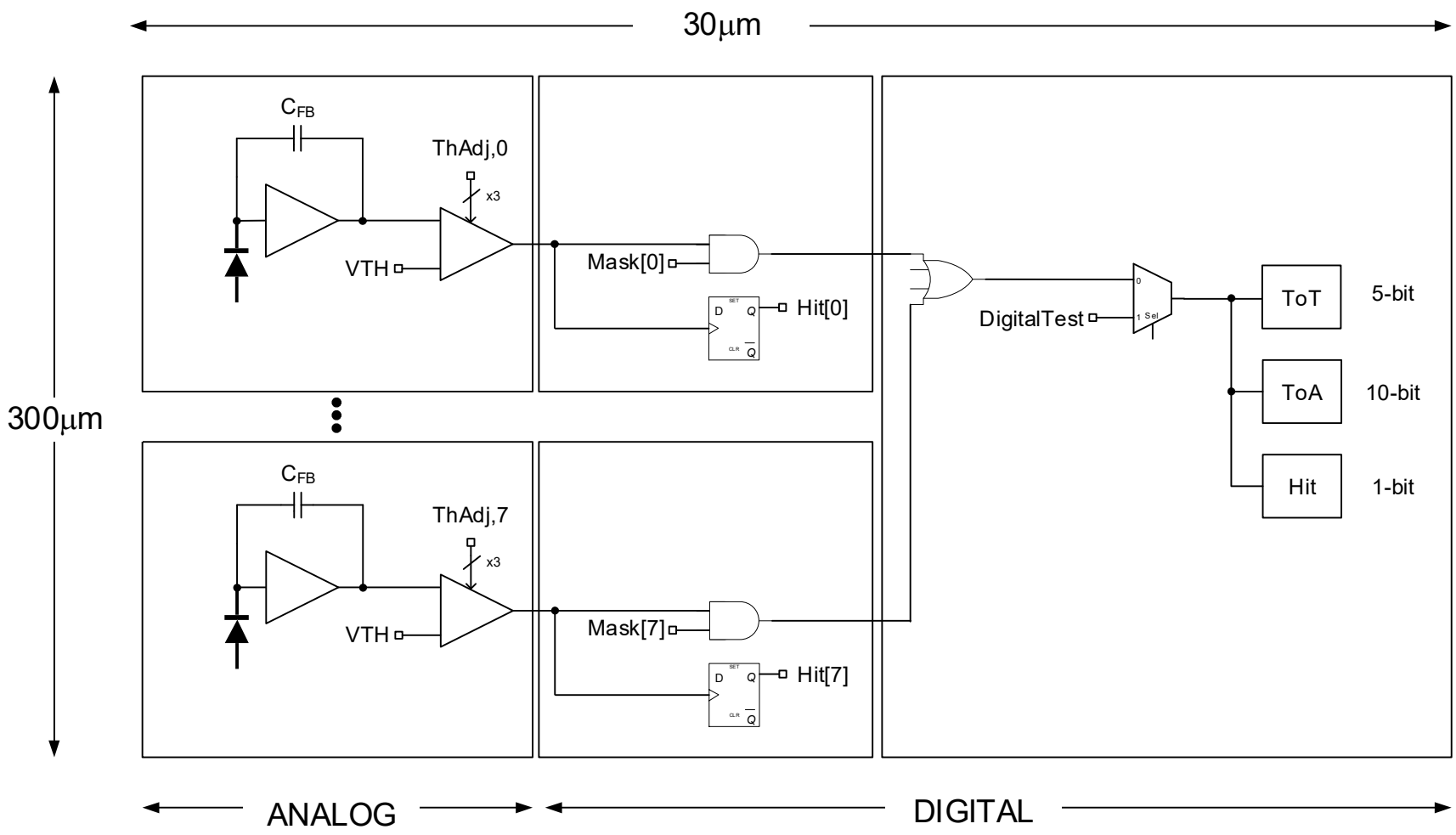
The Readout Channel



- Individual pixel hit information, possibility to mask pixels

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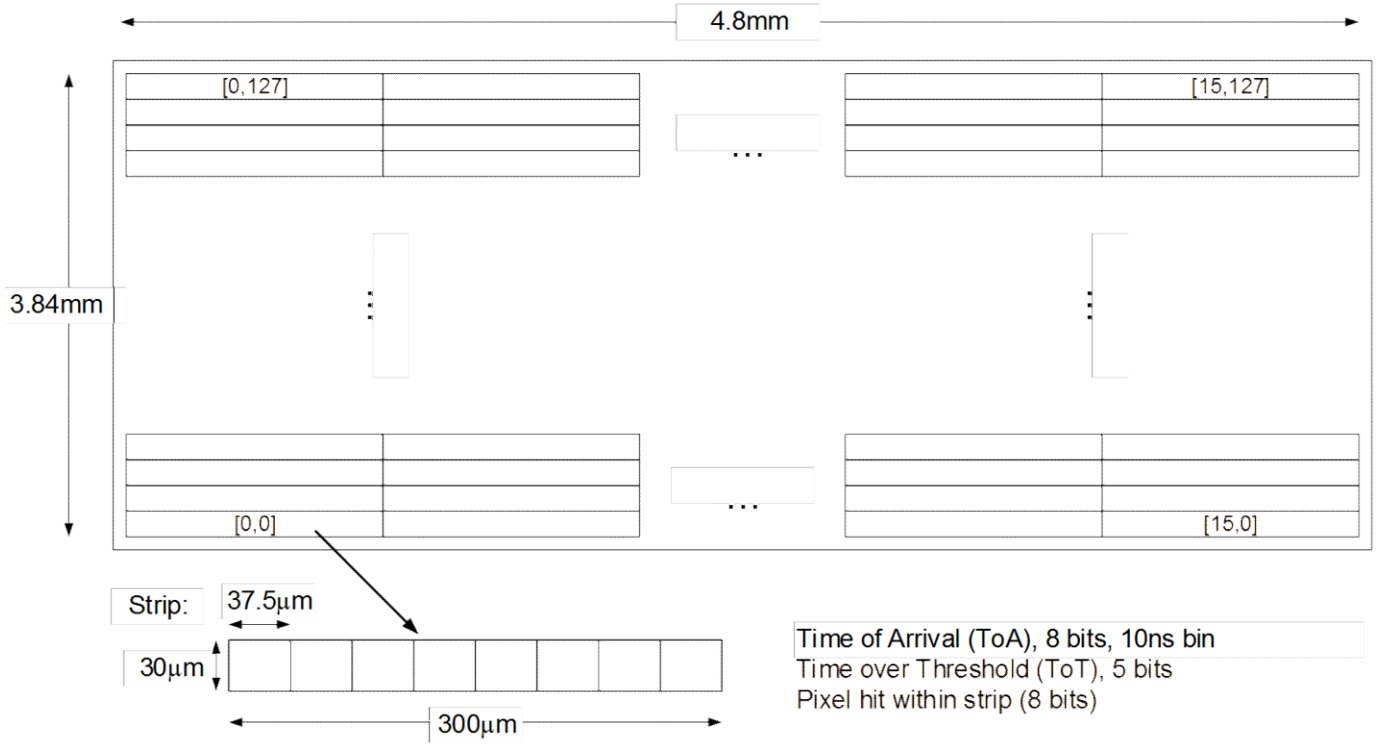
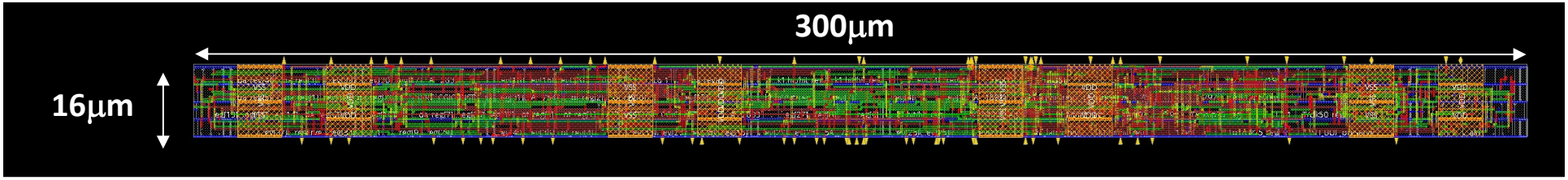
Chip Sensitive Area



CLIC 3 TeV beam has low duty cycle ➔ readout of sensor



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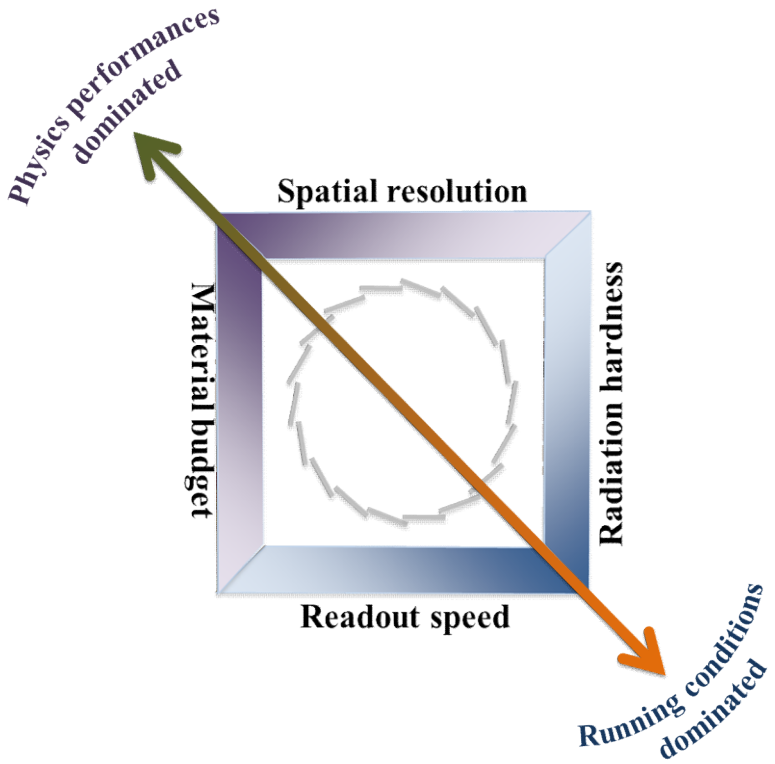
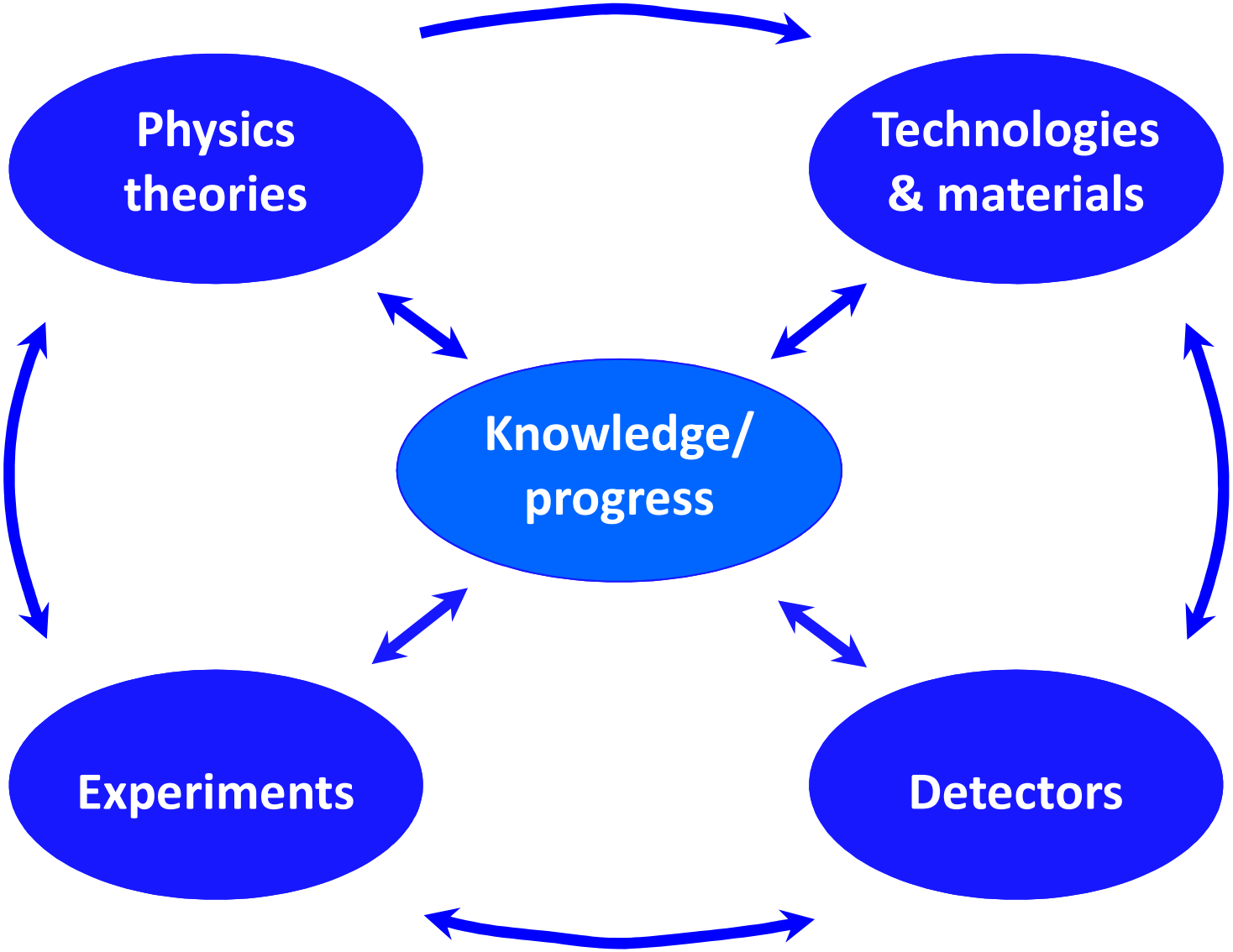
Summary

- MAPS = Market-driven technology, real potential not completely be exploited
- Conflict between physics performance driven parameters and running condition constraints
  - Ultimate performance on all specifications cannot be reached simultaneously
  - Each facility & experiment requires dedicated optimisation (hierarchy between physics requirements and running constraints)

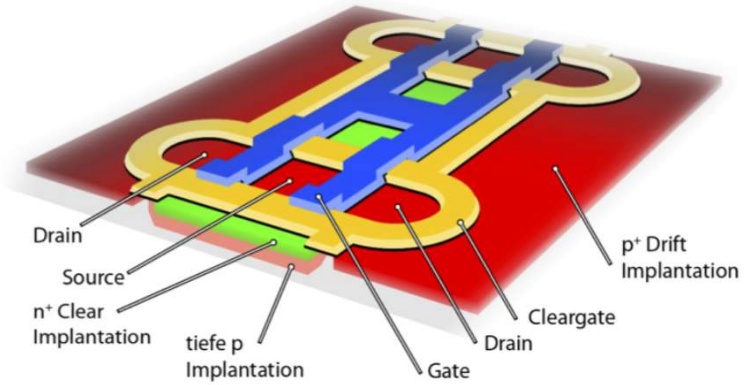


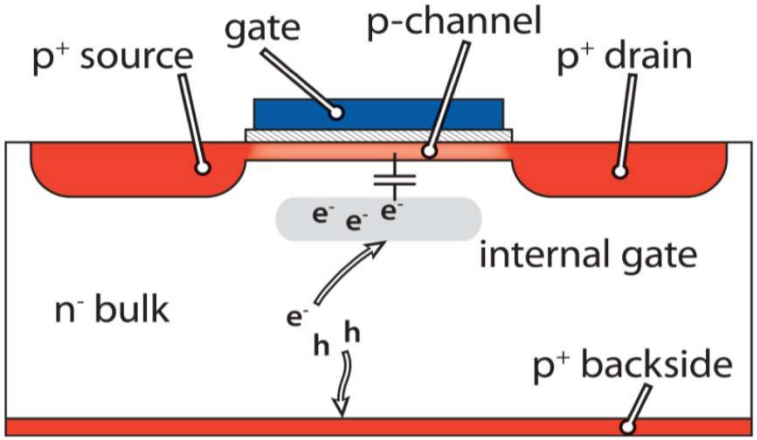
Progress Cycle



SOI Monolithic Pixel Detector

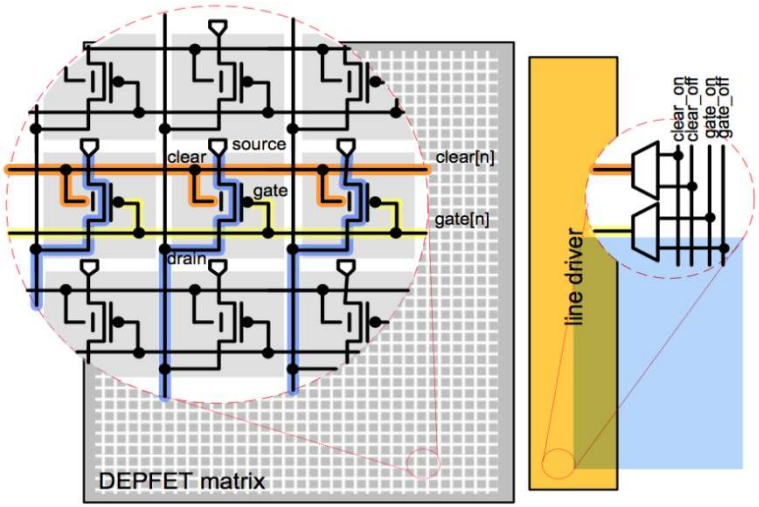
DEPFET (Depleted P-channel FET)

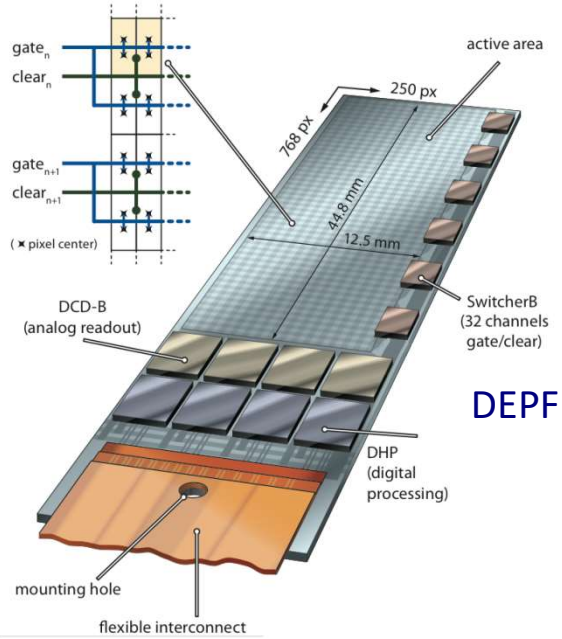




- Each pixel is a p-channel FET integrated in a completely depleted bulk
- A deep n-implant creates a potential minimun for electrons under the FET gate (internal gate)
- Internal gate is capacitive coupled to the FET gate
- The drain current is proportional to then number of electrons collected in the internal gate
  - Internal gain: $g_q \sim 500$ pA/e$^-$

DEPFET Pixel Array

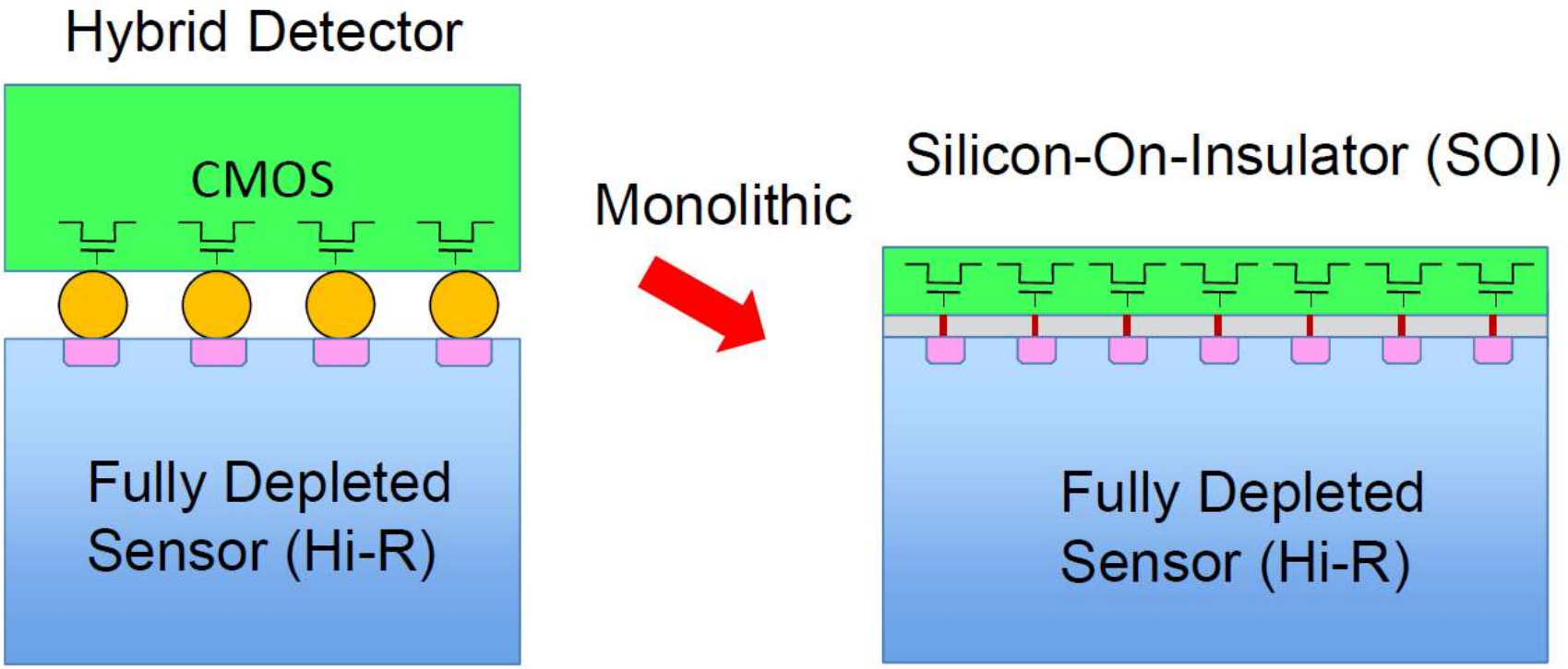




DEPFET half ladder

- Gate and Clear lines need switcher steering chip
- Row-wise readout (for Belle II 4 rows are read at time – 20 µs/frame)
- Long drain read out lines keep most of the material out of the acceptance region
- Only “activated" rows consume power
  - The others rows are still sensitive to charge
  - Low power consumption

SOI



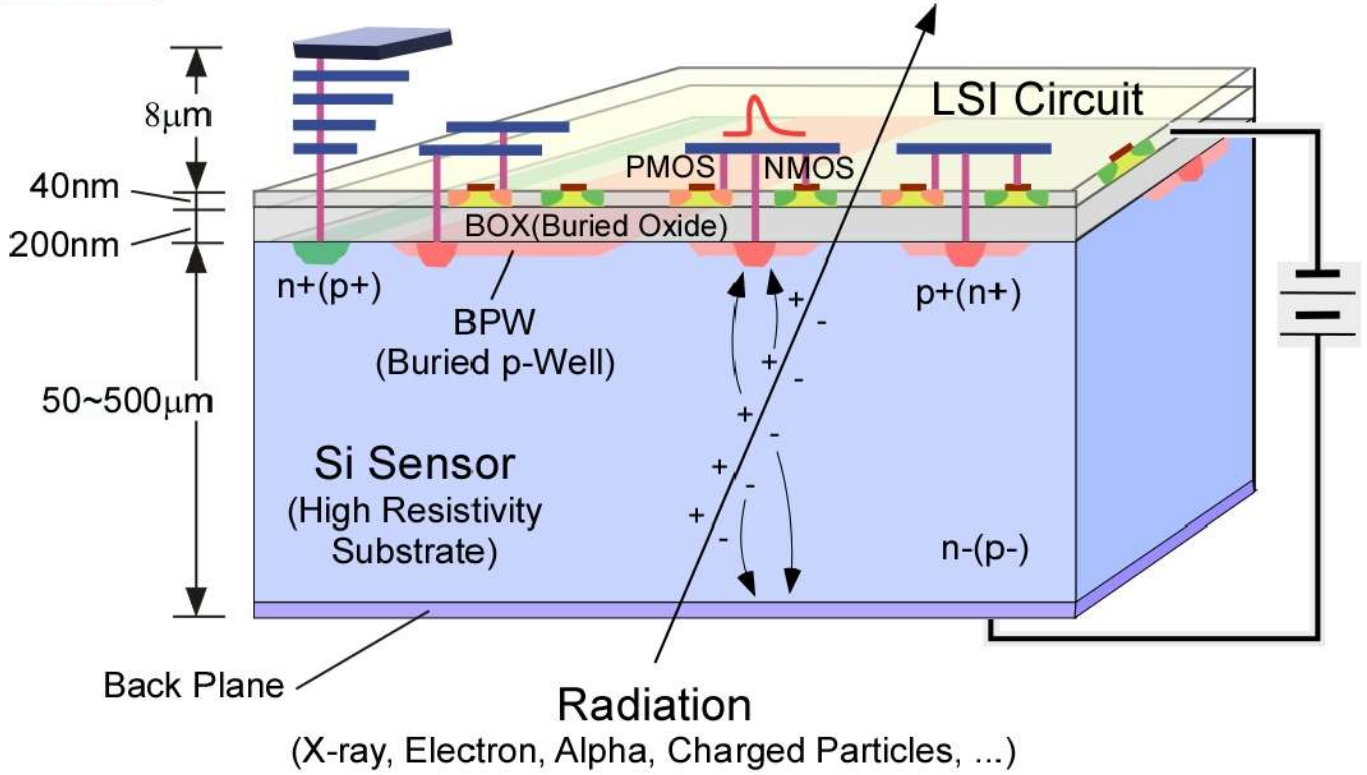
To use SOI technology for pixel detector is already discussed in 1990(*).

(*) Jean-Pierre Colinge, 'An overview of CMOS-SOI technology and its potential use in particle detection systems', NIM A305 (1991) 615-619.

Ref. Y. Arai, SOI Monolithic Pixel Detector Technology, Vertex-2016

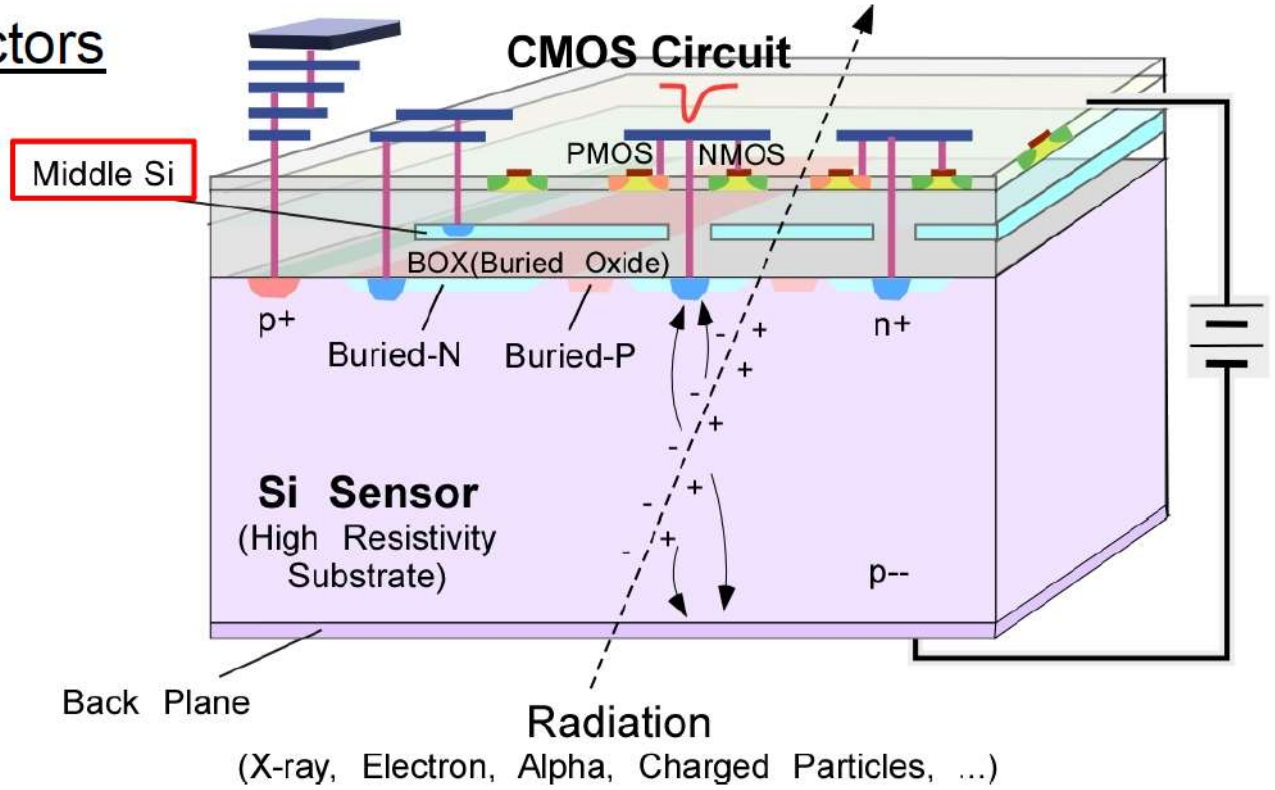
SOIPIX Detector (Single)

SOIPIX Detector (Single)



Single SOI Detector
- Buried-Well shield back-gate potential
- Good for Integration-type sensor
- Relatively Low radiation applications

SOIPIX Detectors (Double)



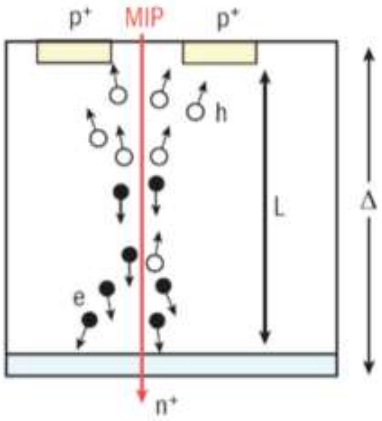
Double SOI Detector
- Middle Si layer shields coupling between sensor and circuit.
- It also compensate E-field generated by radiation trapped hole.
- Good for Complex function and Counting-type sensor.
- Can be used in High radiation environment.

Sensors for Hybrid Pixels

- Hadron fluency (2 10^{16}/cm²) ➔ Silicon sensor bulk damage
  - Charge trapping reduces dramatically minority carriers lifetime (signal loss by recombination)
  - Mitigation: reduce drift time (distance)

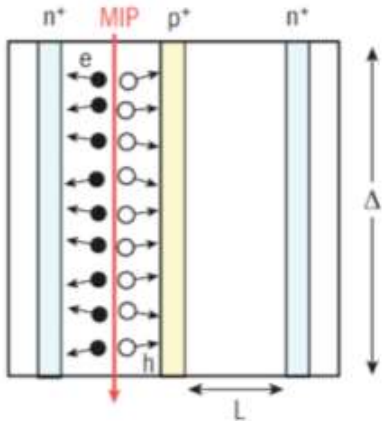
Thin-Planar Sensor

- Drift length L < 200 µm (now: 300 µm)
- L = Δ ➔ thin sensor = reducing the signal amp.
- n-in-p (e signal)
- Outer and possibly also innermost layers/rings



3D Silicon Sensor

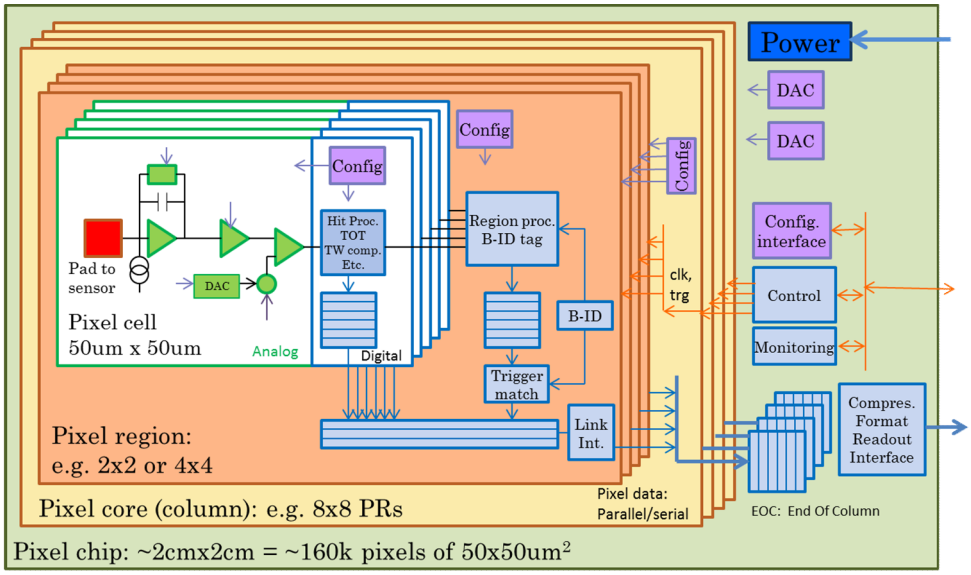
- L << Δ (L less than 50 µm)
- Reduced collection time and depletion voltage
- Less trapping probability ➔ high Rad-Hard
- More complex, lower yield higher cost
- Higher capacitance (more noise)
- Non uniform spatial response
- Inner layer (at most one)



Pixel Readout Chip for ATLAS and CMS at HL-LHC (RD53)

- Extremely challenging requirements for HL-LHC
  - Extreme hit rates: 3 GHz/cm², innermost layer for 200 pileup events
    - ⋆ High granularity: small pixels: 50 x 50 µm² (25 x 100 µm²) with 25 ns tagging
  - Extreme radiation load: 1 Grad, 2x10^{16} 1MeV n_{eq}/cm² over 10 years
  - High readout rate: ~1 MHz ➔ very high data throughput, O(1 Gbit/s per cm²)
  - Long trigger latency ~10 µs (hit buffering requirements increased by a factor 100)
  - Large chip ~2x2 cm² (~1 billion transistors)
  - Low mass, « low » power consumption, « exotic = serial » powering schema

Baseline Technology: 65 nm



Full Scale Demonstrator Chip in August 2017