LHCb SciFi 电子学工作进展

Ming Zeng[1], Guanghua Gong[1], Zhenwei Yang[1], Yuanning Gao[1],
Albert Comerma[2], Xiaoxue Han[2]

[1]Department of Engineering Physics, Tsinghua University
[2]Physikalisches Institut, Universität Heidelberg

June 28th 2018 @ LHC实验物理分析及探测器升级研讨会, 威海

LHCb Tsinghua Group

- Professors： Yuanning GAO，Zhenwei YANG，
- Ming ZENG，Guanghua GONG

- Postdoc： Adam Davis (Scifi Testbeam Simulation)
- Biplab Dey (CCNU，SciFi Track Reconstruction)

- Ph.D. Students： Yuyan Huang (PACIFIC Quality Assurance System)
- Jirong Cang (SciFi Detector Performance Study)
- Yuyue Gan (PACIFIC Quality Assurance System)
- Mengzhen Wang (SciFi simulation and track reconstruction)
- Liupan An (SciFi simulation and track reconstruction)

SciFi readout electronics (FE)

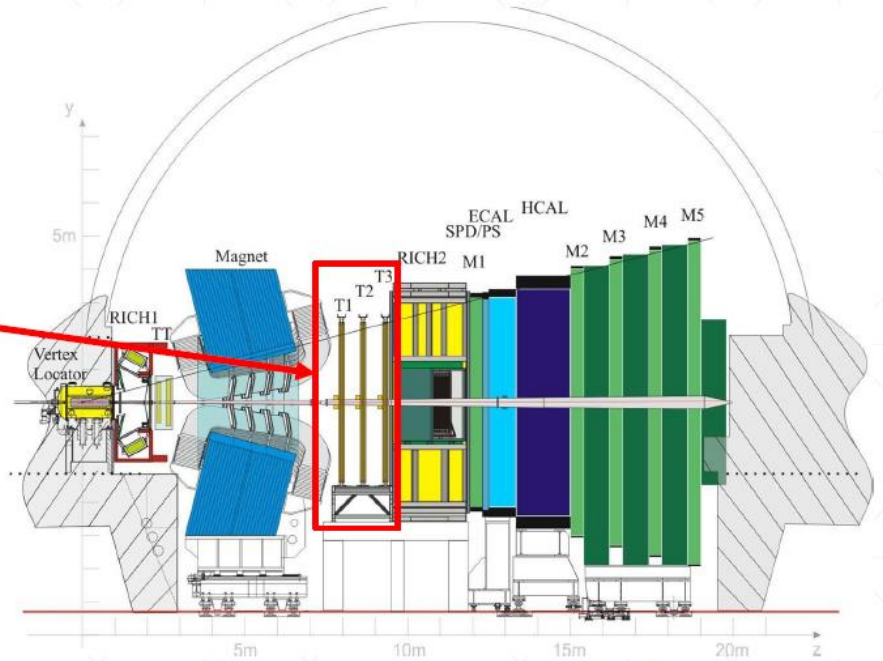
LHCb Upgrade

Goal: increase statistics by more than ×10

- operate at 2×10^{33} cm^{-2} s^{-1} → 50 fb^{-1}
- triggerless 40 MHz readout

the current Tracking Stations
(Gas Straw Tube Tracker + Silicon Tracker)
replaced by
Scintillating Fibre (SciFi) Tracker

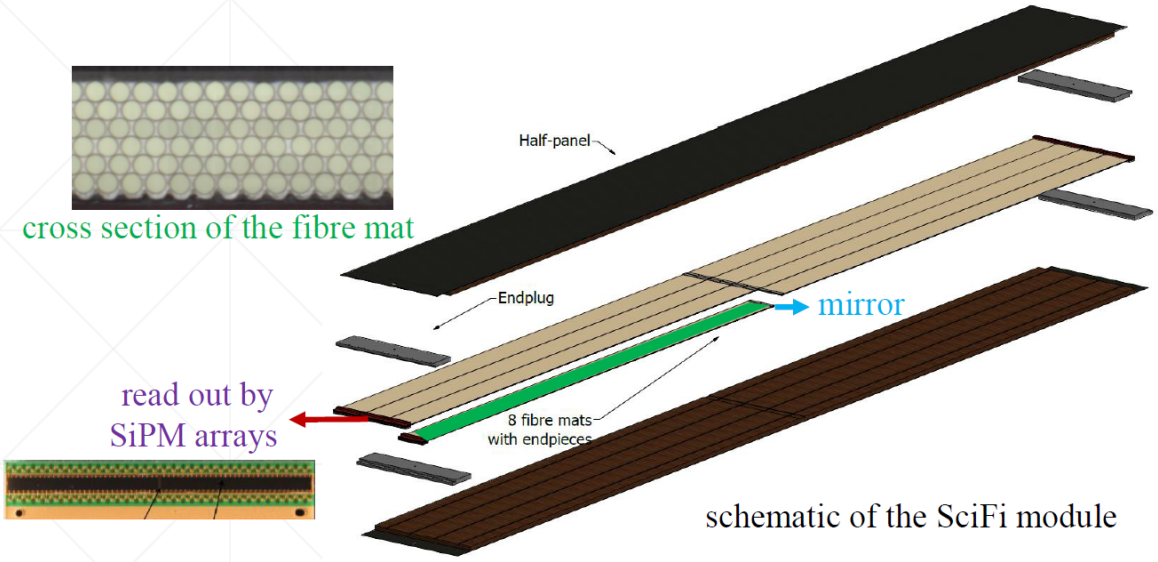
- ✓ fast, high efficiency (~99%)
- ✓ high granularity (250μm)
- ✓ high resolution (<100μm)
- ✓ low mass (<1% X_0 /layer)
- ✓ radiation hardness (up to 35 kGy)



Schematic view of the current LHCb detector

SciFi readout electronics (FE)

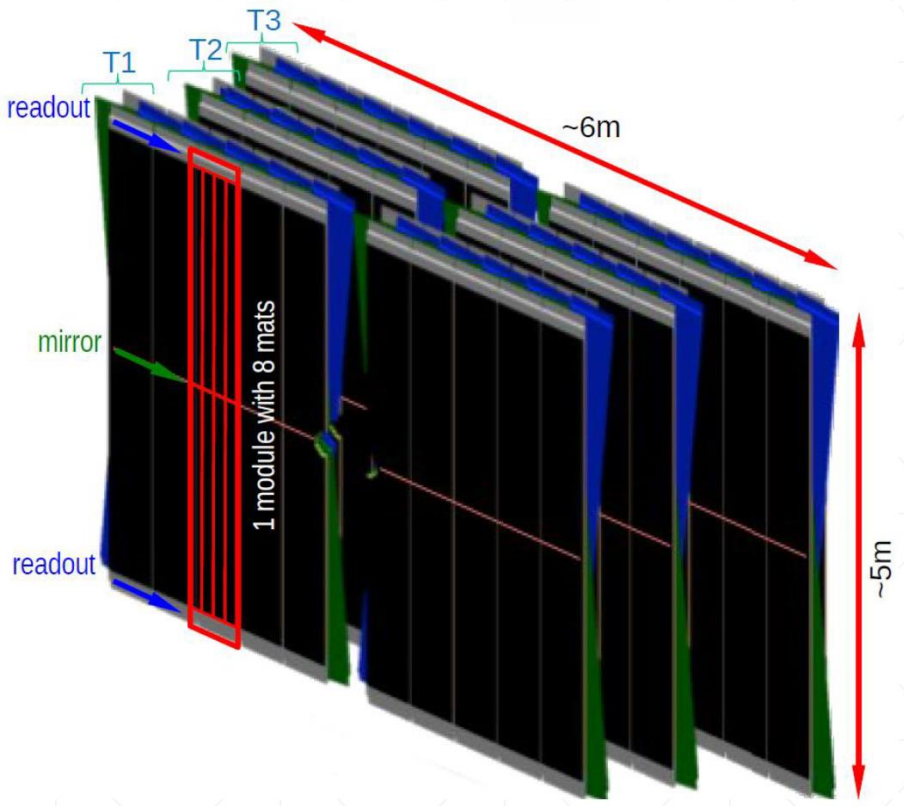
- 250μm diameter scintillating fibre wound into a 6-layer 2.4m-long fibre mat
  - ✓ one end equipped with a mirror
  - ✓ read out by 4× SiPM arrays
- 8 × fibre mat + honeycomb = sandwich-structure 0.5m × 5m module



SciFi readout electronics (FE)

- 128 × modules
- 12 × detector layers (X-U-V-X, 5°)
- 3 × Tracking Stations

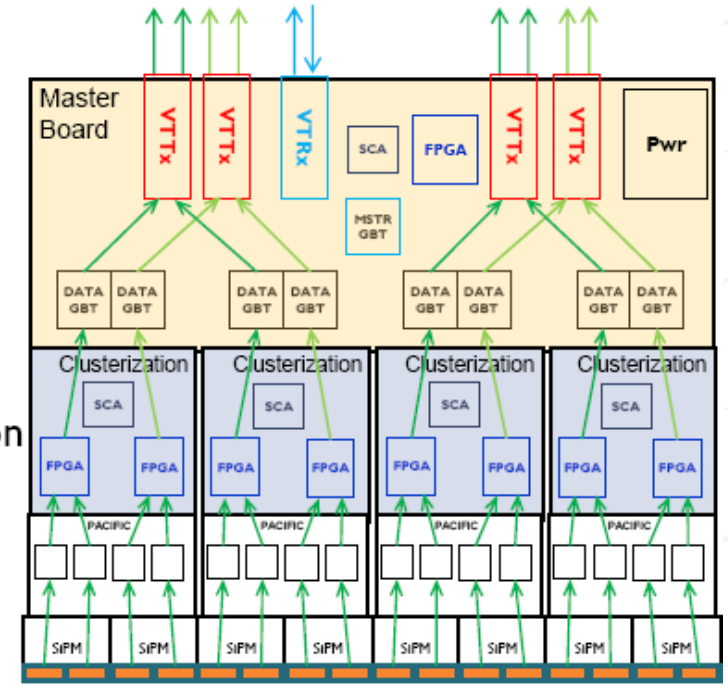
- 11,000 km of fibres
- 524k SiPM channels
- ~340m^2 total active surface

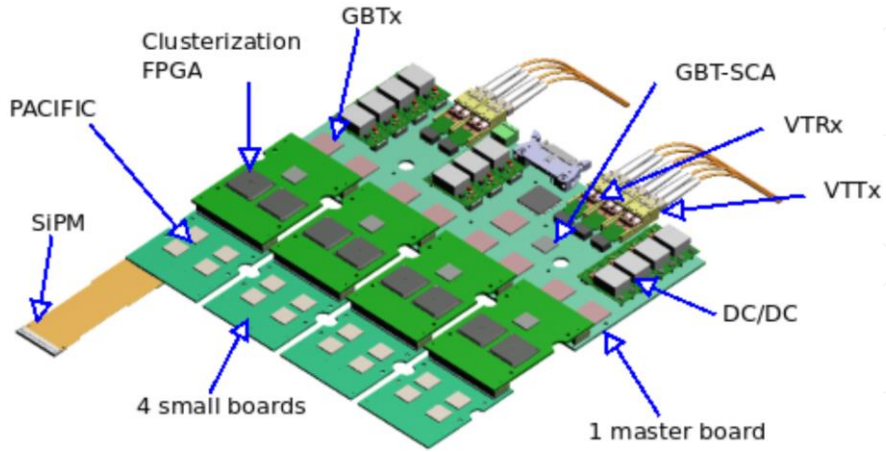


SciFi readout electronics (FE)

½ ROB electronics

- Master Board
  - Master GBT → TFC/ ECS distribution
  - Data GBTs → Data serialisation
  - Power supplies
  - Versatile link optical components
- Clusterization board
  - FPGA based Clustering algoithm
  - SCA for slow controls → Clusterization FPGAs and PACIFIC ASICs
- PACIFIC Board
  - Amplifier, shaper, integrator and ADCs, 2b/channel output based on three threshold values
- SiPM: Silicon Photo Multiplier modules
  - 2 arrays of 64 channel avalanche photodiodes

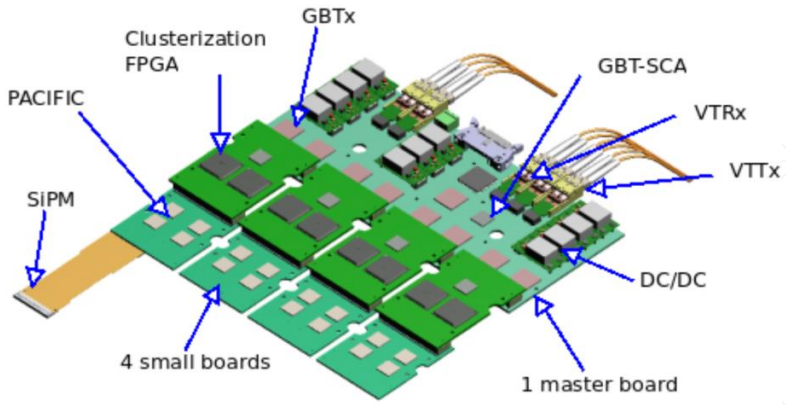


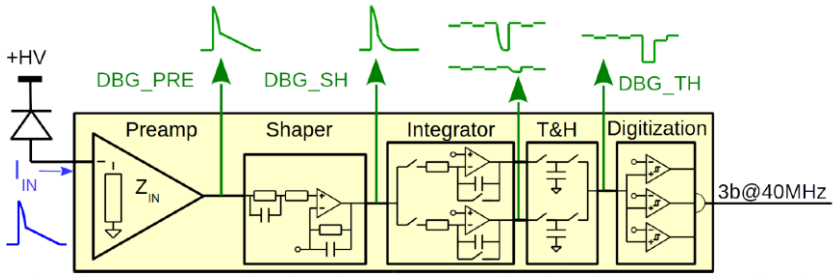


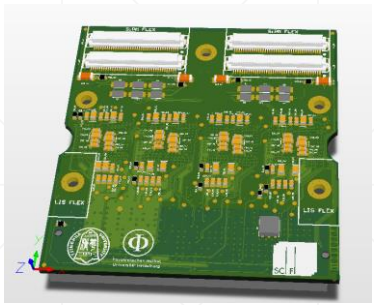
- **<100 µm Resolution (for momentum)**
- **~ 340 m² total active surface**
- **250 µm Scintillating Fiber**
- **524,000 SiPM Channels**

- **PACIFIC – 64 channel SiPM readout ASIC with 16 x 320 MHz digital outputs**
- **> 12,000 Chips needed**
- **> 2,500 Frontend Electronics PACIFIC Boards**

LHCb SciFi Tsinghua Group

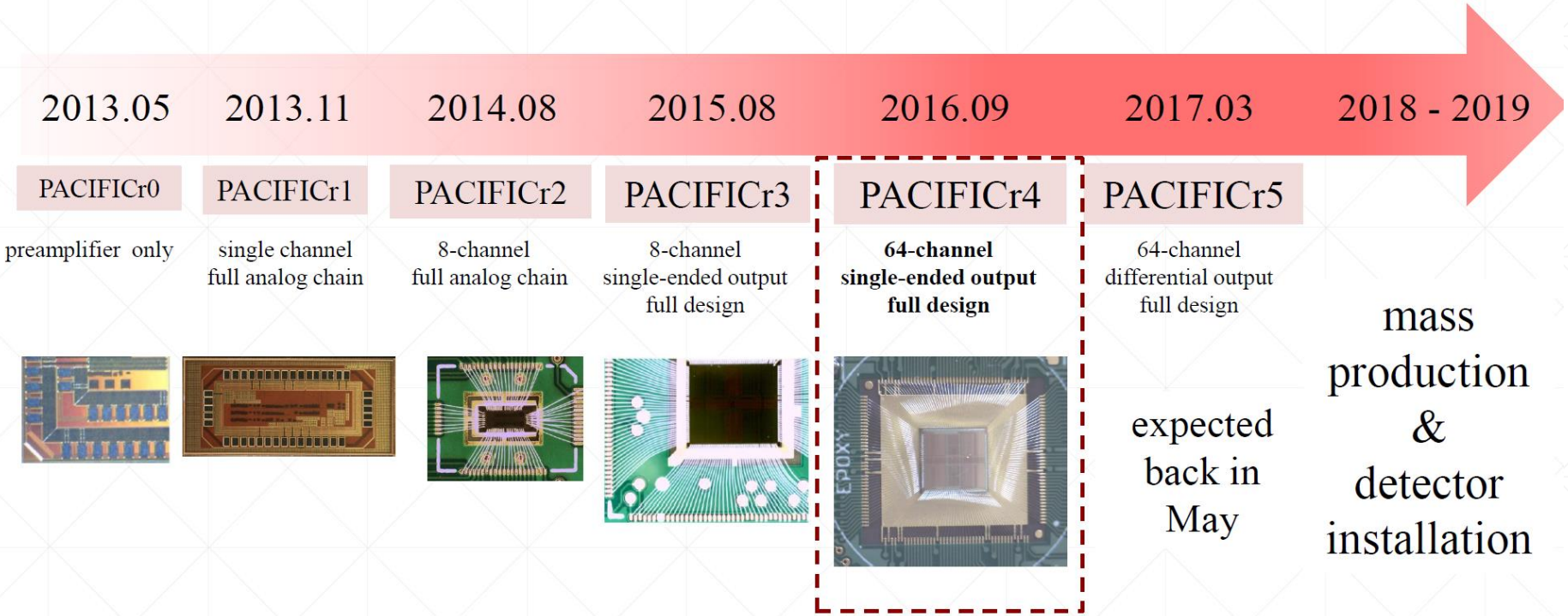






- **LHCb China Group:**
  - **Re-design SciFi Frontend Electronics Boards**
  - **SciFi Readout Electronics (PACIFIC) Quality Assurance System (for chips, and frontend boards)**
  - **Manufacturing ALL Frontend Boards (2,500 boards) in China**
  - **Testing and calibrating half of PACIFIC ASICs & Frontend Boards**
  - Readout Electronics for Detector Performance Evaluation (> 20 Setups in SciFi Group)

PACIFIC ASIC



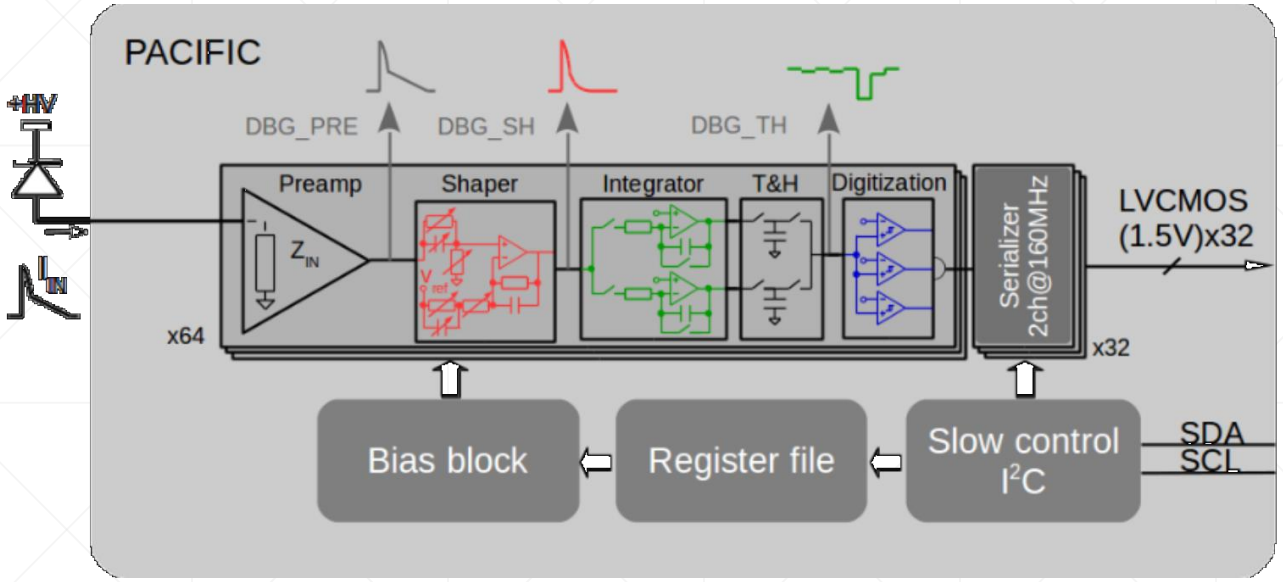
PACIFIC ASIC

PACIFIC a low Power Asic for the sCIntillating FIbre traCker

- 64-channel current mode input
- configurable fast shaper : minimize spillover
- interleaved gated-integrators per channel: minimize dead time
- 2-bit non-linear digitisation per channel : minimum data for sufficient tracking information
- adjustable input anode DC voltage (4-bit DAC, 50mV/LSB)

power consumption <10mW/channel

CMOS 130nm Technology

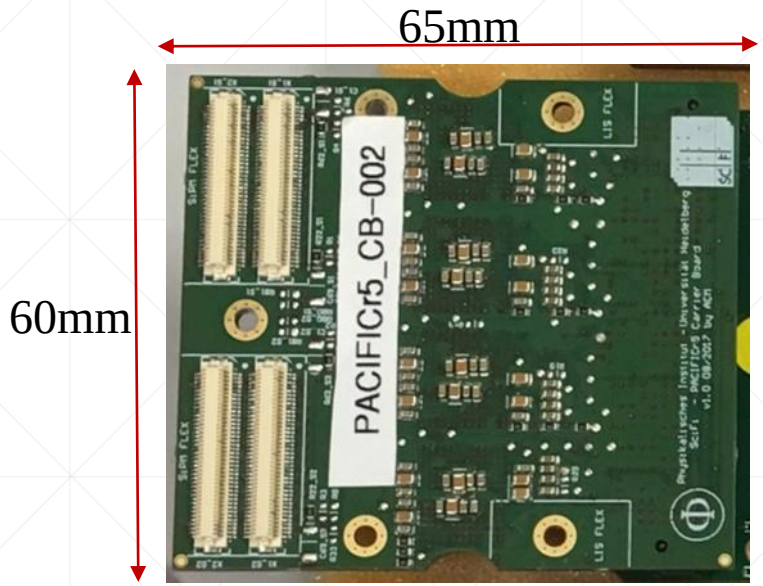


V5 PACIFIC:
320MHz SLVS differential output

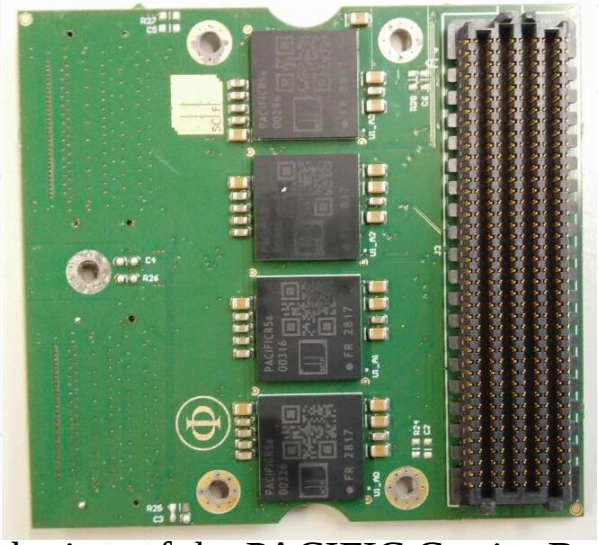
- MORE THAN
- 10K CHIPS NEEDED

PACIFIC Carrier Board

- 4 × PACIFIC ASICs (196-pin BGA packaged)
- 4 × temperature measurement circuits (voltage divider circuits with NTC , 2 for SiPMs, 2 for the ASICs)
- 4 × SiPM bias voltage measurement circuits (voltage divider circuits)
- 1 × BoardID IC (DS2401 64-bit unique, factory-lasered silicon serial number, no permanent damage up to 140Gy)
  http://radwg.web.cern.ch/RadWG/Pages/showExternal.aspx?GotoUrl=https://twiki.cern.ch/twiki/bin/viewauth/Main/TulliosPreferredPartList
- 4 × SiPM flex cable connectors (Hirose DF12(3.0)-80DS-0.5V)
- 1 × FMC connector (ASP-134602-01)



front view of the PACIFIC Carrier Board

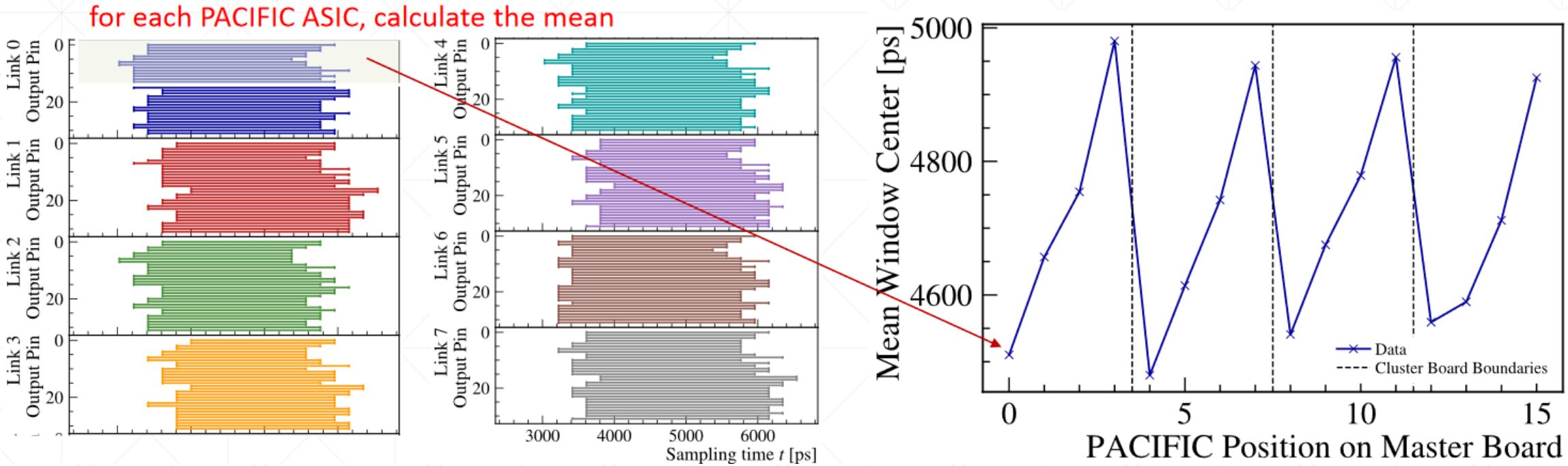

back view of the PACIFIC Carrier Board

A question raised last month (1)

Daniel´s result shown in last SciFi GM meeting

(https://indico.cern.ch/event/721309/contributions/3011775/attachments/1653078/2644967/ElectronicsStatus_0518_SciFiGM.pdf)

different offset of the sampling window across all data output, reduce the sampling window **from 2.4ns to 1.4ns** …



A question raised last month (2)

Together with Wilco and Magali, we checked the routing of the boards :

- we do find some not-optimized routing length on the PACIFIC CLK lines
- the FPGA firmware probably also has some contributions, still under investigation

	PACIFIC Carrier Board (PB)		Cluster Board (CB)		PB+CB
	SYNC routing (mm)	PACIFIC CLK routing (mm)	SYNC routing (mm)	PACIFIC CLK routing (mm)	PACIFIC CLK routing (mm)
ASIC0	35.403	72.142	15.01	100.62	172.762
ASIC1	36.122	59.917	13.27	100.63	160.547
ASIC2	32.245	42.848	13.93	87.27	130.118
ASIC3	37.467	32.794	12.32	91.88	124.674
maximum difference between four ASICs	5.222	39.348	2.69	13.36	48.088

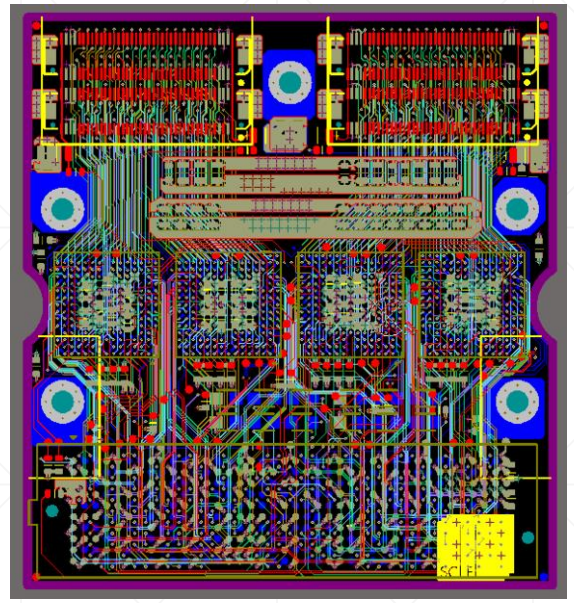
PACIFIC CLK on the master board side , routing difference across all ASICs is < 1mm, too small to be counted in this table

Redesign of PACIFIC Carrier Board

We decided to re-optimize the routing of the PACIFIC Carrier Board

- for a higher production yield
- more strict routing constrains, to gain some margin for the sampling window size

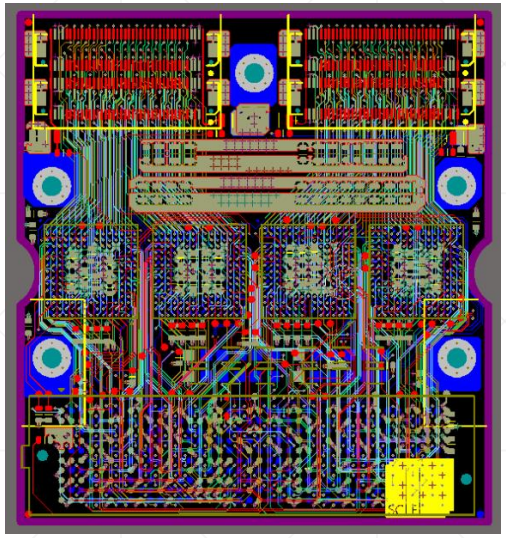
- 4 pairs of PACIFIC Clock lines (CLKIN_0~3) : routing length match < 1mm
- 4 SYNC lines (SYNC_0~3): routing length match < 1mm
- 64 pairs of data lines (DATA_0~3_X) : routing length match <3mm.
- well seperate the analog input signals and the output data lines, the CLOCK lines
- from 8-layers to 14-layers
- Calculate impedance for Halogen Free (TU-862HF), and keep thickness 1.7mm

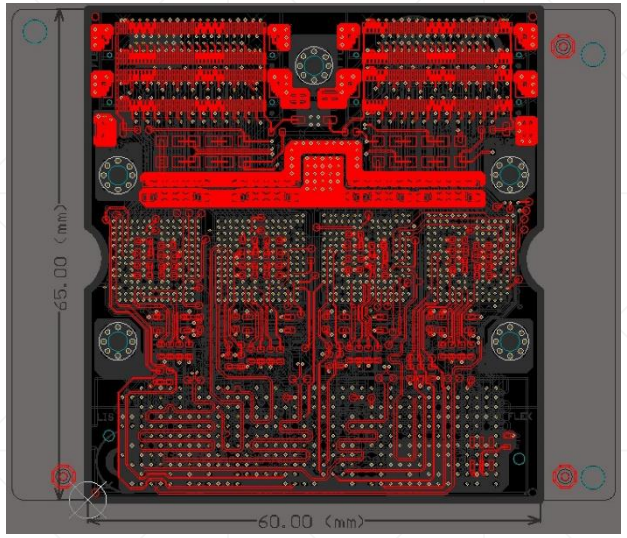


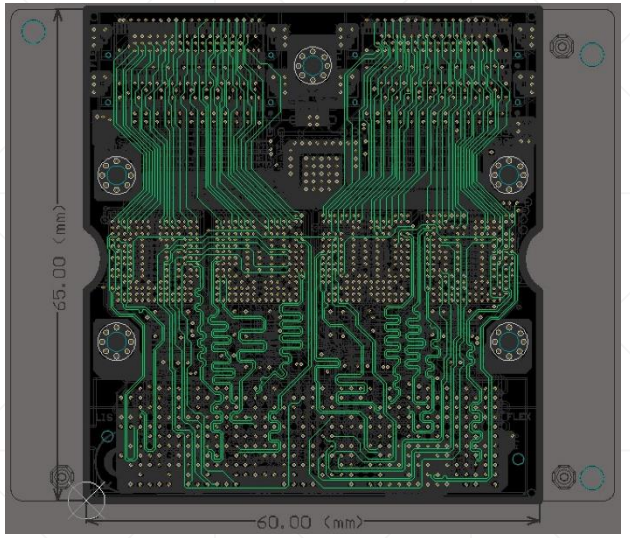
re-optimised PACIFIC Carrier Board r4

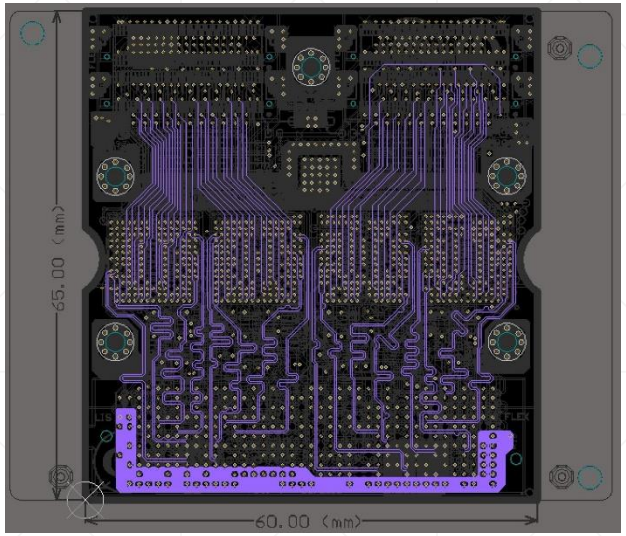
The design has been complete.
For the first 250 PACIFIC Carrier Boards, we will assemble first 10 PCBs, check with the SciFi full electronics (MB+CB) to make sure everything works fine after this optimization.

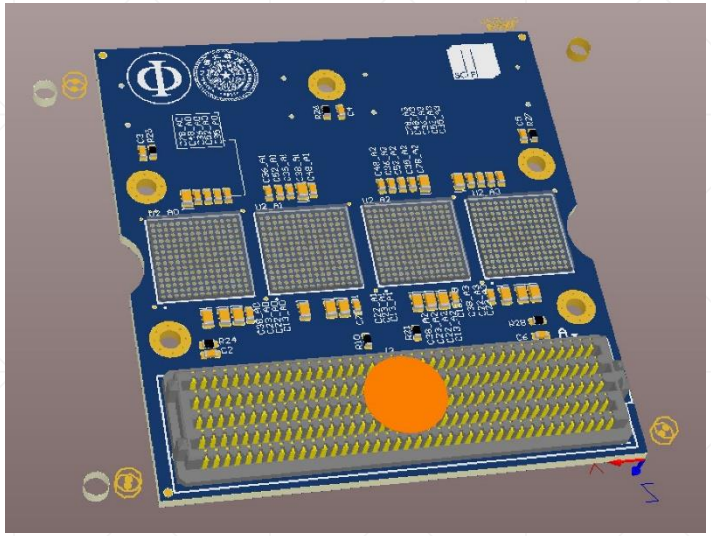
Redesign of PACIFIC Carrier Board

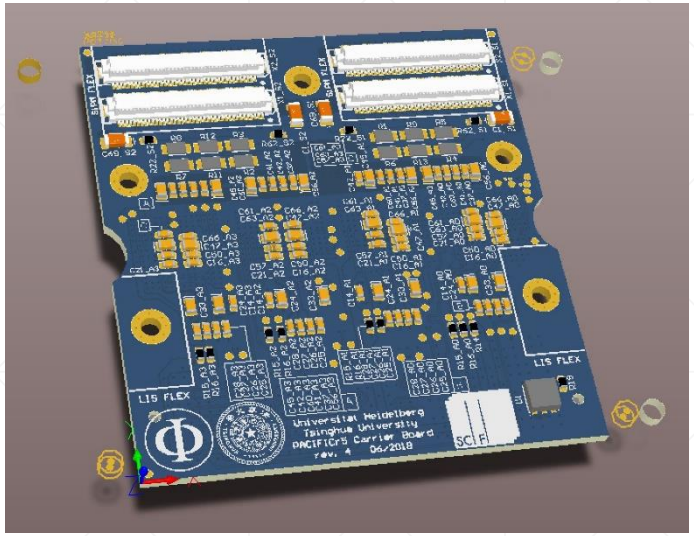








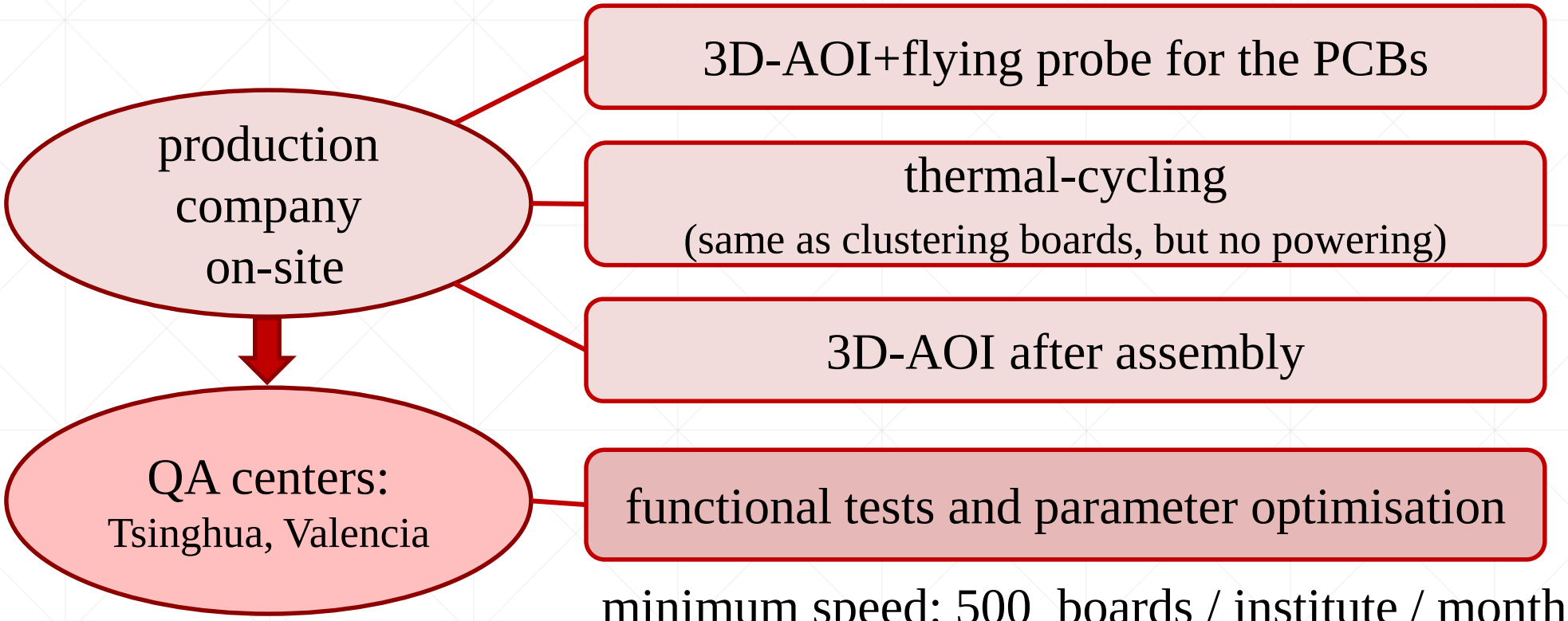




Selection of the production companies

Company	ShenZhen SinoFast Electronics （PCB + Assembly）	ShenZhen Fastprint Circuit Tech （PCB + Assembly）
PCB standard	IPC 600G class 3	
assembly standard	IPC-A-610E CLASS 2	IPC-A-610E CLASS 3
delivery schedule	15 days (10 pcs ~ 2500 pcs)	20 days
On-site QA facilities	✓ AOI for each layer (PCB) ✓ flying probe test: shorts and continuity (PCB) ✓ 3D AOI (assembly) ✓ X-Ray of BGA-packaged components (assembly) ✓ values of all passive component (assembly) ✓ thermal-cycling test (assembly, Fastprint)	
PROs	✓ same manufacturer for CMS GEM frontend boards	✓ Largest and first listed company of PCB manufacturer. ✓ thermal-cycling test
CONs	✓ IPC-A-610E CLASS 2 instead of CLASS 3 ✓ thermal-cycling test has to be done at Tsinghua	✓ longer delivery time

Quality Assurance (QA)



minimum speed: 500 boards / institute / month
<13mins/board

QA functional test setup

- custom designed test DAQ (PACIFICROB)
  [fully tested, 3 for Heidelberg (delivered), 3 for Barcelona, 3 for Valencia]
- FMC connector intermedia board [Finished, under test]
  simple pin-to-pin adapter PCBs
  to avoid broken FMC connectors on the DAQ side due to too many times plug-in and out
- DC power supply (with output 5V/3A at least)
- charge injection board [Finished, under test]
- arbitrary waveform generator
- linux PC

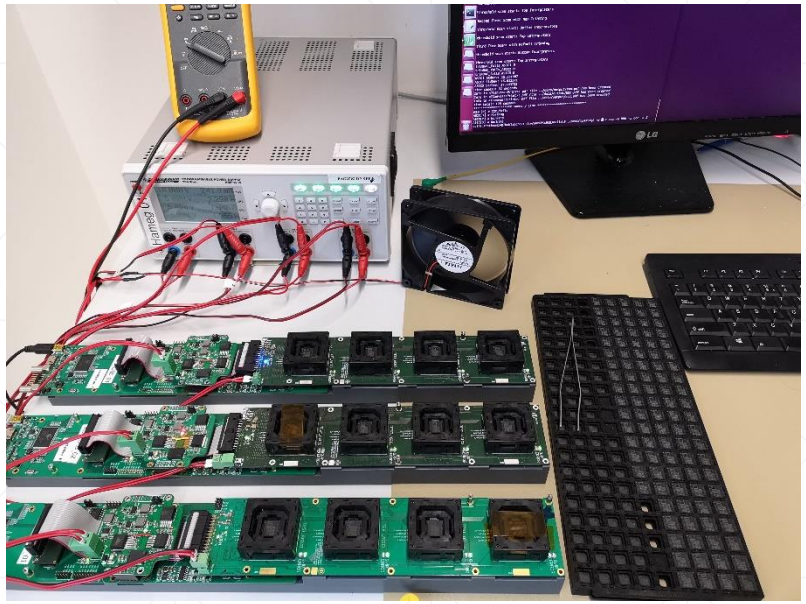
QA setup + procedure verified with the 1420 packaged ASICs last week !

PACIFIC5 Carrier Board

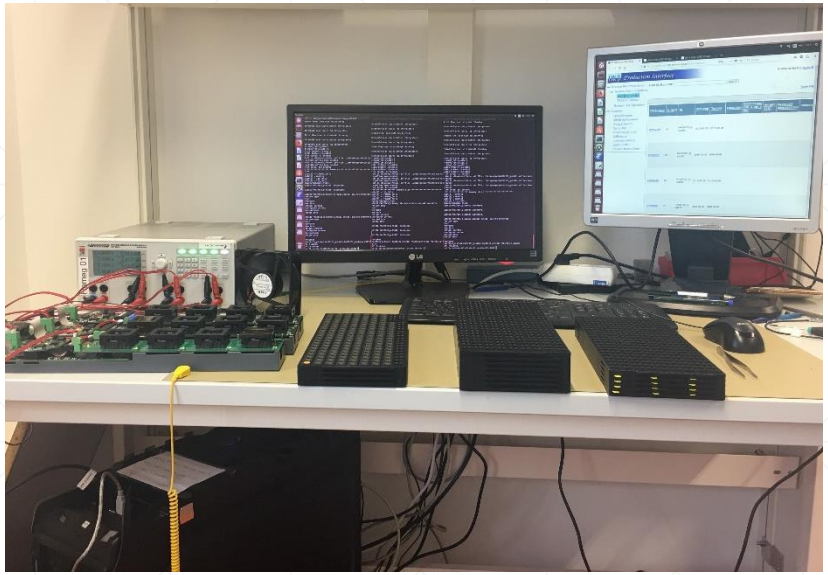
PACIFICROB

test automatically update result to DB

final check the QA test routine



QA test running : 10 ASICs/run , ~100ASICs/hour



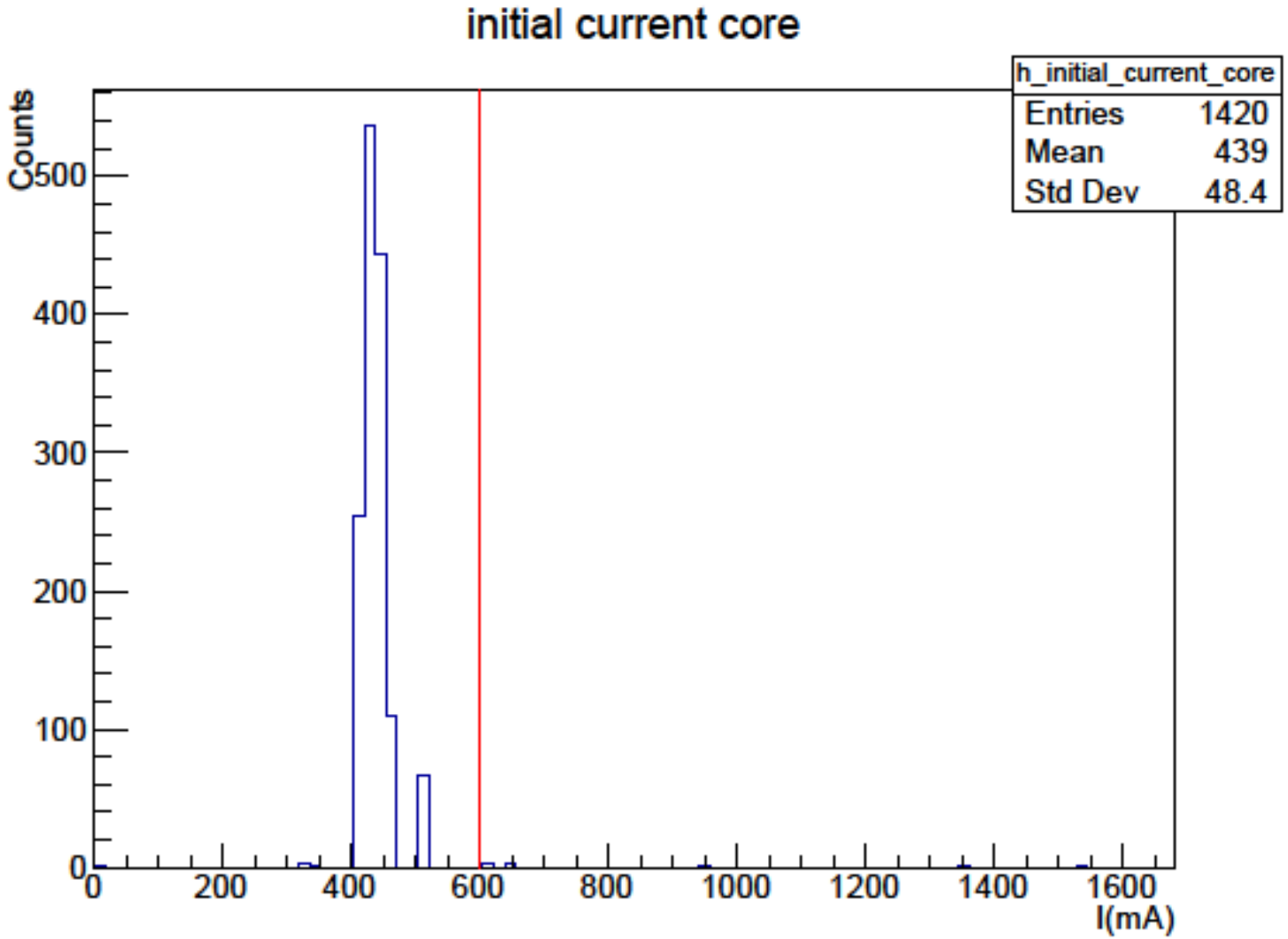
finish all ASICs test

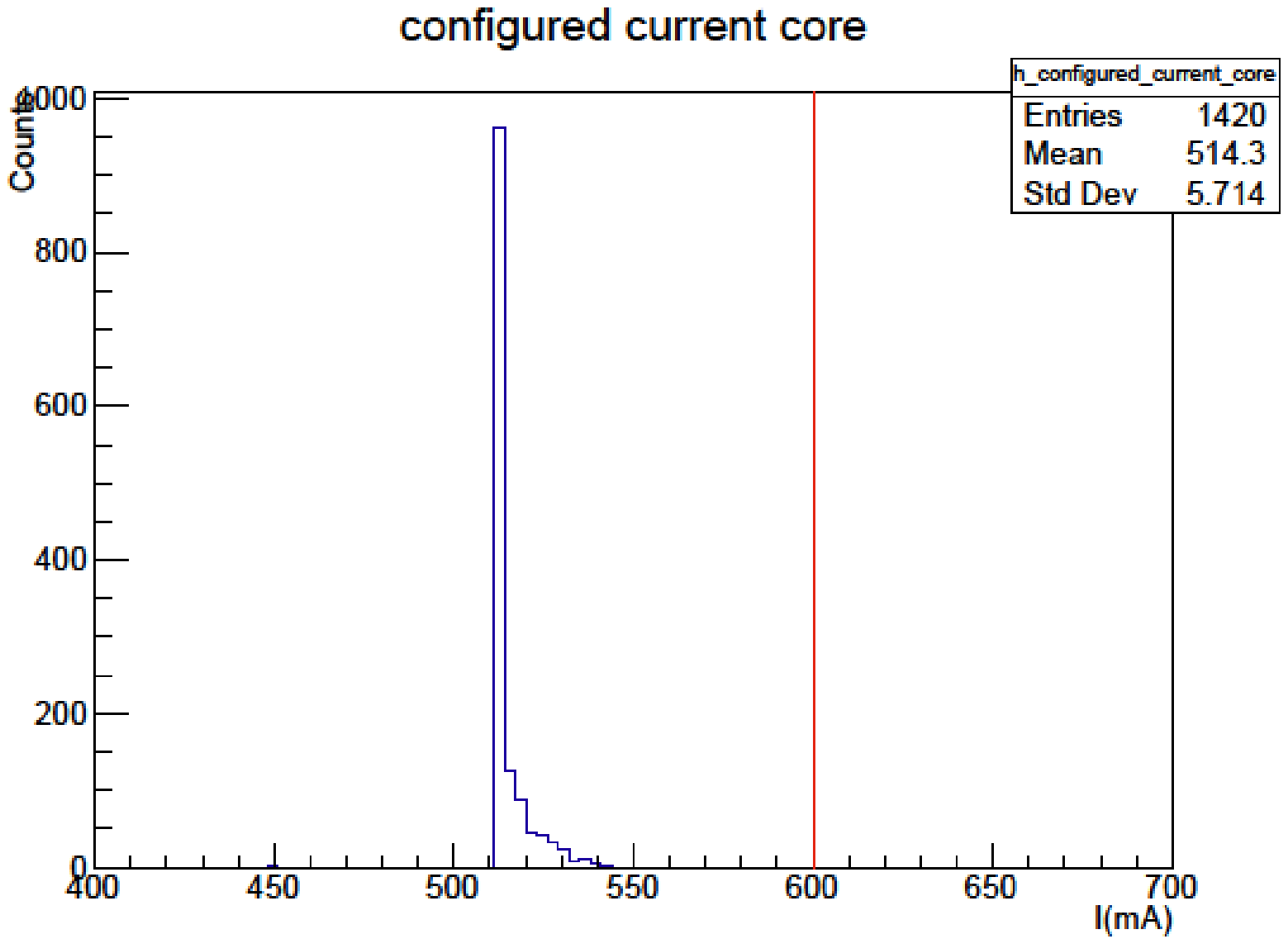
All results can be found in SciFi Production DB

https://scifi.physi.uni-heidelberg.de/db/prod/

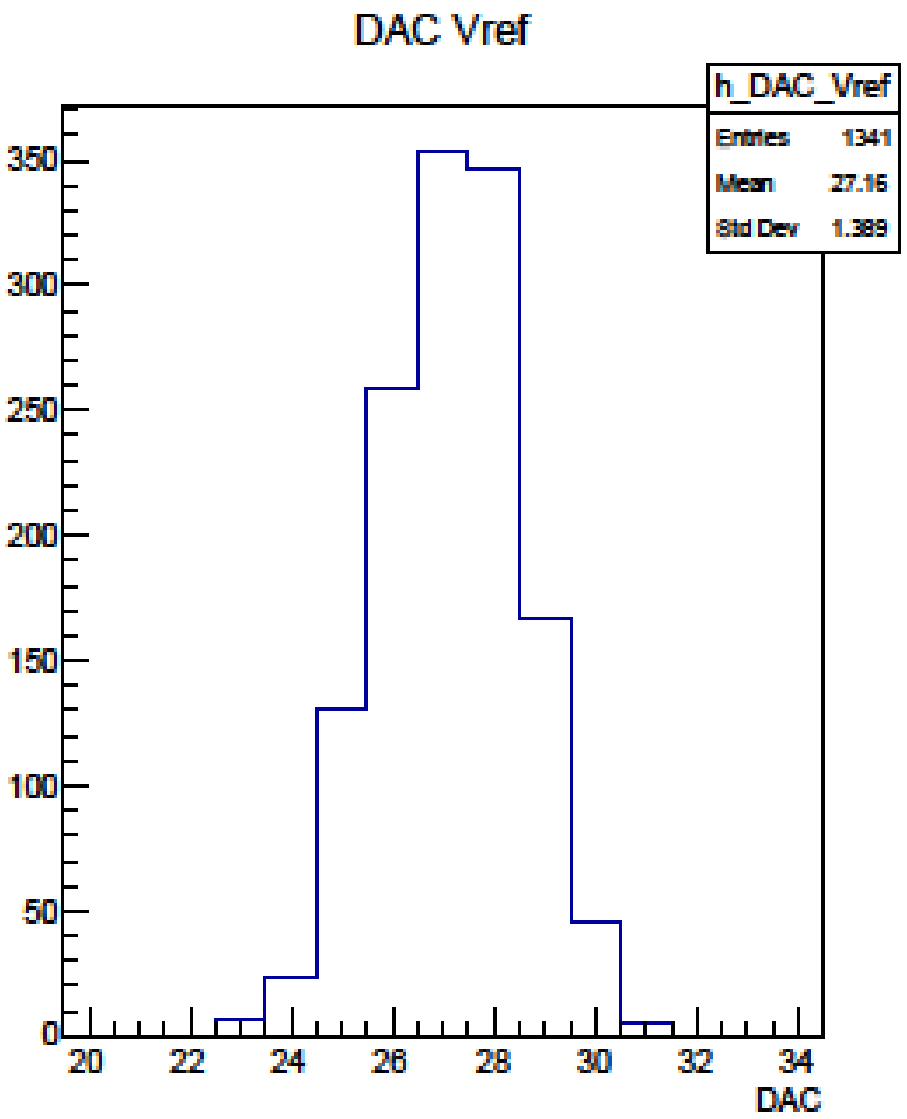
Inventory	Origin	ID	Arrived	Tested	Location	Dimensions [mm x mm x mm]	Weight [kg]	Material composition	Comment	Initial current [mA]	Configured current [mA]	Failure	Vref	VrefDCPB	Summary report [.pdf]	Raw data [.root]	PACIFIC Boards	
EPA00009	PI	PACIFIC5_Q-Adummy	2018-05-26	2018-06-07						0	0	I2C fails	0	0	-	rawData_AsicQA_testsystem8_ASICID_PACIFIC5_Q-Adummy.root 2018-06-07 19:48:46 by Xiaoxue Han	0	Modify
EPA00010		PACIFIC5_Q-A2104	2018-05-26	2018-06-07						434.4	511.8	trimDAC fails	27	6	PACIFIC5_Q-A2104.pdf 2018-06-07 20:21:10 by Xiaoxue Han	rawData_AsicQA_testsystem8_ASICID_PACIFIC5_Q-A2104.root 2018-06-07 19:48:50 by Xiaoxue Han	0	Modify
EPA00011	PI	PACIFIC5_Q-A2105	2018-05-26	2018-06-07						411	511.8	Working	25	9	PACIFIC5_Q-A2105.pdf 2018-06-07 19:48:55 by Xiaoxue Han	rawData_AsicQA_testsystem8_ASICID_PACIFIC5_Q-A2105.root 2018-06-07 19:48:58 by Xiaoxue Han	0	Modify
EPA00012	PI	PACIFIC5_Q-A2106	2018-05-26	2018-06-07						458.8	515	Working	29	9	PACIFIC5_Q-A2106.pdf 2018-06-07 19:49:02 by Xiaoxue Han	rawData_AsicQA_testsystem8_ASICID_PACIFIC5_Q-A2106.root 2018-06-07 19:49:05 by Xiaoxue Han	0	Modify

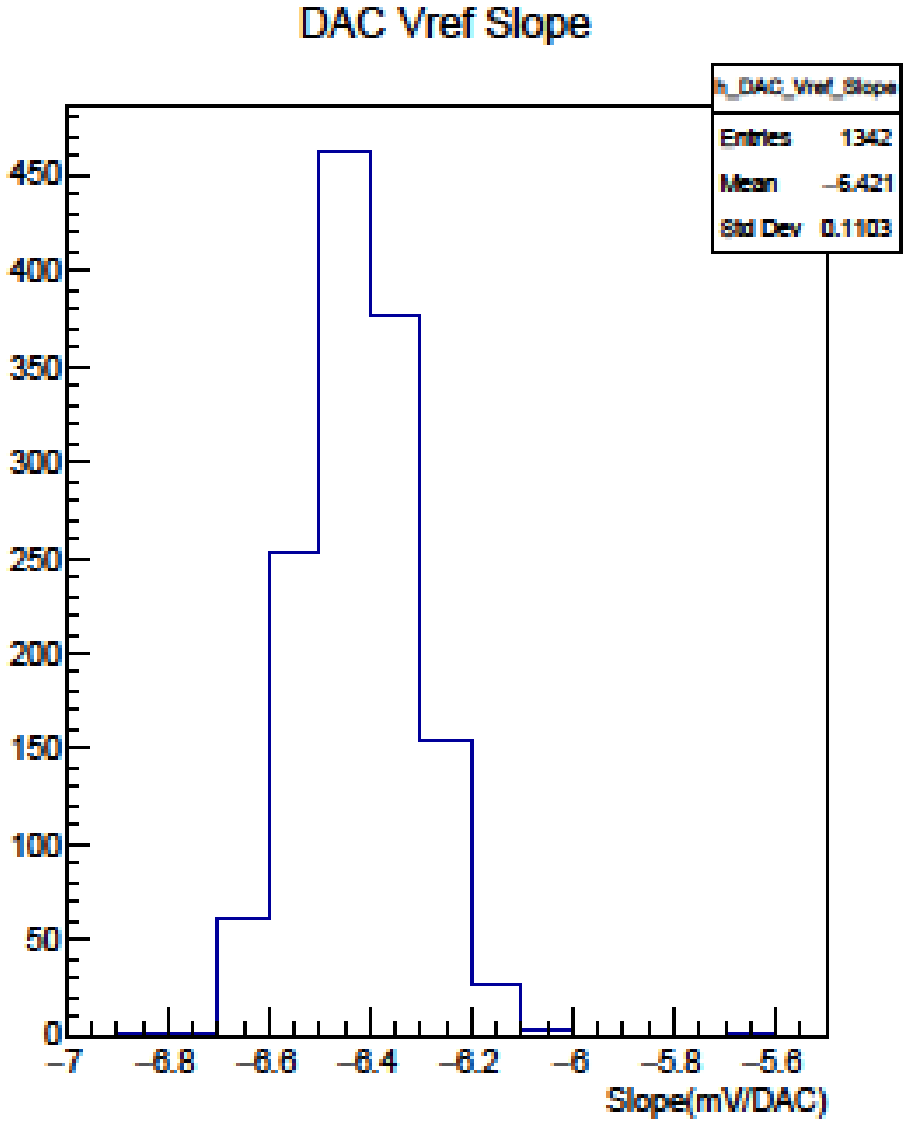
PACIFIC5q Test Result



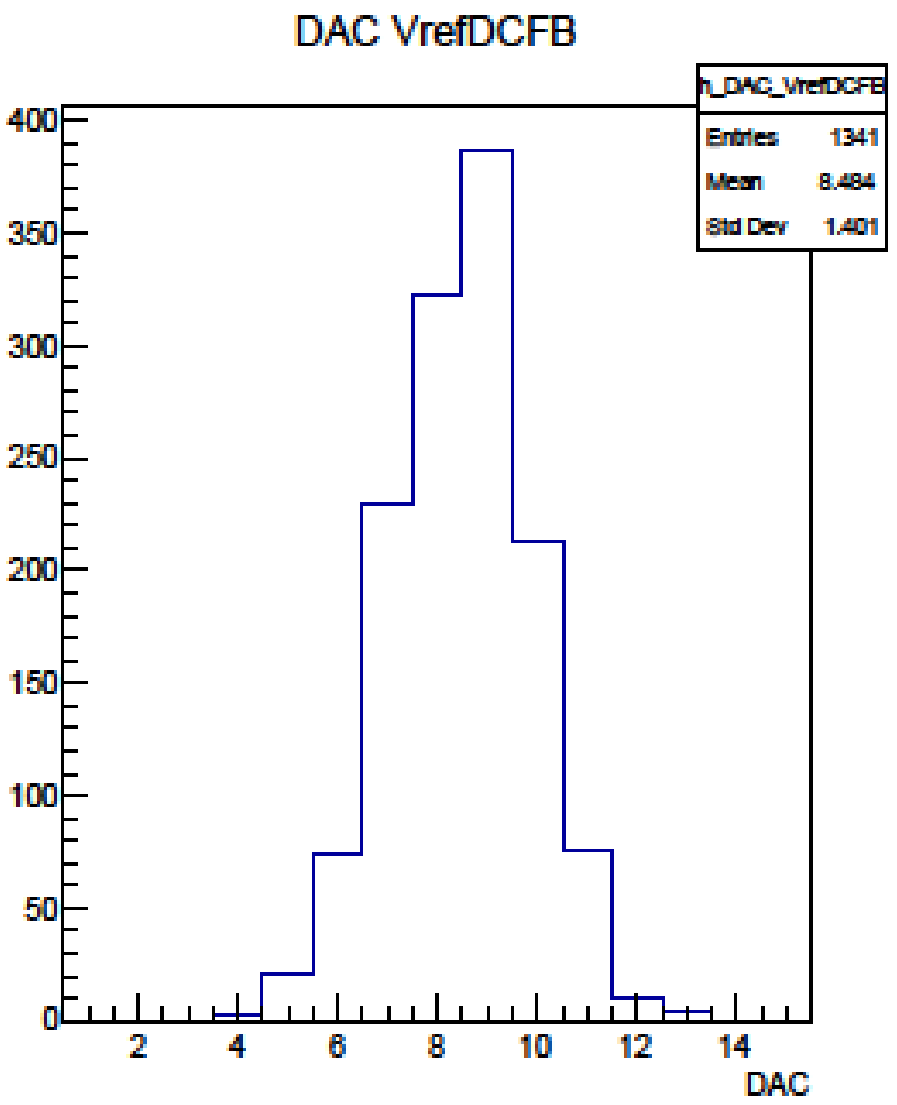


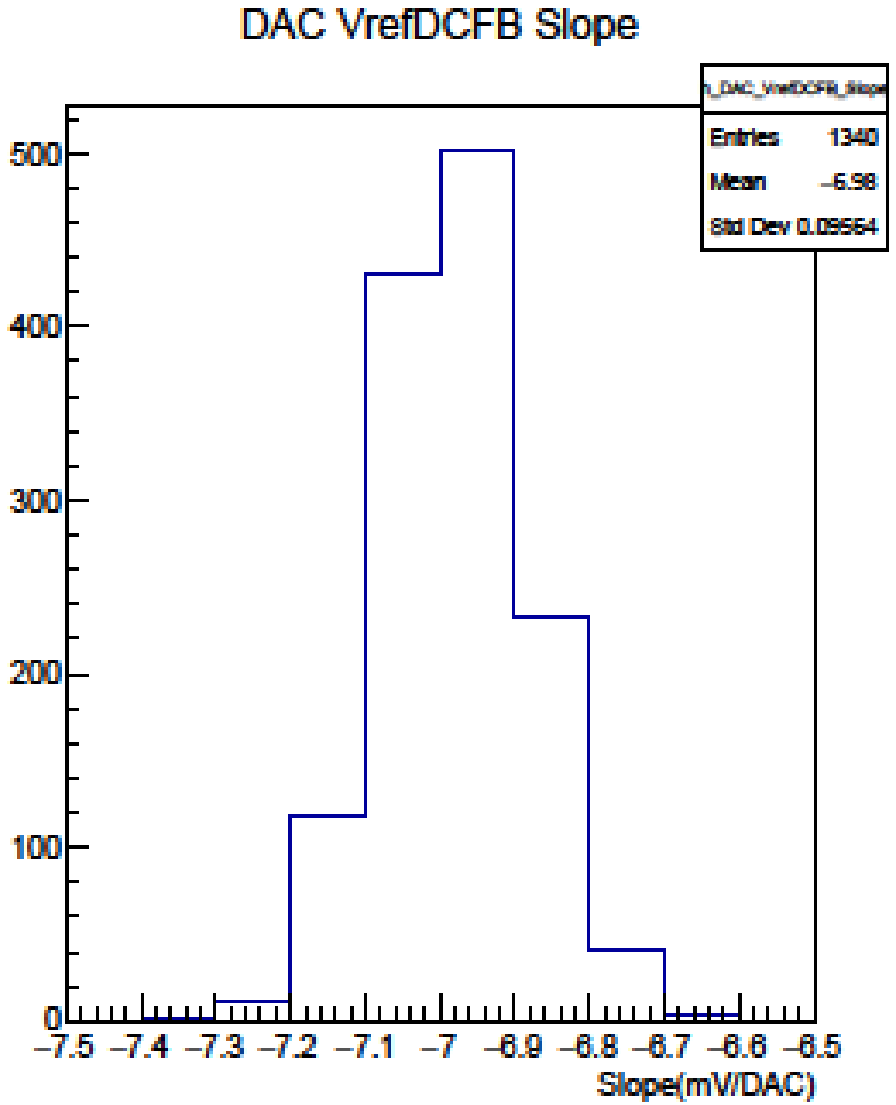
PACIFIC5q Test Result



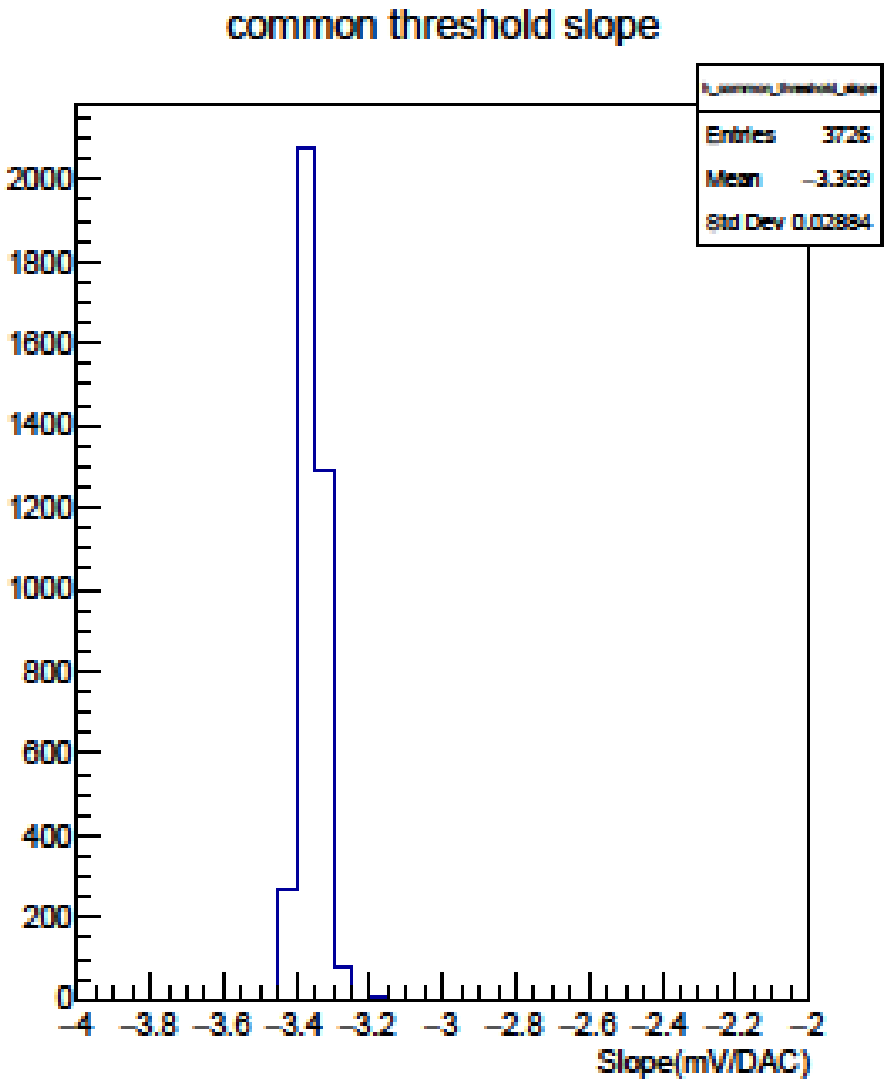


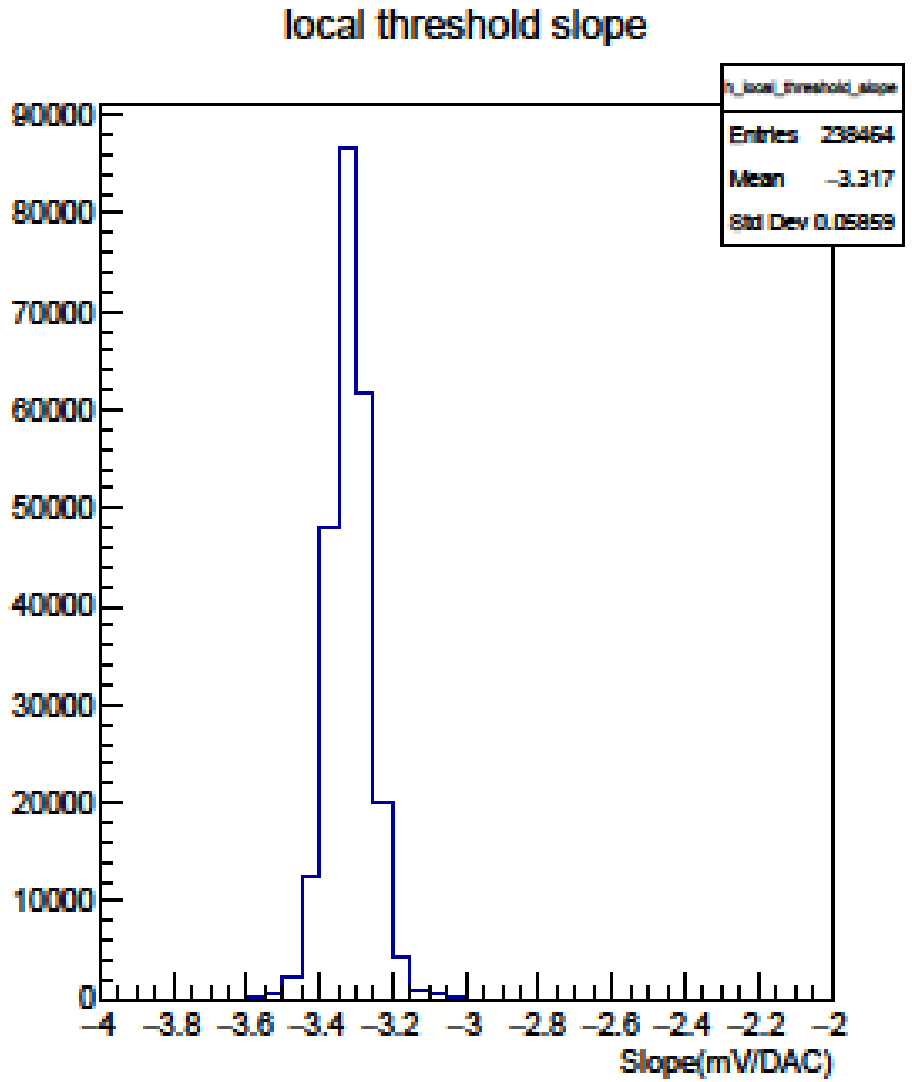
PACIFIC5q Test Result





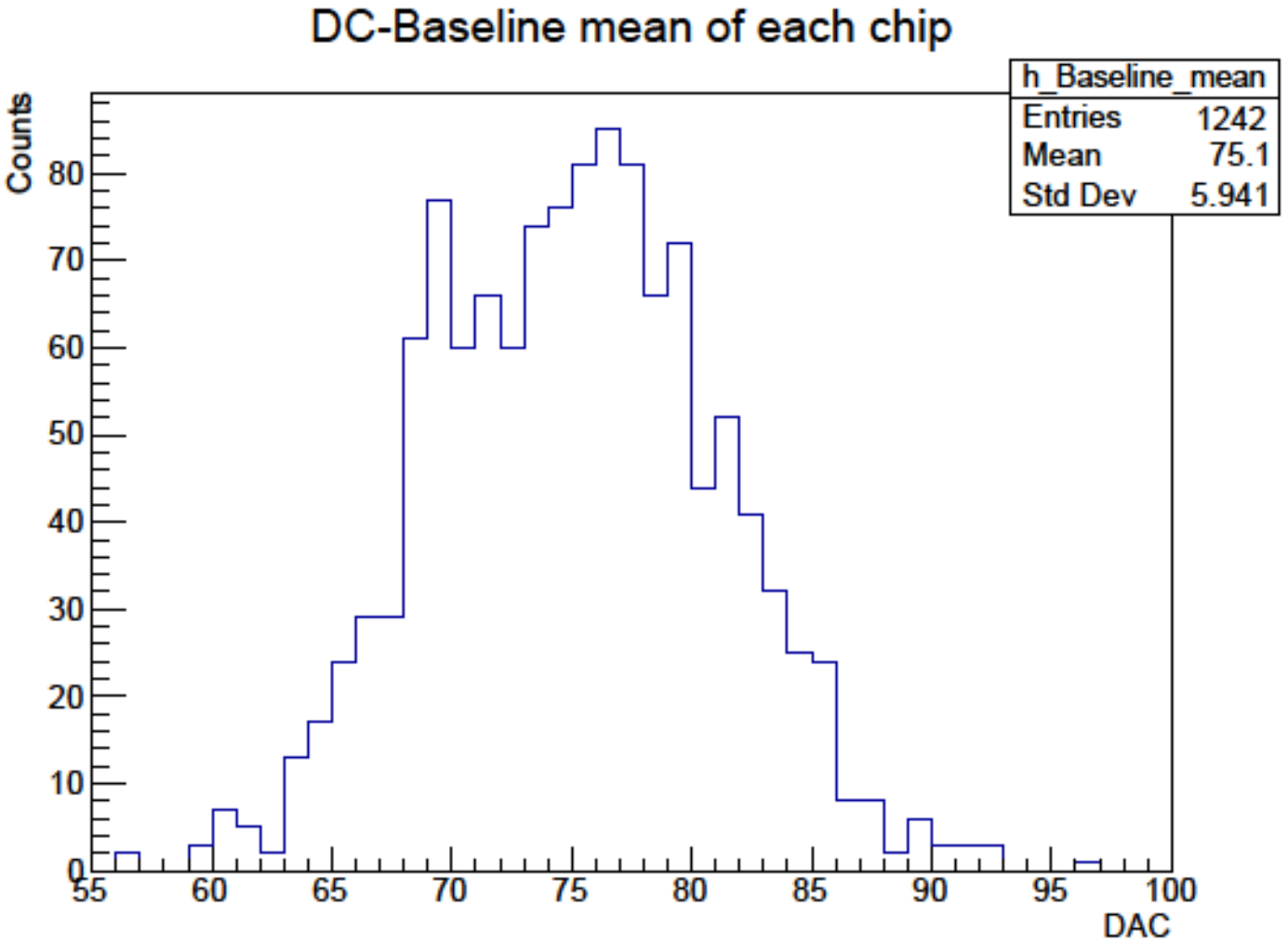
PACIFIC5q Test Result

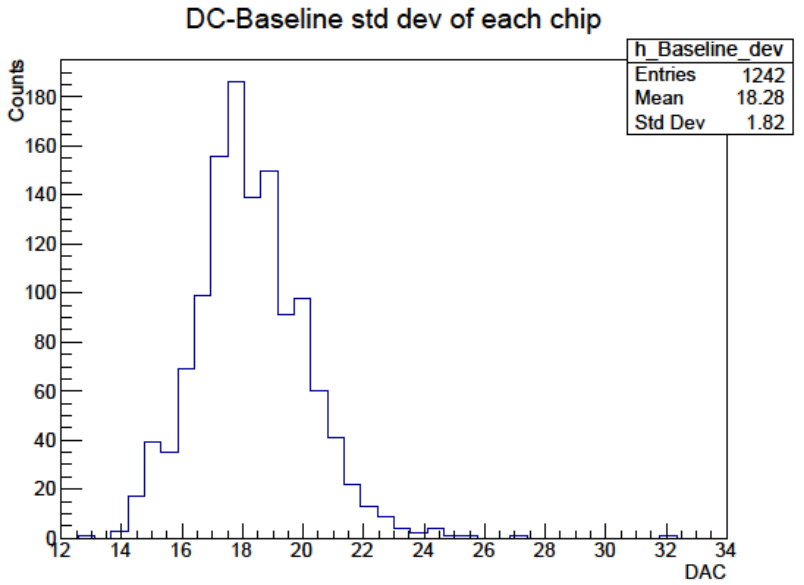


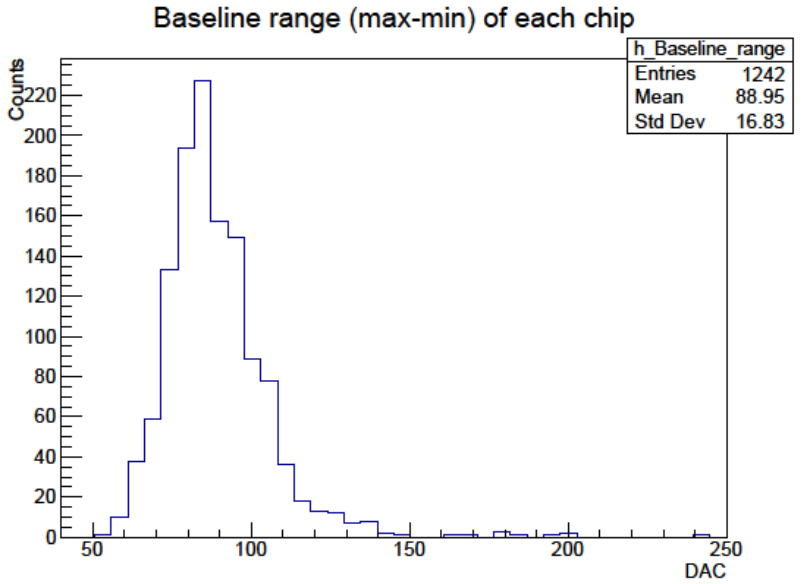


PACIFIC5q Test Result

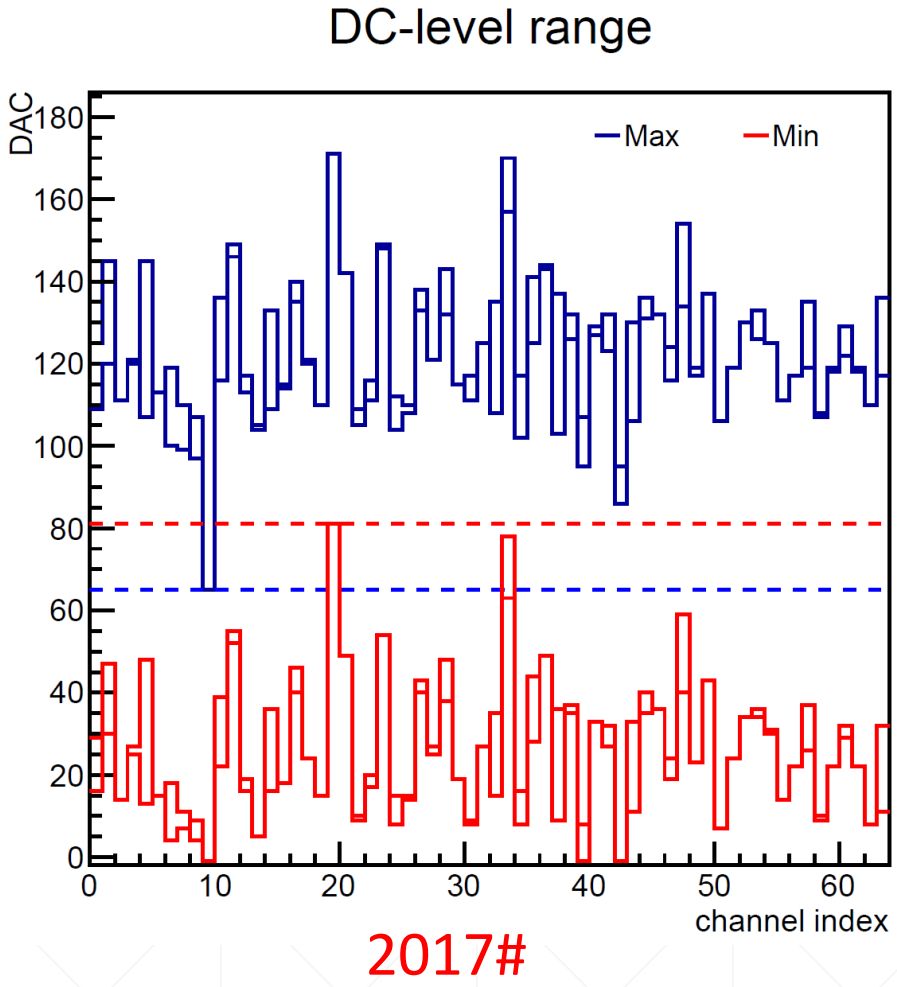
QA test for 1st batch of packaged PACIFIC5q

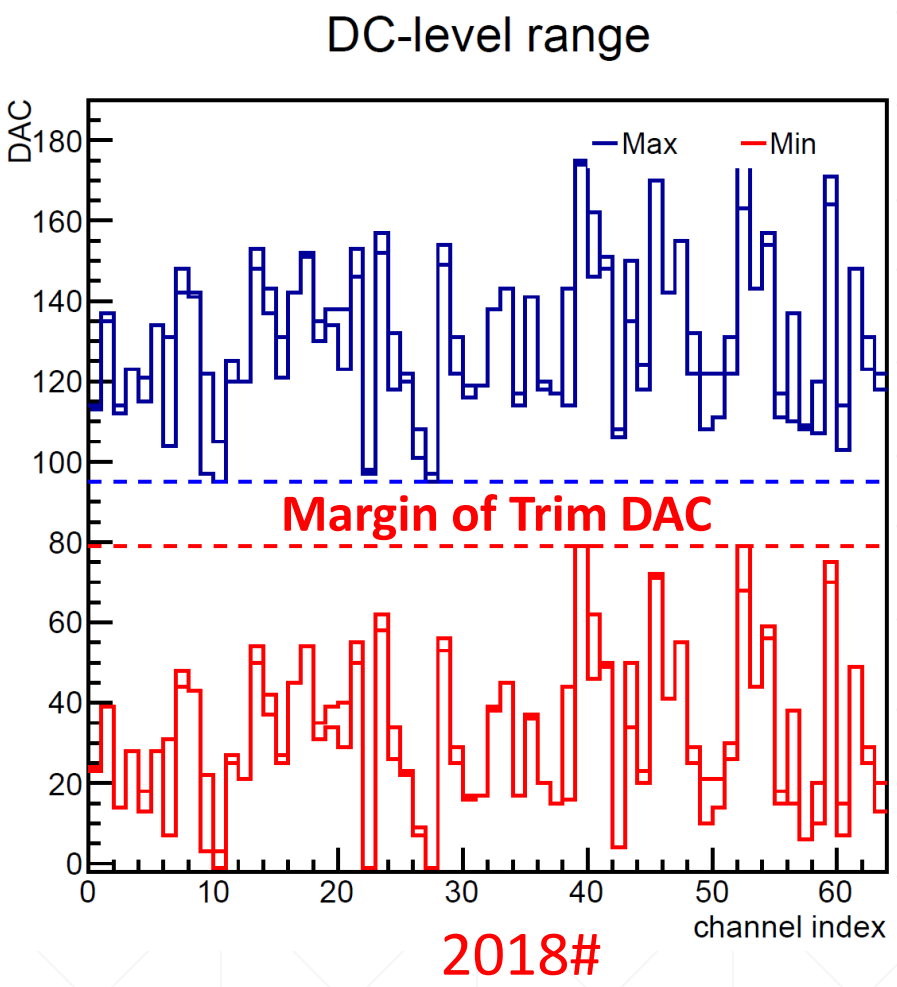




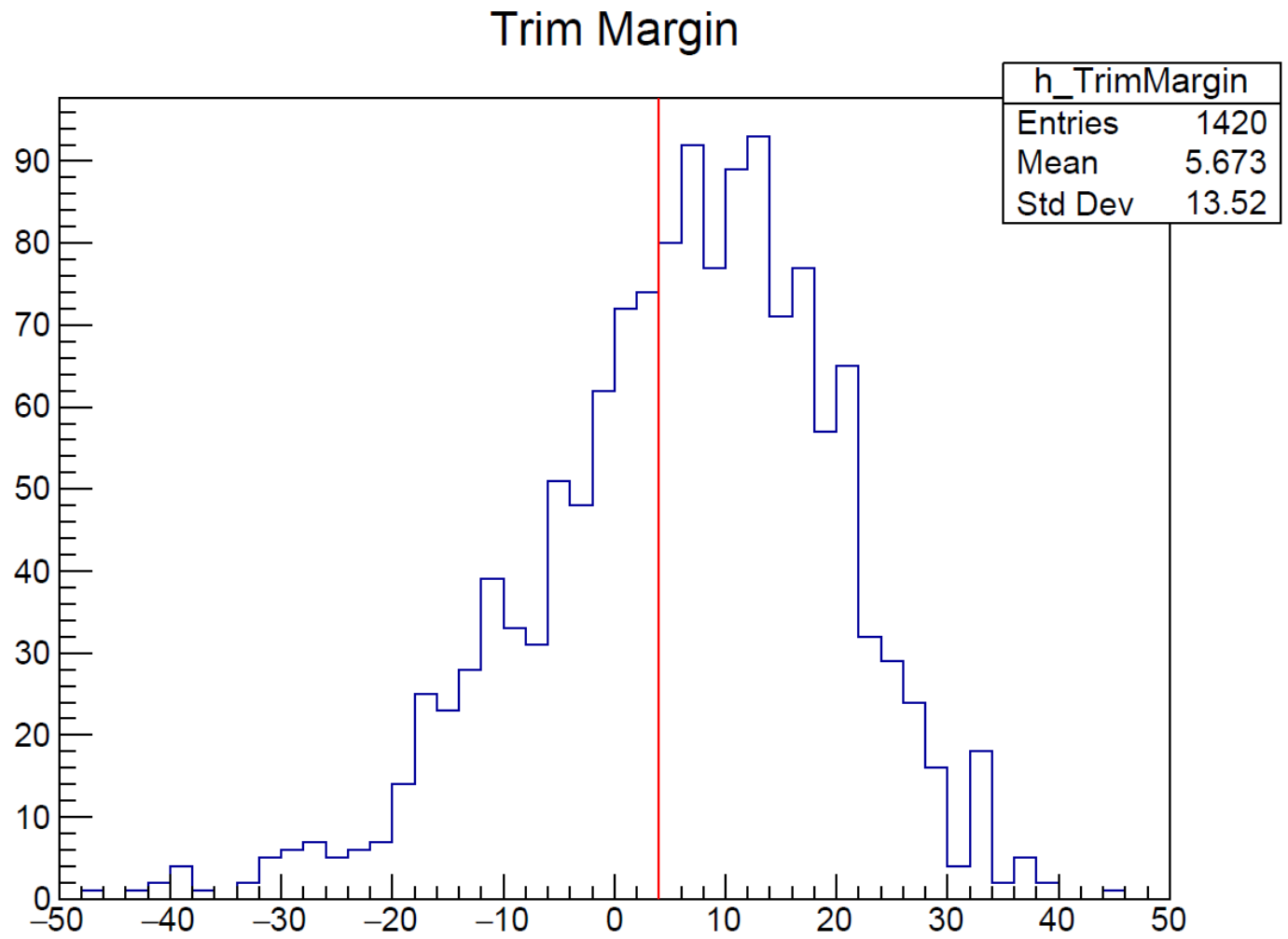


QA test for 1st batch of packaged PACIFIC5q

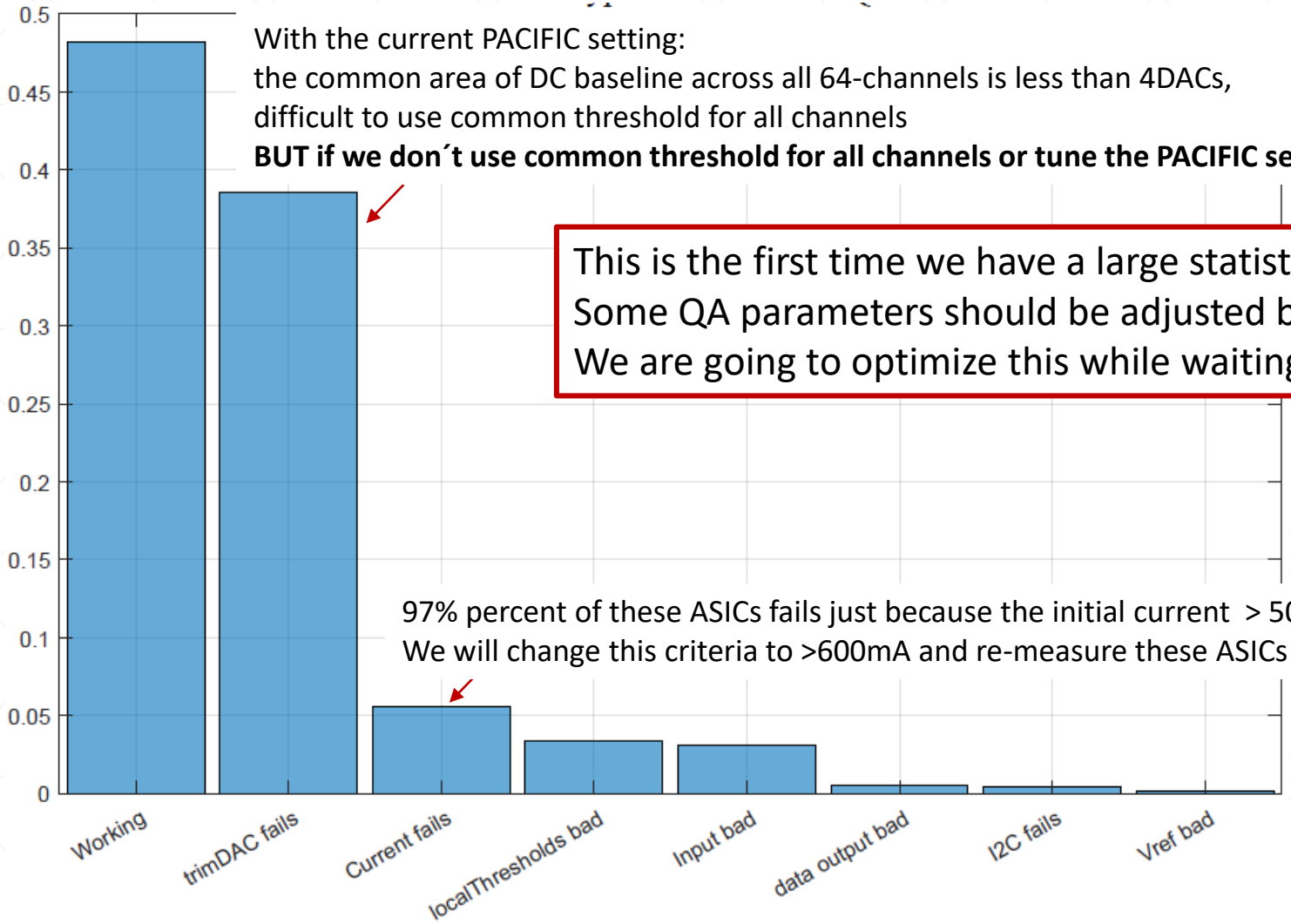




QA test for 1st batch of packaged PACIFIC5q



QA test for 1st batch of packaged PACIFIC5q



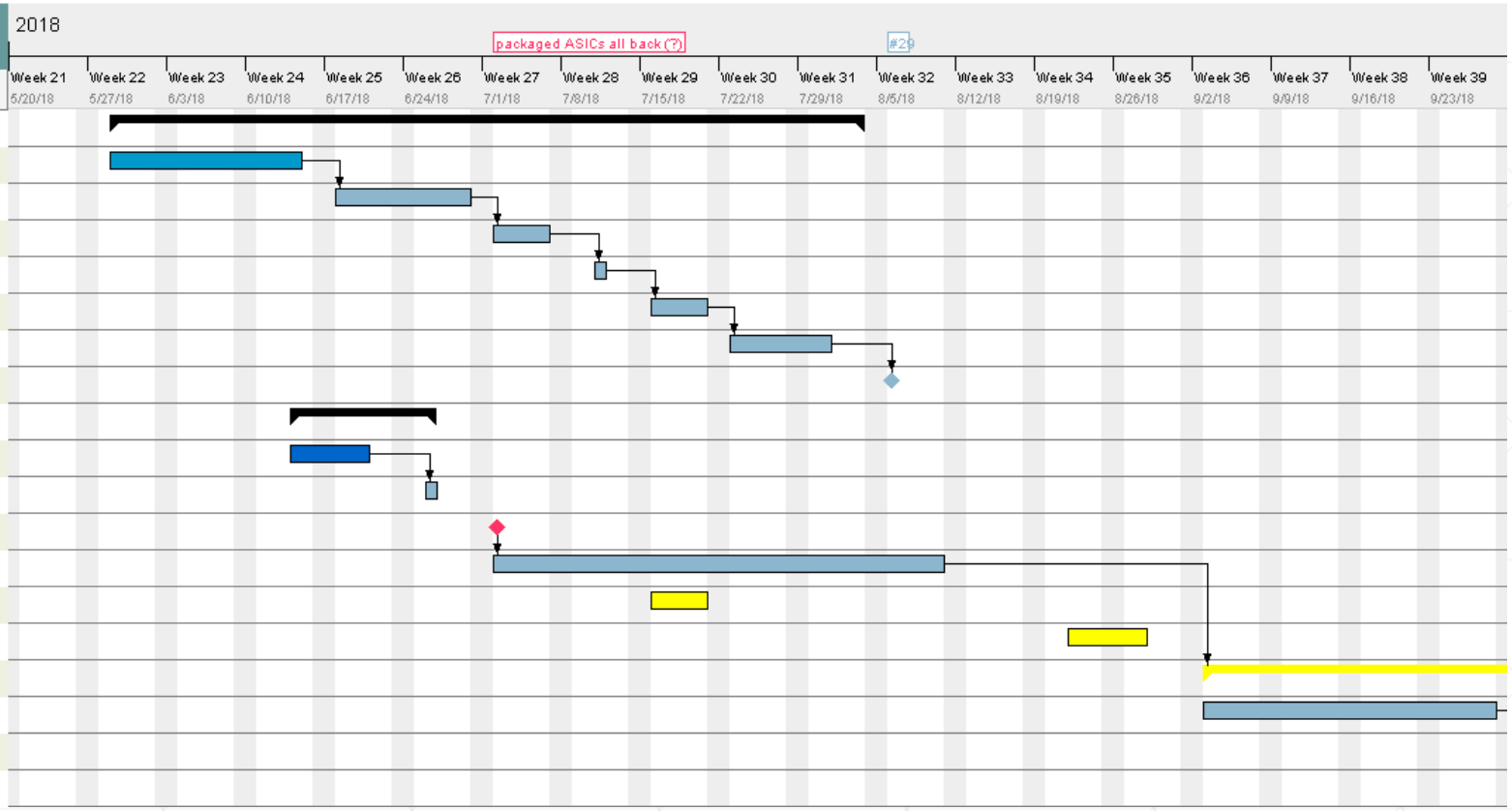
With the current PACIFIC setting:
the common area of DC baseline across all 64-channels is less than 4DACs,
difficult to use common threshold for all channels
BUT if we don´t use common threshold for all channels or tune the PACIFIC settings(?) , these ASICs can be rescued

This is the first time we have a large statistical sample of the ASICs,
Some QA parameters should be adjusted based on this result.
We are going to optimize this while waiting for the next batches

97% percent of these ASICs fails just because the initial current > 500mA
We will change this criteria to >600mA and re-measure these ASICs

Production schedule

Name	Begin date	End date
first 250 PACIFIC Carrier Board Production	5/29/18	8/3/18
optimise the PCB design	5/29/18	6/14/18
production of the PCB (250)	6/18/18	6/29/18
assembly 10 for verification	7/2/18	7/6/18
QA test of the 10 boards	7/11/18	7/11/18
test with SciFi full-electronics	7/16/18	7/20/18
assembly of all the 240 boards	7/23/18	7/31/18
complete the QA test of all the 240 boards	8/6/18	8/6/18
old design PACIFIC Carrier Board + P5q	6/14/18	6/26/18
assembly PCB with P5q	6/14/18	6/20/18
complete QA test	6/26/18	6/26/18
packaged ASICs all back (?)	7/2/18	7/2/18
QA of the mass production ASICs (100ASICs/hour)	7/2/18	8/10/18
commission ASIC QA setup in Barcelona	7/16/18	7/20/18
commision Board QA setup in Valencia	8/22/18	8/28/18
mass production of the PB	9/3/18	11/23/18
500 Boards - batch 1	9/3/18	9/28/18
1000 Boards - batch 2	10/1/18	10/26/18
1000 Boards - batch 3	10/29/18	11/23/18

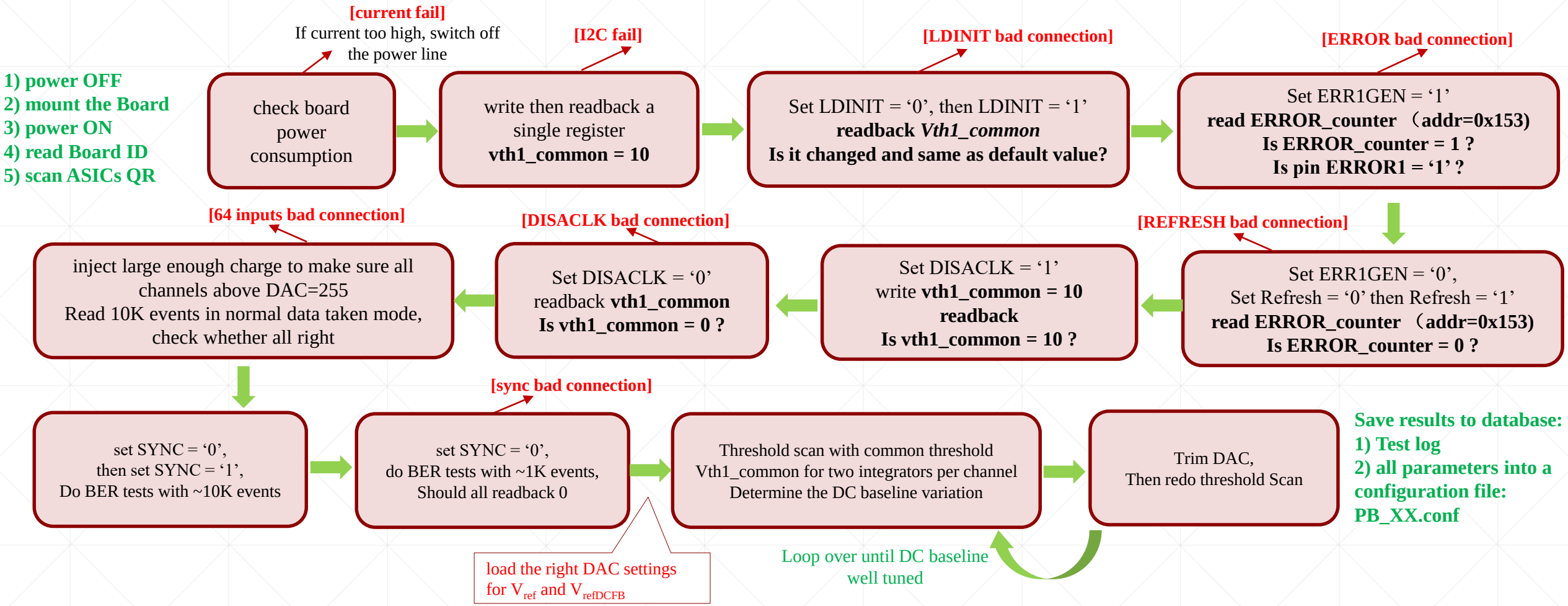


Thank you!

Questions?

Backup Slides

QA functional tests routine



QA functional tests routine

	Step	PAICIFC QA (seconds)	Carrier Board QA (seconds)
0	Time start	6	6
1	Initial current check	13	13
2	I2C check	4	4
3	LDINIT check	<1	<1
4	ERROR1GEN check	<1	<1
5	REFRESH	<1	<1
6	DISACLK check	<1	<1
7	Vref scan	5	\
8	VrefDCFB scan	4	\
9	Configured current check	5	5
10	Charge Injection check	\	100
11	BER test	<1	<1
12	SYNC check	<1	<1
13	Input voltage check	18(per ASIC)	\
14	All threshold DAC scan	57(per ASIC)	\
15	Threshold scan	32	\
16	Threshold scan (Trim DAC)	\	>300
Total		**337(4 ASICs)**	**>430 (1 Board)**

Firmware implementations for QA testbench

✓ current sensors (INA219B) controlled by I2C	[YES]	**<1s**/ASIC
✓ r/w PACIFIC slow control registers	[YES]	**<1s**/ASIC
✓ variant pattern injection tests	[YES]	**<1s**/ASIC
✓ resistor ladder circuit readout by external ADCs	[YES]	**<1s**/ASIC
✓ voltage scans using PACIFIC calibration output readout by external ADCs	[YES]	**<30s**/ASIC for all 197 DACs of PACIFIC
✓ threshold scans : s-Curve analysis	[YES]	**<5s**/scan/ASIC with ~600kHz trigger rate 7 scans needed to determine DC baselines +trimDAC range

We can achieve the goal of ***<5min/ASIC***

PACIFIC ASIC QA routine

Readout QR scan

check 4× ASIC current

[current fail] If current too high, switch the power line for the ASIC

write then readback a single register **vth1_common = 10**

[I2C fail] If readback value is not correct, Stop any further tests

Set LDINIT = '0', then LDINIT = '1'
readback *Vth1_common*
Is it changed and same as default value?

[LDINIT bad connection]

Set ERR1GEN = '1'
read ERROR_counter （addr=0x153)
Is ERROR_counter = 1 ?
Is pin ERROR1 = '1' ?

[ERROR bad connection]

Set ERR1GEN = '0',
Set Refresh = '0' then Refresh = '1'
read ERROR_counter （addr=0x153)
Is ERROR_counter = 0 ?

[REFRESH bad connection]

Set DISACLK = '1'
write **vth1_common = 10**
readback
Is vth1_common = 10 ?

Set DISACLK = '0'
readback **vth1_common**
Is vth1_common = 0 ?

[DISACLK bad connection]

check voltage at the input resistor ladder circuit,
Is voltage correct?

[64 inputs bad connection]

set SYNC = '0',
then set SYNC = '1',
Do BER tests with ~10K events

[16 outputs bad connection]

set SYNC = '0',
do BER tests with ~1K events,
Should all readback 0

[sync bad connection]

V_{ref} scan
Determine the corresoponding DAC value for V_{ref} = +0.5V

[save DAC in database]

Robot arm control

$V_{refDCFB}$ scan
Determine the corresoponding DAC value for $V_{refDCFB}$ = +0.7V

[save DAC in database]

Threshold scan with common threshold Vth1_common for two integrators per channel
Determine the DC baseline variation

[criteria to-be-determined! We need the statistic from pacific5 batch testing …]

Internal ADC calibration [optional]

Internal temperature calibration [optional]

Production plan

- 2,500 × PACIFIC Carrier Boards will produced for the SciFi full detector (20% spare)
- The Carrier Board was optimized.
- Tsinghua University will take responsibility for the mass production
- Mass production companies has been chosen. (Shenzhen Fastprint Circuit Tech).
- Production of 1st batch of boards (10+240 boards) and testing will be finished in July.
- The QA system already test over 1,400 PACIFIC chips, available for mass production.