低物质量MAPS探测模块研究

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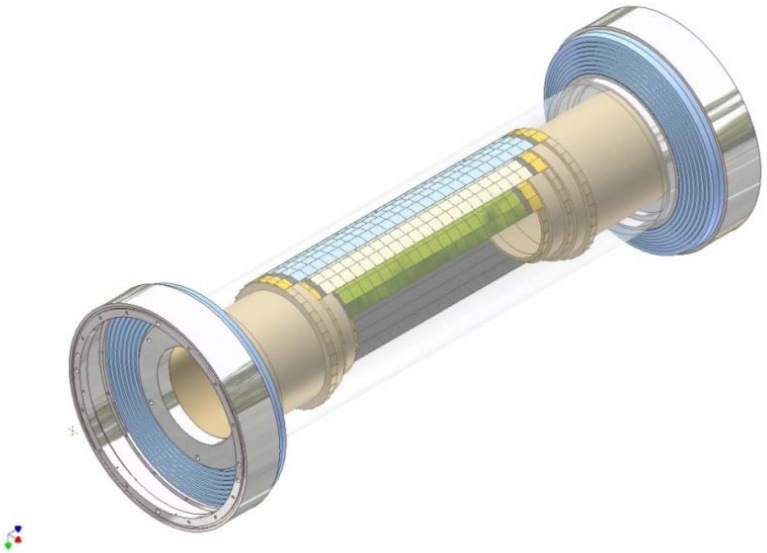
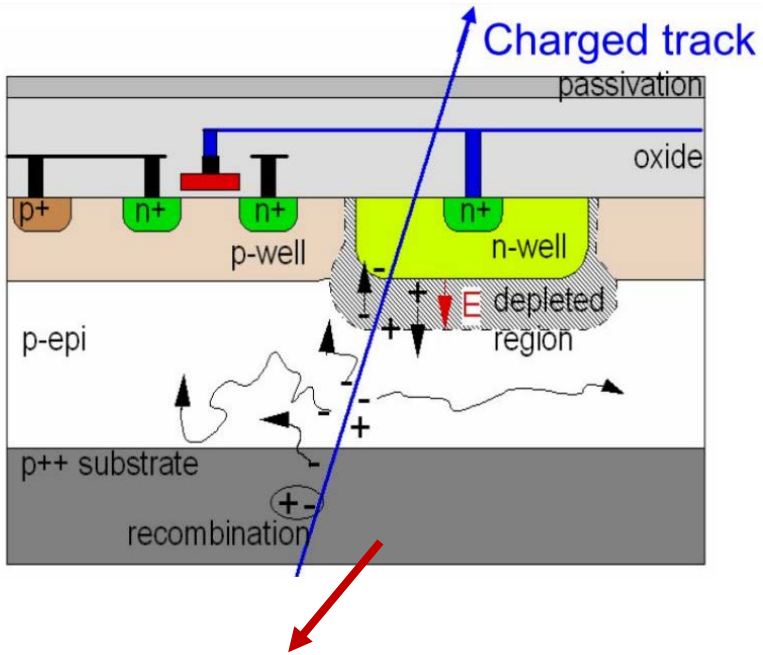
高能物理研究所

MAPS and application in MDC upgrade



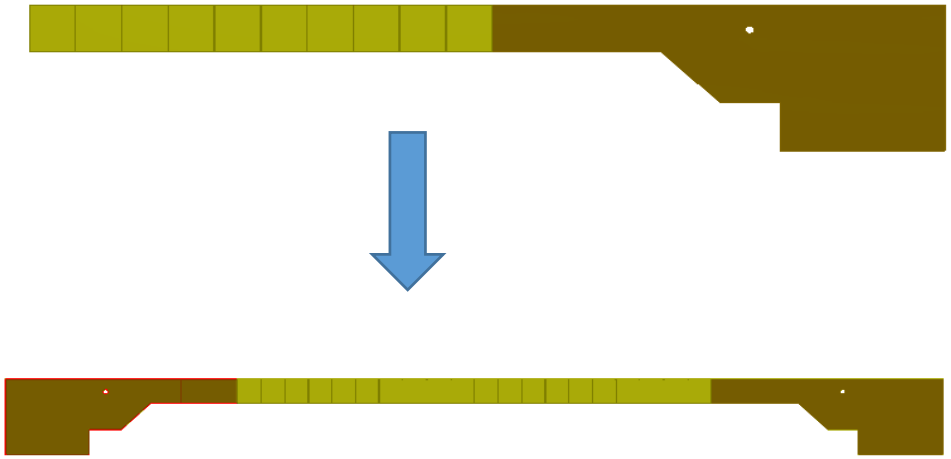


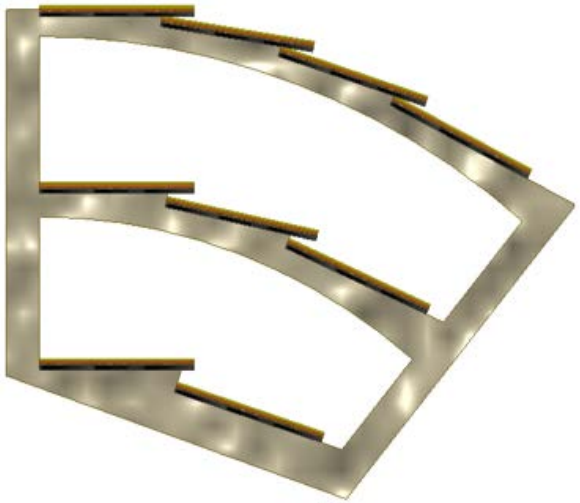
- 高能物理实验对低物质量内径迹室和顶点探测器的需求
- MAPS(Monolithic active pixel sensor)具有低物质量、高空间分辨率等优点
- 法国Strasbourg IPHC
- 应用于STAR vertex detector 及ALICE ITS upgrade 等

MDC内室升级预研采用MIMOSA28

- Density: ~20μm pixel pitch, ~0.9Mpixels/chip
- Spatial resolution: a few μm
- Rating capability: ~10^6Hz/cm^2
- Material budget: ~50μm thick
- Radiation tolerance: ~1 MRad, 10^{13} n_{eq}/cm^2
- Room temperature operation

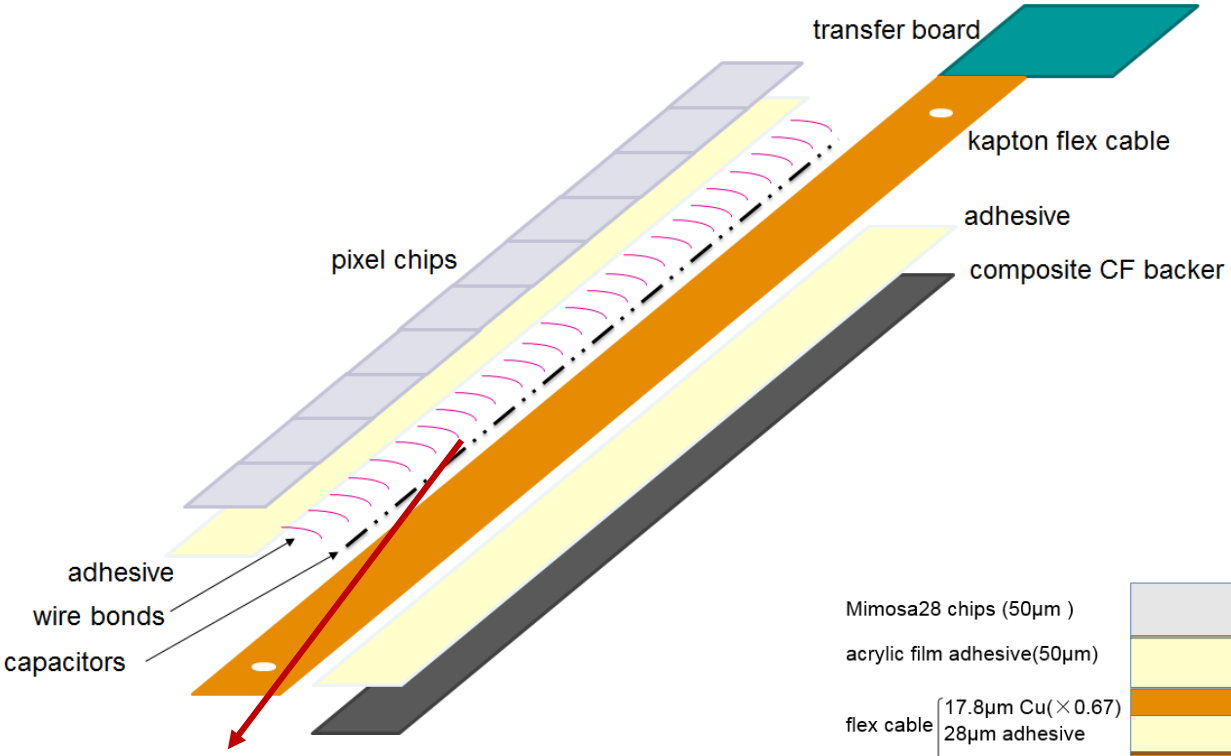
R&D target: a MAPS prototype

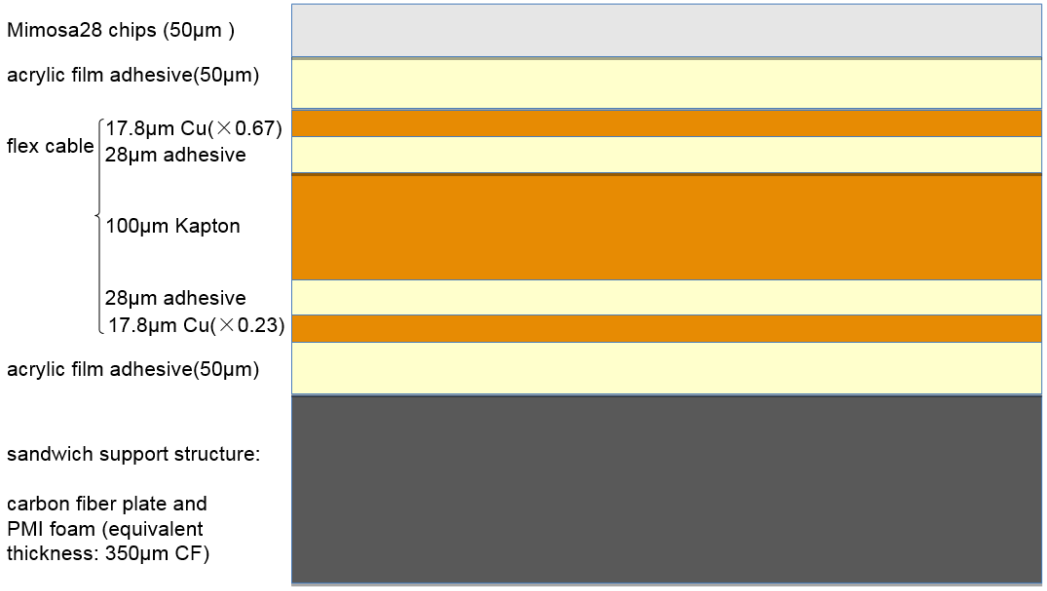




- 探测器模型结构
  - 1/10 Coverage of the inner tracker (~ 720cm^2→180 chips→180M pixels)
  - ϕ direction: 2 , 3 and 4 ladders for the 1st, 2nd and 3rd layer respectively
  - Z direction: 2 sets of ladders each layer
  - 10 Mimosa28 chips with dimension of 2cm×2cm in each ladder
- Chip →ladder →sector → layer →prototype

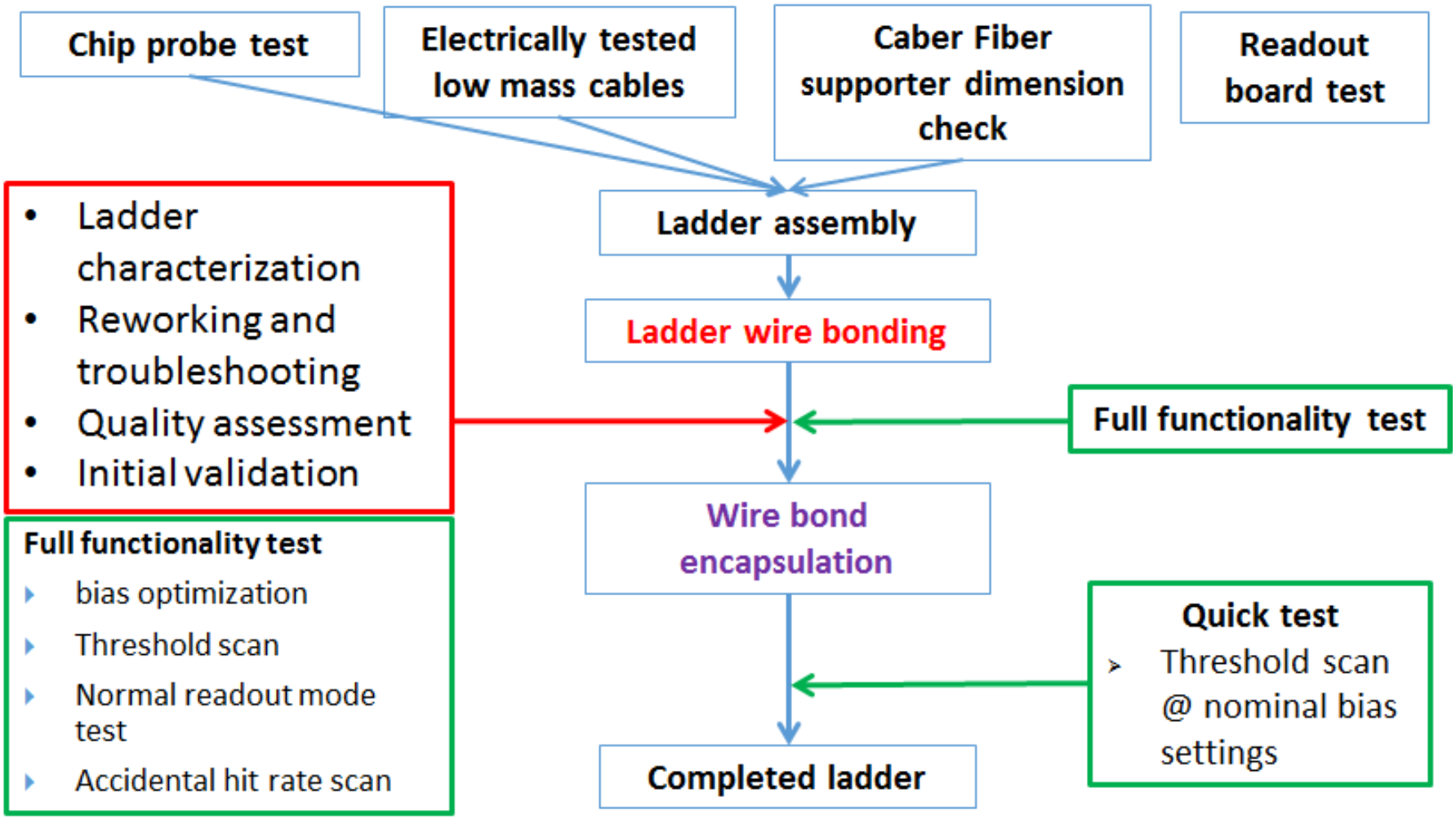
Ladder design





- 探测模块（Ladder）: the basic building block of the detector, key issue for the prototype
  - 10 片 Mimosa28 芯片
  - 柔性电缆
  - 低物质量支撑结构

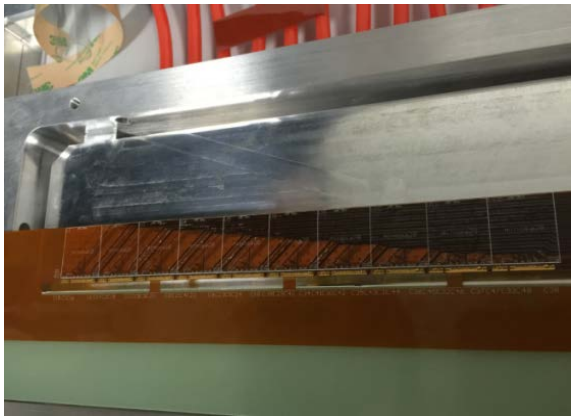
Key procedure

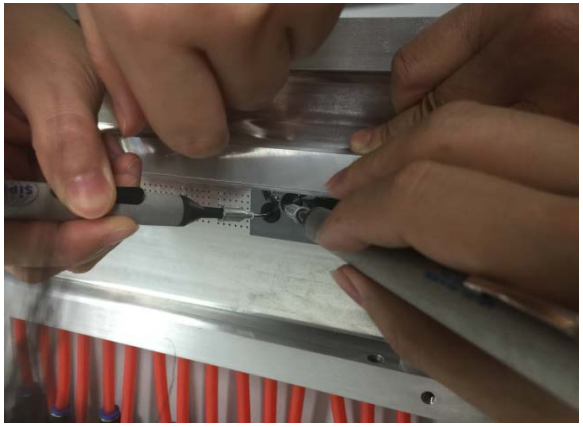


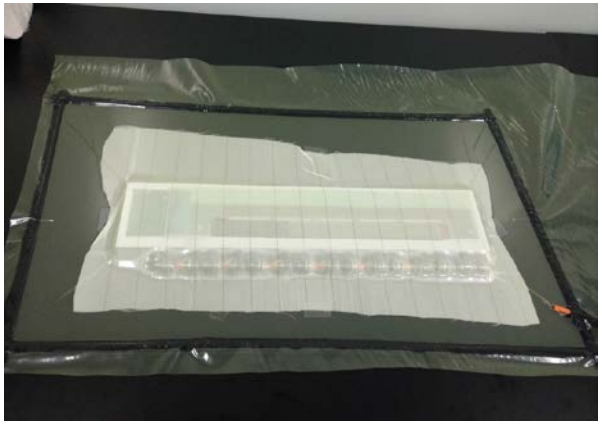
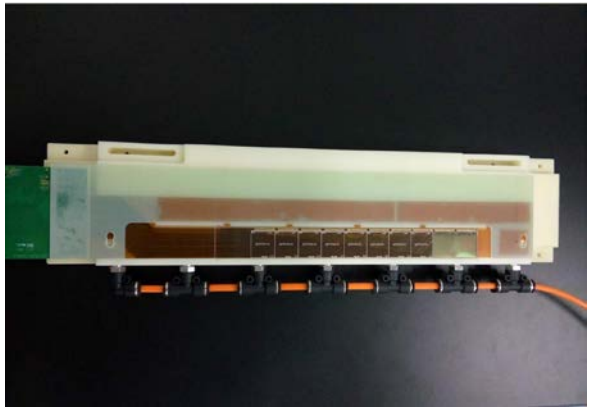
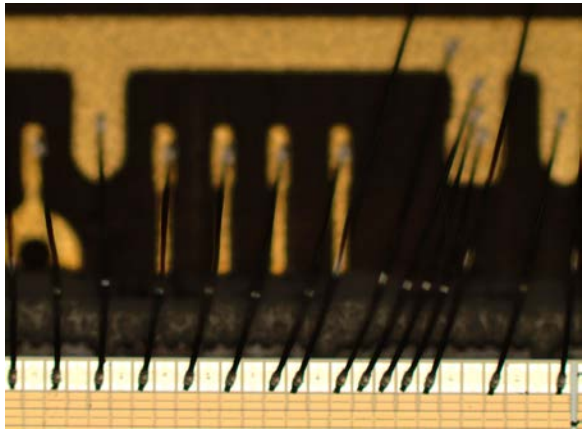
Ladder assembly

- 设计专用工装，确定工艺流程

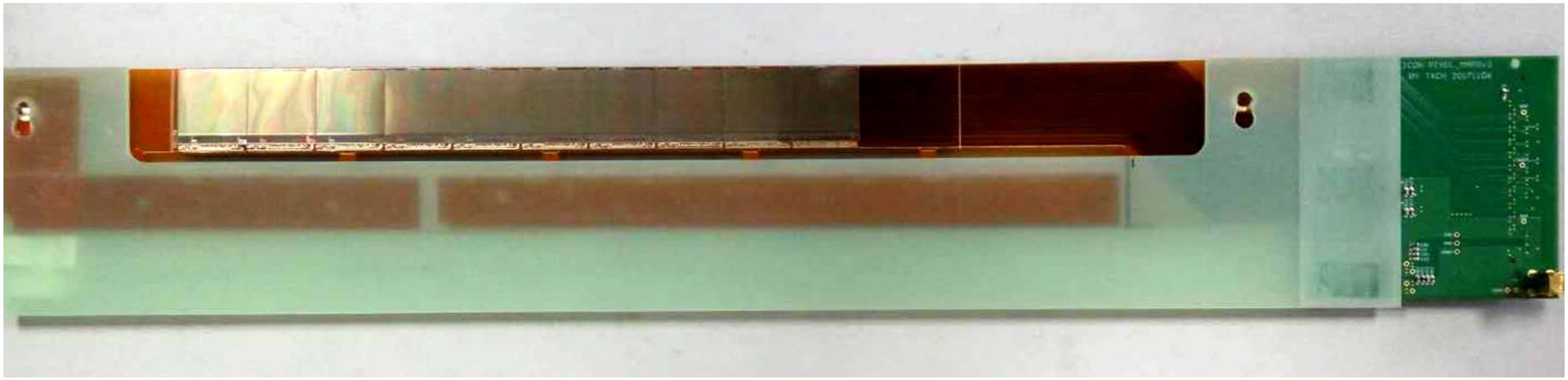
Ladder assembly

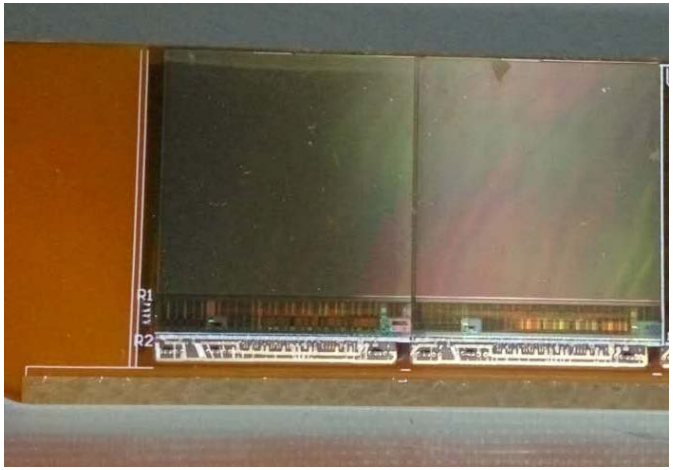


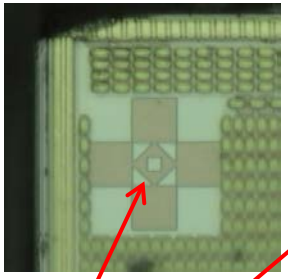



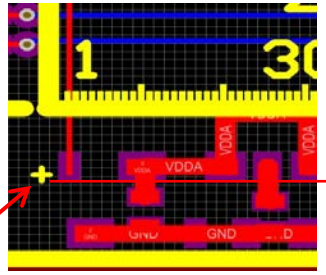





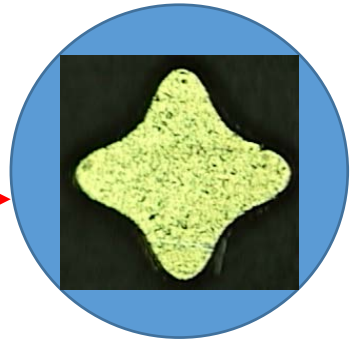
Ladder assembly

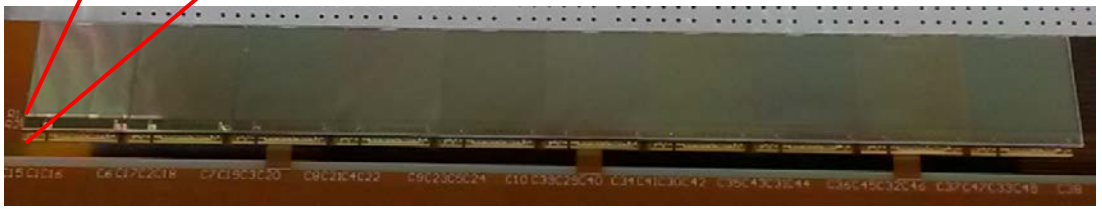






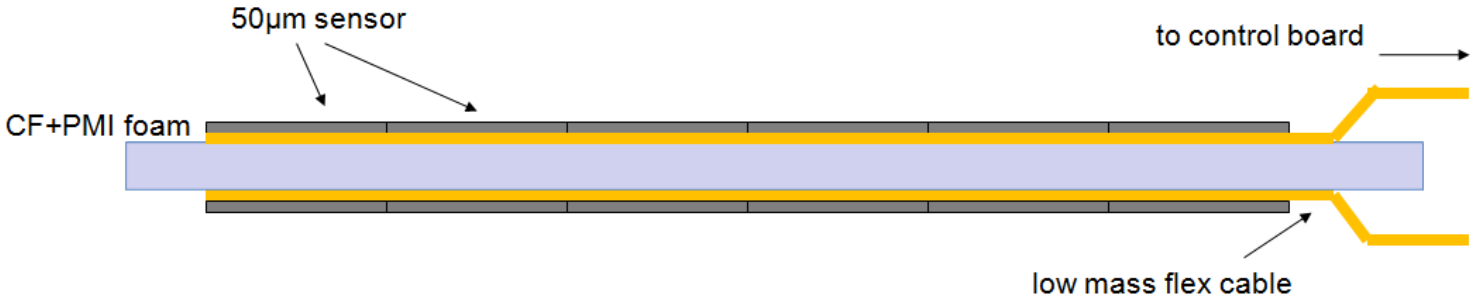






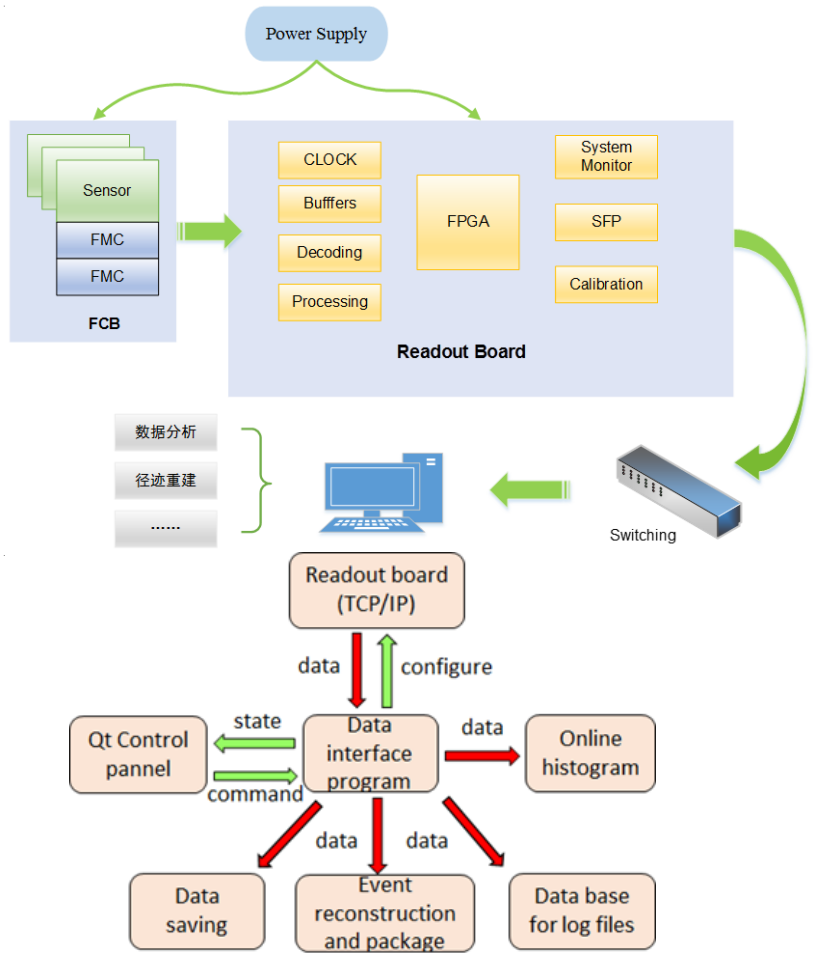
- 低物质量、高位置精度探测模块
  - Material budget: 0.37% X_0 /ladder, 0.51% X_0 /layer (ladder + supporter)
  - Chip location accuracy: < 10μm

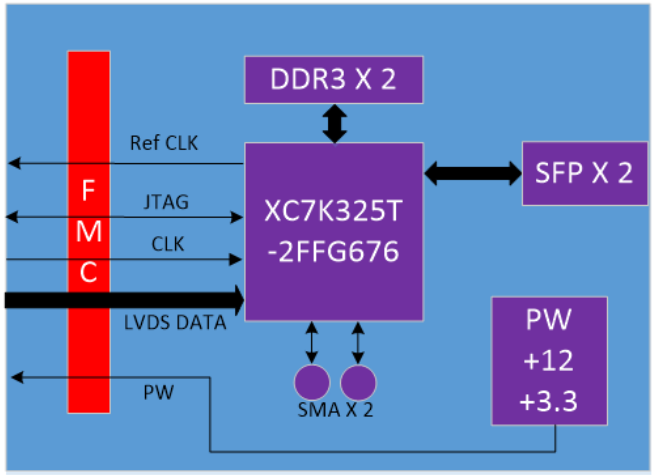
Double-sided ladder 设计



- Single-sided ladder→ Double sided ladder (CEPC vertex 预研)
- Dummy ladder → functional ladder

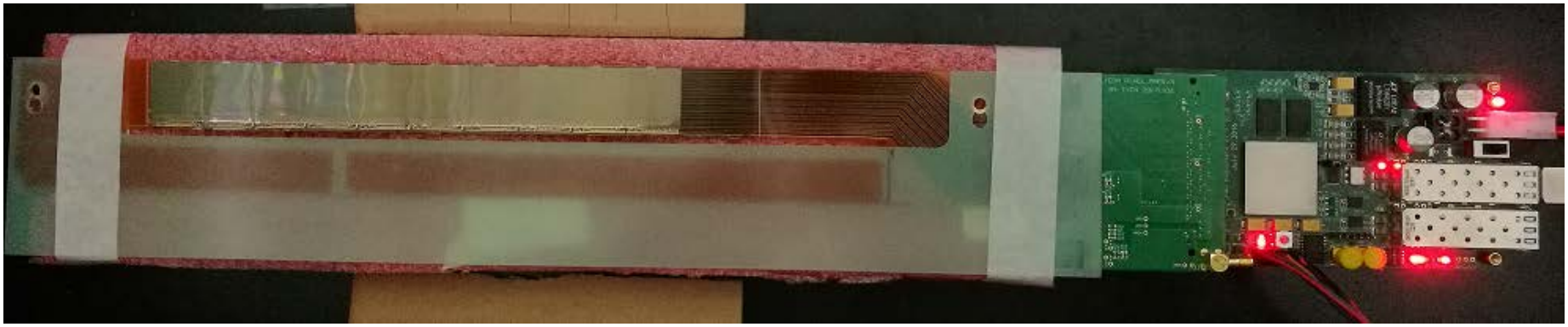
Readout electronics and DAQ





- Distributed system
- Ladder → FCB → Readout Board → Switching → PC
- SiTCP : high-speed and highly reliable data transmission
- Readout speed: 30~40MB/s/ladder

Ladder test



阶段一

硬板PBC，芯片的引脚与功能测试

阶段二

柔性PCB设计、单芯片测试

阶段三

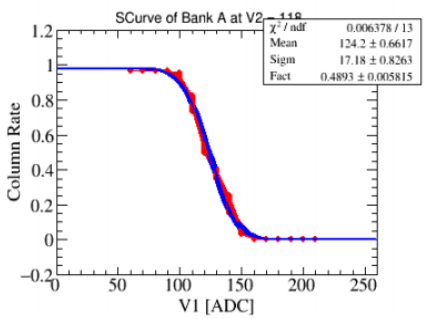
柔性PCB改进设计、双芯片测试

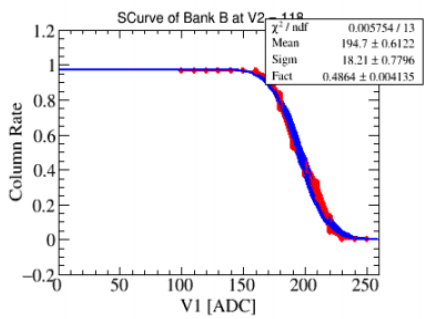
阶段四

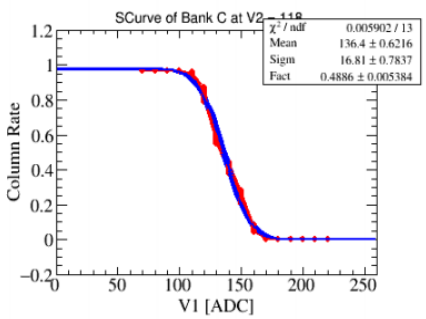
柔性PCB改进设计、满芯片（十个）测试

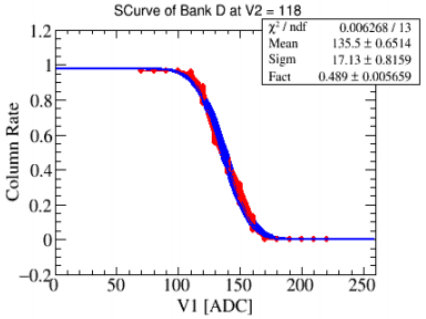
- 硬板PCB→柔性PCB
- 单片芯片测试→双片芯片测试 →完整ladder的测试

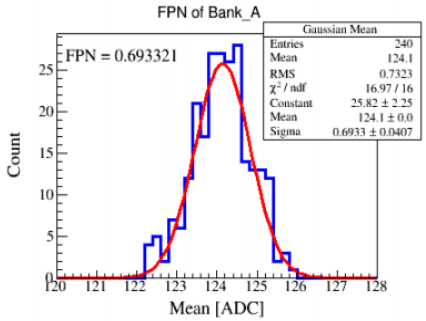
S-curve scan

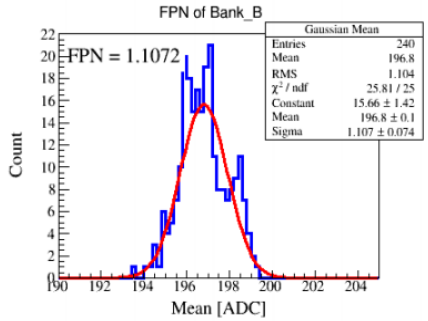


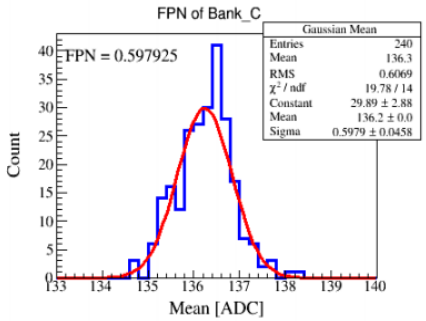


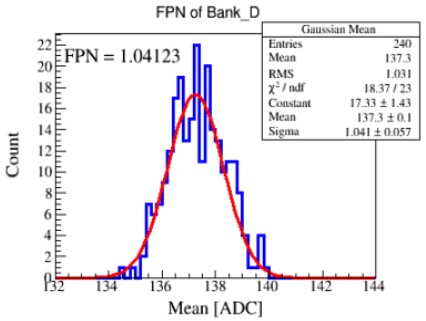


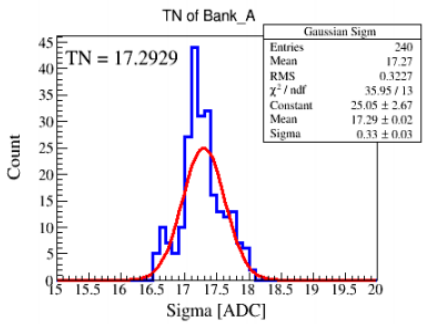


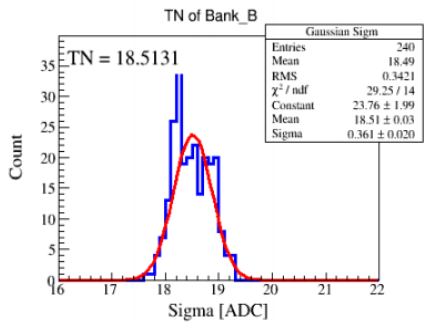


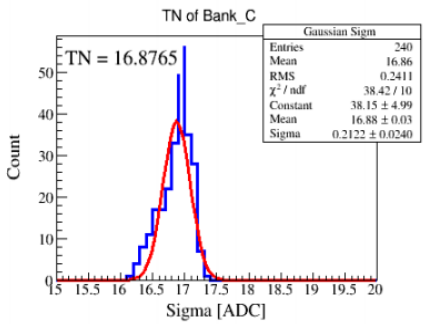


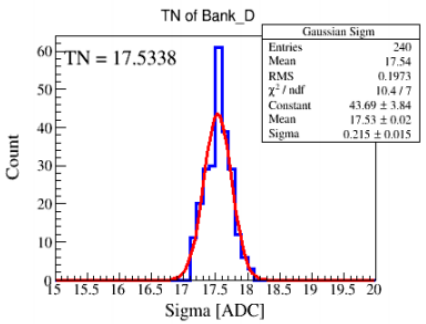






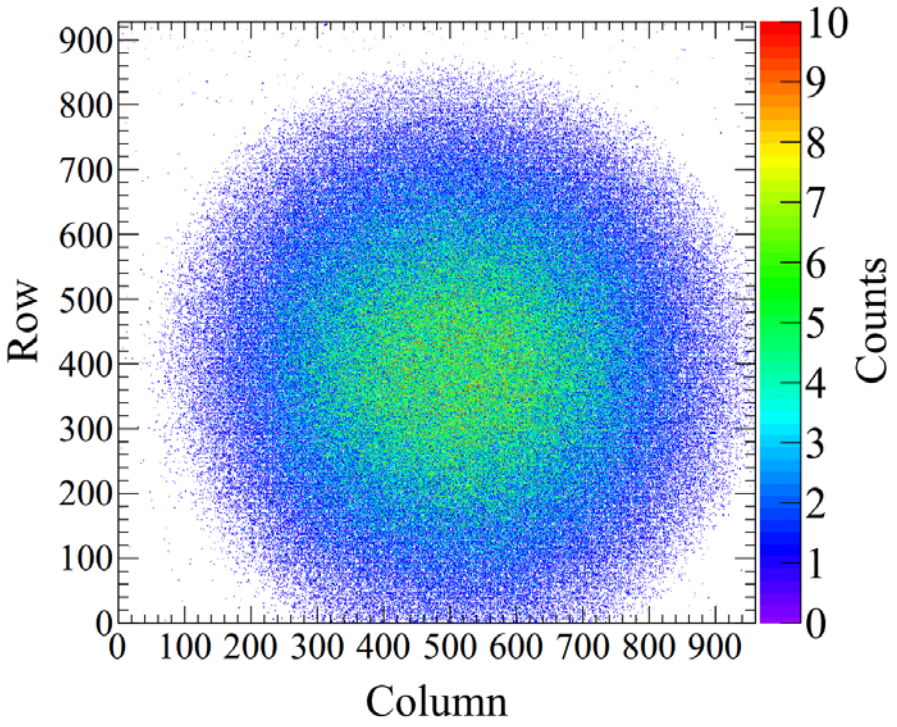


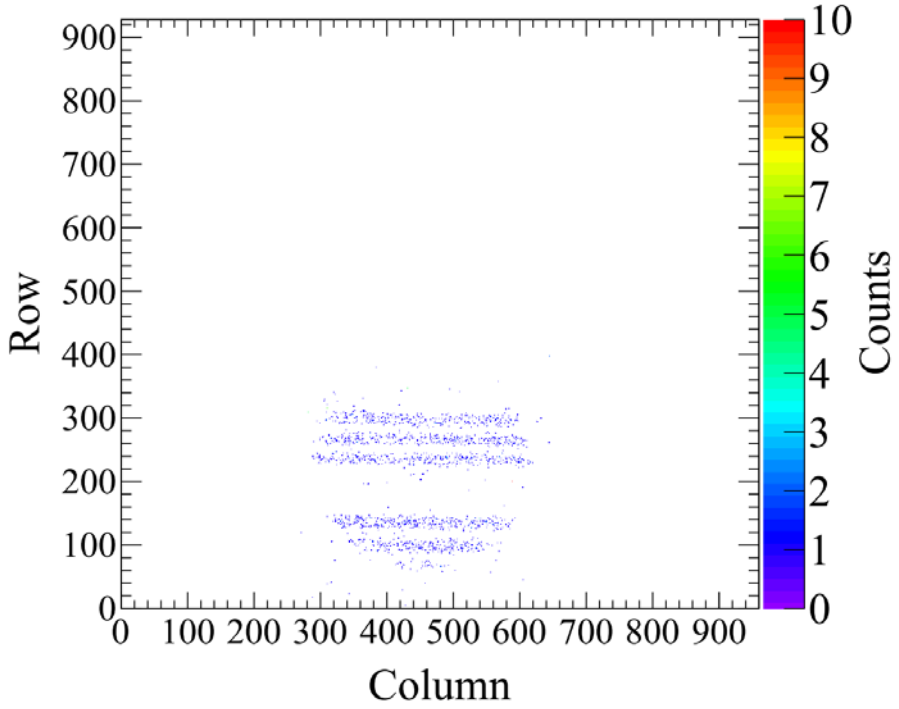




- S-curve scan by column and by pixel
- PFN~1mV, TN, ENC~ 15-20e, Threshold (4~5)σ

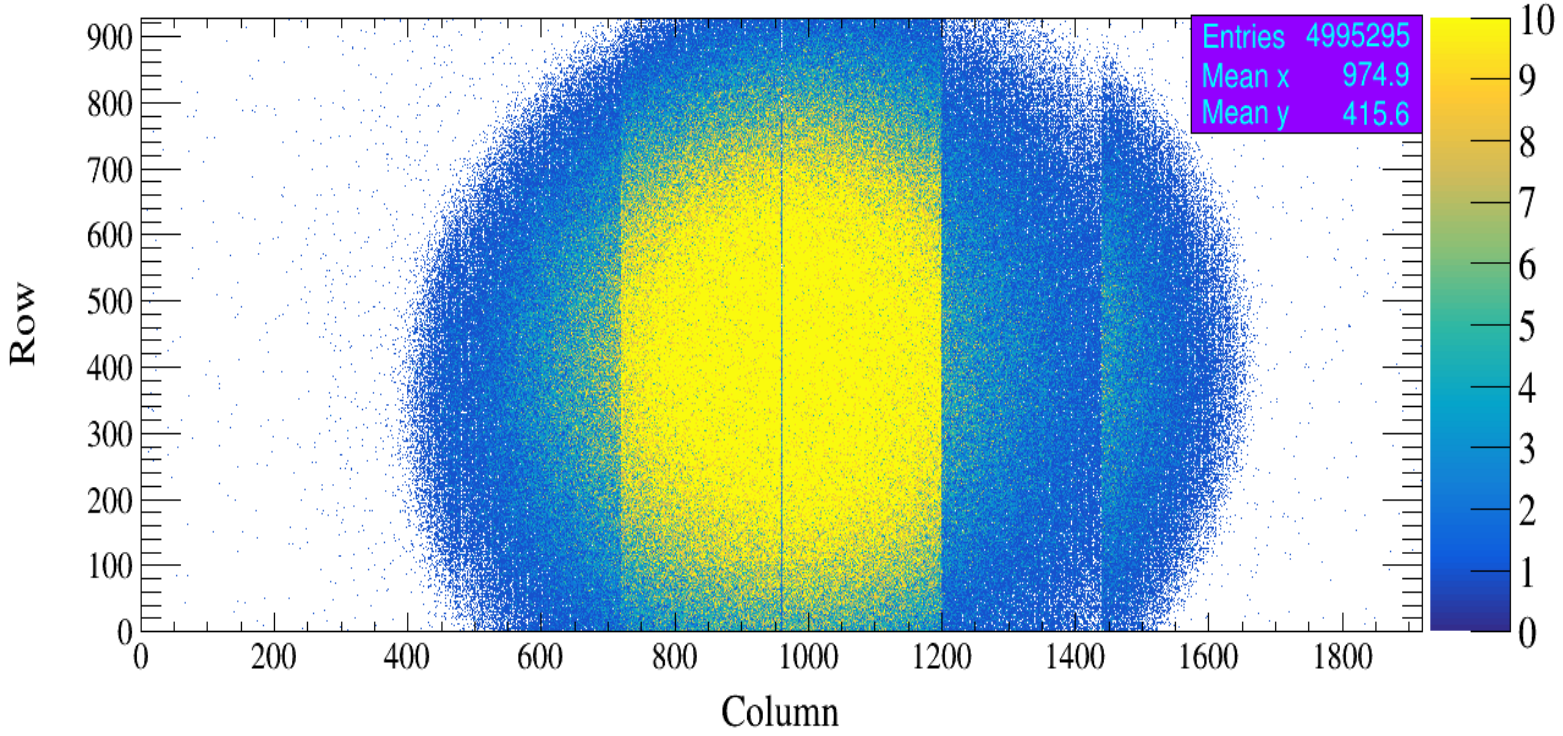
Test by radioactive sources





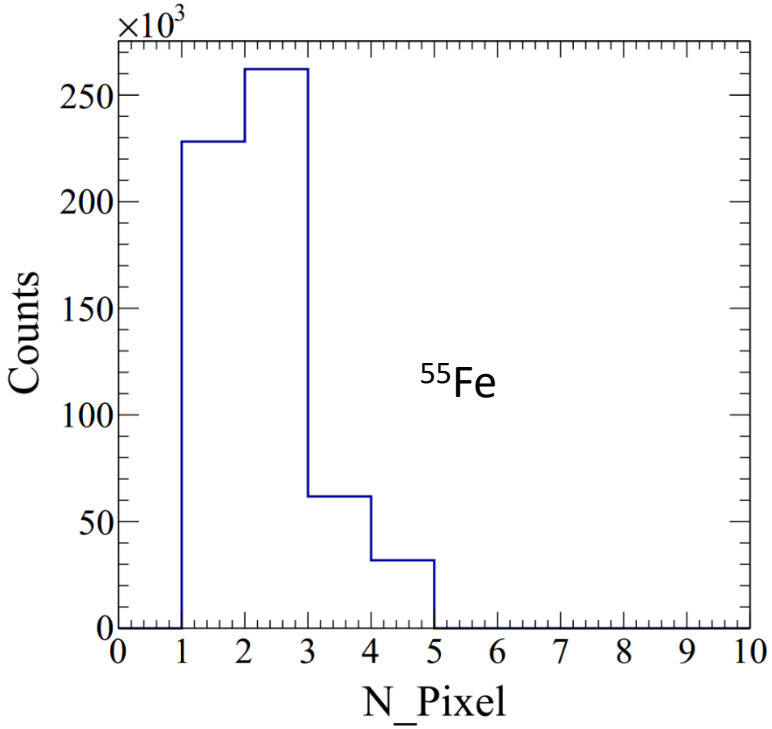
- 芯片像素响应测试 （^{55}Fe and ^{90}Sr 放射源，未准直）
- 串扰测试
- 温度、工作时钟频率对噪声的影响

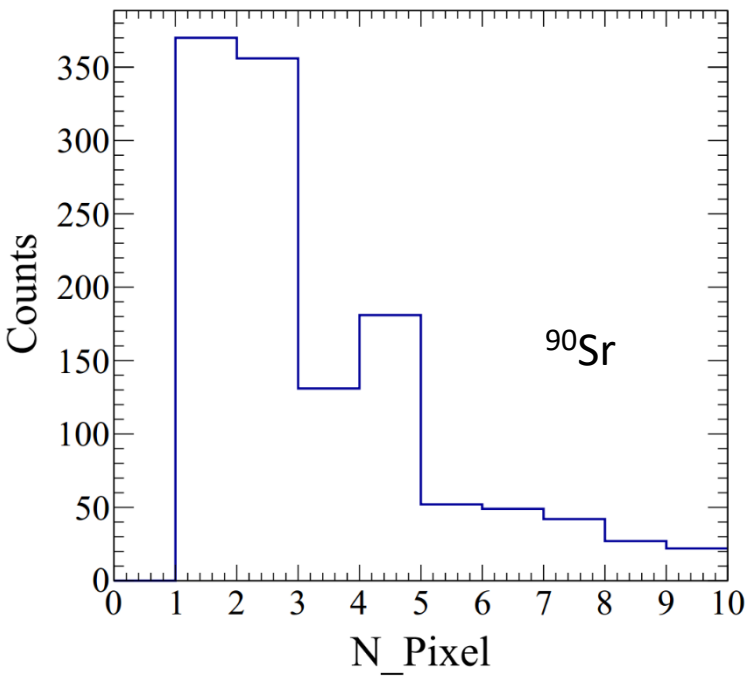
Ladder test



- 芯片响应正常，无串扰

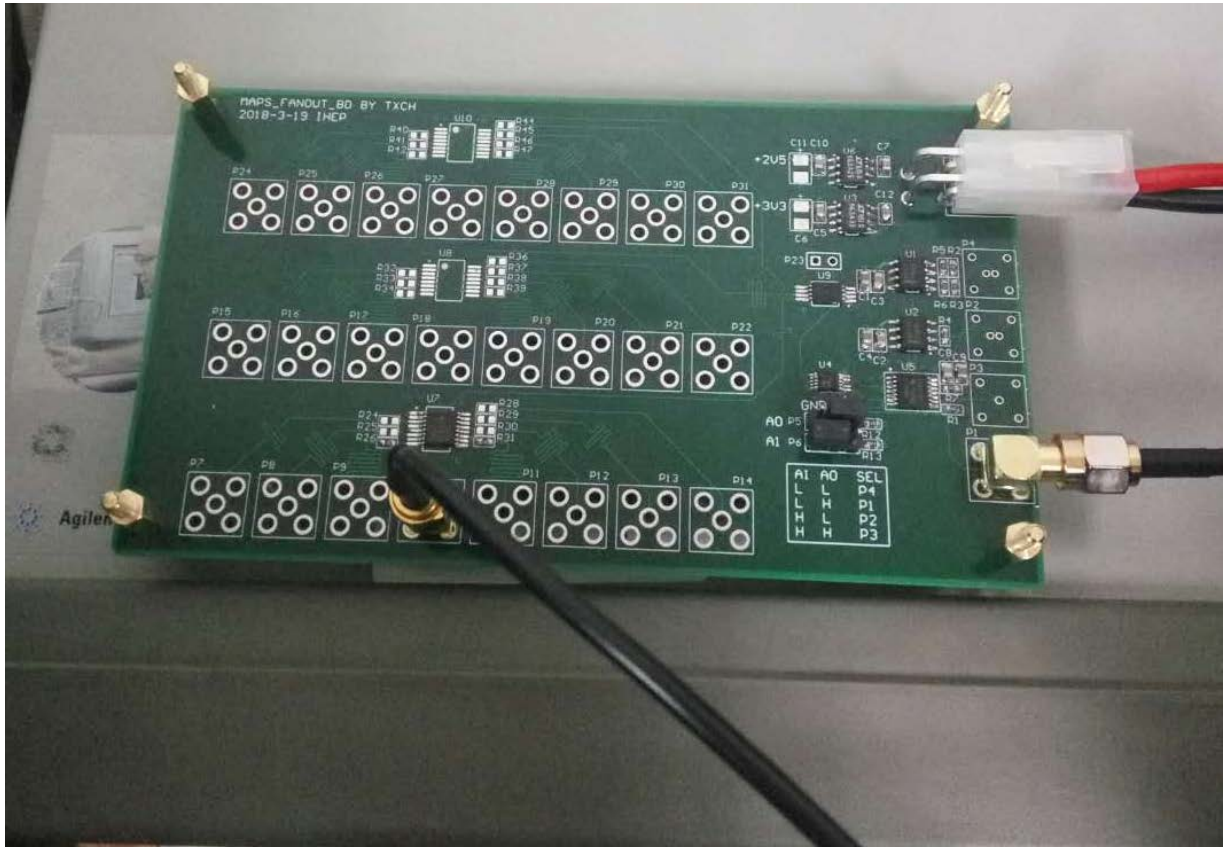
Hit reconstruction algorithm





- 电荷通过热扩散收集→Charge sharing，可以获得更好的空间分辨率
- 信号数字读出
- 击中信息位置重建

Trigger system



- 设计触发系统
- 连续的帧读出→触发读出
- 选择有效事例以及并进行事例标识
- 准备束流实验

Summary and Outlook

- 开展MAPS探测器模型的研制
- 完成低物质量探测模块工艺探索，以及读出电子学和DAQ系统的研发
- 放射源测试验证了系统正常工作
- 下一步将进行批量制作及束流测试

Thanks for your attention !