低温低噪声读出电子学研制进展

—适用于0νββ的nEXO实验

报告人：吴文欢

核探测与核电子学国家重点实验室学术年会

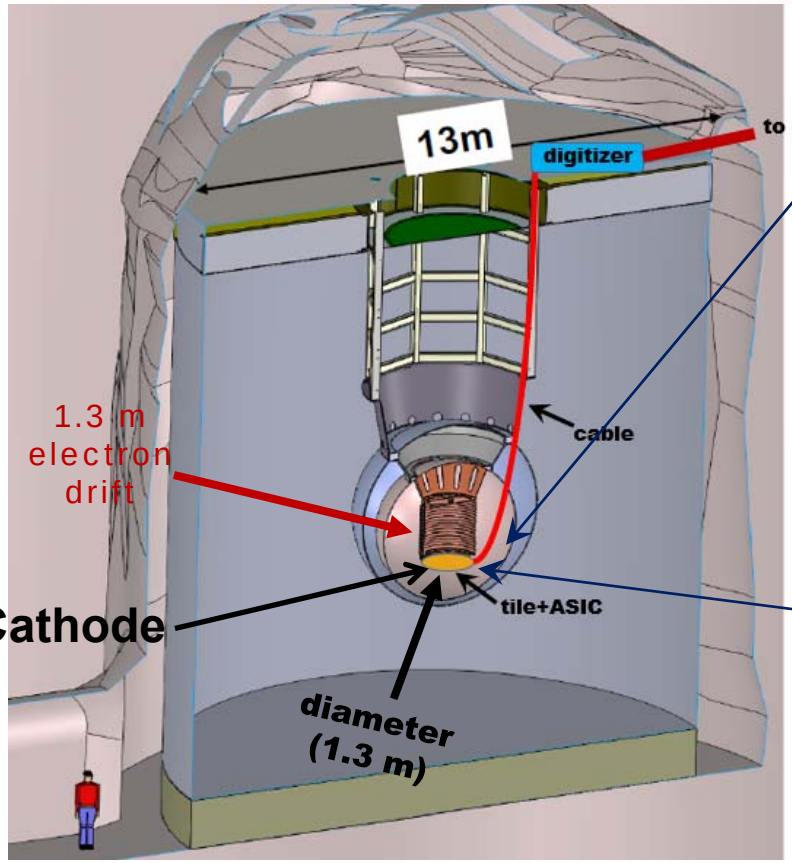
高能所实验物理中心

2018/4/26

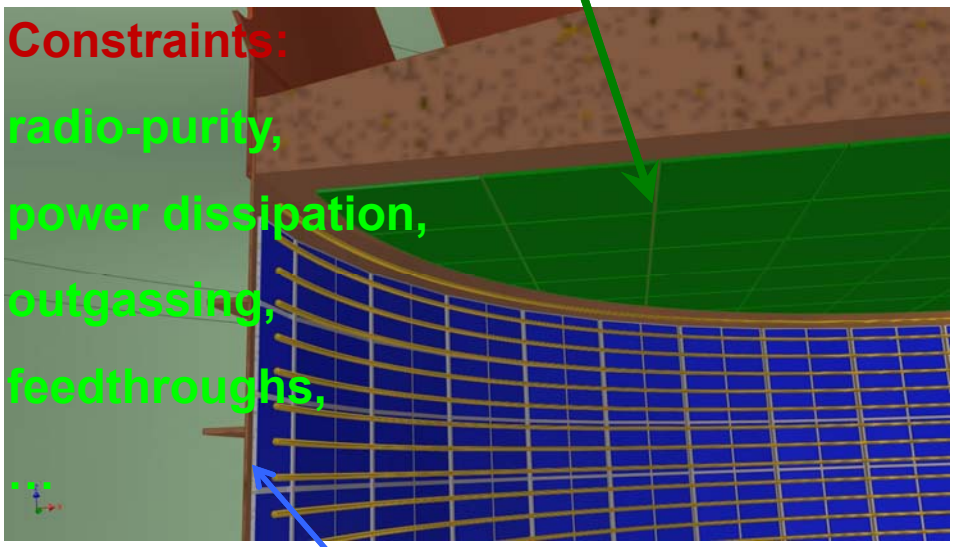
Outline

- **R&D status**
  - **Brief introduction of the ASIC**
  - **Chip functionality**
  - **Several test results**
- **Recent efforts**
  - **System integration concept**
  - **Back-end electronics and DAQ system**
- **Recent plan**

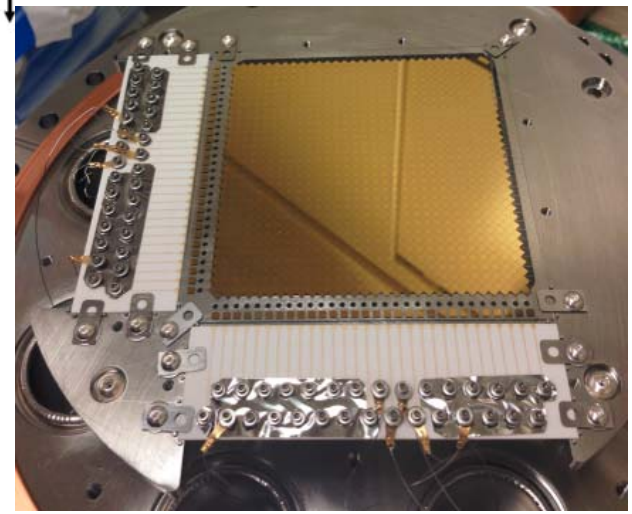
nEXO TPC 概念设计

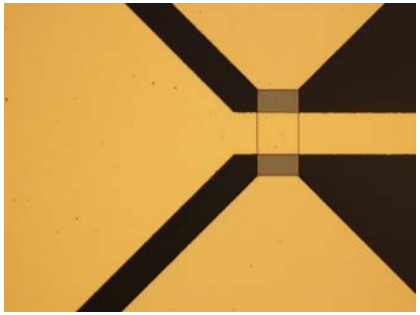


Charge Readout Tiles + ASIC



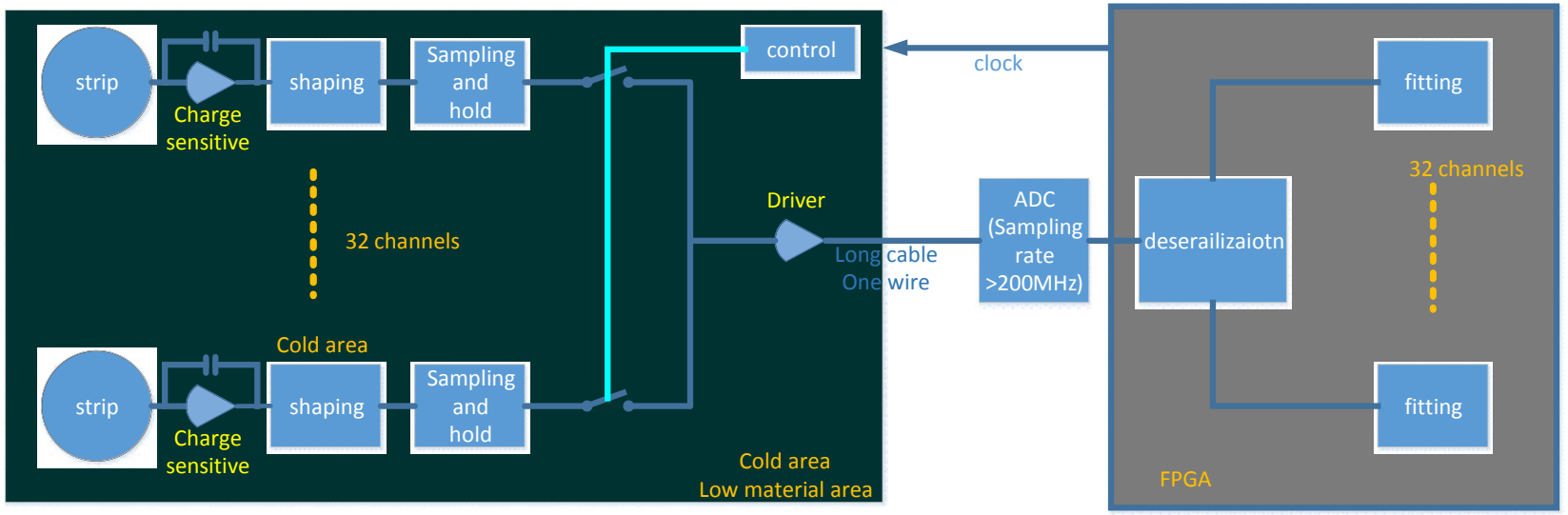
Silicon Photomultipliers (SiPMs) + ASIC



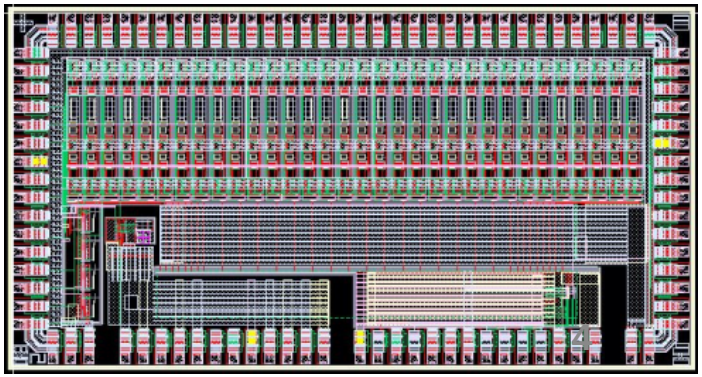


- ~ 5 tonne LXe TPC, 4.7 tonnes of active ^{enr}Xe (90% or higher)
- < 1.0% (σ/E) energy resolution

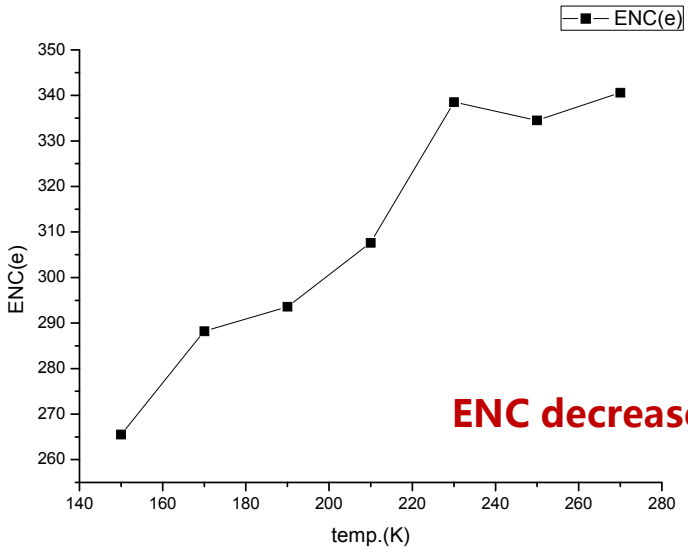
Analog serial readout ASIC



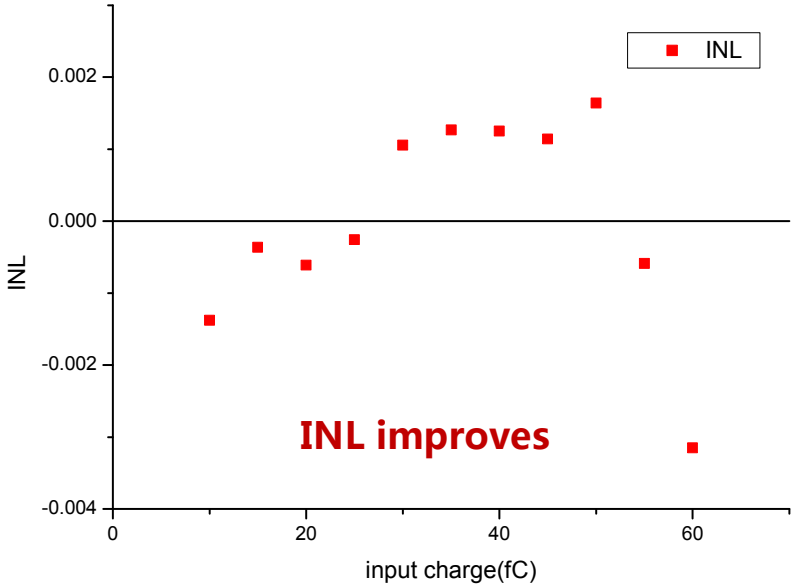
- **32 channels per chip, serial readout channel by channel**
- **ENC down to 190e@300K,20pF(sim.) , LVDS CLK(up to 200M)**
- **1output+2power+2clock pin to room temperature**
- **All 100 tiles need:**
  - **2outputs/per tile*100**
  - **2power+2clock**
  - **Reduce cables significantly(background)**



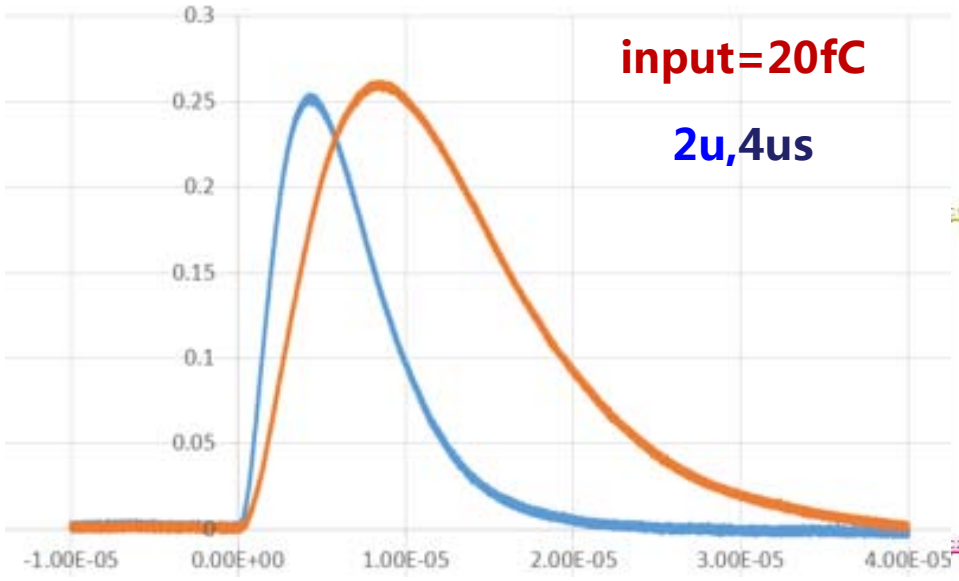
Some measurement results(160K)



ENC decreases

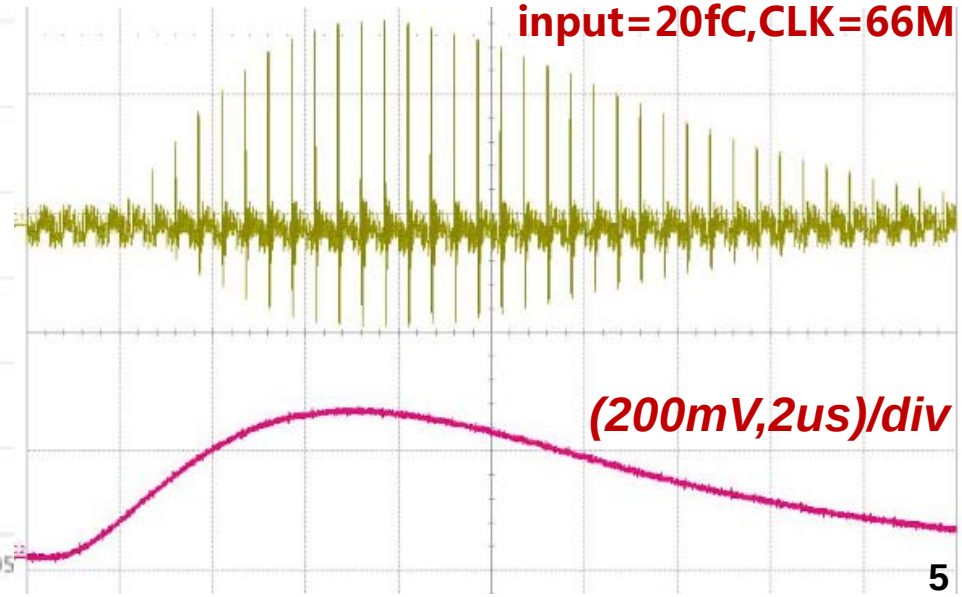


INL improves



input=20fC

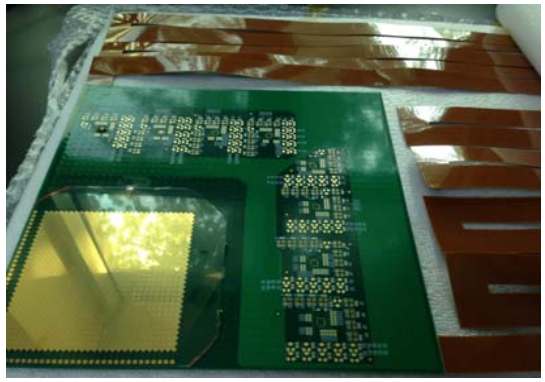
2u,4us

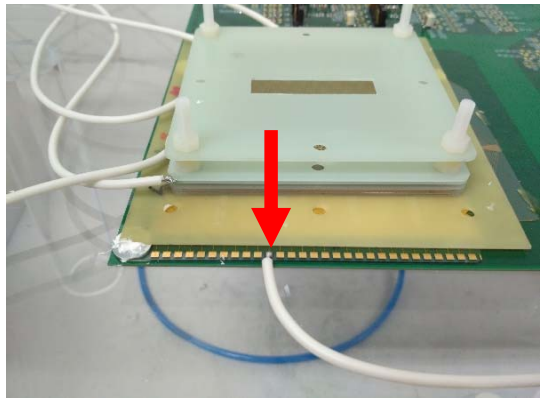


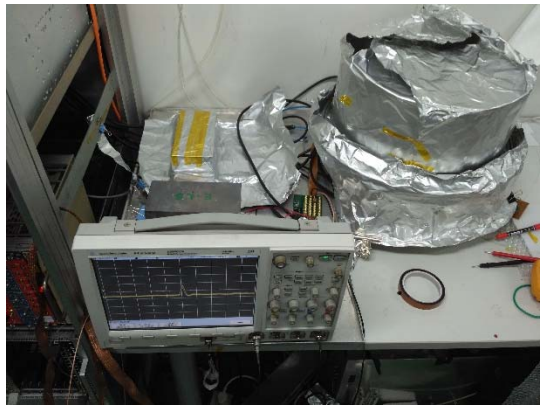
input=20fC,CLK=66M

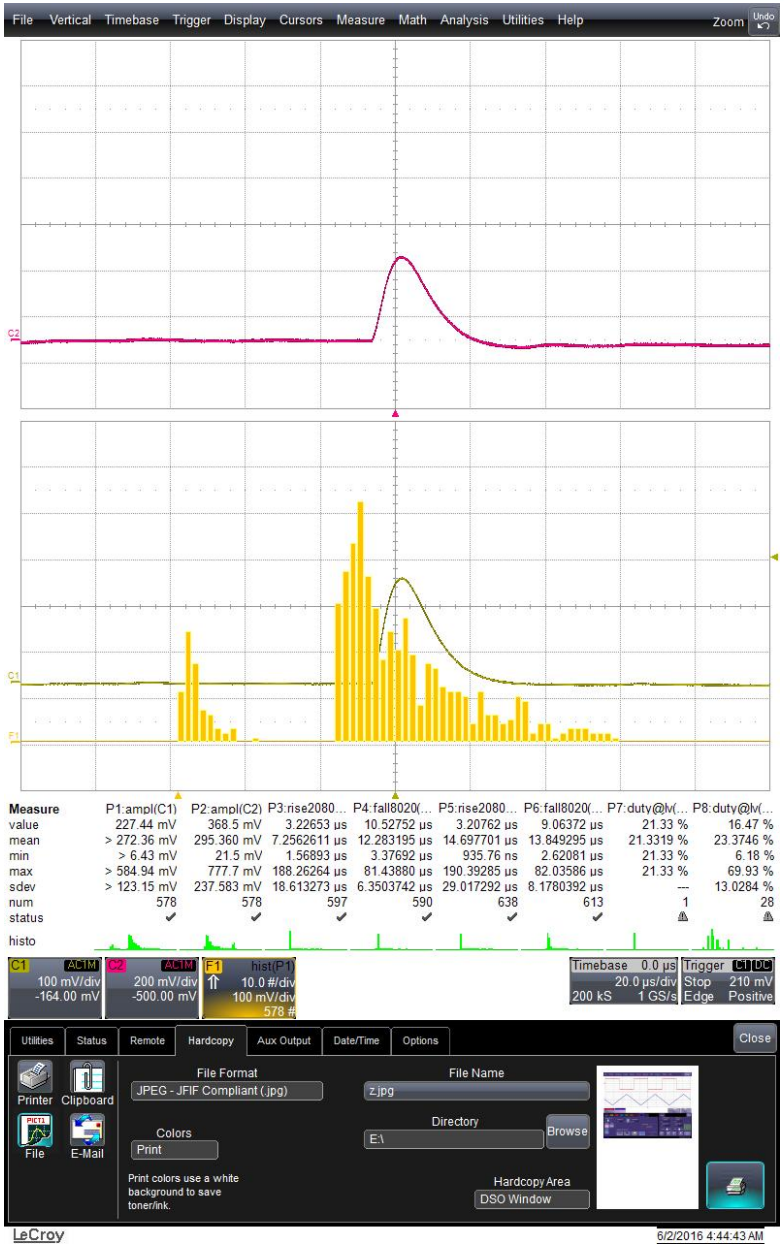
(200mV,2us)/div

与tile联调(带增益、刚挠板)

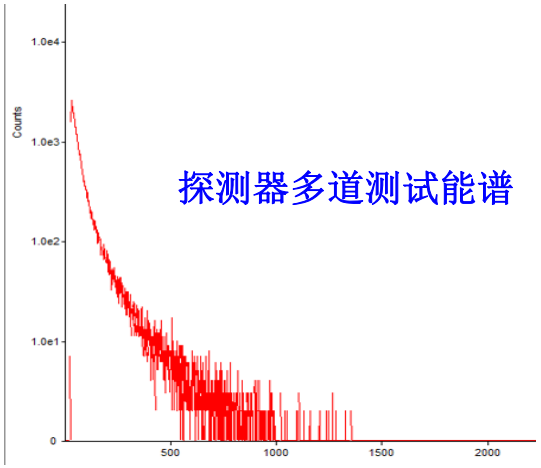








- 放射源： ^{90}Sr
- 探测器：双层THGEM
- 计数率约百KHz
- 约2m柔性板信号读出
- 随机选取芯片两通道输出
- 波形正常，**与放射源能谱基本吻合**，正常工作

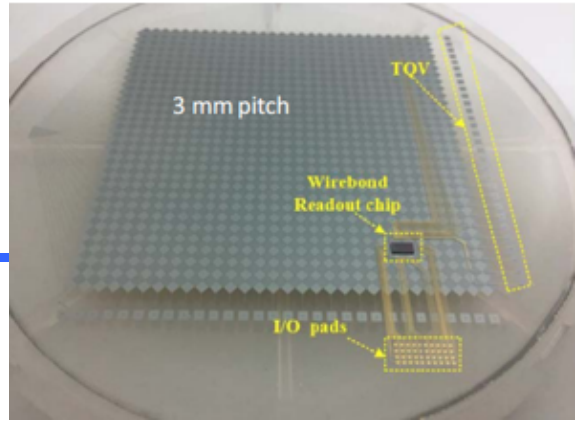


探测器多道测试能谱

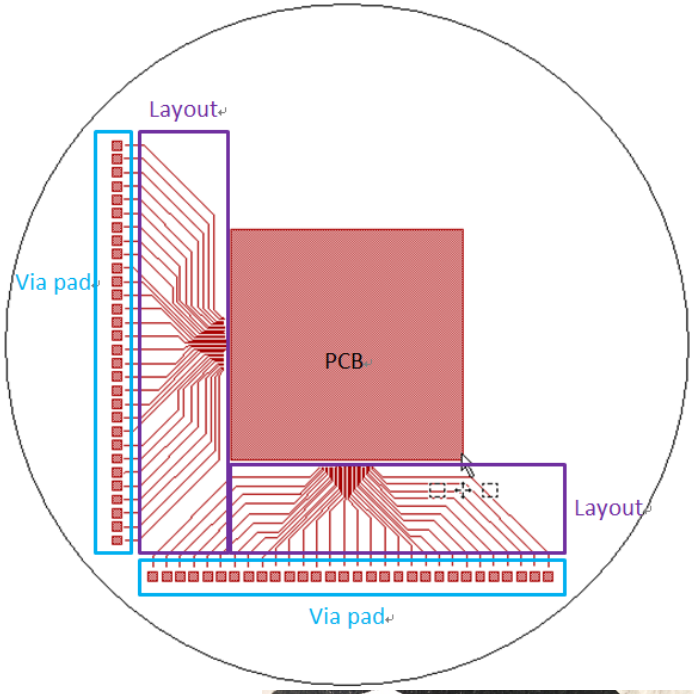
Outline

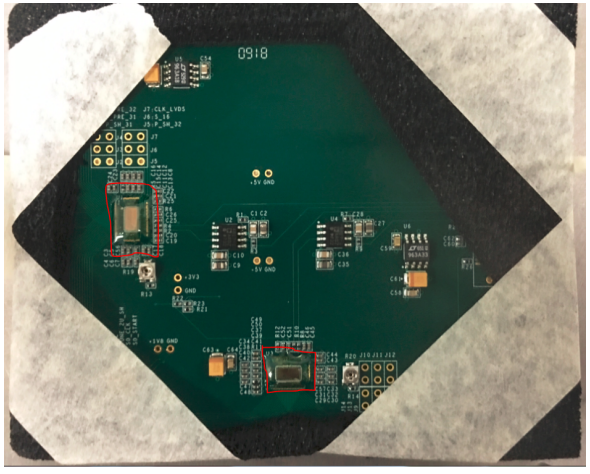
- **R&D status**
  - **Brief introduction of the ASIC**
  - **Chip functionality**
  - **Several test results**
- **Recent efforts**
  - **System integration concept**
  - **Back-end electronics and DAQ system**
- **Recent plan**

ASIC nEXO_v1 Test Board

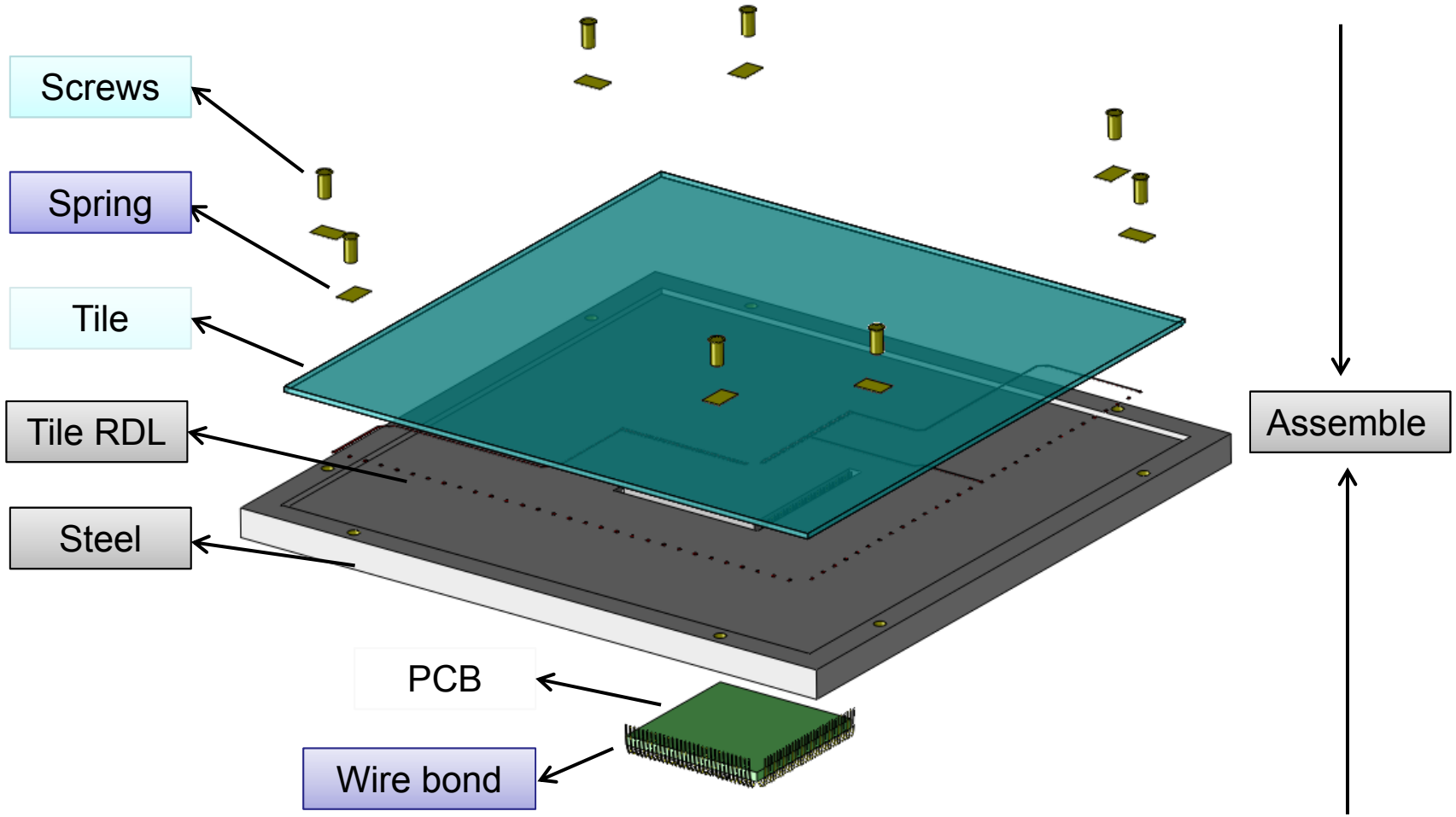


- **Two different size nEXO_v1 ASIC Test Boards are designed**
  - **~ 5cm × 5cm**
  - **~ 10cm × 10cm (same as the wafer)**
- **5cm×5cm PCB**
  - **Can verify the backside routing process**
  - **First impression of the impact of the ground plane vs 10cm×10cm PCB**
- **10cm×10cm PCB**
  - **Better ground shielding**
  - **Less bonding inductance (smaller PCB needs 3 bondings: TQV pads -> fanout, fanout -> PCB, PCB -> ASIC)**





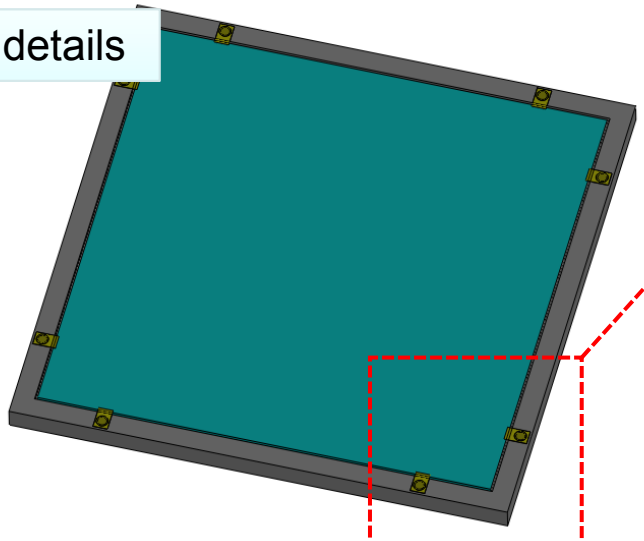
System integration concept

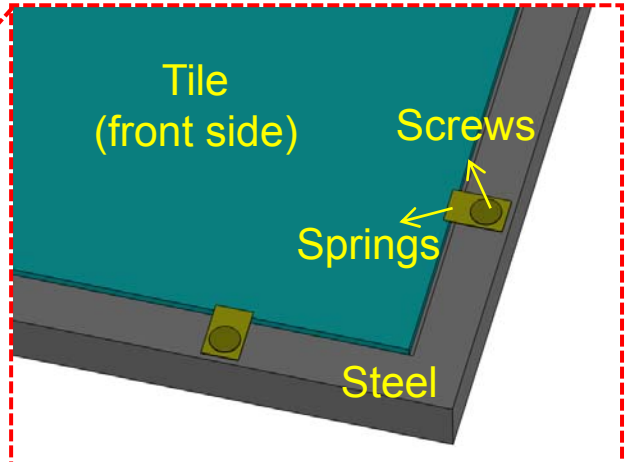


3D of installation

from Qidong

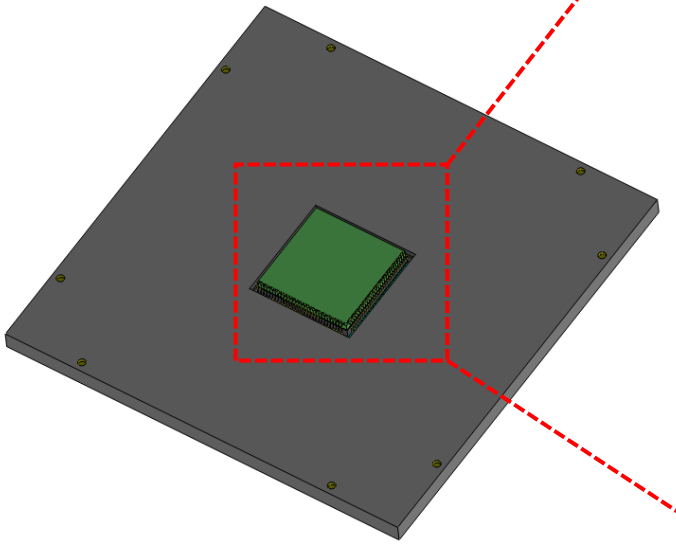
Front side details

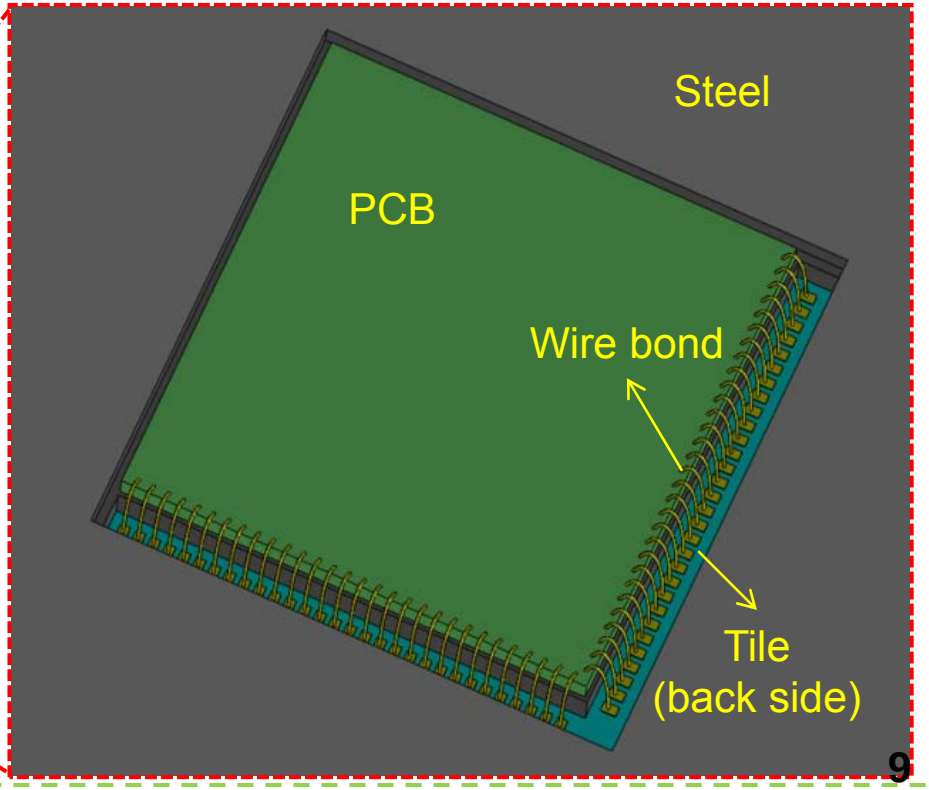




Details

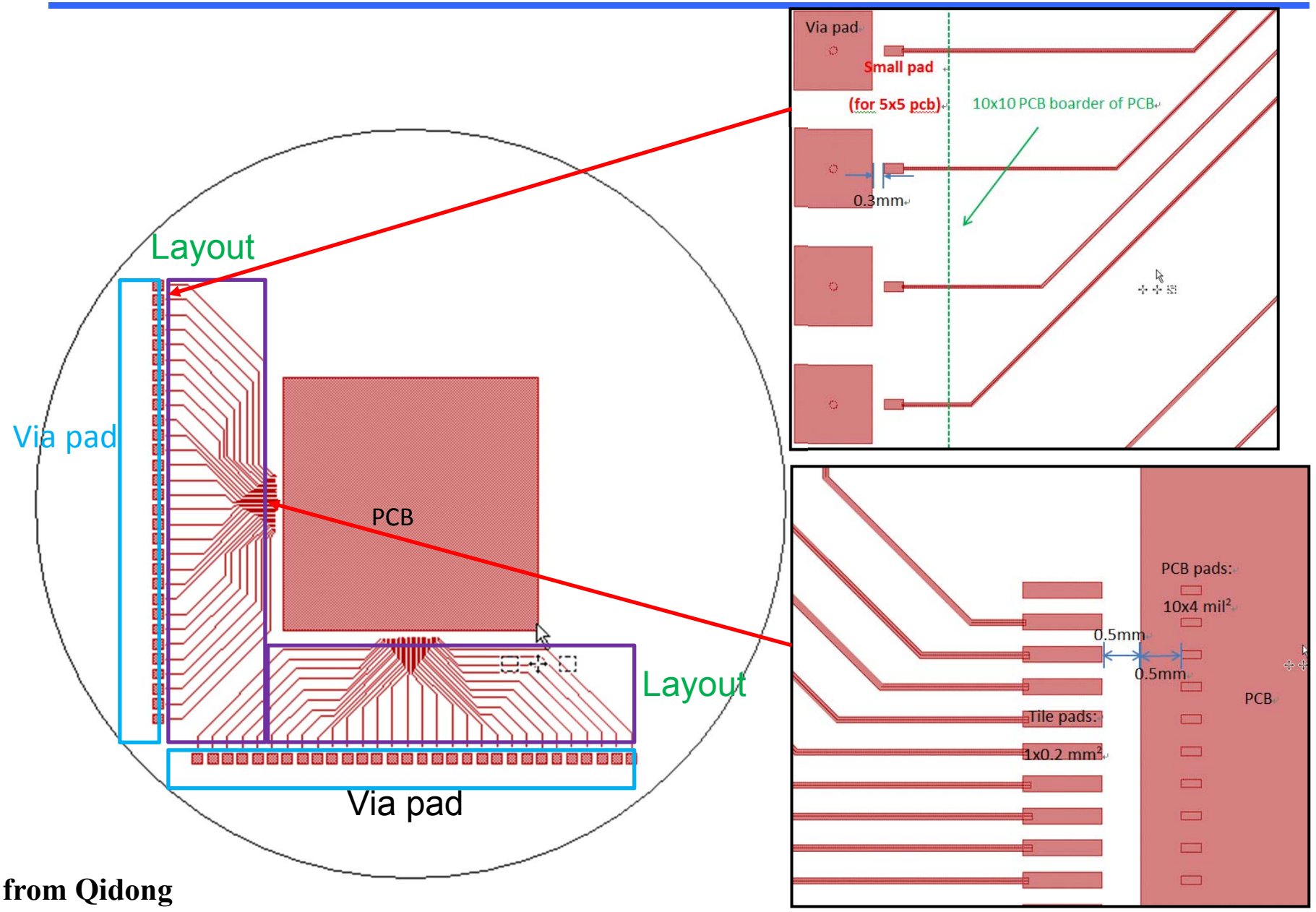
Back side details





from Qidong

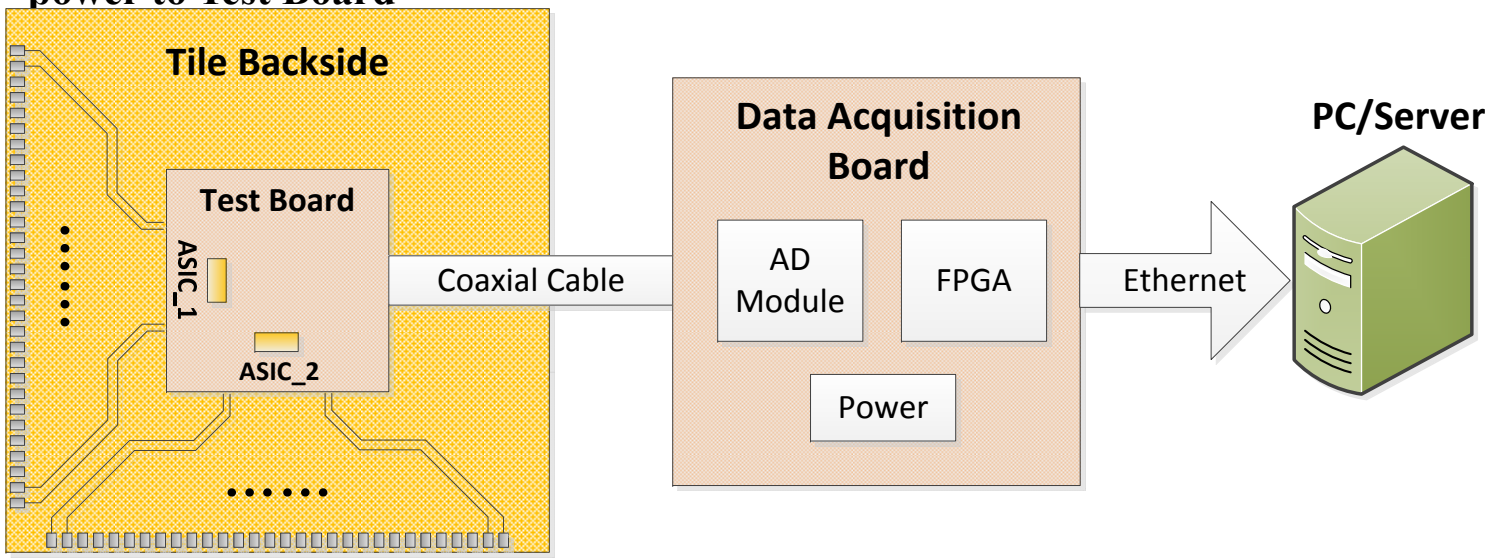
Interconnections between PCB & the Tile



from Qidong

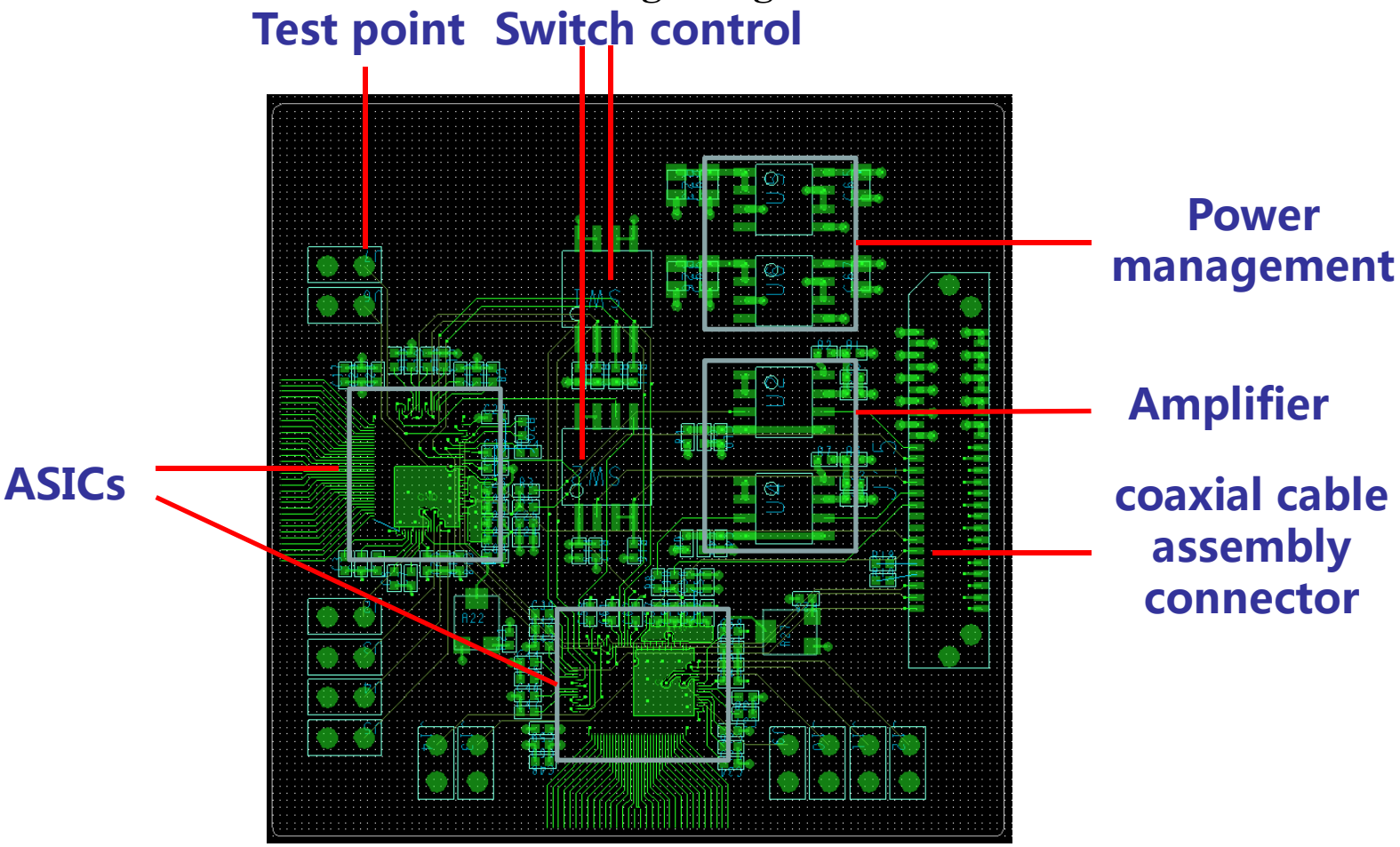
Backend electronics design

- **nEXO_v1 ASIC Test Board**
  - **Two 32-chn nEXO_v1 ASICs on one board**
    - **30 horizontal chns + 30 vertical chns**
  - **Limited numbers of extra components: power + driver**
    - **To verify the full channel readout first**
- **Coaxial Cable**
  - **Transfer the analog signal to Data Acquisition Board, as well as providing clock and power to Test Board**



Test Board Layout

- 5cm × 5cm 4 layer PCB design
  - All components are placed at the front side of PCB
  - A flat and smooth backside for glueing on the frame



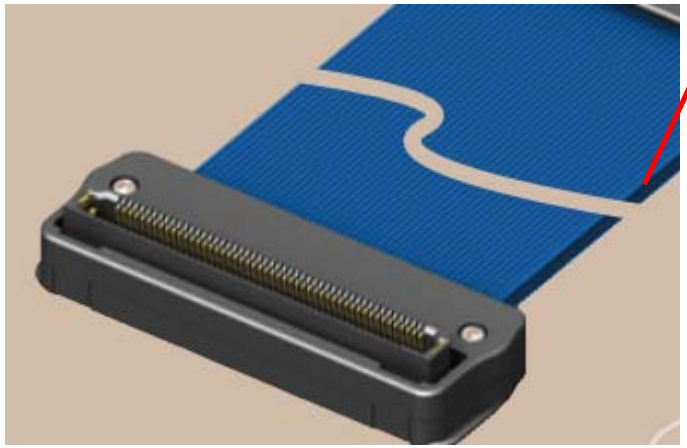
Coaxial Cable Assembly

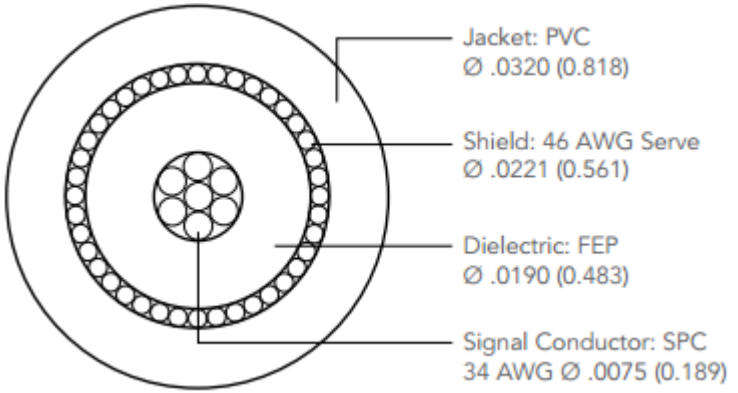
- **Prepare two kinds of coaxial cable assemblies**
  - **ERCD-025-40.00-TTR-TTL-1-D, 0.80 mm edge rate high-speed micro coaxial cable assembly, Samtec.**

5 cables for +5V,

5 cables for -5V,(optional)

other cables for signals.





PERFORMANCE DATA

Capacitance:	27 pF/ft (nominal)
Propagation Delay:	1.30 ns/foot
Flex Cycles:	80,000 cycles, 20-wide ribbon*
Current Rating:	Single conductor = 1.8 Amps** 20 conductors = 7.0 Amps**
Shield DCR:	116 Ω/1000 ft
CC DCR:	258 Ω/1000 ft
Min. Bend Radius:	.125"
Availability:	Single, 2-35 ribbon, tape bonded
Temperature Rating:	-25 °C to 105 °C, UL VW-1 Tested ***
DWV Working Voltage:	250 V†

Coaxial Cable Assembly (subst.)

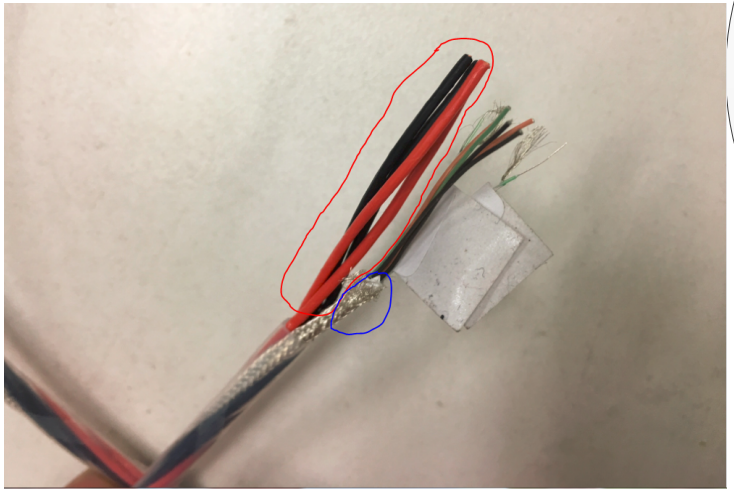
- **Custom Coaxial Cable Assembly, Ao Xun Tong Technology Co. Ltd**
  - **A local Chinese cable vendor**

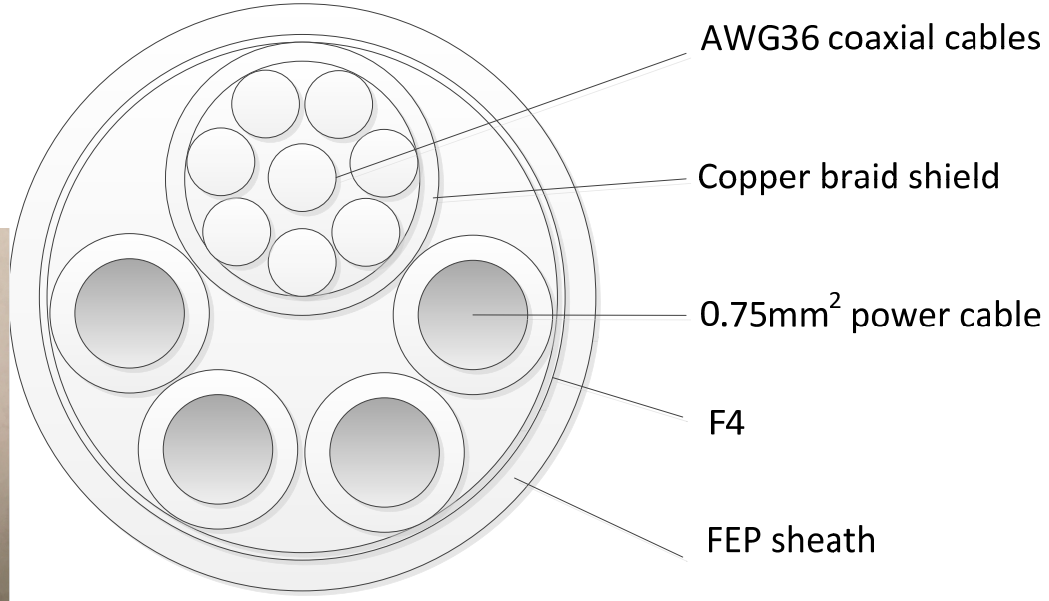
Four 0.75mm^2 cables for power supply,

8 AWG 36 coaxial cables for signals.

Min. temperature: -55 ℃

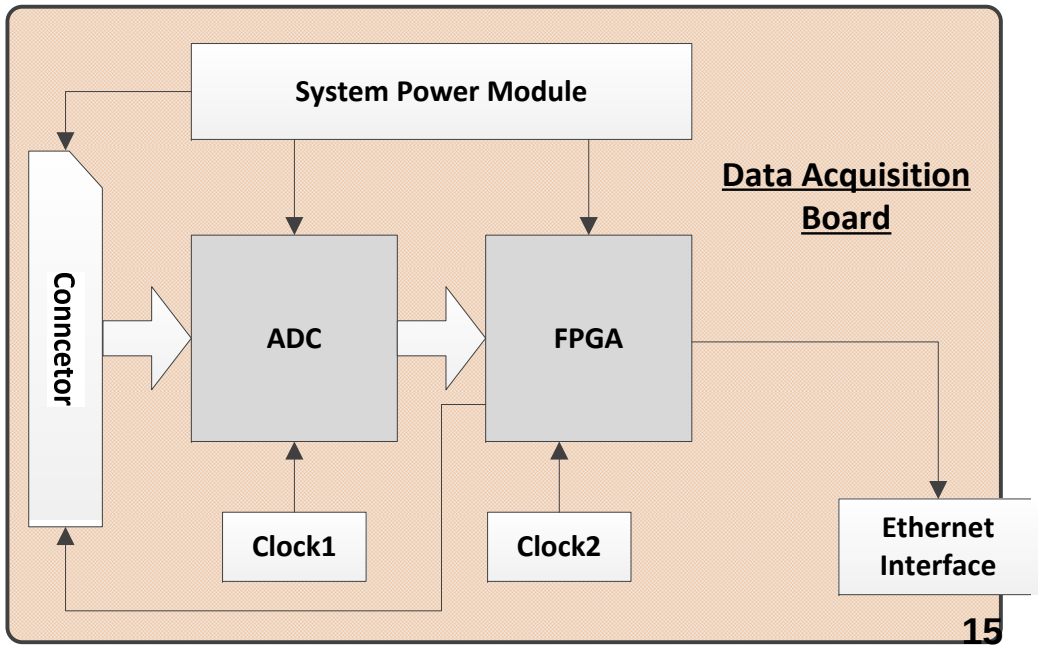
Performance tested and can be customized according to nEXO





Data Acquisition Board

- Data acquisition board designing element list as below
  - Connector: micro-coaxial cables, Samtec
  - ADC: 10-bit with 1.25 Gsps, ADI
  - FPGA: Vertex 5, Xilinx
  - CLK: Frequency range: 125 - 3000 MHz, 78 fs RMS Jitter Generation
  - Clock2: 100MHz OSC
  - Ethernet Interface
  - System Power Module
- PCB is designed



小结及计划

- Backend electronics
  - Design almost ready
  - Full system & debugging will be ready in May
  - Electronics selftest in 2 weeks
- Quartz wafer
  - Waiting for the full recovery of the equipments
  - Processing takes 1~2 month
- System integration & test
  - Full channel readout with a GEM as the source
  - Aiming at testing in LXe in 2018
- Future plans
  - ASIC improvement afterwards
  - Radioactivity test: ASIC + micro-coaxial cables

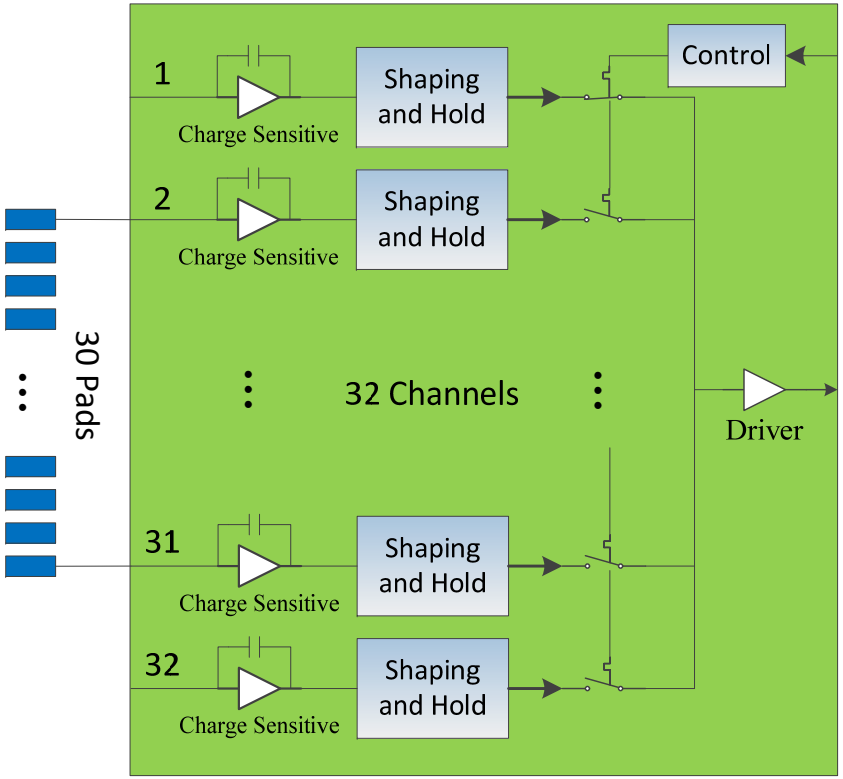
小结及计划

- Backend electronics
  - Design almost ready
  - Full system & debugging will be ready in May
  - Electronics selftest in 2 weeks
- Quartz wafer
  - Waiting for the full recovery of the equipments
  - Processing takes 1~2 month
- System integration & test
  - Full channel readout with a GEM as the source
  - Aiming at testing in LXe in 2018
- Future plans
  - ASIC improvement afterwards
  - Radioactivity test: ASIC + micro-coaxial cables

谢谢重点实验室支持/谢谢各位老师

Backup Slides

ASIC nEXO_v2 Test Board2



- **nEXO_v2 ASIC inputs**

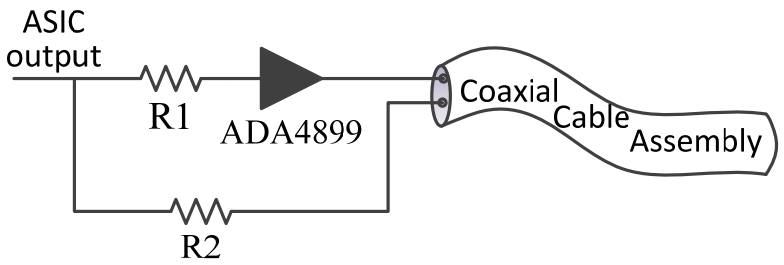
  30 pads on the tile backside input to 30 channels of all the 32 analog input channels of ASIC, 2 channels are reserved.

- **nEXO_v2 ASIC output**

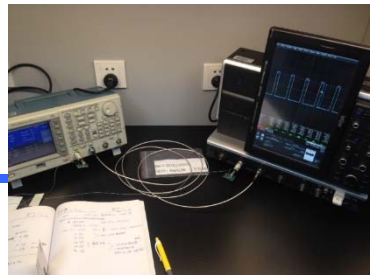
  The ASIC output signal to Coaxial Cable by two ways.

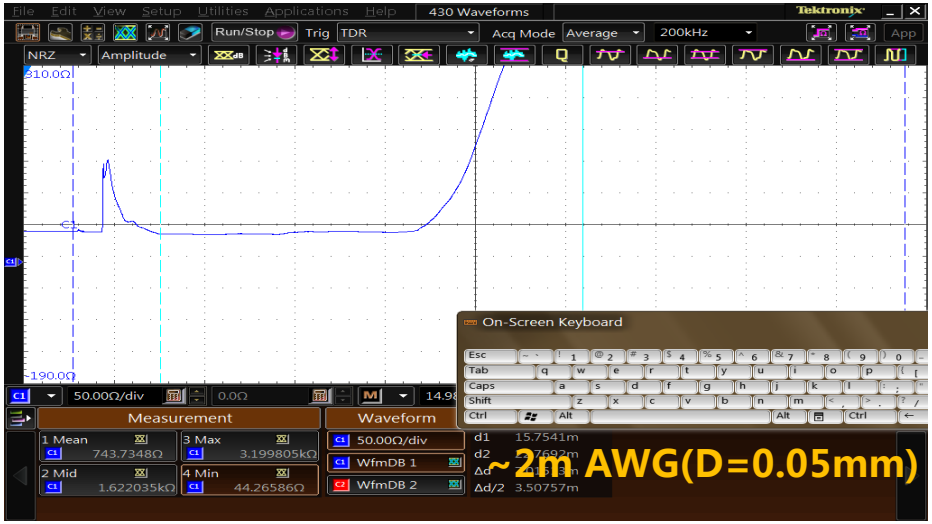
  – Directly output to cable

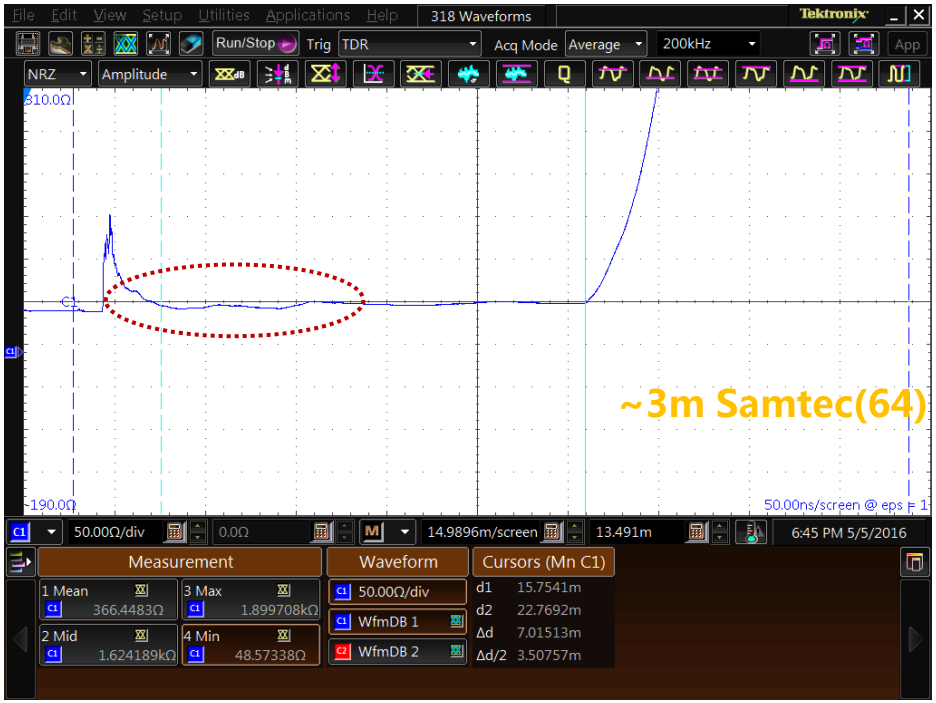
  – After driven by a amplifier (ADA4899)



cables test results







- Micro coaxial cables
- INL<0.08%(AWG cable, ~2m)
- AWG cable shows better transmission characteristics than Samtec cable
- DC resistance may impact the analog signal amplitude
- Radioactivity will be tested later