SKL
Particle Detection&Electronics

重点实验室自主部署项目
“用于低能X射线成像的高分辨计数型SOI芯片的研究”

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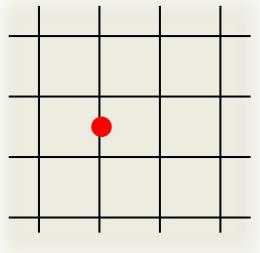
内容提要

- 研究目标
- CPIXTEG3b测试结果
  - 原型芯片
- CNPIX1设计
  - 实用化芯片
- CNPIX1初步测试结果
  - 问题与应对
- 总结

研究目标

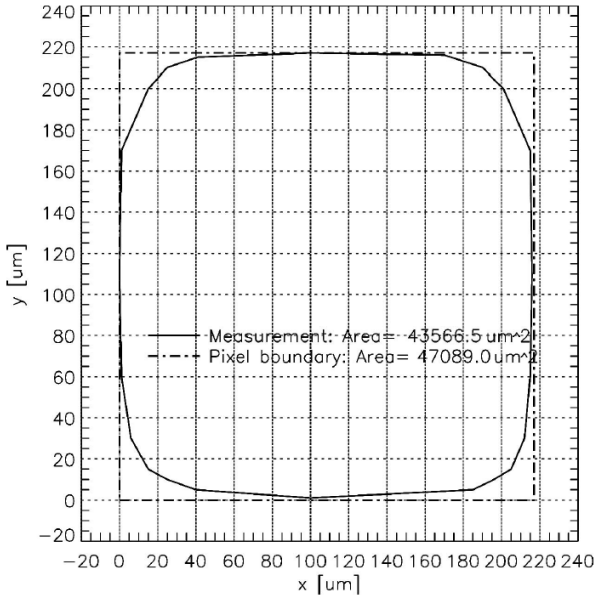
- 同步辐射中的X射线成像探测器
  - 成像板（IP），例如MAR345，180mm/9s
  - CCD，例如SX-165，165mm/1s
  - 像素阵列（PAD），例如PILATUS 3X 1M，170mm/500Hz
  - 读出速度对于蛋白质晶体学非常重要！
- 计数型像素阵列探测器的商业产品
  - 像素尺寸从172um缩小到75um
  - 能区从6-20keV（Si）扩展到100keV（CdTe）
  - 先发和技术优势，市场垄断
- SOI计数型芯片瞄准的是<50um像素和2-12keV能区
  - 新型有机复合材料的铁电性研究，30um，8keV
  - 二维GISAXA方法测量细胞膜的结构变化，2.1~4.5keV，入射窗1um
  - 覆盖了蛋白质晶体学能区（10-12 keV）

像素缩小带来的问题



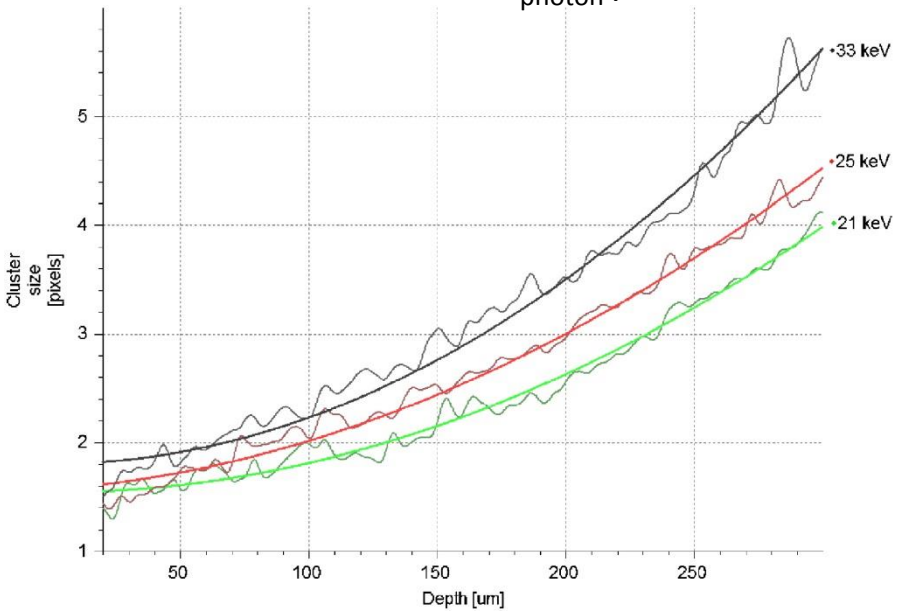
- Charge sharing
  - 单个X射线的载流子簇团在相邻电荷收集极（像素）感应出电流信号，导致多重计数或者零计数问题（取决于甄别器阈值）

像素217um，阈值 > E_{photon} / 2



虚线：像素尺寸
实线：有效探测区域92.5%
引用自J. Synchrotron Rad. (2006). 13, 120-130

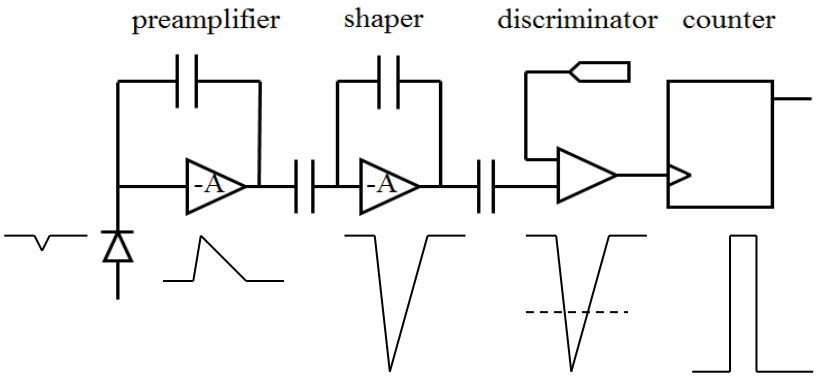
像素55um，阈值 < E_{photon} / 2

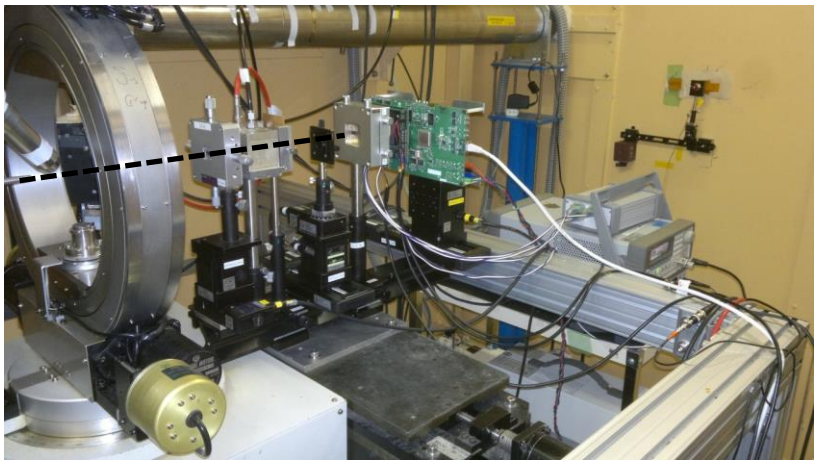


横轴：载流子簇团漂移距离
纵轴：计数的多重度
引用自NIMA 607 (2009), 192-195

CPIXTEG3b测试结果

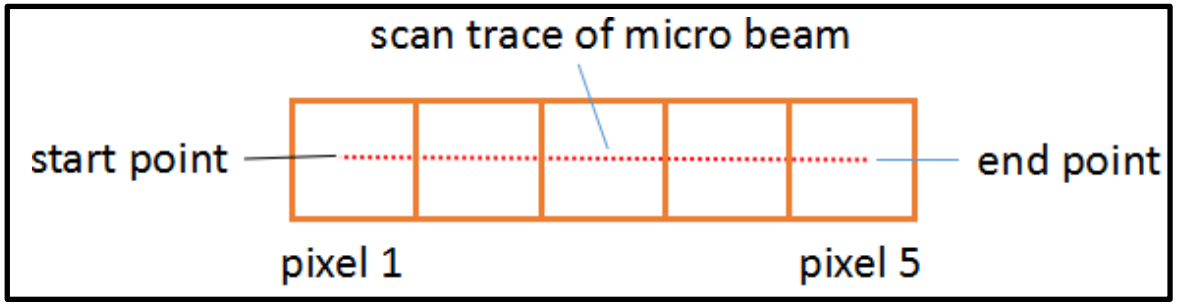
- 计数型SOI像素阵列原型芯片
  - 面积6mm*6mm
  - 像素尺寸50um
  - 阵列规模64*64
  - 甄别器阈值独立可调
  - 像素内6bit计数器
- 同步辐射束流测试setup
  - 原初束斑0.8mm
  - 经3um pin hole截取后 < 10um
  - 6 keV & 16 keV

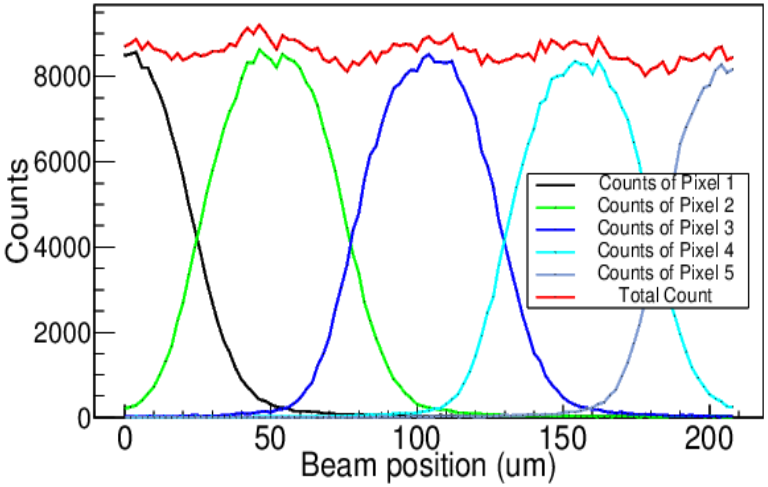


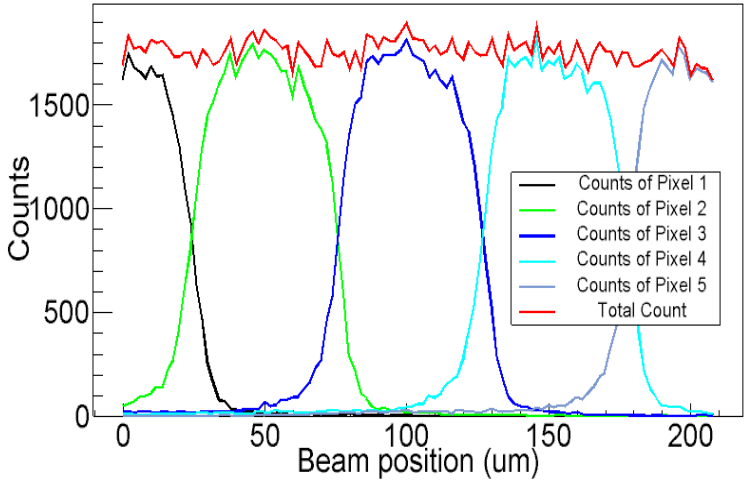


Charge sharing at pixel edge

- Scan across 5 pixels from center to center
  - Step size = 2um
- Uniform efficiency can be achieved at pixel edge
  - Threshold = ½ E_{photon}





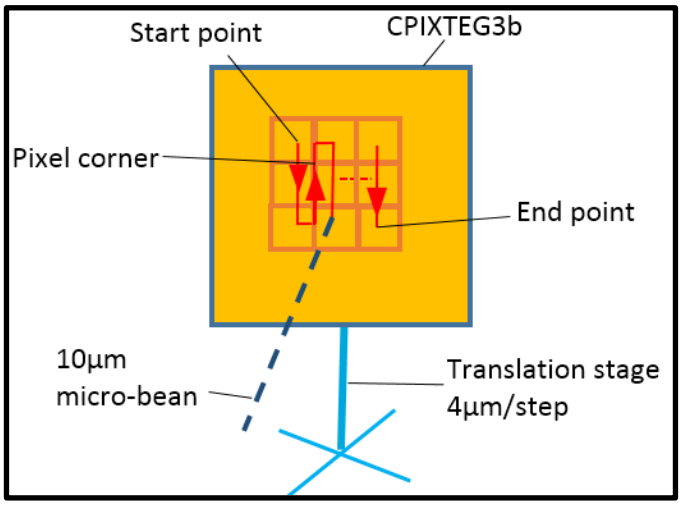


Charge sharing at pixel edge for 6 keV (left) and 16 keV (right) X-ray

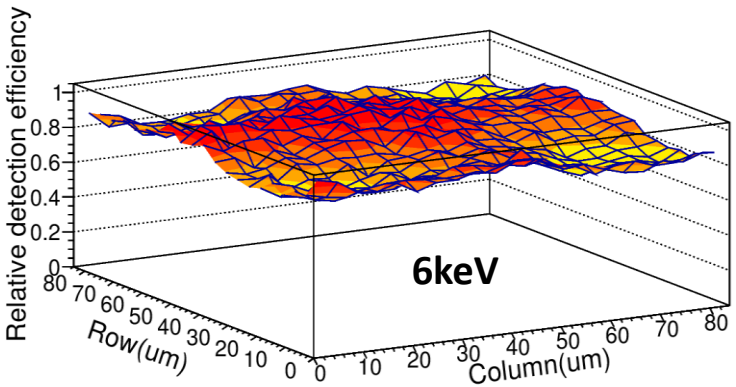
Charge sharing at pixel corner

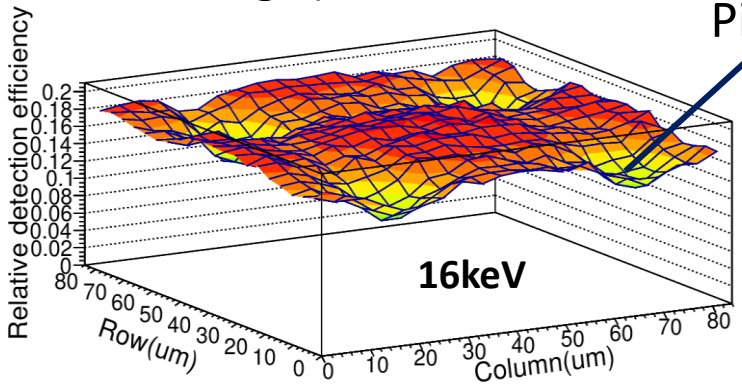
- Across 3×3 pixel-square
  Step = 4um for two direction

- Inevitable loss of efficiency at the corner
  Threshold = ½ E_{photon}
  Charge shared by 4 pixels adjoined



- Considerable effects on pixel sensor with small pixel size
  - Solution: to compare the charge between adjoining pixels and make the winner take the count (winner-takes-all logic)

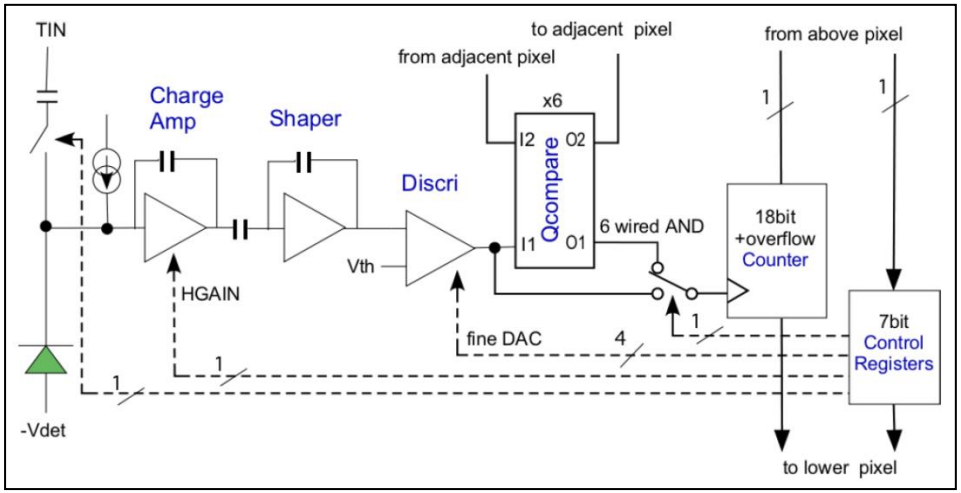




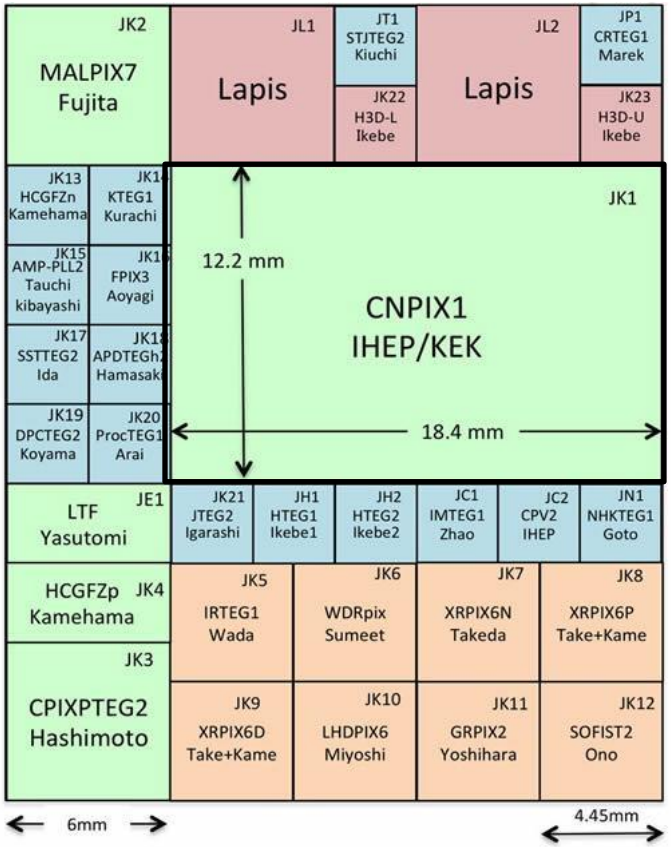
Charge sharing at pixel corner for 6 keV (left) and 16 keV (right) X-ray

CNPIX1设计

- 大面积实用化芯片
  - 单芯片面积18.4mm × 12.2 mm
  - 阵列规模：328x256（84K）
  - 像素尺寸：52um ×45um （正六边形）
  - ENC+FPN < 60e
  - 计数器增加为18+1bit
- Charge sharing仲裁逻辑
  - Qcompare模块

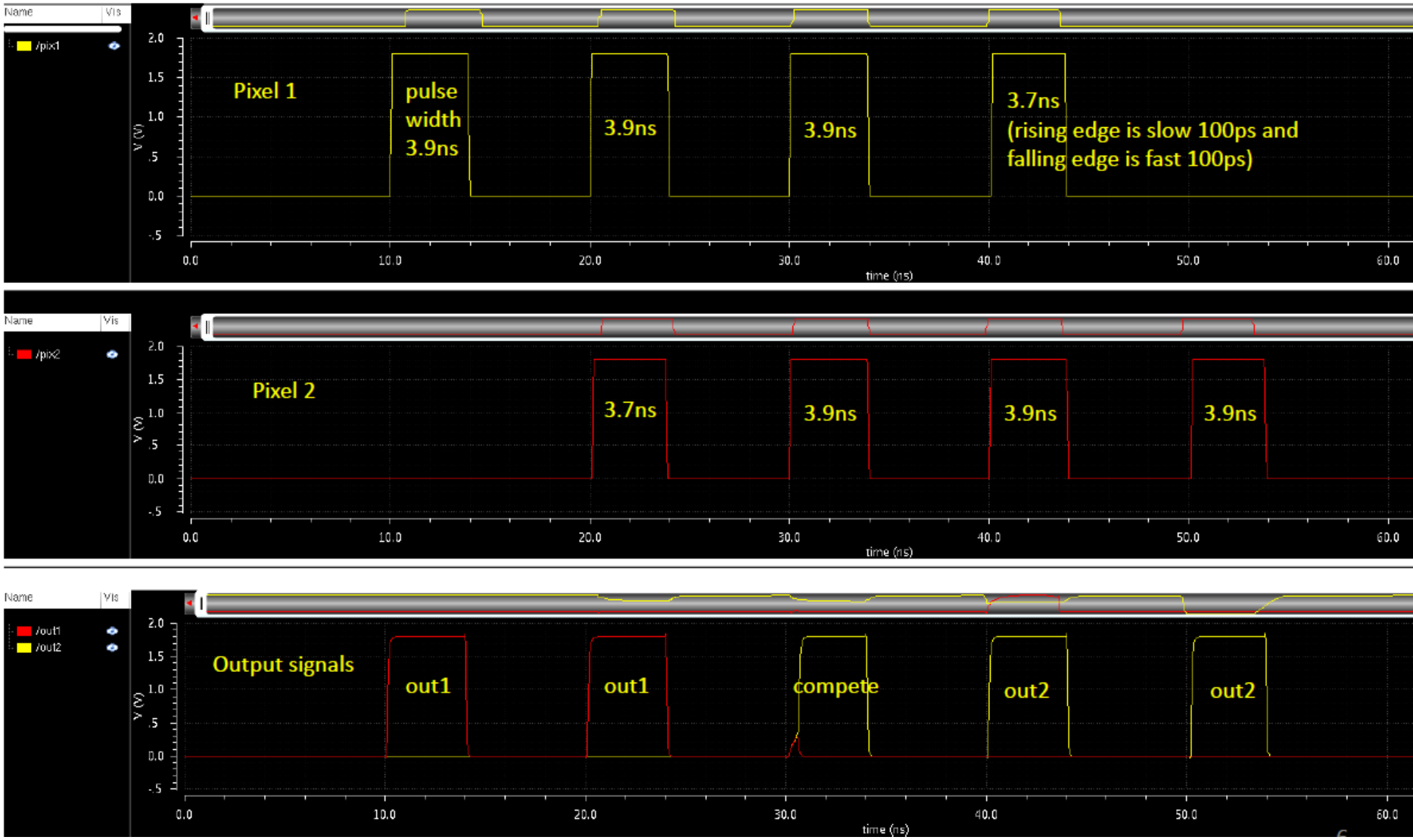


FY16-1 MPW 流片概览

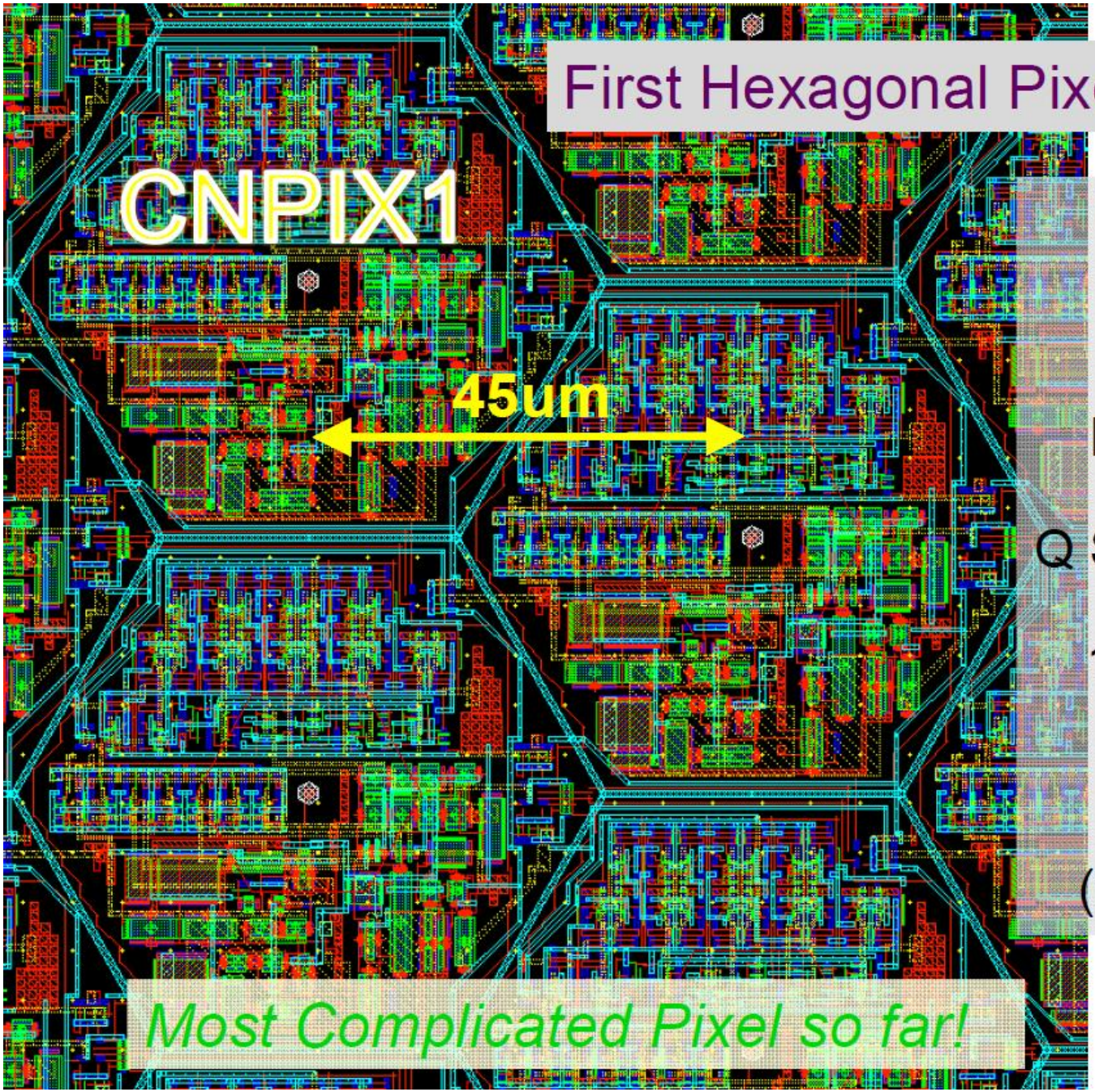


Assuming output signal from a discriminator, which receive larger signal than adjacent cell, has faster rising edge and longer pulse width, the Compare circuit can select right counter clock.

Simulation results



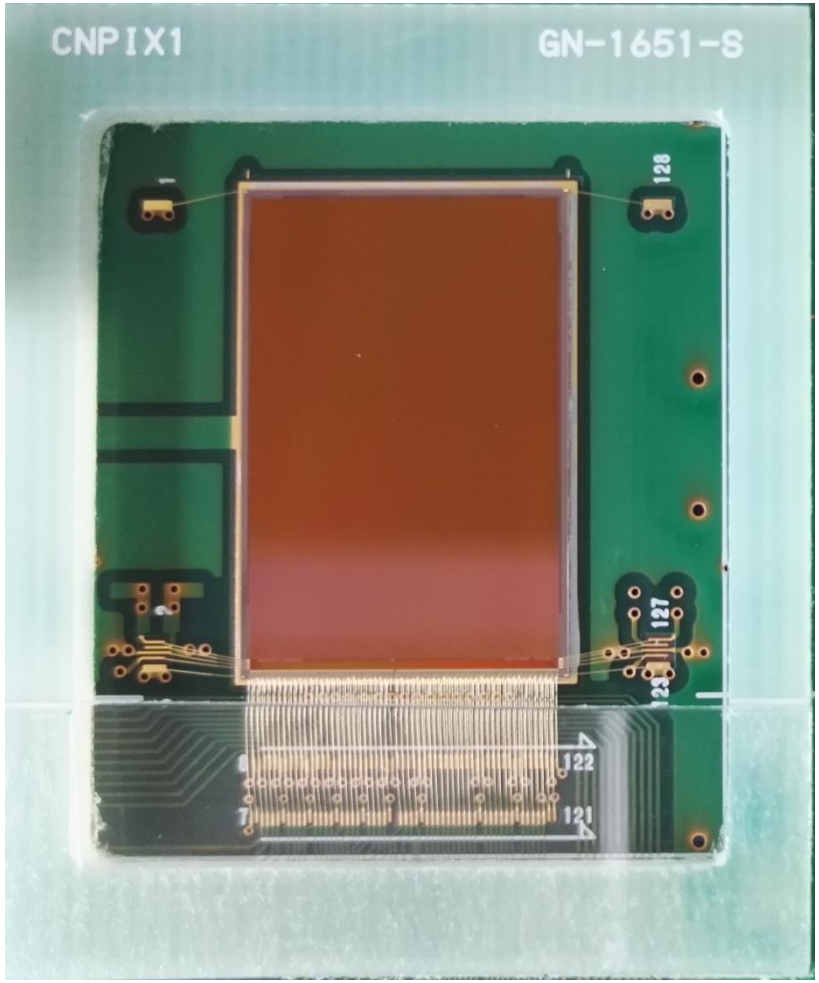
First Hexagonal Pixel in SOIPIX



Charge Amp
+
Shaper
+
Discriminator
+
Q Share Handling
+
19bit Counter
+
7bit register

(in 2,340 um^2)

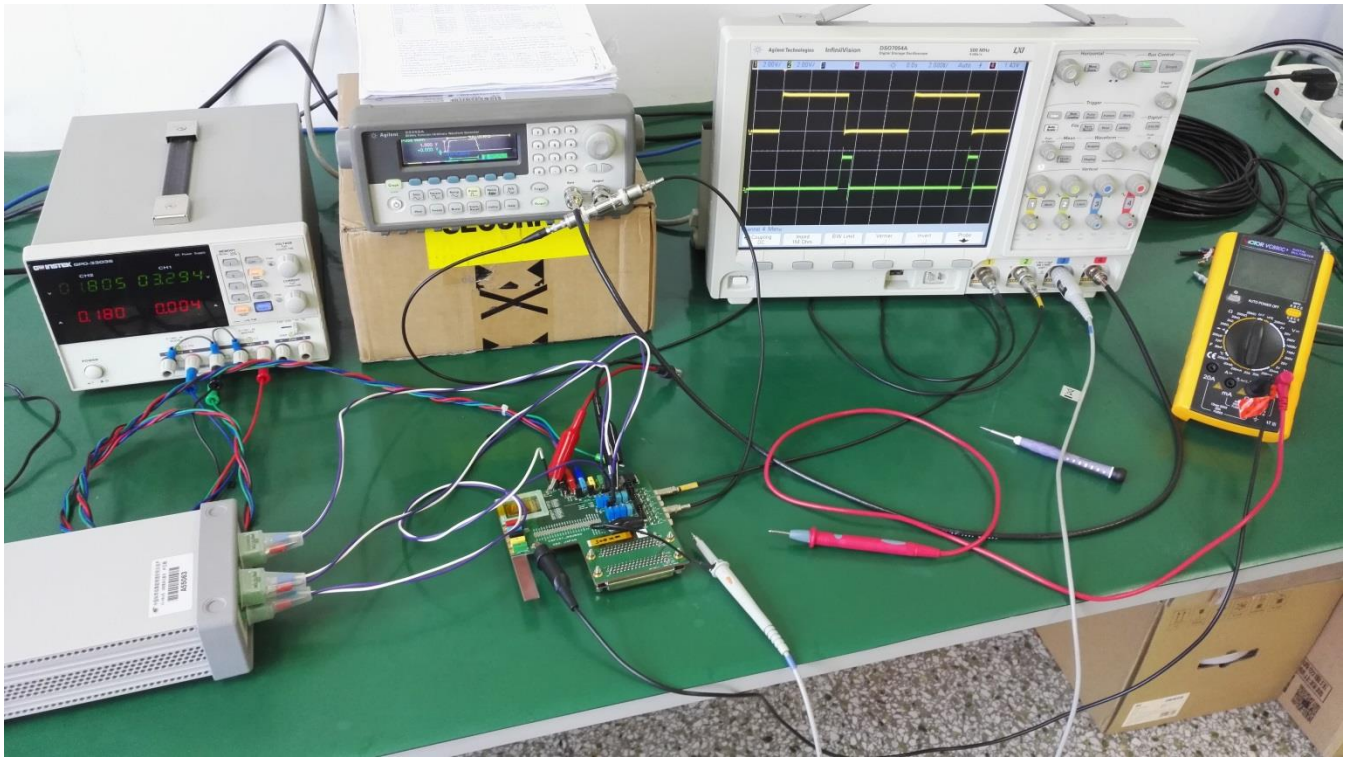
	Pilatus3	Eiger	Medipix3RX	Timepix3	HEPS_TF	CNPIX1
Pixel size	172um x 172um	75um x 75um	55um x 55um	55um x 55um	150um x 150um	**45um x 52um**
No. of pixels	487 x 195 (94,965)	256 x 256 (65,536)	256 x 256 (65,536)	256 x 256 (65,536)	72 x 104 (7488)	**304 x 224 (68,096)**
counter depth	20bits	12bits	12bits x 2 or 24bits x1	14bits(ToA) + 10bits(ToT)	20bit	**18+1 bits**
No. of threshold	1	pixel size	1 or 2	1	1	**1**
Care for Charge Sharing	No	No	Yes	No	No	**Yes**
Lowest threshold energy (noise)	2.7 keV	2.7 keV	72 e-	Unkown	116e-	**60e-（1.5 keV）**
Counting rate	10 MHz (with retrigger)	~1 MHz	Unkown	Unkown	3.5MHz	**1MHz**
Pixel Shape	Square	Square	Square	Square	Square	**Hexagonal**



- 2017.5收到芯片
  - ✓ Wire bonding到测试子板
  - ✓ 基于KC705和SiTCP的读出系统

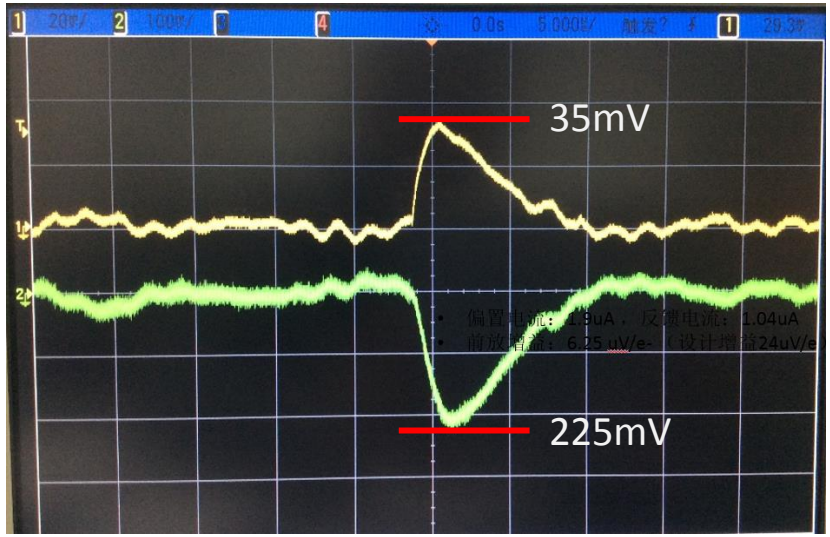
Standalone test setup

- DSUB-50 board standalone
  - Power and signal supplied by instruments
  - 8 single test pixels configured properly



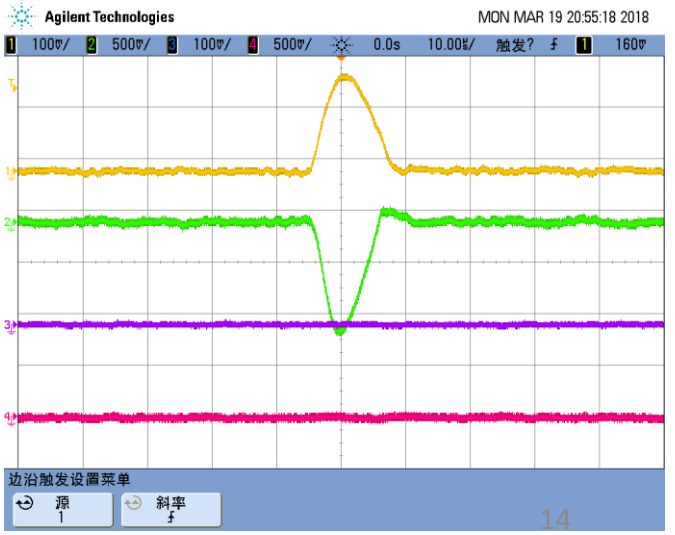
单像素功能验证

- ^{55}Fe源测试
  - ✓ 5.9 keV X射线响应
- 红外激光测试
  - ✓ 1064 nm激光脉冲响应



前放

成形

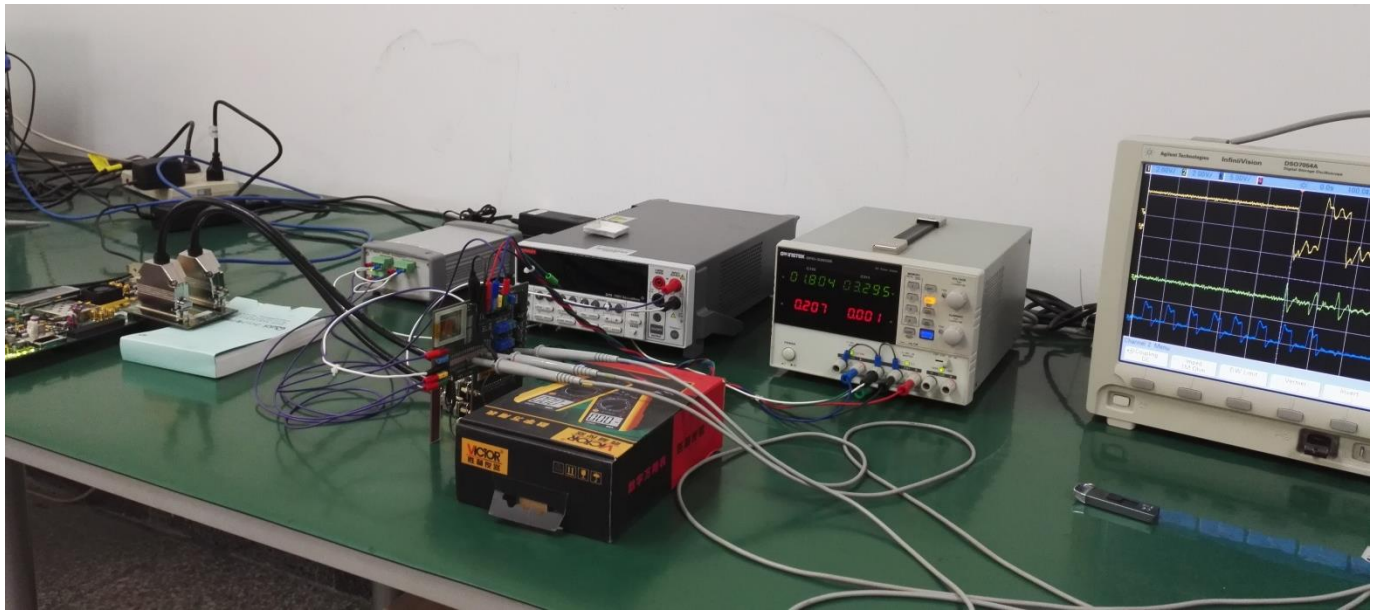


cnateg2 [amplifier / shaper

cnateg4 [amplifier / shaper

Full test system setup

- Full test system configured
  - Chip current: 207mA@1.8V / 0.001mA@3.3V
  - IIN_DAC grounded due to incorrect VR8 value.

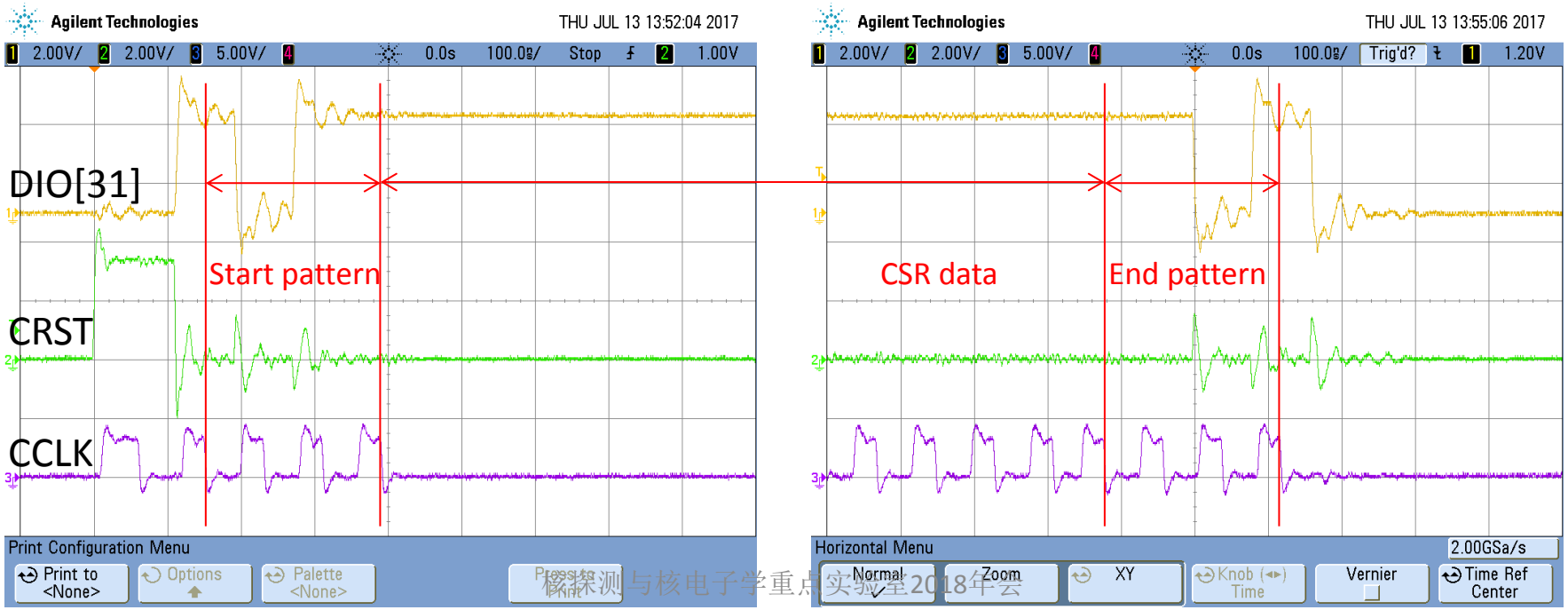


CSR register write (without readback)

- DAQ configuration:
  - CSR initialize value = 127 (111_1111)
  - Enable Array Block: from 7 to 7
- DIO[31], CRST, CCLK verified by oscilloscope
  - Significant crosstalk on CRST

Table. 3. Serial data Start/End bit pattern (left bit is first).

	Start Pattern	End Pattern	Total No. of bits
Data	1010	1001	6240 (328x19+8)
CSR	1011	1101	2304 (328x7+8)



CSR register readback

- DAQ configuration:
  - Enable Array Block: from 7 to 7
- No start/end pattern, no data

Table. 3. Serial data Start/End bit pattern (left bit is first).

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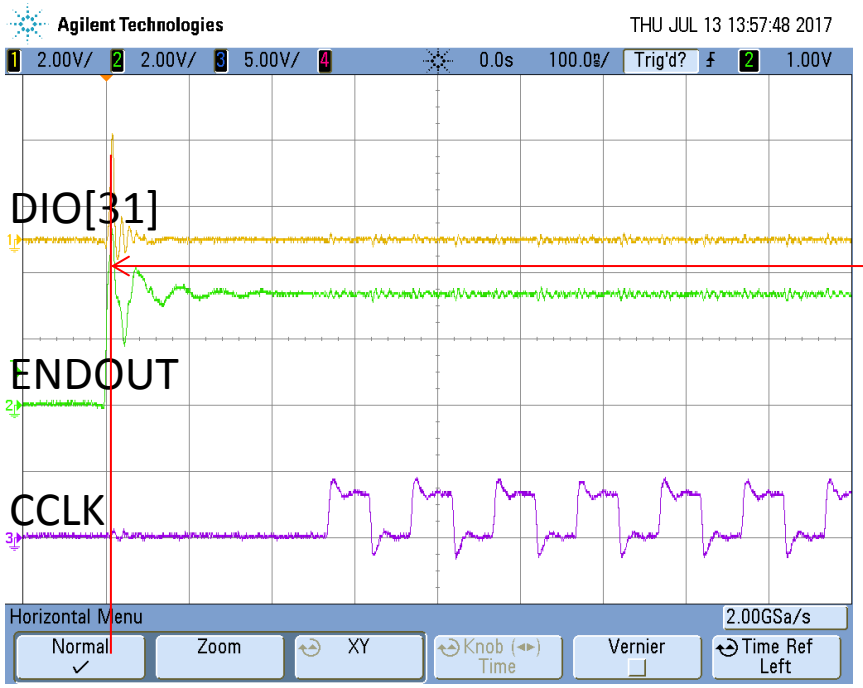
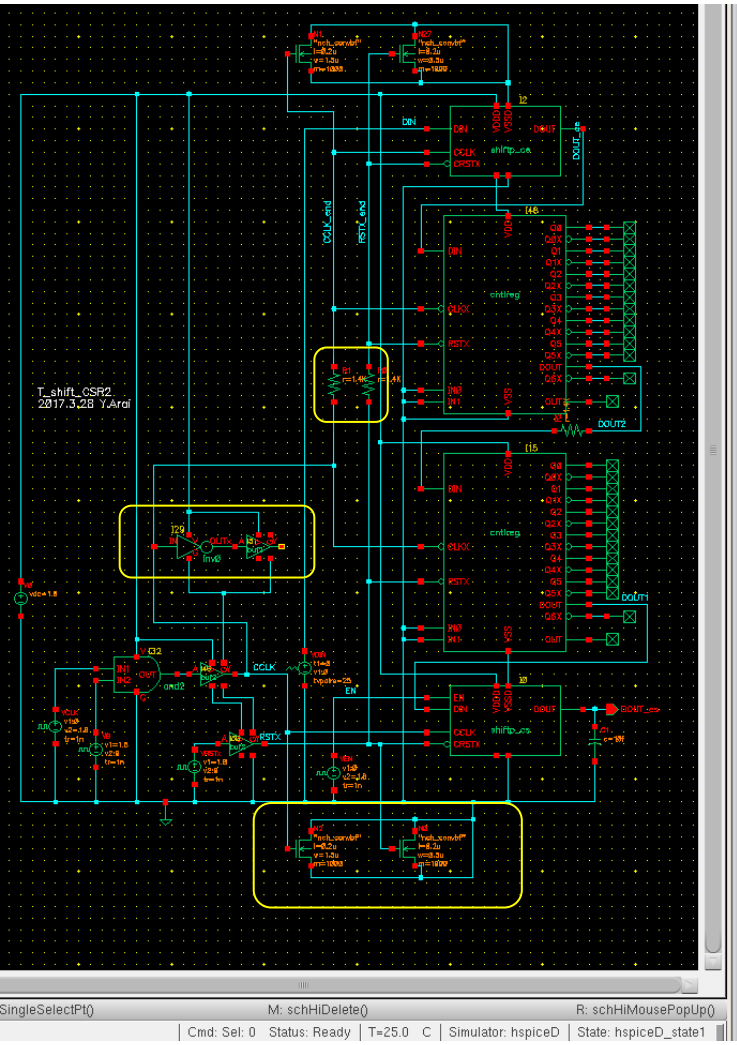
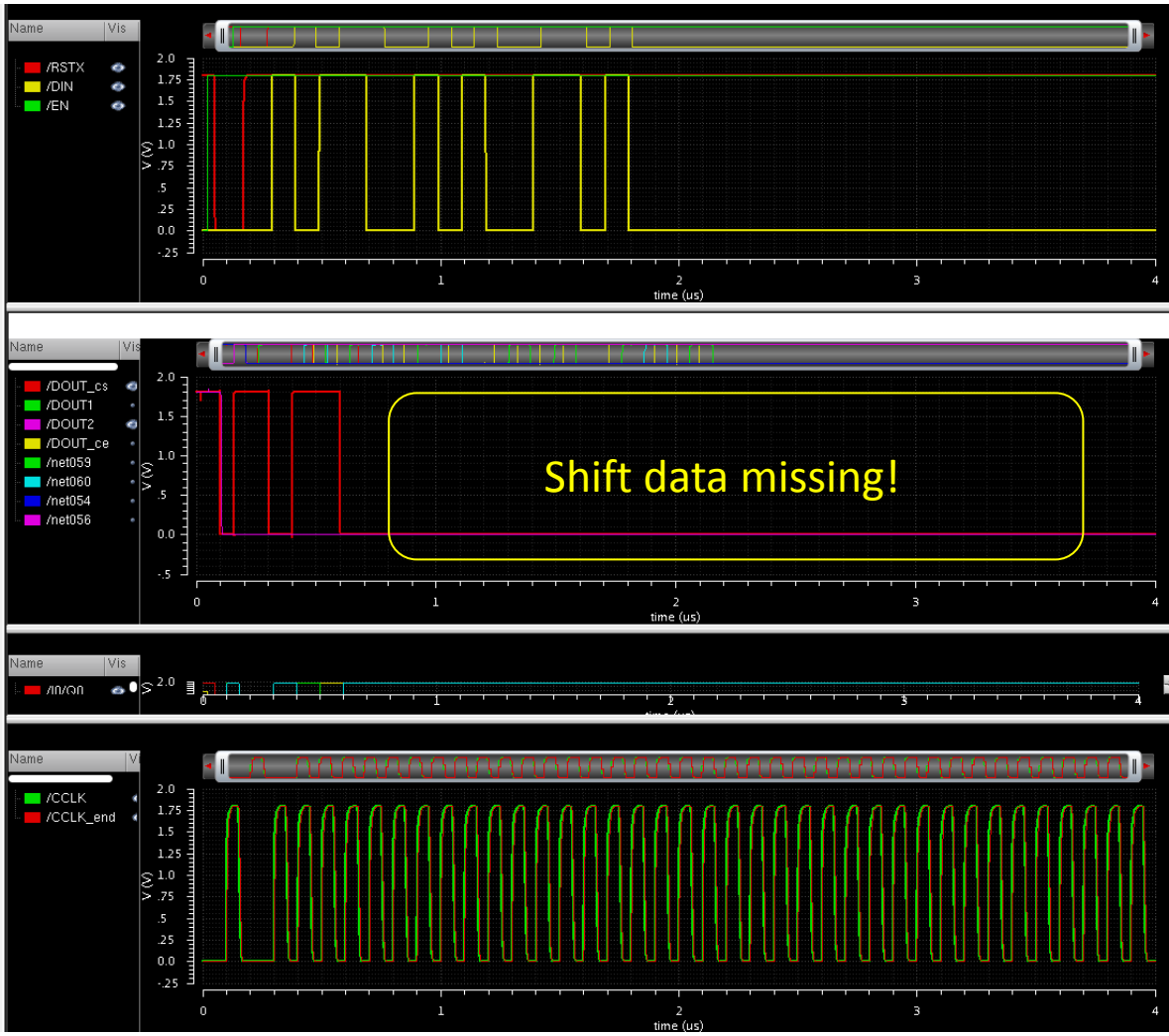
Data	1010	1001	6240 (328x19+8)
CSR	1011	1101	2304 (328x7+8)



Clock distribution problem identified

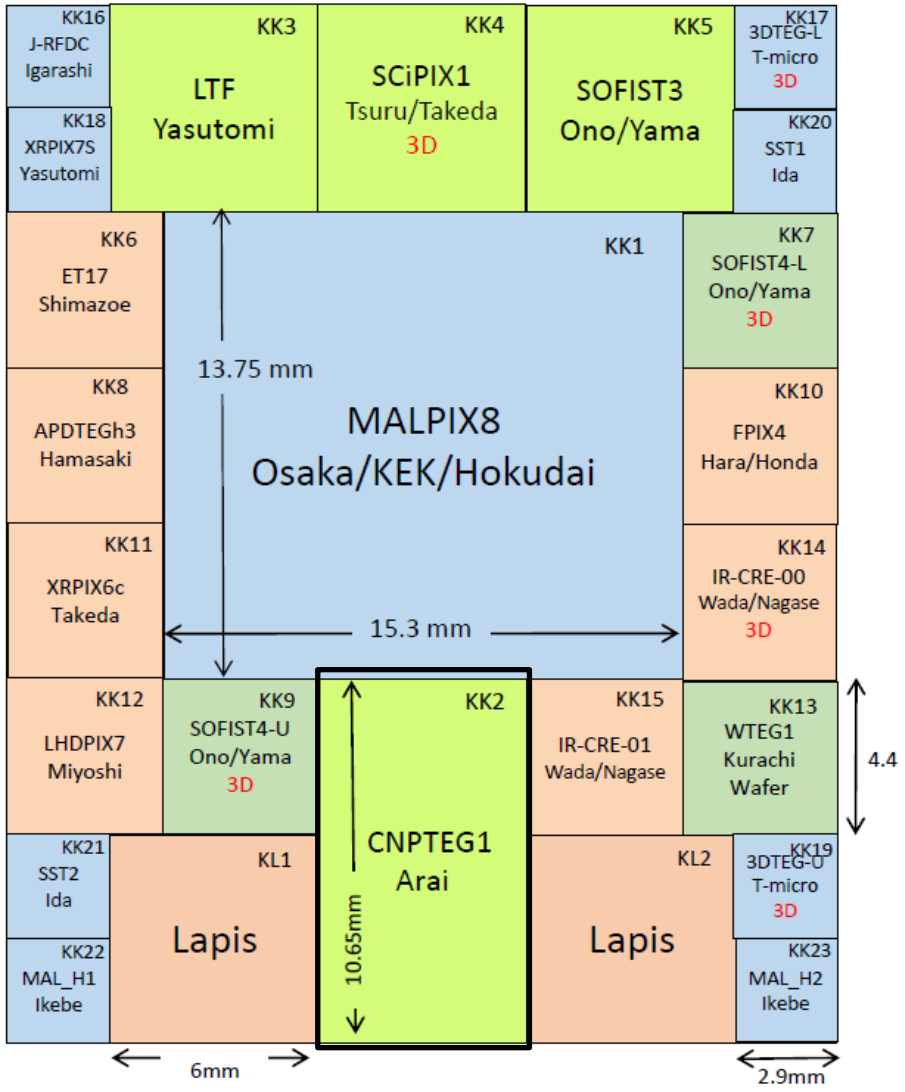
CSR shift (bad case）





New prototype CNPTEG1

- CNPIX1的修正版本
  - 解决了发现的各种问题
  - 2017.6提交
  - Wire bonding组装进行中
  - 2018.5交付高能所



总结

- 针对低能X射线成像的高分辨计数型SOI芯片
  - 小像素，45um*52um
  - 低噪声，ENC+FPN < 60e^-
- CNPIX1是首个针对实用的大面积芯片
  - 单像素功能已验证
  - 阵列寄存器配置存在问题，原因已找到
  - 新的设计CNPTEG1将于下月交付测试