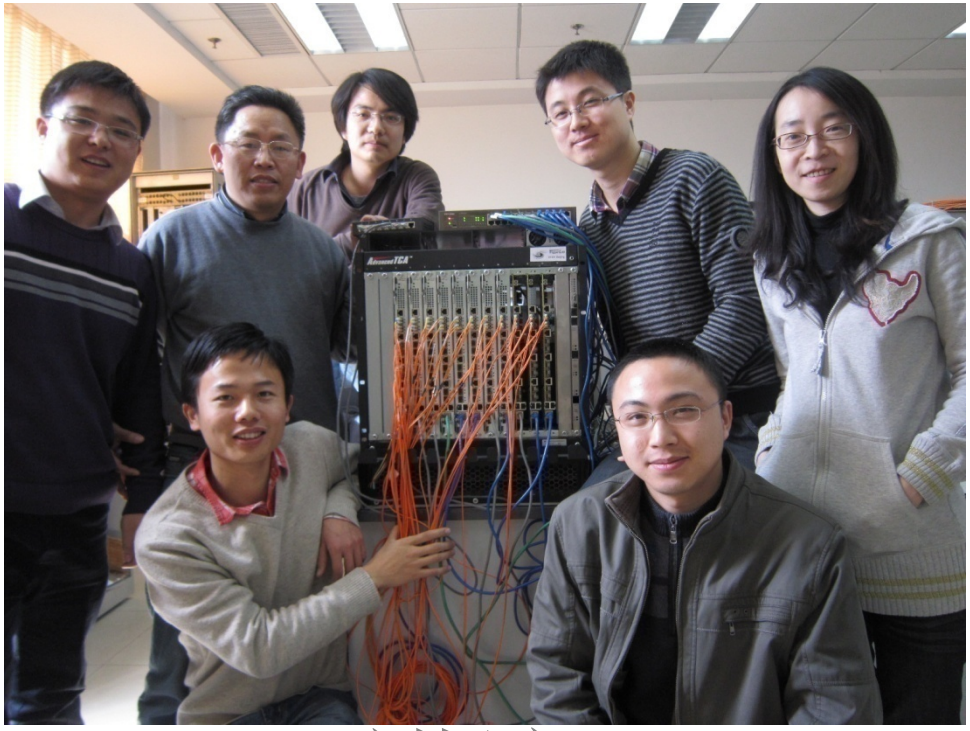
PANDA 实验的TDAQ系统预研介绍



刘振安
中科院高能物理所触发实验室
南开大学物理科学学院
2017年4月26-27日

报告内容

- 简单历史回顾
  - BESIII／PANDA互助合作
  - 973项目研究及其成果
  - 基金委重点项目支持及结果
  - DEPFET的技术升级
  - CMS实验的相关技术升级
- PANDA TDAQ中国组现状及进展
- 未来展望

BESIII/PANDA 互助合作

- 2006年开始德国团队加入BESIII
- 王贻芳介绍认识吉森大学的Wolfgang Kuehn 教授
  - BESIII Trigger？ Too late
- 2007年开始考虑PANDA 合作

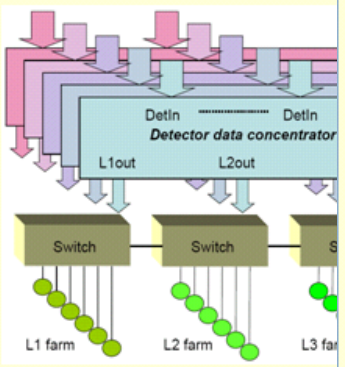
Overall review on PANDA Collaboration

- TrigLab started working on PANDA since W.K.'s visit to IHEP in 2006
- Start thinking Triggerless TDAQ and Compute Node(CN)

PANDA TDAQ

- Motivation
  - Interaction rate of 10 Mio events/s
  - Expected data rate: 40-200GB/s
- Triggerless Data Acquisition (DAQ) System
- Continuously sampling DAQ : *flash ADCs*
  - *"self-triggered"* detector front end
  - Local feature extraction
    - Parametrized pulse shapes
    - Local cluster finding
- High quality clock distributed detector wide
  - Jitter ~ 25ps
  - Each signal gets a *timestamp*
  - *Necessary for event bulding*

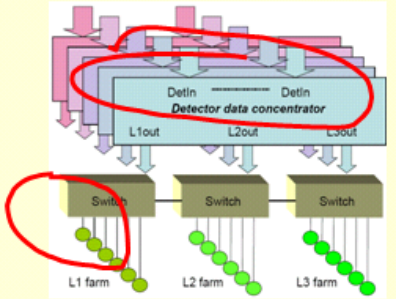
K. Korcyl, J. Otwinowski, Krakow



Oct.19 2008 *Zhen'An LIU, IHEP/Beijing* *3*
NSS/MIC2008,Dresden

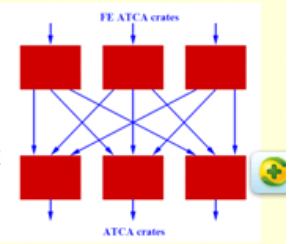
Why a Compute Node

- Data Concentrator
- Impossible *(complicated)* to store to disk
  - Need to pre-processing and online selection
- L1 farm
  - L1 trigger
  - Feature extraction
- TPC online tracking
  - Need of a compute device with large compute power, local memory and I/O capabilities
  - BUT: Commercial computing solutions do not fulfil our needs neither in bandwidth nor in computing power



New structure: KEY device Compute Node

Dedicated processors with very large I/O bandwidth based on FPGAs to have whatever logic we need



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Overall review on PANDA Collaboration

- Frequent Technical Discussions were made at IHEP and Fermlab with RT07 for new TDAQ system

CN Optimization

- Prototype: Beijing (together with Giessen)

  After Discussion:=>Universal high performance platform for multiple applications

Fearure:

- High Performance Compute Power:
  - 5x (Virtex-4 FPGA + 2Gb DDR2)
- ~32Gbps Bandwidth
  - 13x RocketIO to backplane
  - 5x Gigabit Ethernet
  - 8x Optical Link
- 2 Embedded PowerPC in each FPGA
  - Real time Linux
- ATCA compliant

Oct.19 2008
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Zhen'An LIU, IHEP/Beijing

国家重点基础研究发展计划（973计划）

项目编号：2008CB817700
项目名称：自由电子激光和反质子加速器重大基础研究
项目负责人：姜晓明

课题编号：2008CB817702
课题名称：FAIR有关的大型实验探测器关键技术问题研究

课题负责人：徐瑚珊
子课题负责人：沈肖雁 -> 刘振安

一、任务完成情况 之 研究内容

1. CsI晶体的γ探测阵列样机
2. 气体探测器样机 (TPC, Micromegas, RETGEM)
3. 硅微条探测器样机
4. PWO晶体
5. 高计数率MRPC和LMRPC原理样机的研制
6. PANDA实验事例组建和触发判选系统

一、任务完成情况 之 概述2

- **PWO晶体探测器原理样机研制（上海硅酸盐所＋近物所）**

  成功研制出了PANDA量能器所需PWO探测器单元样机，并建立了一套PWO晶体生长质量控制体系及性能测试平台系统。

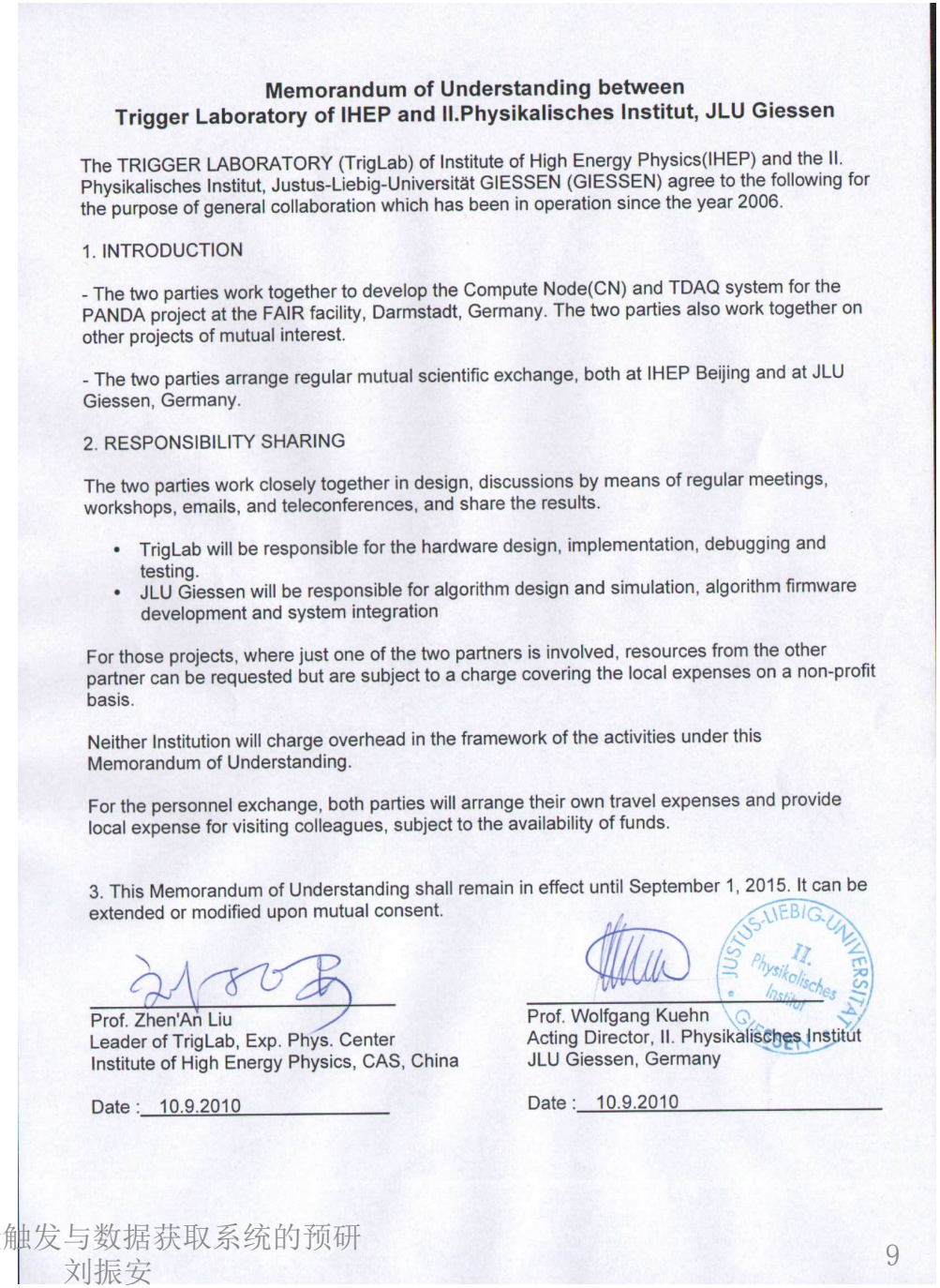
- **高计数率MRPC和LMRPC原理样机研制（清华＋科大）**

  成功研制出计数率高达100kHz/cm^2、时间分辨优于40ps的高计数率MRPC样机（清华）；成功研制出大面积/长读出条多气隙电阻板室（LMRPC）样机（科大）。水平国际领先，被CBM合作组采用。

- **PANDA实验事例组建和触发判选系统研制（高能所）**

  成功为PANDA实验研究设计出了一套具有高速传输与高性能在线事例特征提取、触发与事例预选择和事例组建能力的高性能计算机节点样机。该技术被PANDA合作组采用。

- 2010年10月触发实验室与德国吉森大学第二物理研究所签署了5年合作备忘录。



Memorandum of Understanding between
Trigger Laboratory of IHEP and II.Physikalisches Institut, JLU Giessen

The TRIGGER LABORATORY (TrigLab) of Institute of High Energy Physics(IHEP) and the II. Physikalisches Institut, Justus-Liebig-Universität GIESSEN (GIESSEN) agree to the following for the purpose of general collaboration which has been in operation since the year 2006.

1. INTRODUCTION

- The two parties work together to develop the Compute Node(CN) and TDAQ system for the PANDA project at the FAIR facility, Darmstadt, Germany. The two parties also work together on other projects of mutual interest.

- The two parties arrange regular mutual scientific exchange, both at IHEP Beijing and at JLU Giessen, Germany.

2. RESPONSIBILITY SHARING

The two parties work closely together in design, discussions by means of regular meetings, workshops, emails, and teleconferences, and share the results.

- TrigLab will be responsible for the hardware design, implementation, debugging and testing.
- JLU Giessen will be responsible for algorithm design and simulation, algorithm firmware development and system integration

For those projects, where just one of the two partners is involved, resources from the other partner can be requested but are subject to a charge covering the local expenses on a non-profit basis.

Neither Institution will charge overhead in the framework of the activities under this Memorandum of Understanding.

For the personnel exchange, both parties will arrange their own travel expenses and provide local expense for visiting colleagues, subject to the availability of funds.

3. This Memorandum of Understanding shall remain in effect until September 1, 2015. It can be extended or modified upon mutual consent.

Prof. Zhen'An Liu
Leader of TrigLab, Exp. Phys. Center
Institute of High Energy Physics, CAS, China

Date : 10.9.2010

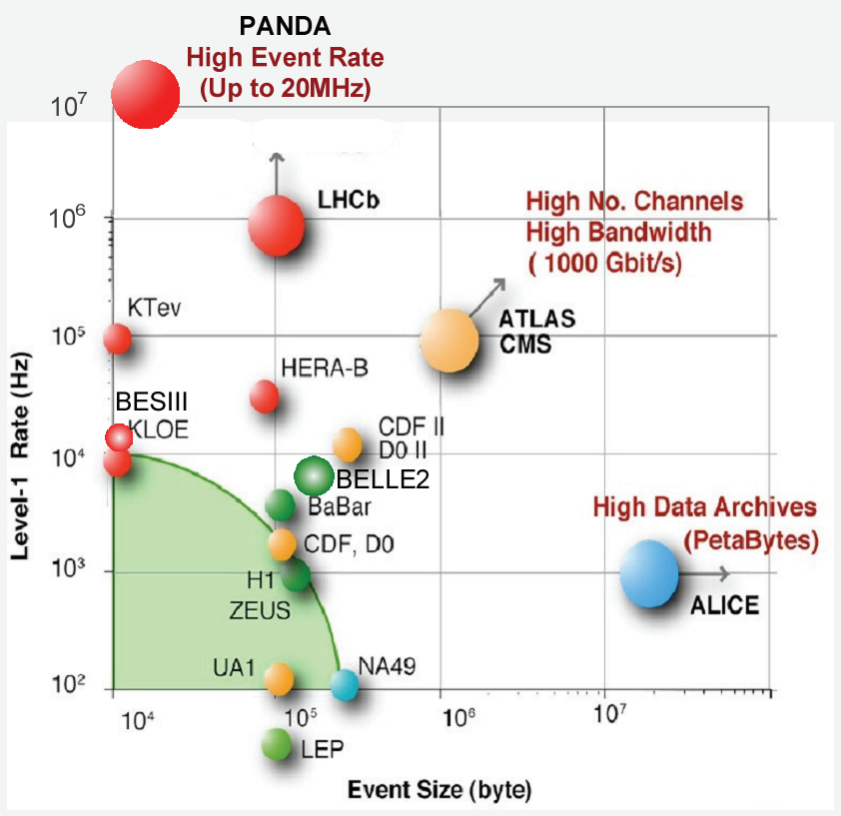
Prof. Wolfgang Kuehn
Acting Director, II. Physikalisches Institut
JLU Giessen, Germany

Date : 10.9.2010

PANDA实验之TDAQ系统

- 要求
  - 预计打靶所产生反应事例率在20MHz（预留50MHz的处理能力），通过前端电子学进行初步的噪声压低及数据筛选，事例大小在4kB到8kB（处决于最终探测器的选择），TDAQ系统需要处理的数据通量达到200GB/s;

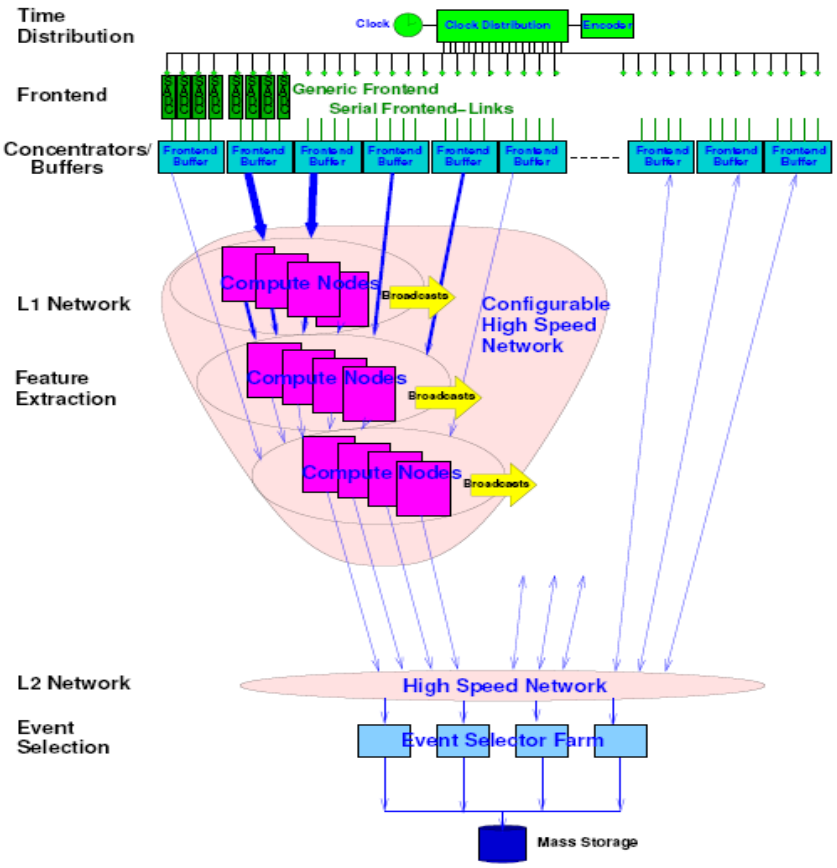
在线触发与数据获取系统需要具有高速数据传输、大数据量缓存及快速数据处理的能力(事例重建)



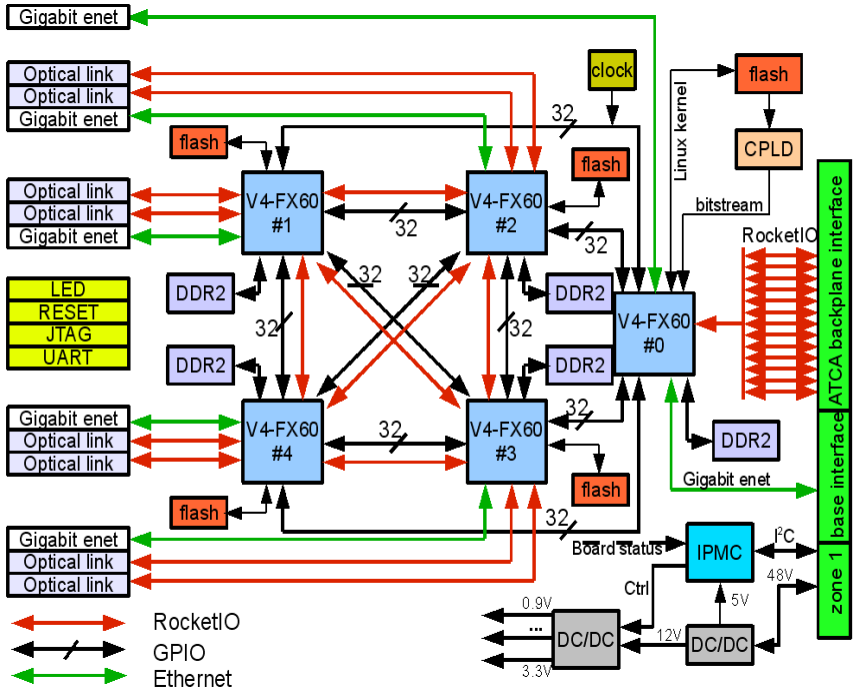
PANDA触发与数据获取系统体系结构

采用自触发前端电子学及数据推动的结构(Self-triggered Data Push Architecture)，没有独立的触发数据通路，采用打全局时间戳的办法来对齐事例，同时解除了对触发Latency的限制.

- L1:特征提取：来自前端的数据被打上精确的时间戳(Timestamp)后送入公共数据缓冲区；若干高性能的计算节点（Compute Node）通过高速串行传输技术组成可重配置的高速互联网络，采用多种特征提取手段挑选出感兴趣的物理信息；
- L2:事例重建与筛选：L1提取的物理信息在L2进行基本事例重建，通过事例筛选来压缩数据量，经过L2的数据最后存储进海量存储设备供离线数据分析；



通用硬件平台—计算节点（高能所设计）



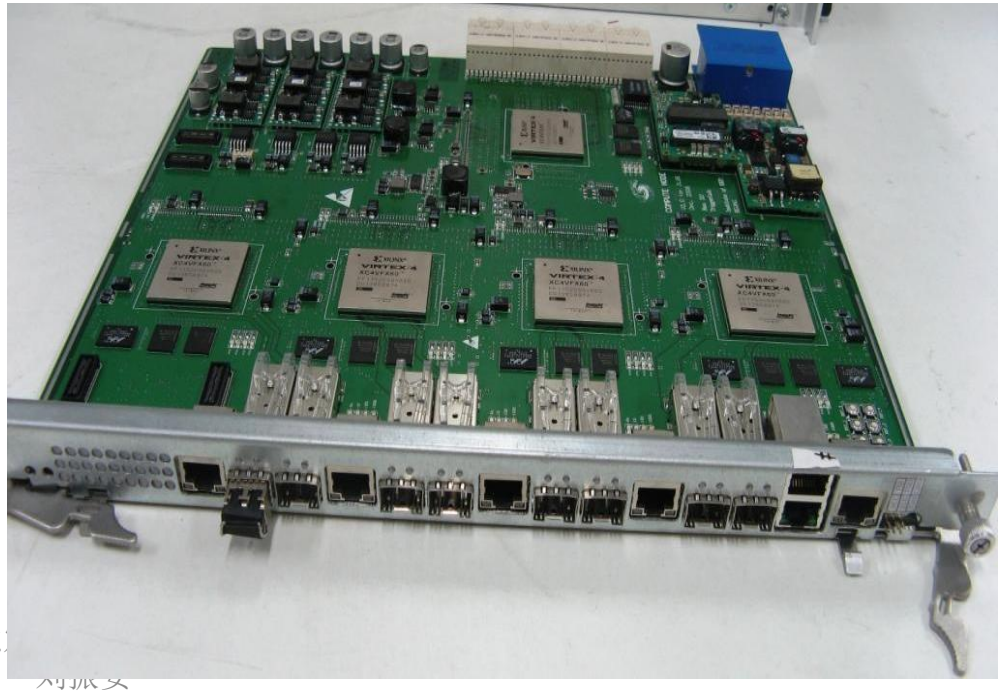
它是构成**PANDA TDAQ**系统的核心模块，具有以下特点：

大容量数据处理能力

- 5x (Virtex4 FX 60 FPGA + 2GB DDR2)

高数据传输带宽

- 6 个千兆网口(包括背板的)
- 8 个光纤口(到3.125Gbps)
- 13个RocketIOs通过背板与同机箱内的其他板进行点对点的互联



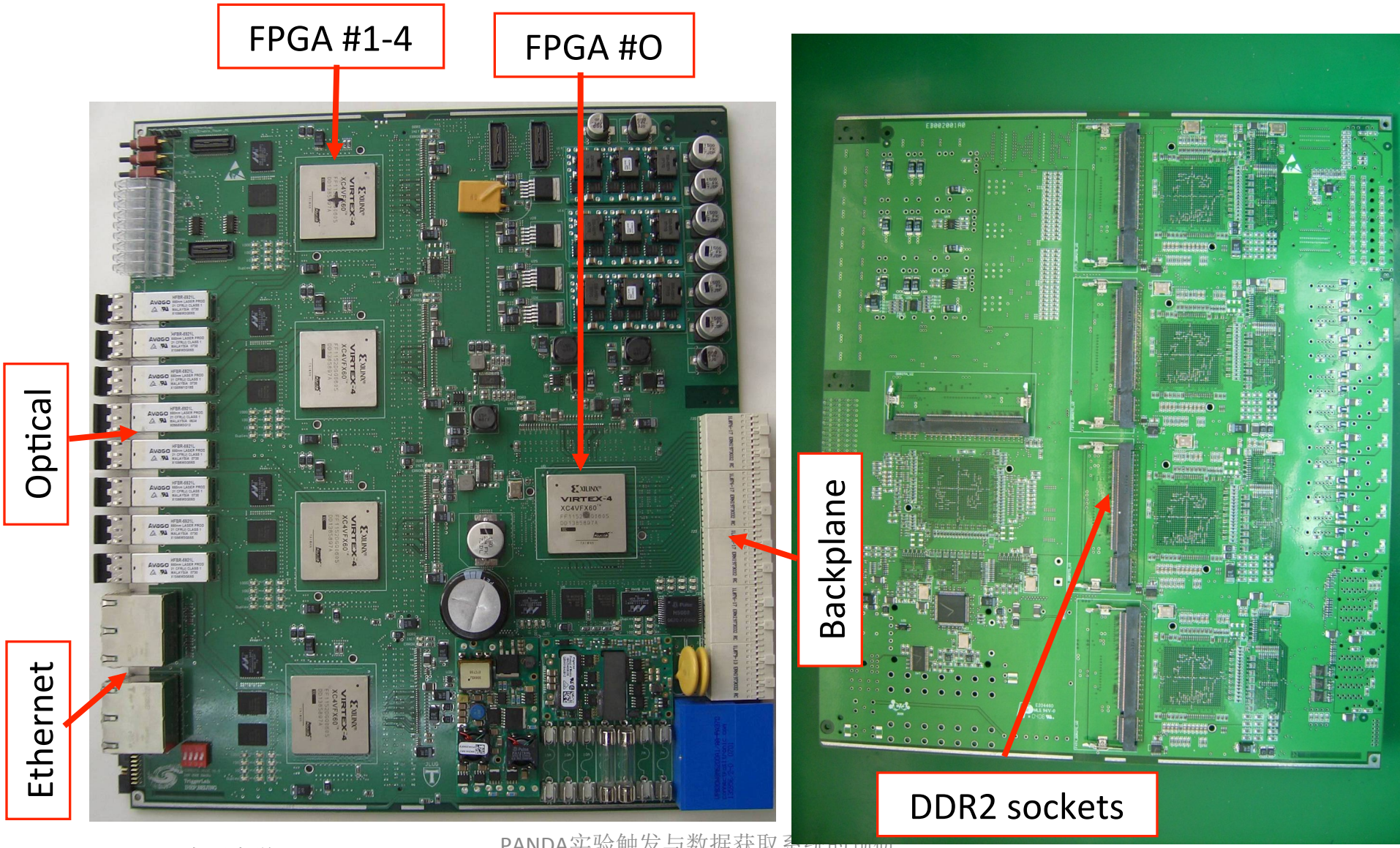
嵌入式设计方式

- 通用的系统+专用的数据处理模块

智能平台管理

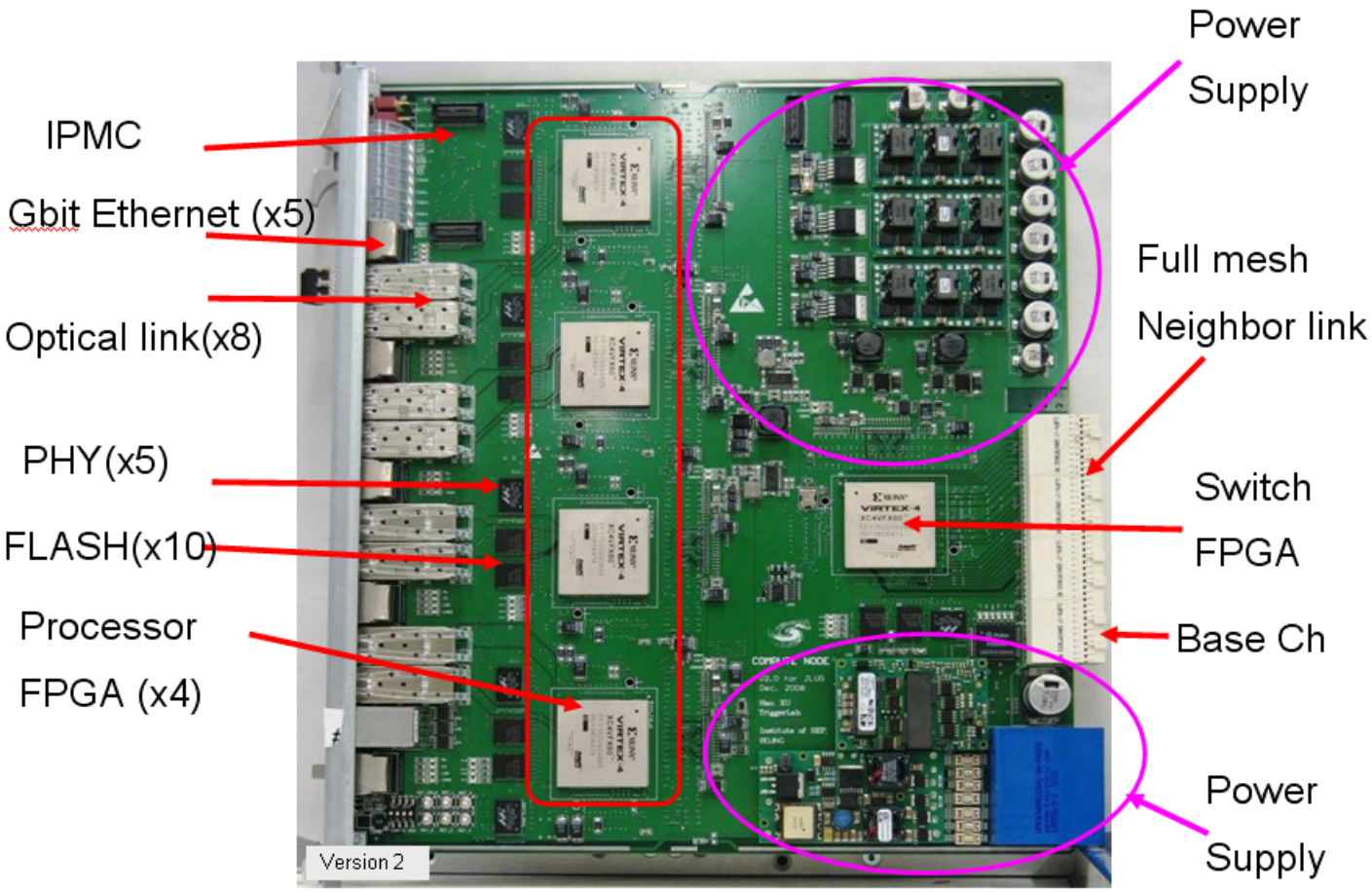
- 基于板上IPMC子板与机箱控制器的通信来实现系统监测及管理功能

第一版：固定光纤收发器

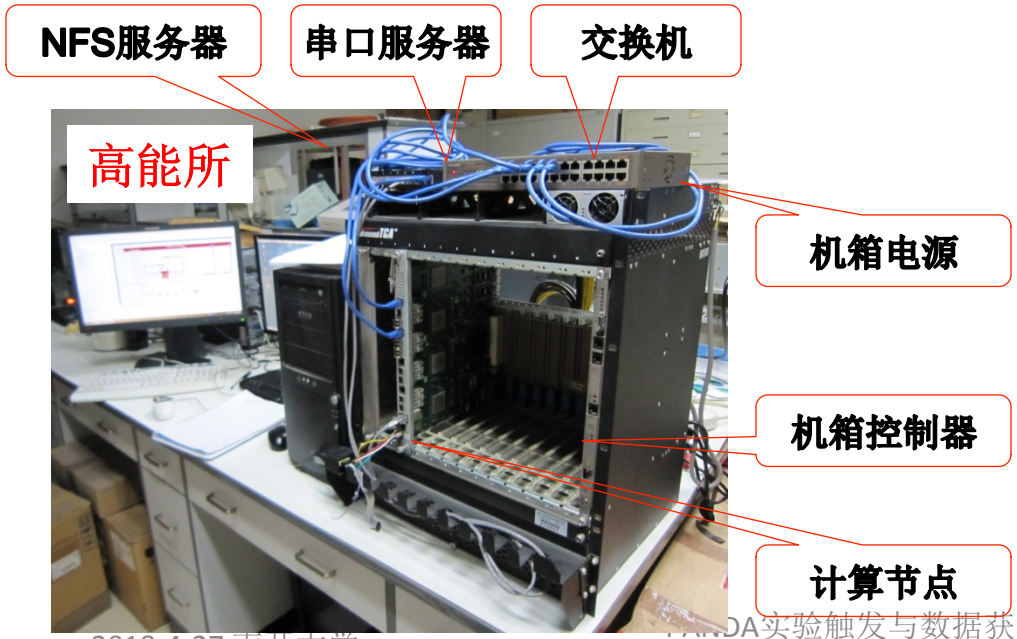


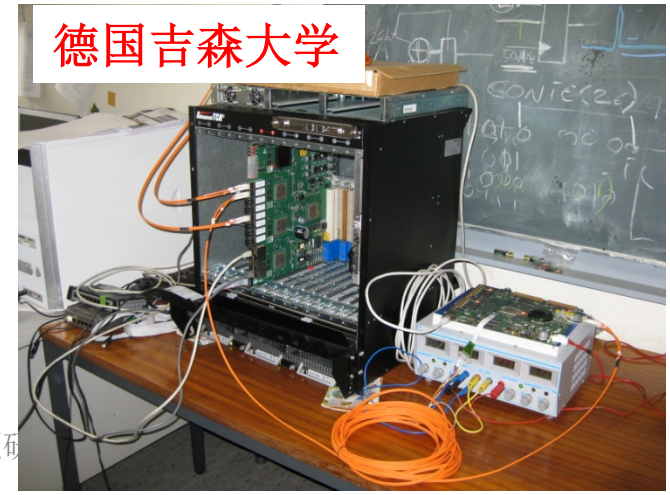
第二版：光纤收发器可插拔

- SFP pluggable
- Mono RJ45 socket
- Higher bandwidth / SFP+
- Front Pannel
- Better LEDs

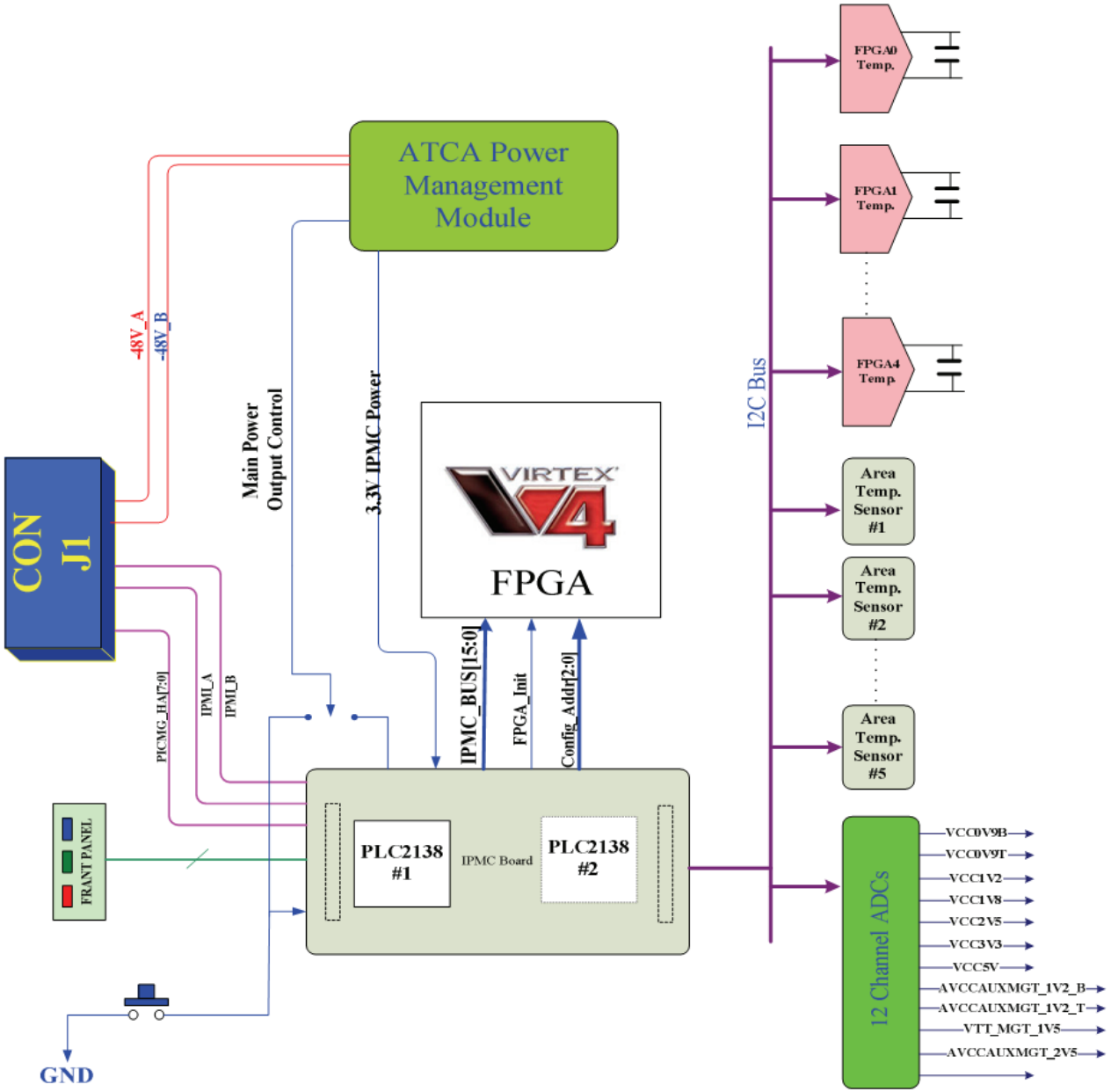


通用高性能硬件平台

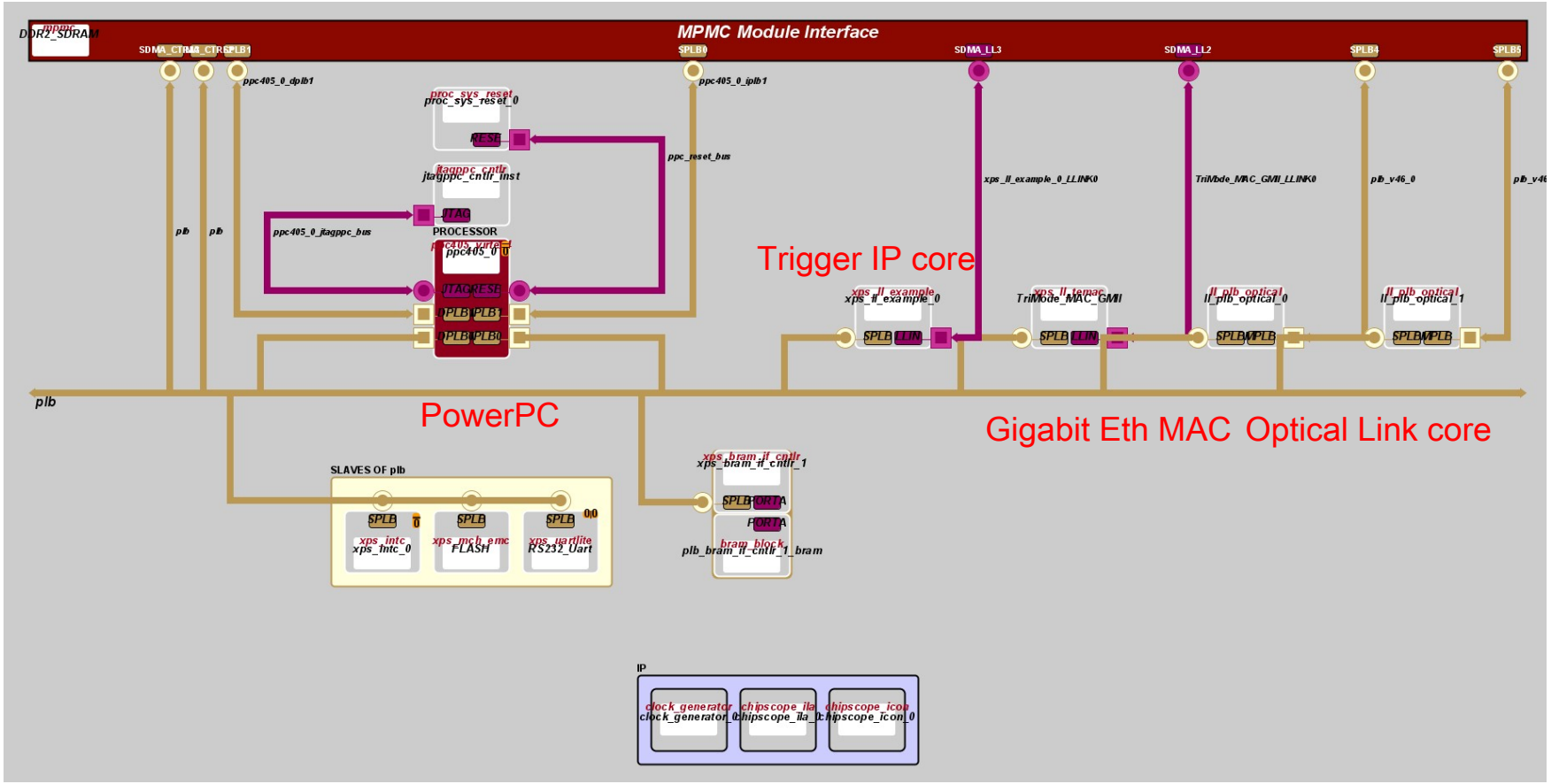




通用硬件平台—板级监测与控制管理

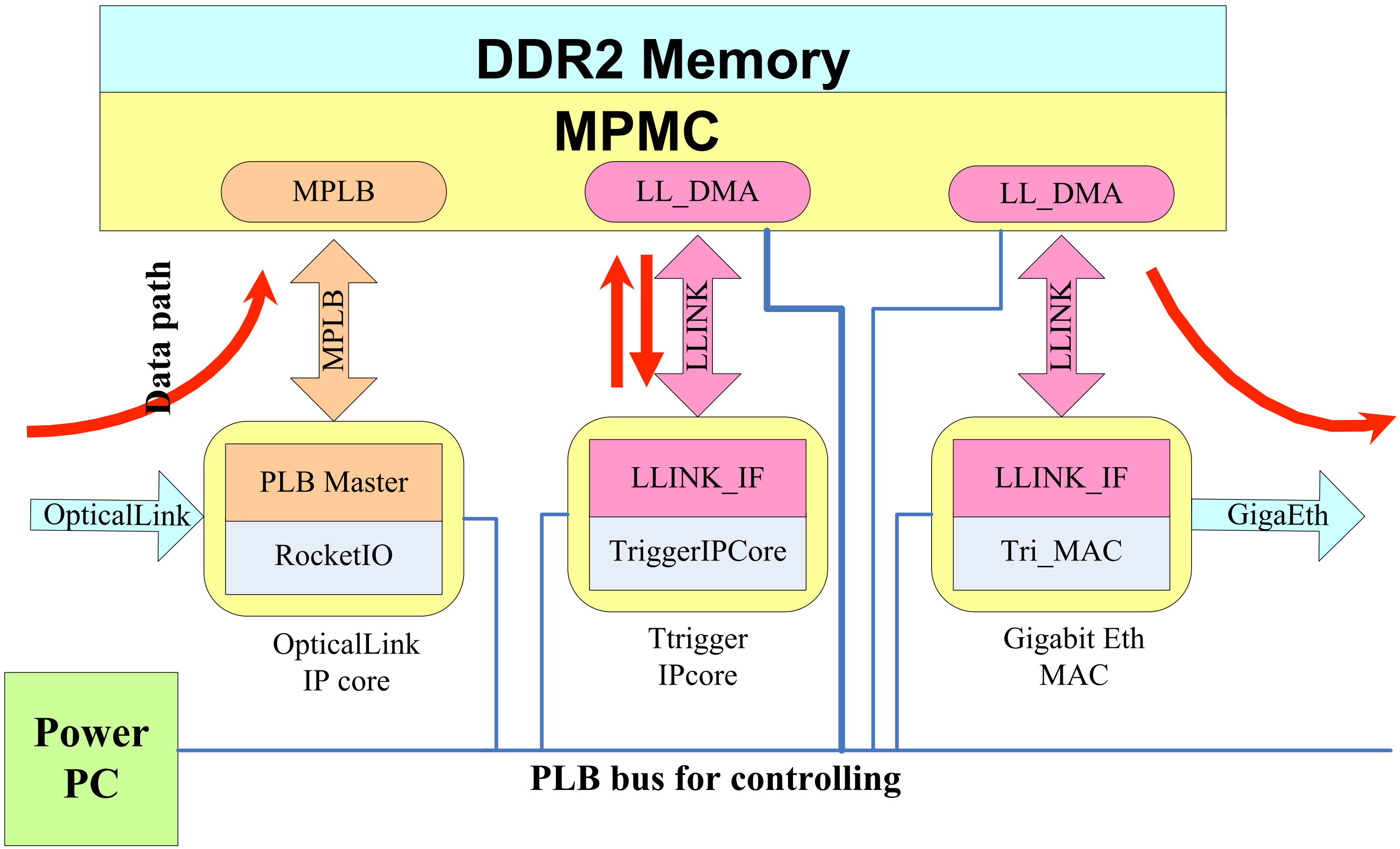


System on Programmable Chip



- 基于Xilinx FPGA内嵌的PowerPC硬核和一些开源的IP和构建一个通用的硬件系统,移植开源Linux来实现系统管理以及UDP/TCP 协议栈的处理
- 在线触发算法设计成专用IP核以及基于多端口内存控制器实现片上数据交换模块

数据流的问题



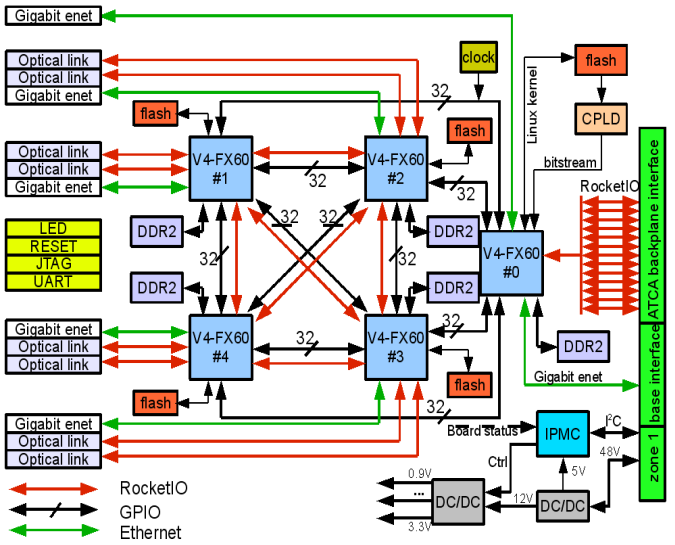
- 从高速光口接收到的粗数据在DDR2内缓存（通过PLB主设备：低延时，高带宽）
- 数据从DDR2发送到触发算法IP核以及处理结果写回DDR2（通过LocalLink DMA设备，更加灵活，高带宽）
- 结果通过Gigabit Ethernet送出（通过UDP/TCP，标准设计）

一、任务完成情况 之 PANDA触发系统

原型样机研制

成功研制2版实用计算节点原型样机，完全实现了预定的功能：

- 高数据传输带宽（6 个千兆网口，8 个光纤口（到3.125Gbps），13 个RocketIOs 板板点对点的互联）
- 大容量数据处理能力（5个V4 FPGA + 2GB DDR2)
- 嵌入式设计方式（通用的系统+专用的数据处理模块）
- 智能平台管理（基于板上IPMC子板与机箱控制器的通信来实现系统监测及管理功能）

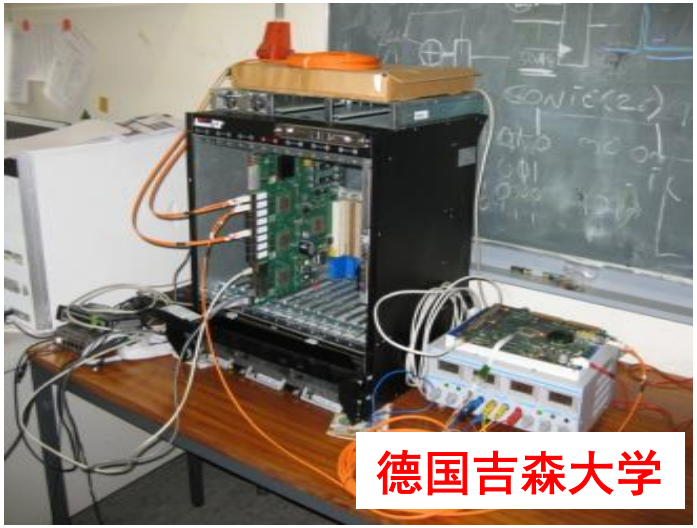


计算节点原理方框图

计算节点实物图

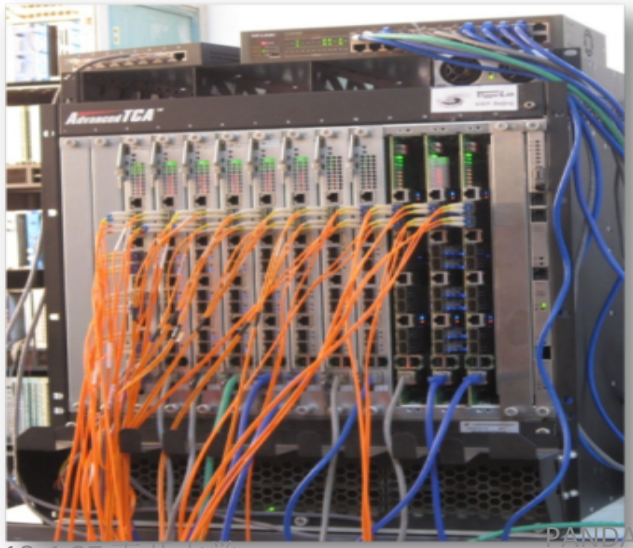
一、任务完成情况 之 PANDA触发系统

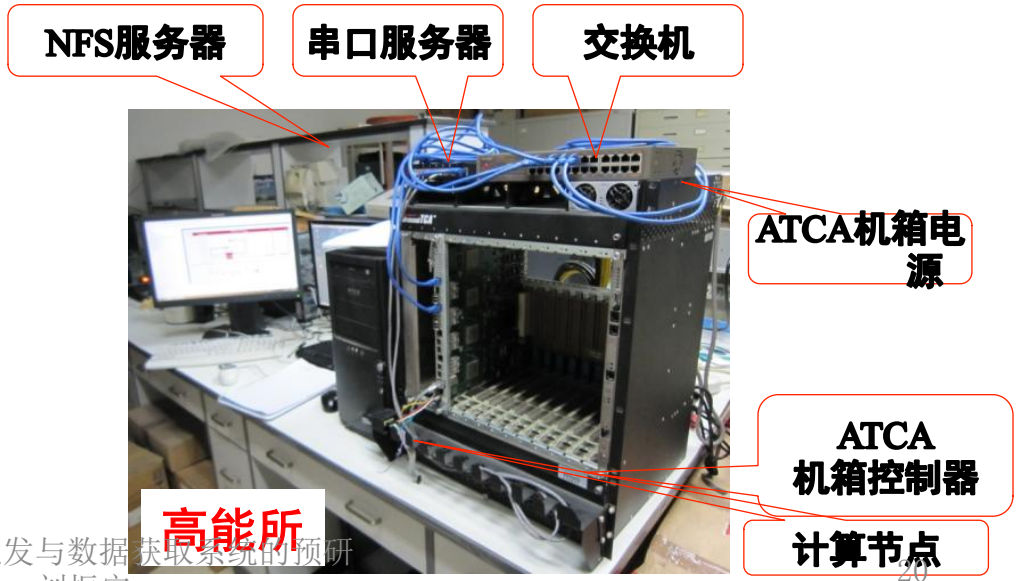
搭建了5套验证系统（高能所1套，吉森大学2套，波恩大学1套，荷兰KVI 1套），实现了PANDA EMC电磁量能器在线事例特征提取、触发与事例预选择和事例组建，开启了后续研究（xTCA相关）。



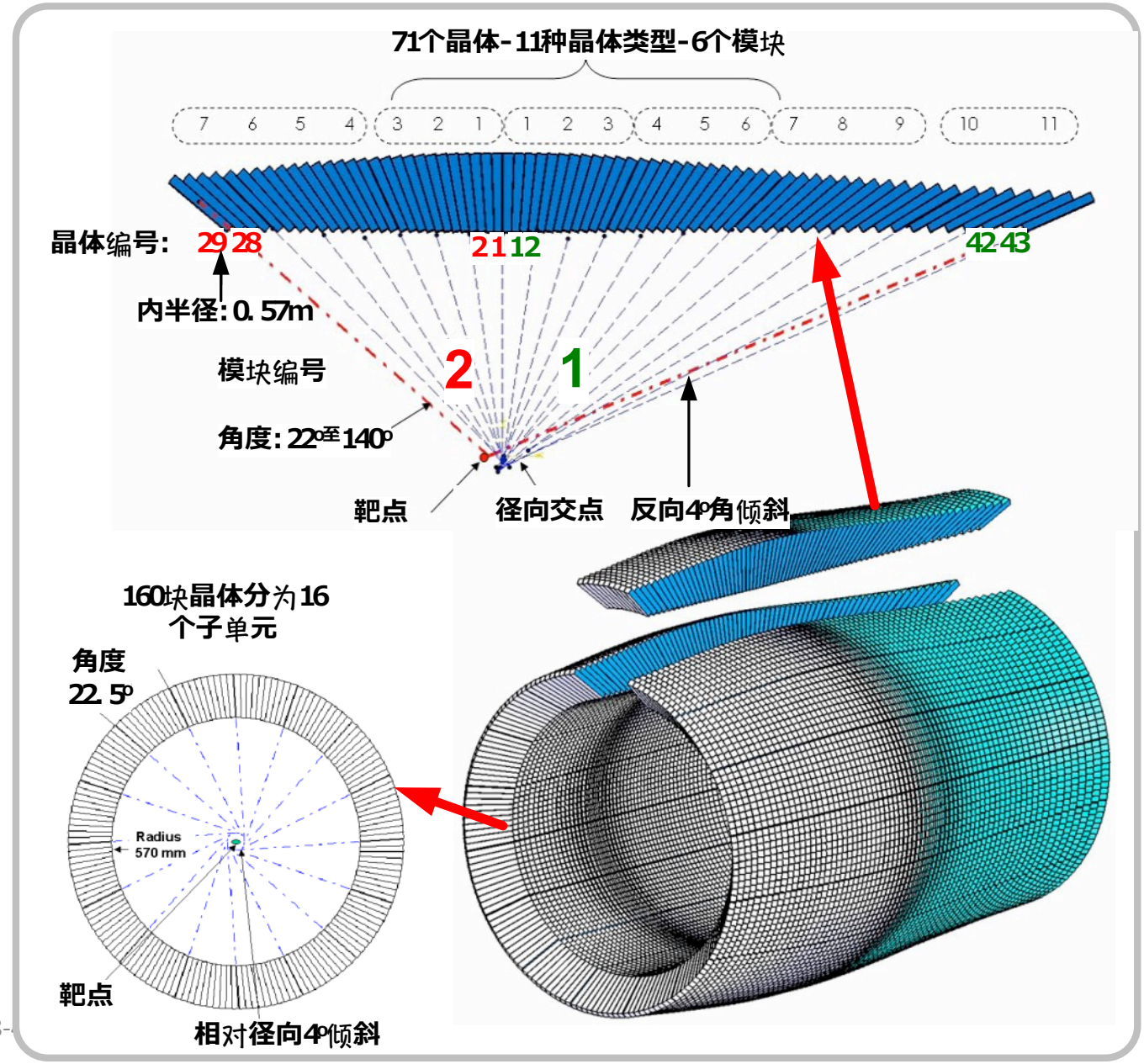
国际领先水平

25Gbps光口，5Gbps以太口，40Gbps板板互联





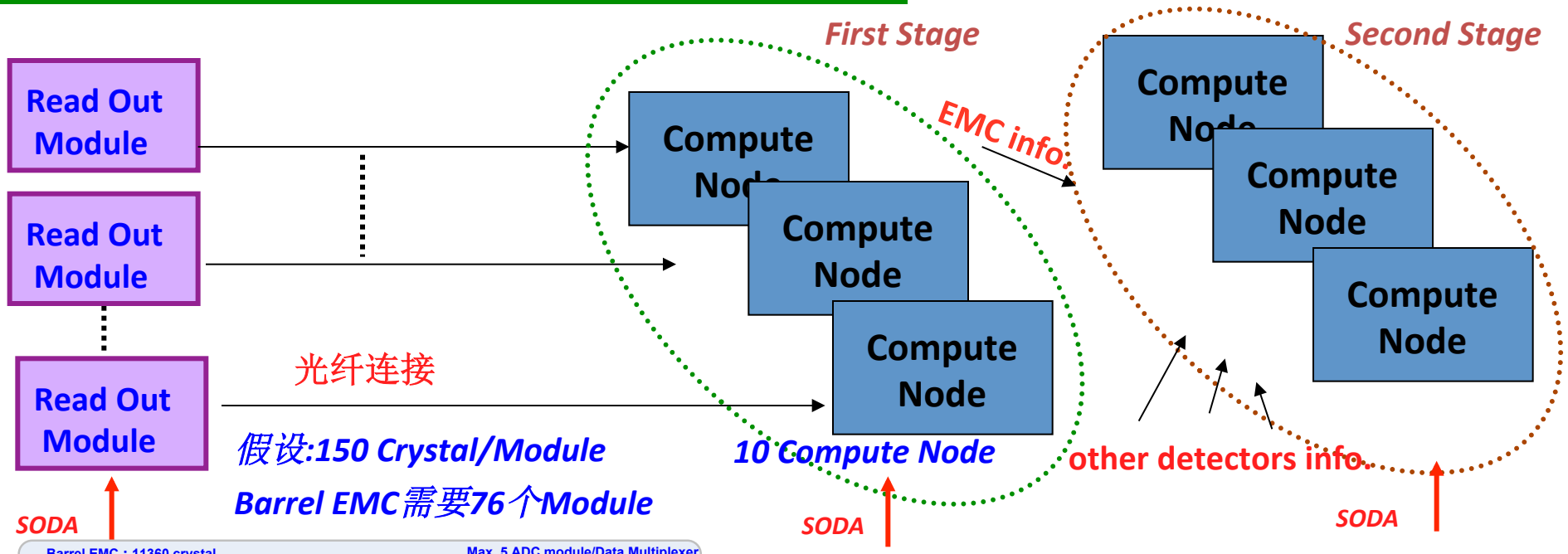
EMC探测器触发研究



Barrel EMC:

11360块晶体

EMC TDAQ系统框图



SODA: Synchronization Of Data Acquisition

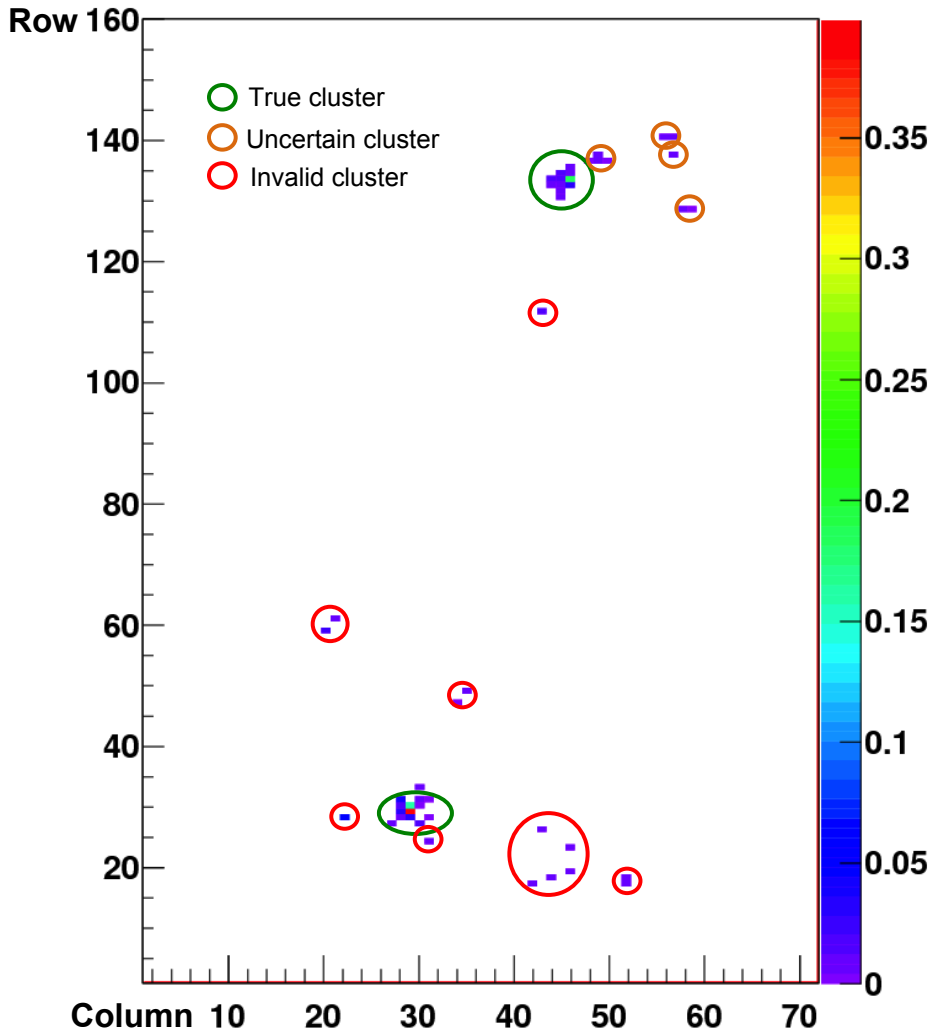
任务

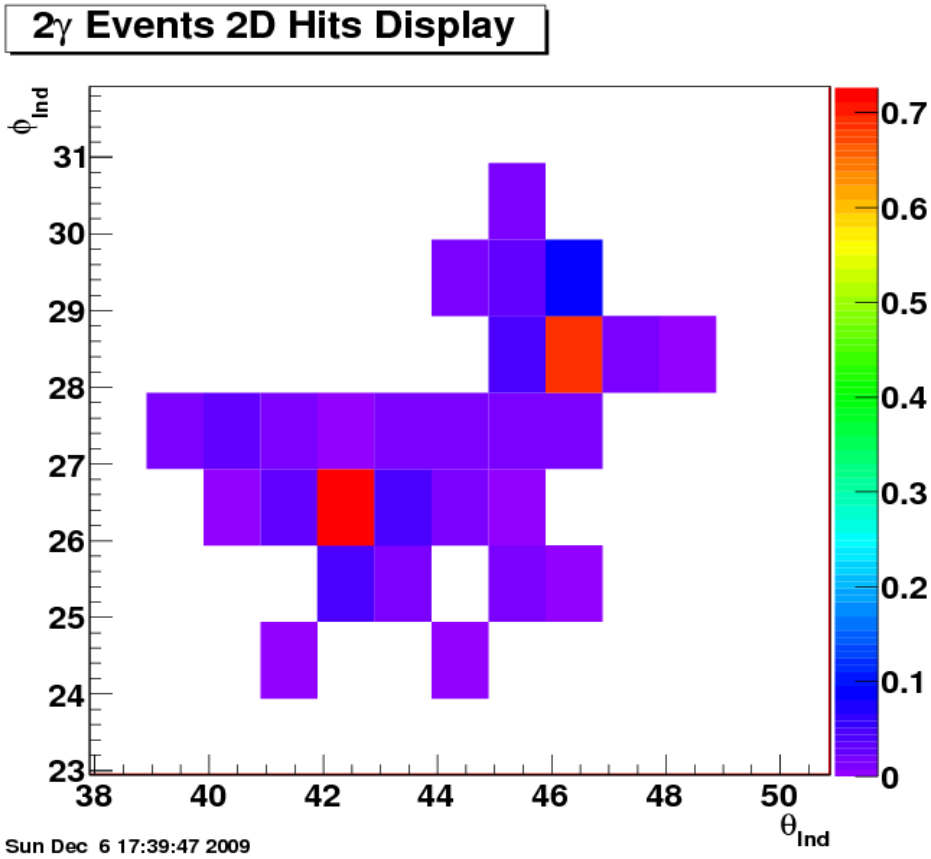
1. Signal Feature extraction (Time, Amplitude)
2. Data Zero suppression

1. Clustering
2. Cluster Properties extraction
3. Pattern recognition

1. Correlation
2. Physical parameters calculation
3. Event building

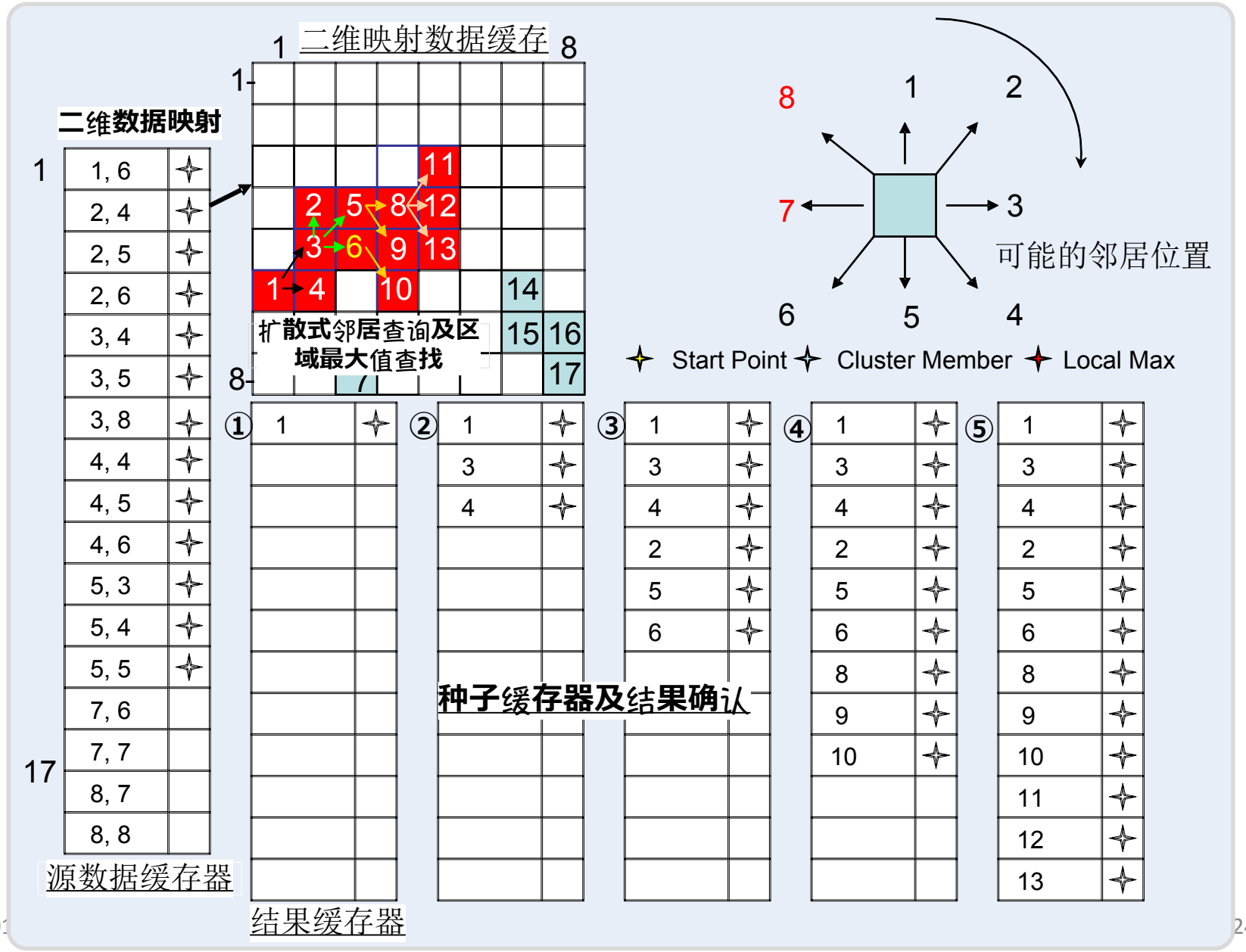
簇团重建需要解决的问题





- 簇团查找
- 重叠簇团的处理
- 重建簇团信息:能量,位置
- 在线簇团重建：速度，效率

二维簇团查找算法


二维映射数据缓存
二维数据映射
扩散式邻居查询及区域最大值查找
可能的邻居位置
Start Point
Cluster Member
Local Max
种子缓存器及结果确认
源数据缓存器
结果缓存器

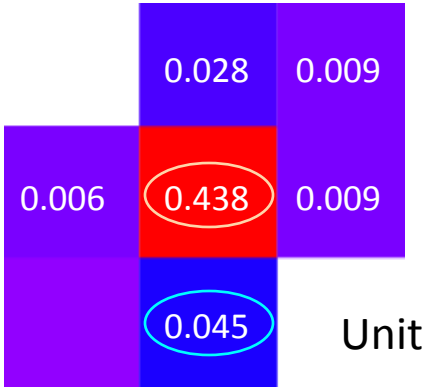
寻找区域最大值

为了避免找到假的区域最大值，需要选择更加严格的判选条件

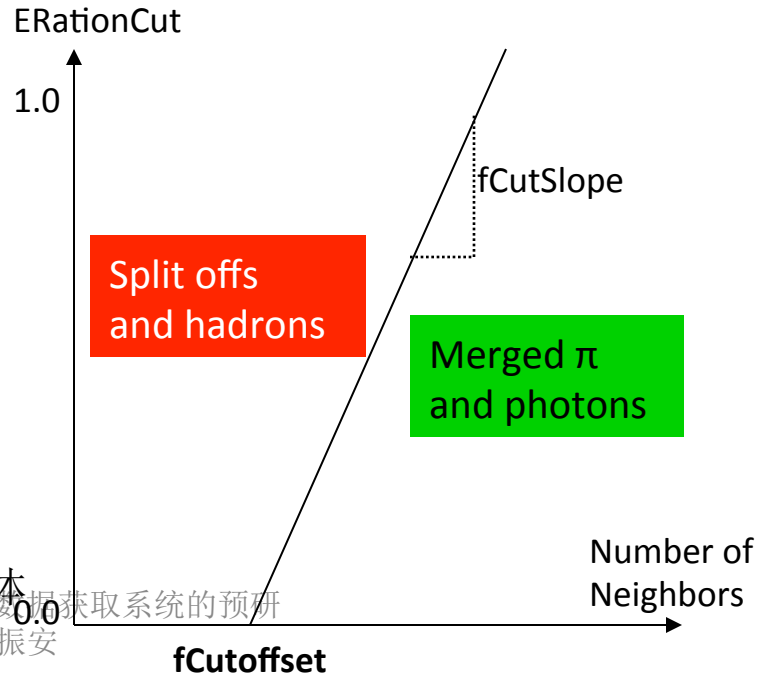
- ✓ Eseed>20MeV
- ✓ ERatio<ERatioCut

$$ERatio = \frac{MaxEofNeighbors - fERatioCorr}{MaxE - fERatioCorr}$$

$$ERatioCut = fCutSlope \times (NumberofNeighbors - fCutoffset)$$



Unit: GeV

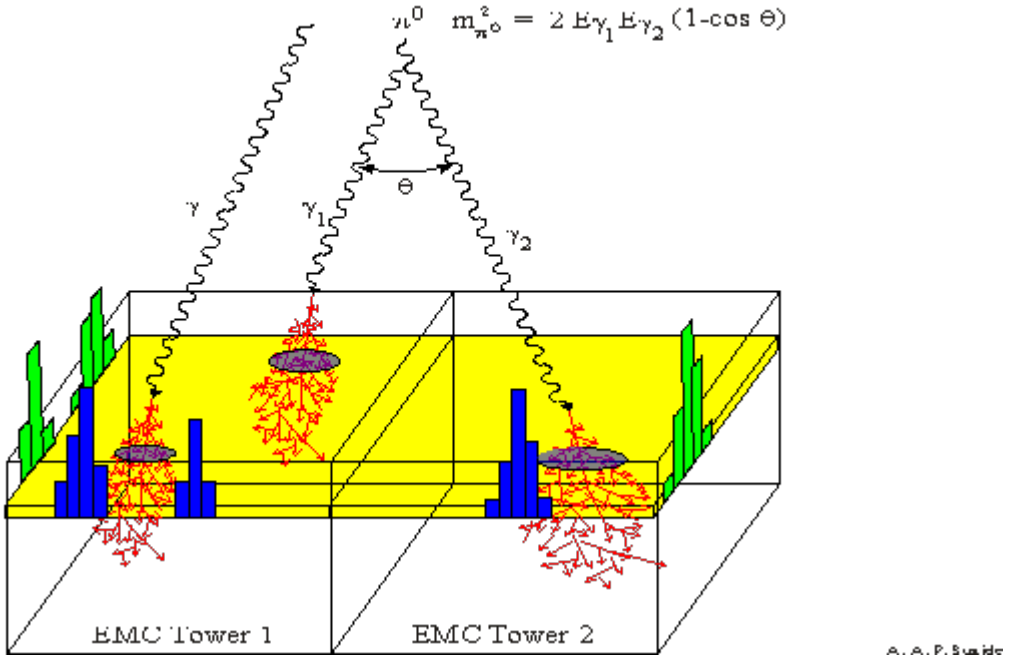


一个模拟的簇团有一个区域最大值以及6个相邻晶体

簇团位置计算

- 带电粒子必须提供簇团位置来与径迹探测器做匹配；
- 光子位置重建准确性对 π_0 质量的重建影响特别大；

EMC π^0 reconstruction



$$Wi = Ei$$

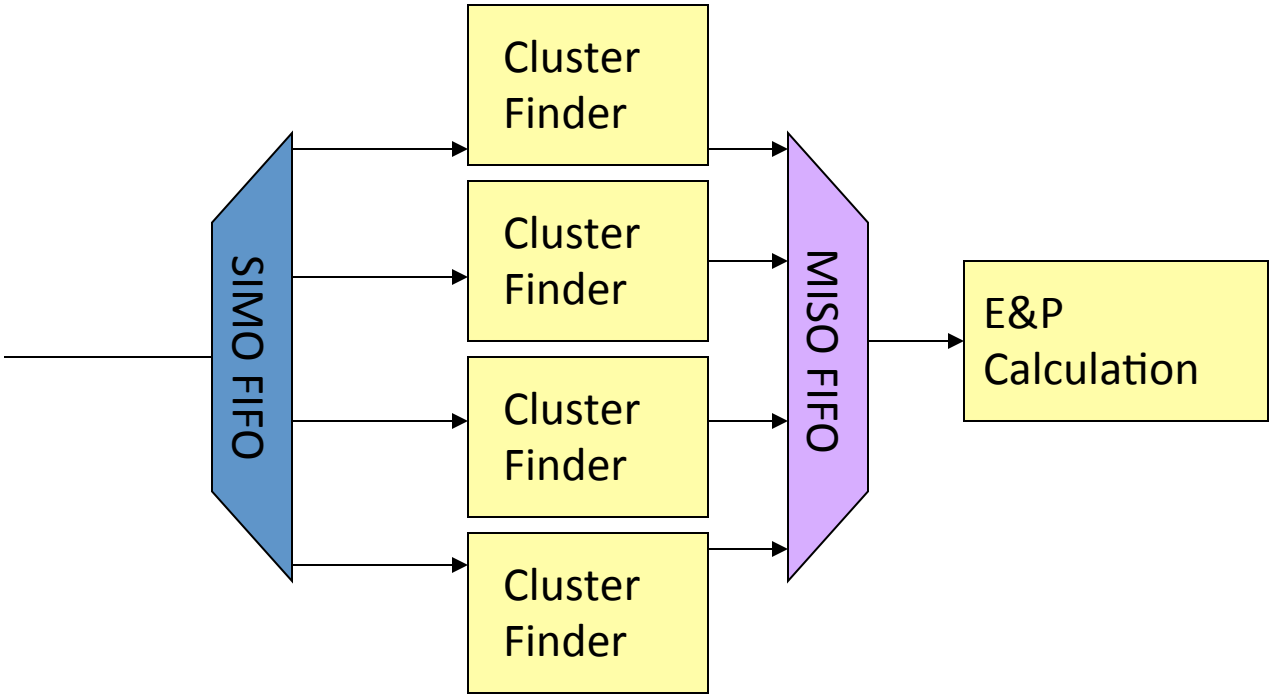
权重

$$Xcal = \frac{\sum_i Wi * Xi}{\sum_i Wi}$$

线性权重位置计算

适合V4Fx60 FPGA的设计

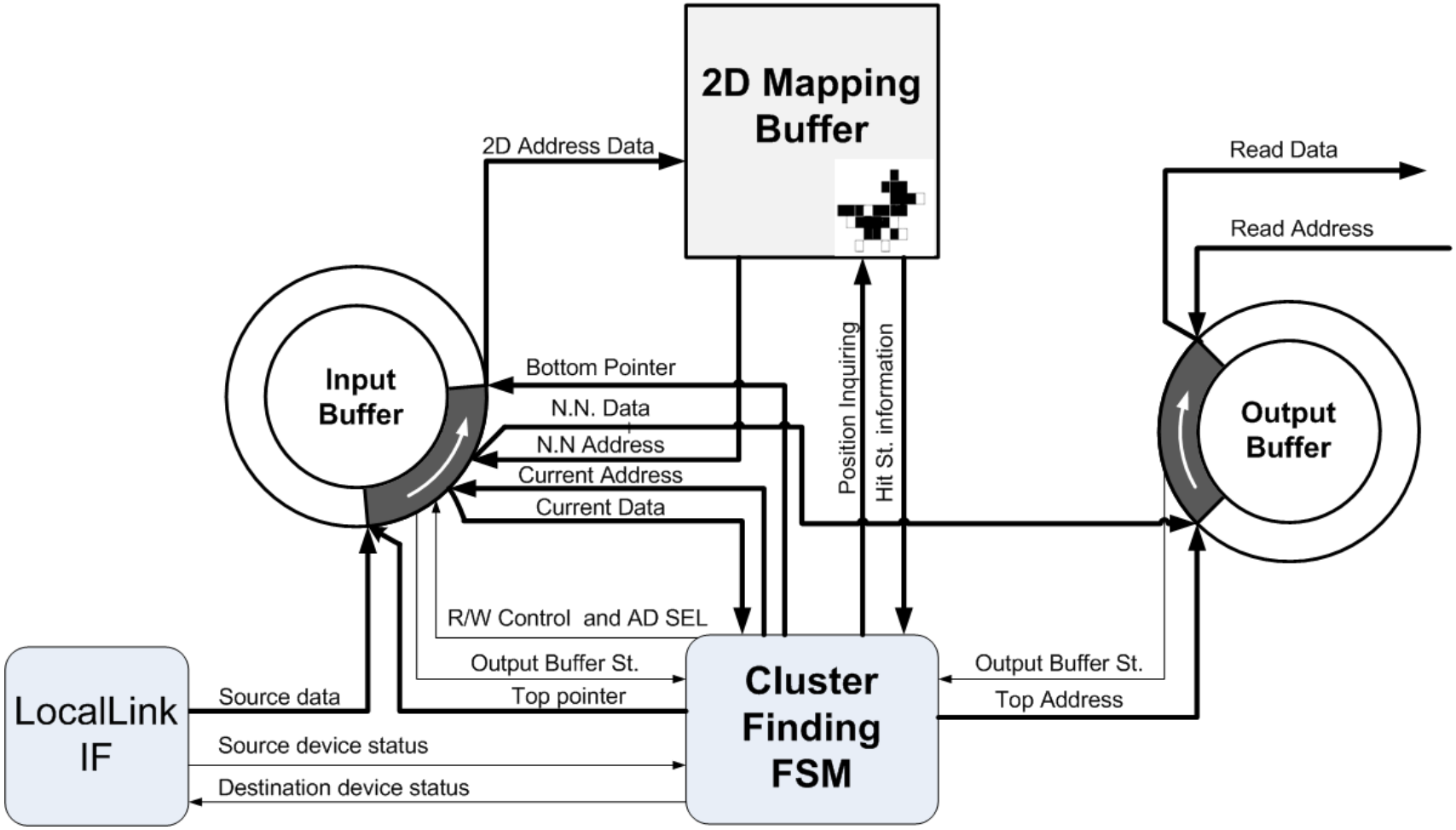
- 能量/位置计算模块速度较快，能完全流水线运行
- 从资源使用量上看，这是最优的配置



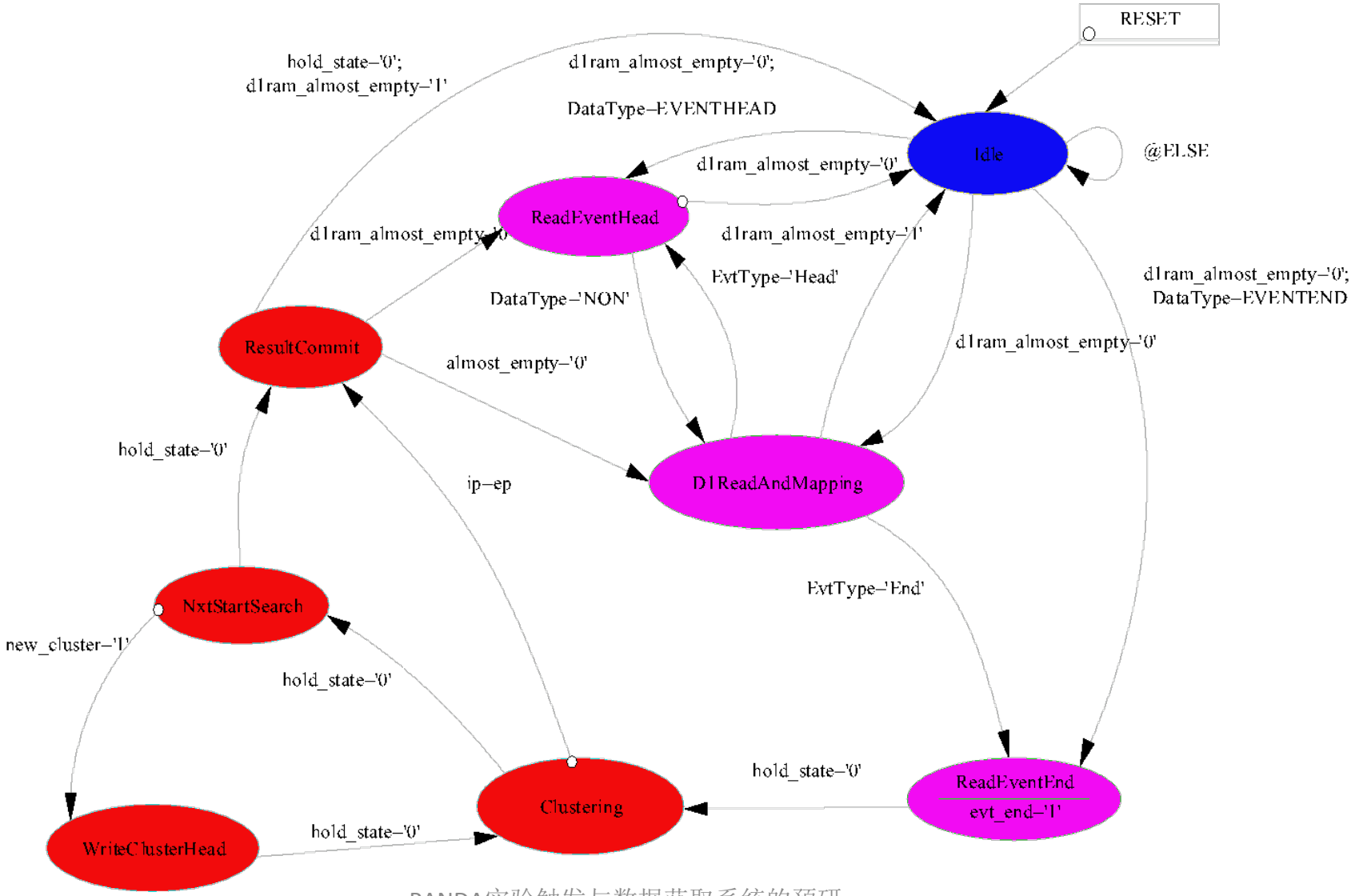
- 4 Cluster Finder + 1 Energy and Position Calculation

400KHz Events/FPGA=>1.6MHz/CN

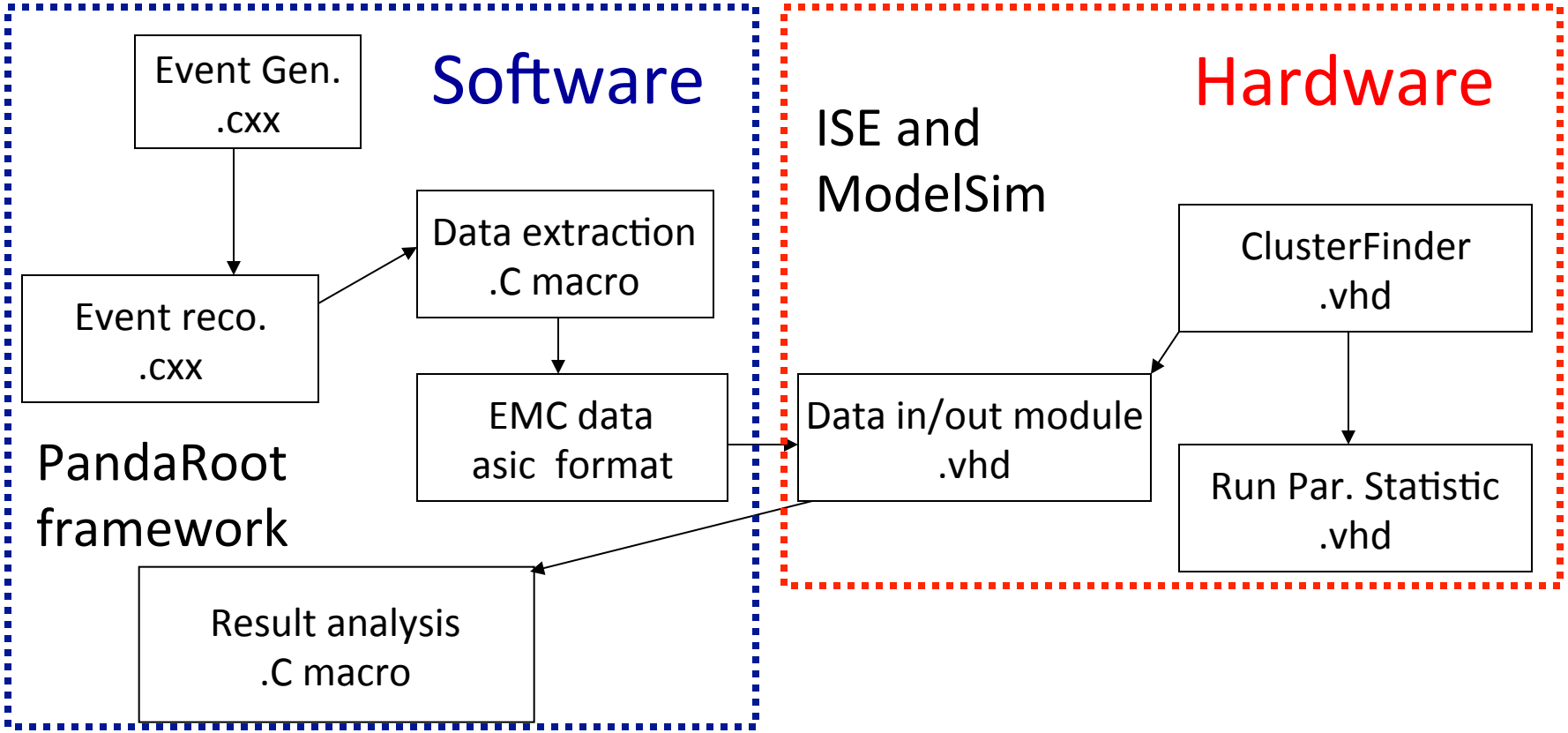
Cluster Finder 模块框图



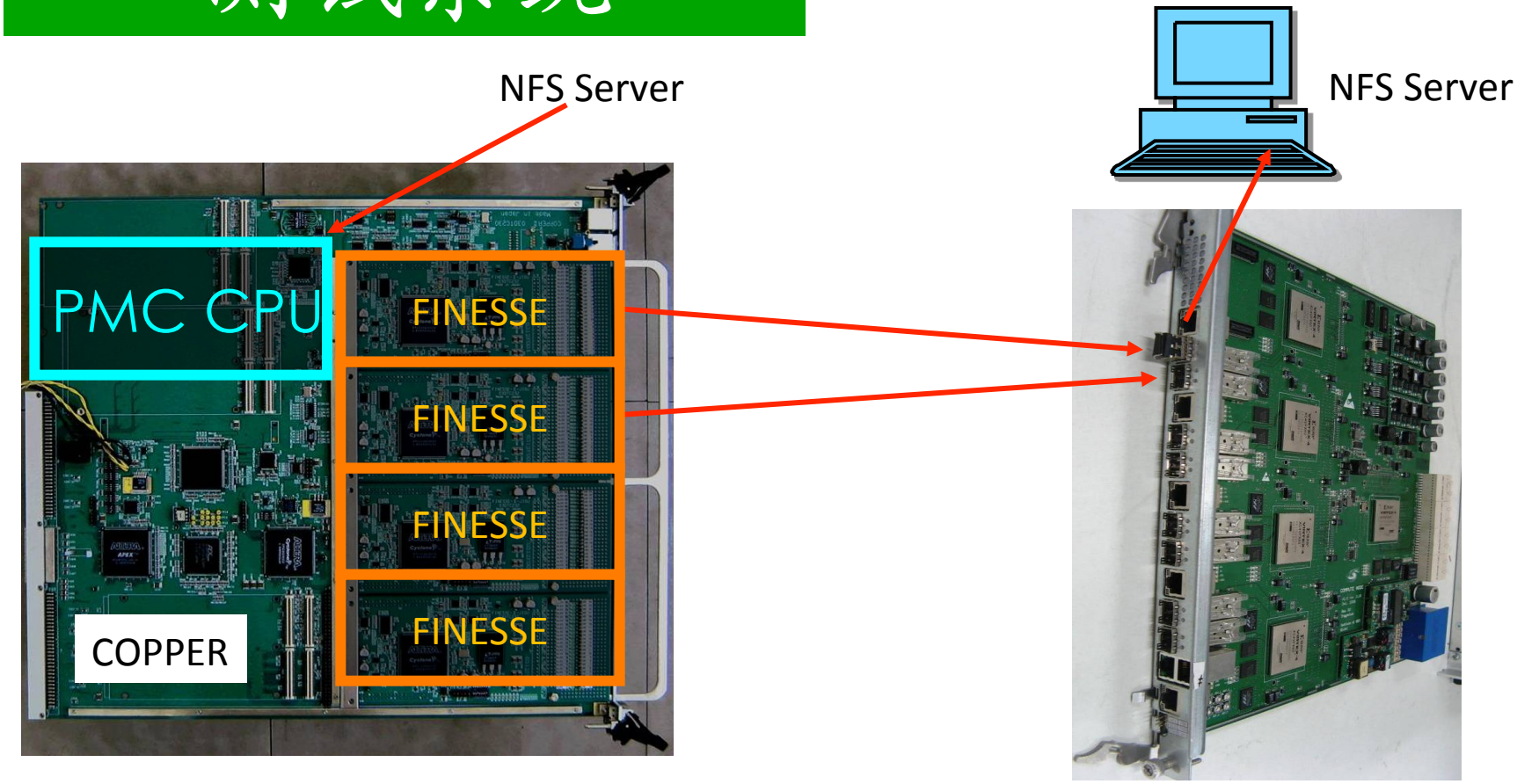
簇团查找有限状态机

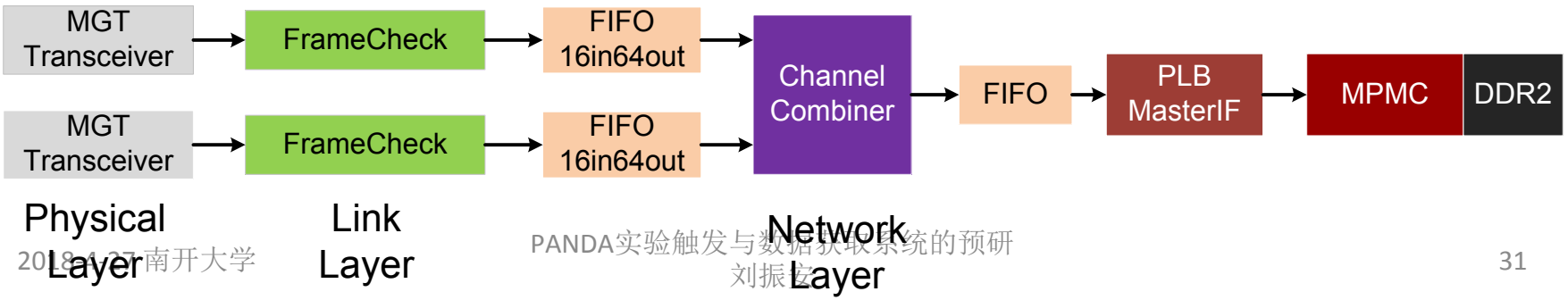

RESET
Idle
@ELSE
hold_state='0';
dlram_almost_empty='1'
dlram_almost_empty='0';
DataType=EVENTHEAD
dlram_almost_empty='0'
ReadEventHead
dlram_almost_empty='0'
dlram_almost_empty='1'
EvtType='Head'
DataType='NON'
dlram_almost_empty='0';
DataType=EVENTEND
ResultCommit
almost_empty='0'
dlram_almost_empty='0'
hold_state='0'
ip=ep
DlReadAndMapping
EvtType='End'
NxtStartSearch
new_cluster='1'
hold_state='0'
hold_state='0'
ReadEventEnd
evt_end='1'
Clustering
WriteClusterHead
hold_state='0'

逻辑验证方法

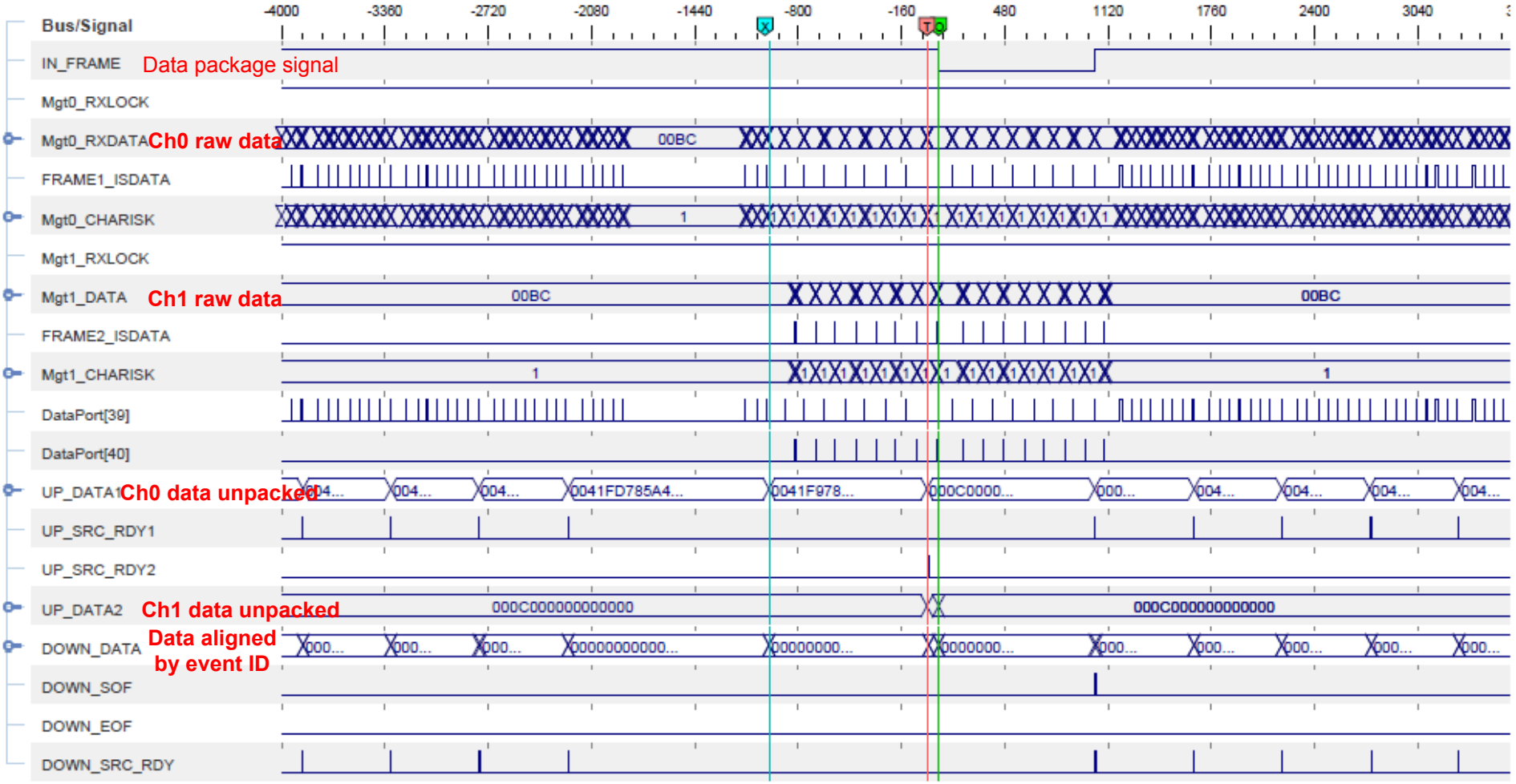

Event Gen.
.cxx
Software
Hardware
ISE and
ModelSim
Data extraction
.C macro
ClusterFinder
.vhd
Event reco.
.cxx
EMC data
asic format
Data in/out module
.vhd
PandaRoot
framework
Run Par. Statistic
.vhd
Result analysis
.C macro

测试系统


NFS Server
NFS Server
PMC CPU
FINESSE
FINESSE
FINESSE
FINESSE
COPPER


MGT Transceiver
MGT Transceiver
FrameCheck
FrameCheck
FIFO 16in64out
FIFO 16in64out
Channel Combiner
FIFO
PLB MasterIF
MPMC
DDR2
Physical Layer
Link Layer
Network Layer

Chipscope 截图



文件传输测试

```
####################################################
##                                                ##
##      Compute Node Ver2 Application Programs    ##
##  OpticalLink Received Data Through DDR2 Memory ##
##                                                ##
####################################################
-- Entering main() --
XIntc init successful
XIntc start successful
intr controller enabled
ll_plb_optical intr enabled in the intr controller
Reg0 is: 2000000 Reg1 is: 4000000

The 0 th Daq Run
Data transmission finished
CLK cycles needed for 1024 KByte Data Transmission: 1300889748 Cyc, Transmit Speed: 236 KByte/s
Received Data Checking ......
|A:2000000|D:00000000|A:2000004|D:00000000|A:2000008|D:00080030|A:200000C|D:00000000|A:2000010|D:0041FD60|A:2000014|D:634FB3B0|
|A:2000018|D:0041F960|A:200001C|D:634FEDB0|A:2000020|D:0041FD68|A:2000024|D:604FCAD8|A:2000028|D:0041F968|A:200002C|D:607FE370|
|A:2000030|D:0041F568|A:2000034|D:604DC400|A:2000038|D:0041F168|A:200003C|D:604DD0D8|A:2000040|D:00420170|A:2000044|D:5D50D6D8|
|A:2000048|D:0041FD70|A:200004C|D:5D4FD2F0|A:2000050|D:0041F970|A:2000054|D:5D4FC0F0|A:2000058|D:0041F570|A:200005C|D:5D4DF400|
|A:2000060|D:0041FD78|A:2000064|D:5A4FDD28|A:2000068|D:0041F978|A:200006C|D:5A4FCCA0|A:2000070|D:000C0000|A:2000074|D:00000000|
|A:2000078|D:0008043C|A:200007C|D:00000000|A:2000080|D:0041D8F0|A:2000084|D:9546CCA0|A:2000088|D:0041D8F8|A:200008C|D:9146EFC8|
|A:2000090|D:0041D4F8|A:2000094|D:9145D2F0|A:2000098|D:0041E100|A:200009C|D:8D48CCA0|A:20000A0|D:0041D900|A:20000A4|D:8D47C050|
|A:20000A8|D:0041D500|A:20000AC|D:8D47CEC0|A:20000B0|D:0041D100|A:20000B4|D:8D45E9C8|A:20000B8|D:0041CD00|A:20000BC|D:8D43CCA0|
|A:20000C0|D:0041E108|A:20000C4|D:8948CCA0|A:20000C8|D:0041DD08|A:20000CC|D:8947E378|A:20000D0|D:0041D908|A:20000D4|D:895FE150|
|A:20000D8|D:0041D508|A:20000DC|D:896FFBF8|A:20000E0|D:0041D910|A:20000E4|D:8646FA00|A:20000E8|D:0041D510|A:20000EC|D:8645D6D8|
|A:20000F0|D:00202010|A:20000F4|D:F4788CA0|A:20000F8|D:000C0000|A:20000FC|D:00000000|A:2000100|D:00080838|A:2000104|D:00000000|
|A:2000108|D:0041E0F0|A:200010C|D:954ADD78|A:2000110|D:0041DCF0|A:2000114|D:956FEEB8|A:2000118|D:0041D8F0|A:200011C|D:9546E8A0|
|A:2000120|D:0041E4F0|A:2000124|D:9549C050|A:2000128|D:0041E0F8|A:200012C|D:9148EFC8|A:2000130|D:0041DCF8|A:2000134|D:9147C488|
|A:2000138|D:0041D8F8|A:200013C|D:9147D730|A:2000140|D:0041D4F8|A:2000144|D:9145FDE8|A:2000148|D:0041F4F8|A:200014C|D:914DCCA0|
|A:2000150|D:0041E100|A:2000154|D:8D48EFC8|A:2000158|D:0041E0E8|A:200015C|D:9948EFC8|A:2000160|D:0041DCE8|A:2000164|D:9957DDA0|
|A:2000168|D:0041E0E0|A:200016C|D:9D48D6D8|A:2000170|D:0041DCE0|A:2000174|D:9D47D6D8|A:2000178|D:000C0000|A:200017C|D:00000000|
|A:2000180|D:00080C34|A:2000184|D:00000000|A:2000188|D:004154D0|A:200018C|D:A426AFC8|A:2000190|D:004150C8|A:2000194|D:A827E160|
|A:2000198|D:00414CC8|A:200019C|D:A824FA00|A:20001A0|D:004154C0|A:20001A4|D:AC26FA00|A:20001A8|D:004150C0|A:20001AC|D:AC759458|
|A:20001B0|D:00414CC0|A:20001B4|D:AC2EBA18|A:20001B8|D:004148C0|A:20001BC|D:AC2386A0|A:20001C0|D:004154B8|A:20001C4|D:B027C748|
|A:20001C8|D:004150B8|A:20001CC|D:B025FCC0|A:20001D0|D:00414CB8|A:20001D4|D:B0269340|A:20001D8|D:004148B8|A:20001DC|D:B023D0D8|
|A:20001E0|D:004154B0|A:20001E4|D:B427E378|A:20001E8|D:004150A8|A:20001EC|D:B8258CA0|A:20001F0|D:000C0000|A:20001F4|D:00000000|
|A:20001F8|D:0008103C|A:20001FC|D:00000000|A:2000200|D:002044F0|A:2000204|D:9580F3B0|A:2000208|D:002040F0|A:200020C|D:957FDD28|
|A:2000210|D:00203CF0|A:2000214|D:957FC4D8|A:2000218|D:002048F8|A:200021C|D:9181E378|A:2000220|D:002044F8|A:2000224|D:9182FE38|
|A:2000228|D:002040F8|A:200022C|D:91FFE598|A:2000230|D:00203CF8|A:2000234|D:917FE378|A:2000238|D:002034F8|A:200023C|D:917CDAC0|
|A:2000240|D:00204900|A:2000244|D:8D81E760|A:2000248|D:00204500|A:200024C|D:8D80FA00|A:2000250|D:00204100|A:2000254|D:8D7FCAD8|
|A:2000258|D:00203D00|A:200025C|D:8D7ECB28|A:2000260|D:00203900|A:2000264|D:8D7DCCA0|A:2000268|D:00204508|A:200026C|D:8980CCA0|
|A:2000270|D:00204108|A:2000274|D:897FD6D8|A:2000278|D:000C0000|A:200027C|D:00000000|A:2000280|D:00081450|A:2000284|D:00000000|
|A:2000288|D:00427D18|A:200028C|D:826F8CA0|A:2000290|D:00427518|A:2000294|D:826D8CA0|A:2000298|D:00427920|A:200029C|D:7E6EAFC8|
|A:20002A0|D:00427528|A:20002A4|D:7B6DCCF0|A:20002A8|D:00427128|A:20002AC|D:7B6CD2F0|A:20002B0|D:00426D28|A:20002B4|D:7B6B5728|
|A:20002B8|D:00426928|A:20002BC|D:7B6AF3B0|A:20002C0|D:00427530|A:20002C4|D:776DFA00|A:20002C8|D:00427130|A:20002CC|D:777CA908|
|A:20002D0|D:00426D30|A:20002D4|D:776B4CA8|A:20002D8|D:00426530|A:20002DC|D:776BDDC8|A:20002E0|D:00427938|A:20002E4|D:746EAFC8|
```

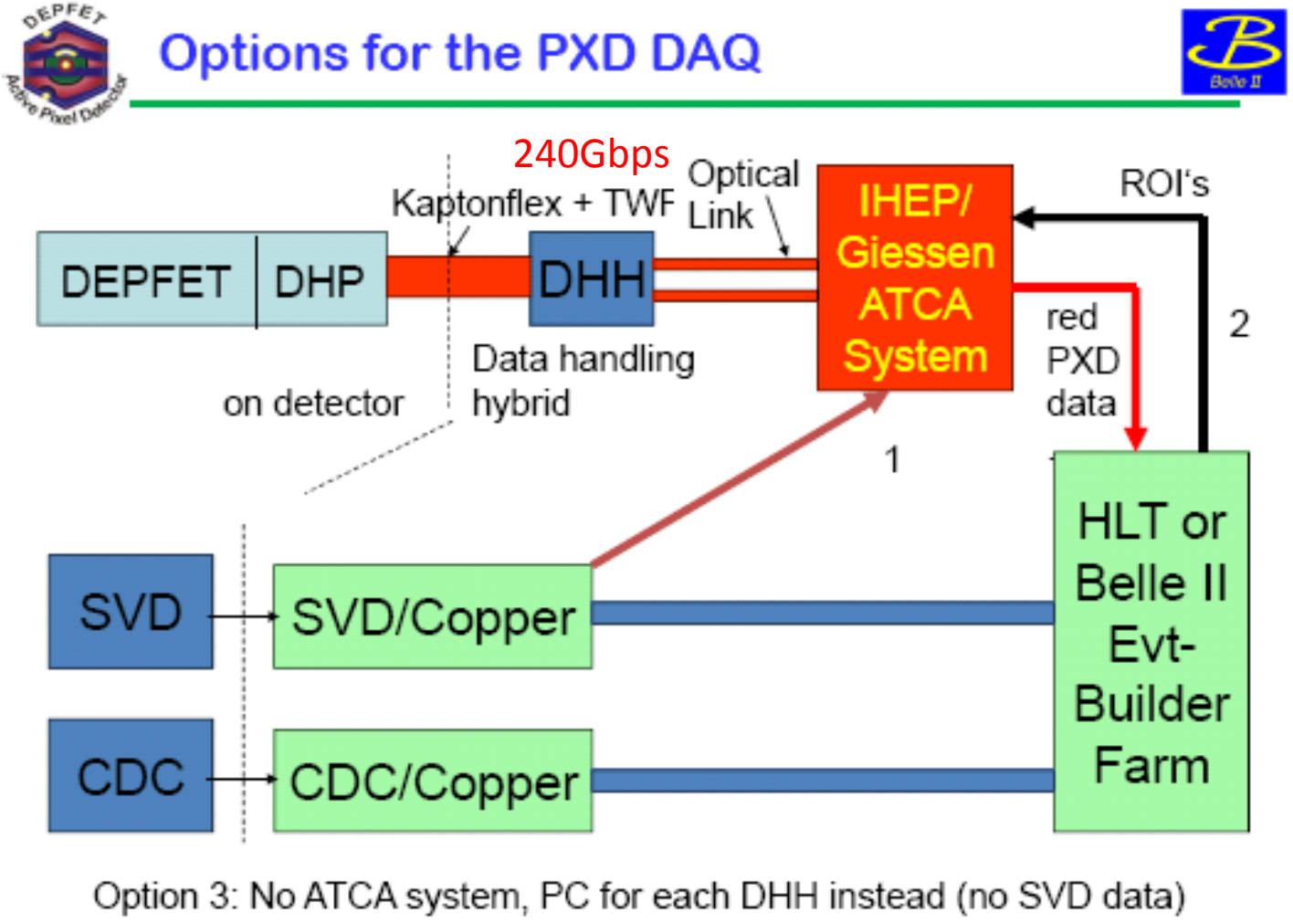
Event head

Event data

Event end

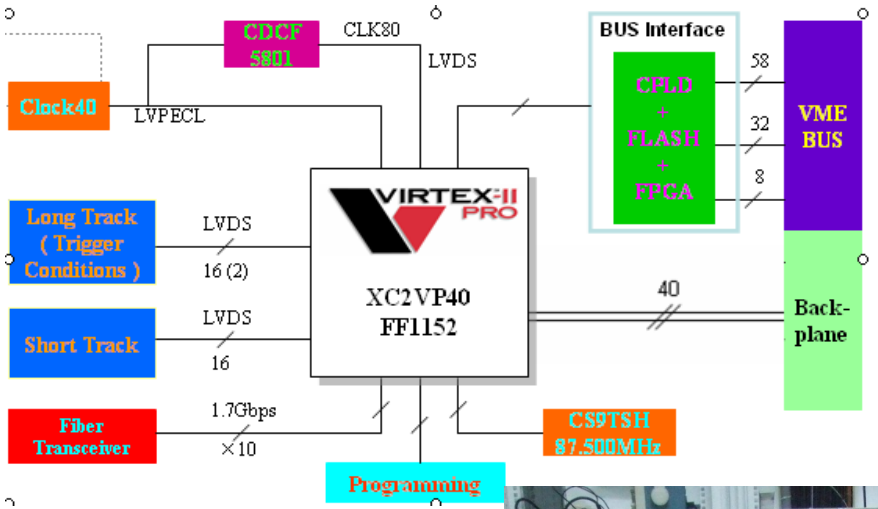
插件xTCA标准化
基金委重点项目新型触发与数据获取技术研究

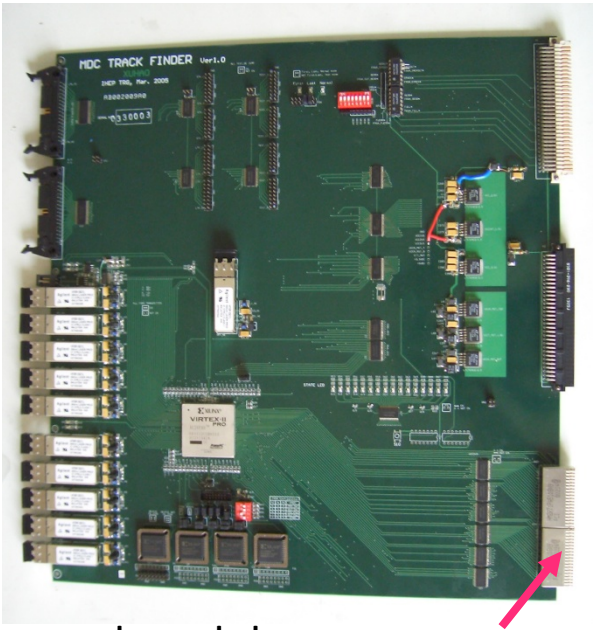
- Structure of PXD readout

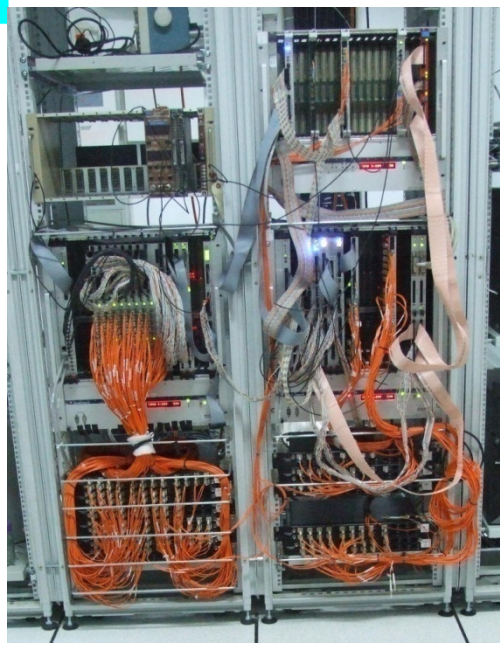


xTCA简介： Why-2:VME/CPCI is not sufficient

- Life time for a standard
- New standard for demand
- BESIII development
  - 200Gbps is needed
  - VME 6U/9U is used
  - Bandwidth is not enough
    - 500Mbps on backplane
- Solution
  - RocketIO
  - Optical Fiber
  - Private backplane
- NEW STARTNDARD is needed







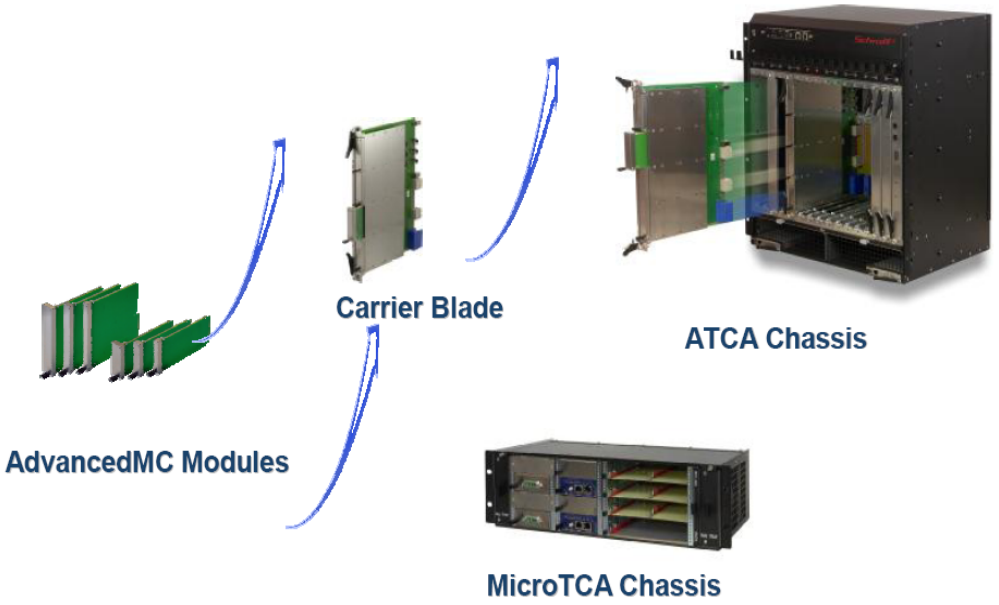
BESIII general module

Private backplane

205Gbps synchonized

What-1: Totally new standard?

- New standard:
  - Totally new?
  - Adoption from Industry ?
- TeleCommunication Industry
  - CPCI ~600 Mbps
  - VME 64x ~300Mbps
  - Limmitation in bandwith,
- PICMG Consortium
  - >105 companies
  - ATCA committee for nev
  - PICMG3.0 ATCA in 2002
  - MicroTCA in 2006



What-2: Adopted one?

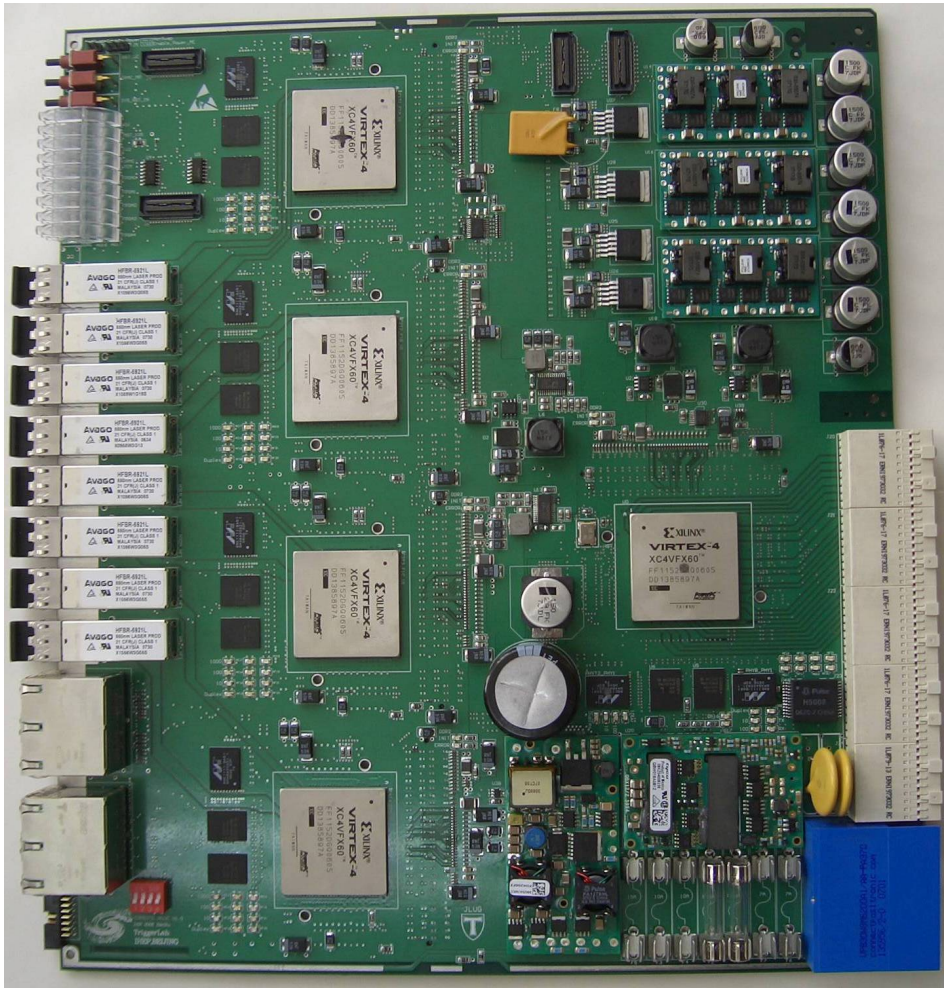
- ATCA
  - Advantages
    - High Speed IO and
    - Interconnections 10Gb/s
    - HA ~99.999%
    - Intelligent Management
- MicroTCA (MTCA)
  - with adv. of ATCA
  - Smaller/flexible
- AdvancedMC（AMC）
  - Universal card

Adopt Industrial one like with VME?

For sure this is a good start.

What-3 Extention

- ATCA backwards：
  - 8U, to big for machine control
  - No rear transition module connection(RTM)
  - No difinition for AMC and signals
  - No RTM modules（HA）
  - No control signal lines…
- MTCA backwards：
  - No RTM connections
  - No RTM module（HA）
  - No control signal lines…
  - High precision timing?
- AMC backwards：
  - interconnection？
  - No Control signal
  - …
- ATCA+MTCA+AMC+Extentions



Compute Node by IHEP Beijing

制定新标准：xTCA for Physics

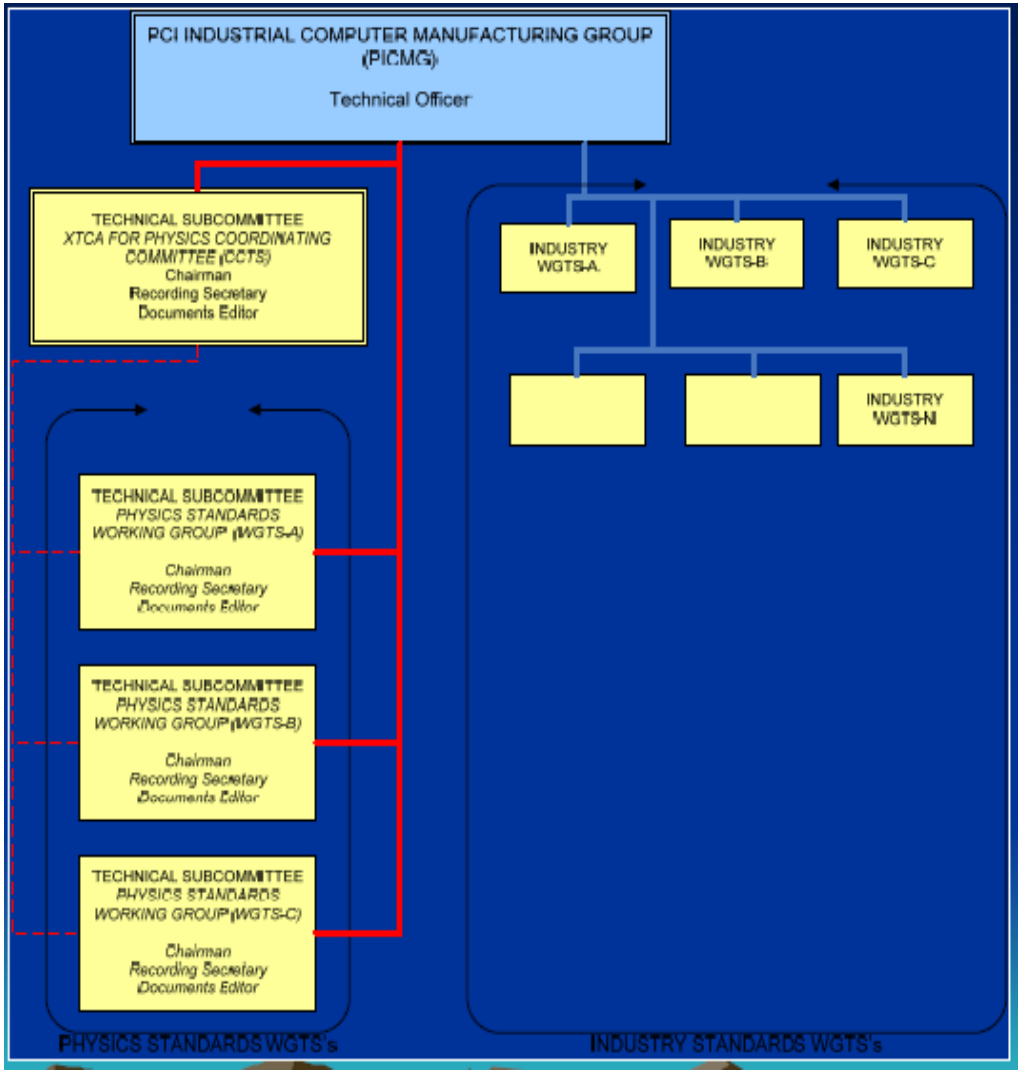
What-4: Working groups for xTCA for Physics

- **Physics Requests：**
  - **Physics User Survey Task Group**
- **Hardware Working Group WG1：**
  - **Physics xTCA I/O, Timing and Synchronization Working Group**
- **Software working Group WG2 ：**
  - **Physics xTCA Software Architectures & Protocols Working Group**

What-5: Tasks for WG1

- Hardware specification
  1. ATCA Rear Transition Module Interface for IO
  2. ATCA Carrier Boards for AMC's w/ Rear IO (2)
  3. AMC (Advanced Mezzanine Cards) w/Rear IO (2)
  4. MTCA (MicroTCA) Chassis w/ Rear IO (2)
  5. ATCA/MTCA Clock & Trigger Distribution (2)
- Priority One
  - Finish MTCA.4 and then PICMG 3.8
- Next Project
  - Precision timing using an ATCA backplane
  - PICMG 3.x specification or an application document on using ATCA backplane for precision clocking
  - Could look somewhat like a PICMG fabric interface document

When-1: xTCA for Physics



Coordination Committee (CCTS) founded March 10 2009 under PICMG

- Founding Institute: IHEP,SLAC,FNAL,DESY
- Founding Companies: >40
- Offices elected:
  - Chair： Ray Larsen from SLAC
  - Secretory:Augustus Lowell from Tripple Circle
  - Document Editor:Zhen-An LIU from IHEP Beijing
- CCTS monthly meeting
- WG weekly meeting
- F. Vince Pavlicek vince@fnal.gov HW WG secretory

Who-2: example in xTCA CCTS meeting

xTCA Coordinating Committee Meeting Agenda
October 28, 2010 0700-0800 Pacific Daylight – Live Meeting

1. Call to Order – Chair Ray Larsen
   a. PICMG Patent Call – Secretary Gus Lowell
   b. Roll Call, member changes since last meeting – Secretary
   c. Approval of Minutes of last meeting – Secretary
2. Review of Purpose & Scope of Coordinating Committee – Chair Ray Larsen
3. 3-slide reports from Technical Subcommittees
   a. Hardware WG (Timing, Synchronization & IO) – Chair Robert Downing
      SOW-Roadmap-Progress
   b. Software WG (Interoperability, high availability guidelines) – Chair Stefan Simrock
      SOW-Roadmap-Progress
4. 1-slide reports from Lab members
   a. DESY
   b. FNAL
   c. IHEP
   d. IPFN
   e. ITER
   f. CERN
   g. SLAC
5. 1-slide reports from Industry
   - Submit single slides in advance to larsen@slac.stanford.edu
6. 1-slide report from PICMG, MTCA Summit etc
7. New Business
8. Next Meeting Topic Suggestions
9. Motion to Adjourn

Where-1: xTCA for Physics events

- May 2007:1st ATCA workshop at FNAL
  + session in IEEE RT07
- Beginning 2008 discussion on feasibility of forming a new standard
- Oct. 2008: 2nd ATCA workshop in Dresden
  + session in IEEE NSS
- Mar. 10 2009: Founding of xTCA CCTS
- May 2009 : 3rd xTCA workshop in IHEP Beijing
  + session in IEEE RT09
- May 2010: 4th xTCA workshop in Lisbon Portugal
  + session in IEEE RT10
- Oct. 2011: 5th xTCA workshop in Valencia Spain
  + session in NSS/MIC xTCA
- 2012-2018: regular xTCA Workshop

Where-2:Progress/Status

- Two specifications publicized:
  1. MTCA.4 for MTCA extension
  2. PICMG 3.8 for ATCA extension
- One specification to be proved
  1. PDG 1.0 for clocking, Trigger and Control
- Under development
  - Software
- Hardware development
  - Prototypes

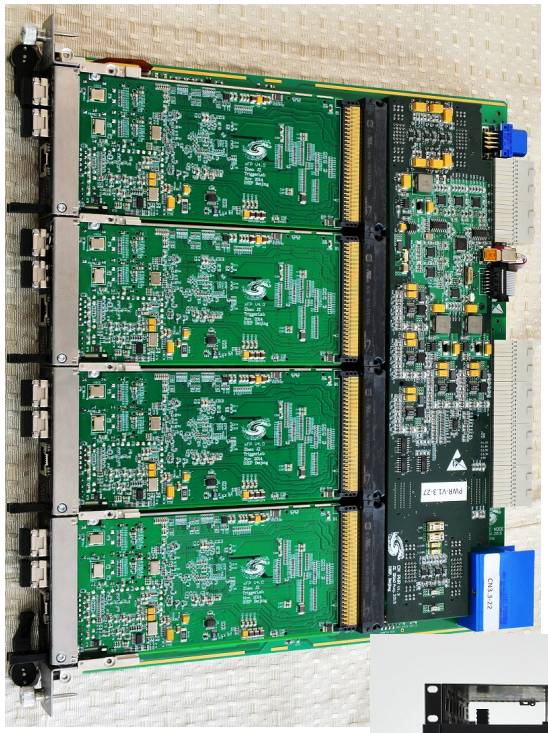
基于xTCA的计算节点及PXD系统

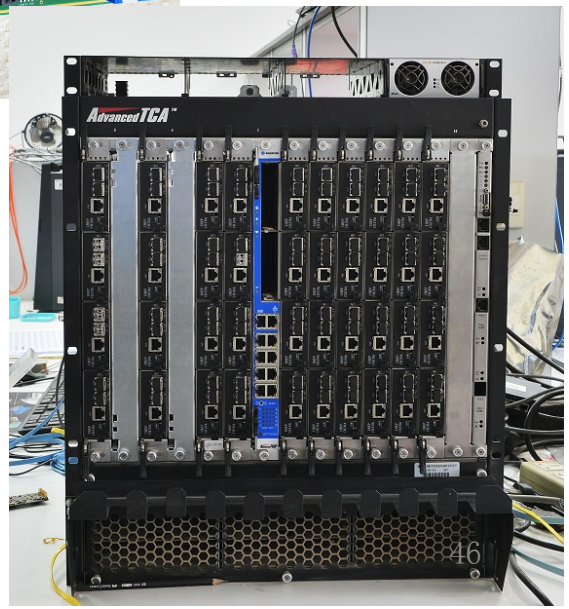
- Which Platform ---------→Carrier/AMC
  - xTCA: ATCA Carrier + AMC
- 6.25Gbps/ch -→ 2x3Gbps
  - 6G/FPGA
  - 2 X 3Gbps/link
- DDR2 …… → 2X DDR2
- V4 or V5 or V6 or SP6? -------→ V5
- Memory 4G/FPGA(total of 20Gb)->4(20)G
- Clocks and controls ---- Yes

- Good chance for xTCA

New Development in xTCA standard

- Key Features
  - xTCA Compliant
  - Both Front and Rear IO
  - Carrier Board: Ver 3
  - Daughter Board: Ver. 5
  - RTM: Ver.2
- Application
  - Belle II/PXD DAQ system





PXD-DAQ: 进展与计划

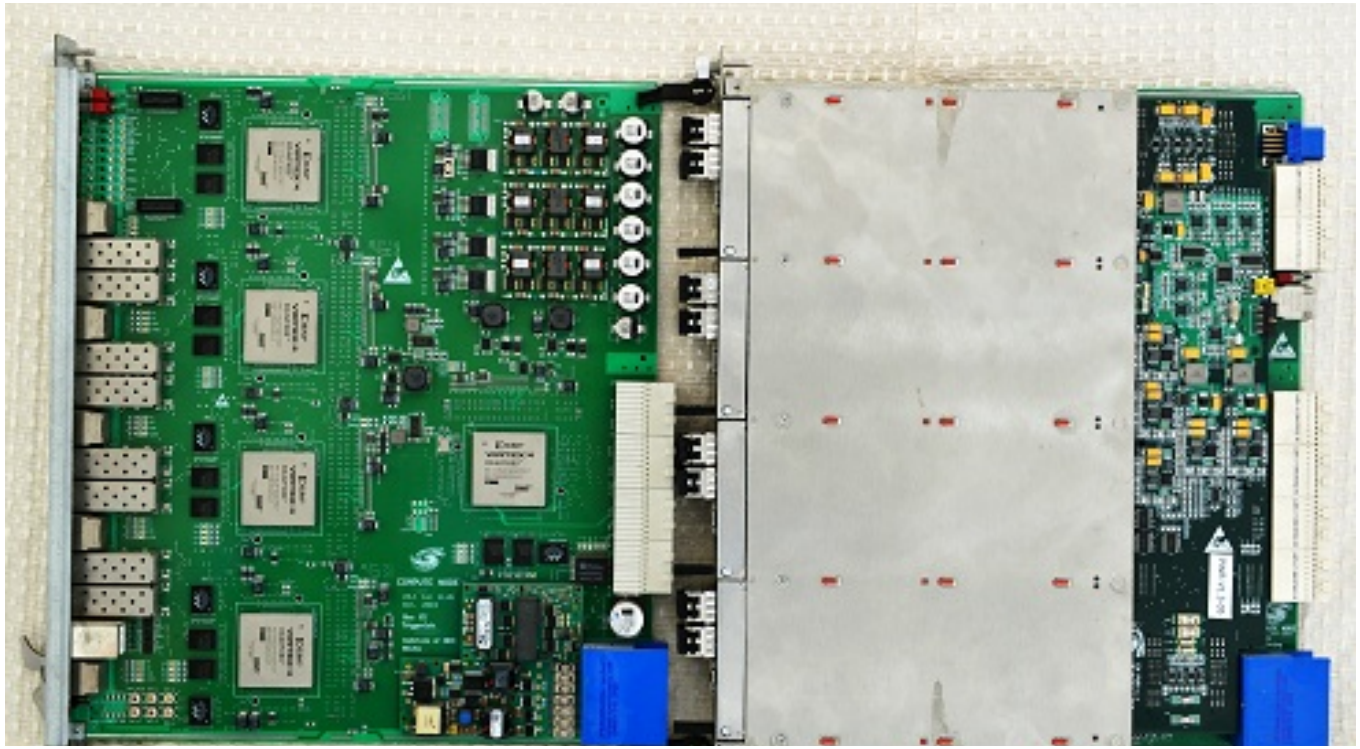
触发组

- 原型设计
  - 所有原型板及完整计算节点原型在高能所完成
  - 计算节点完整板(CN)在吉森大学进行了测试
  - 安排了ATCA机箱与控制器的订货
- 已经开始了量产的准备
- 2016计划
  - 完成量产
  - 完成在DESY和KEK的宇宙线实验
  - 完成在KEK的DAQ集成测试
  - 系统组装

Compute Node

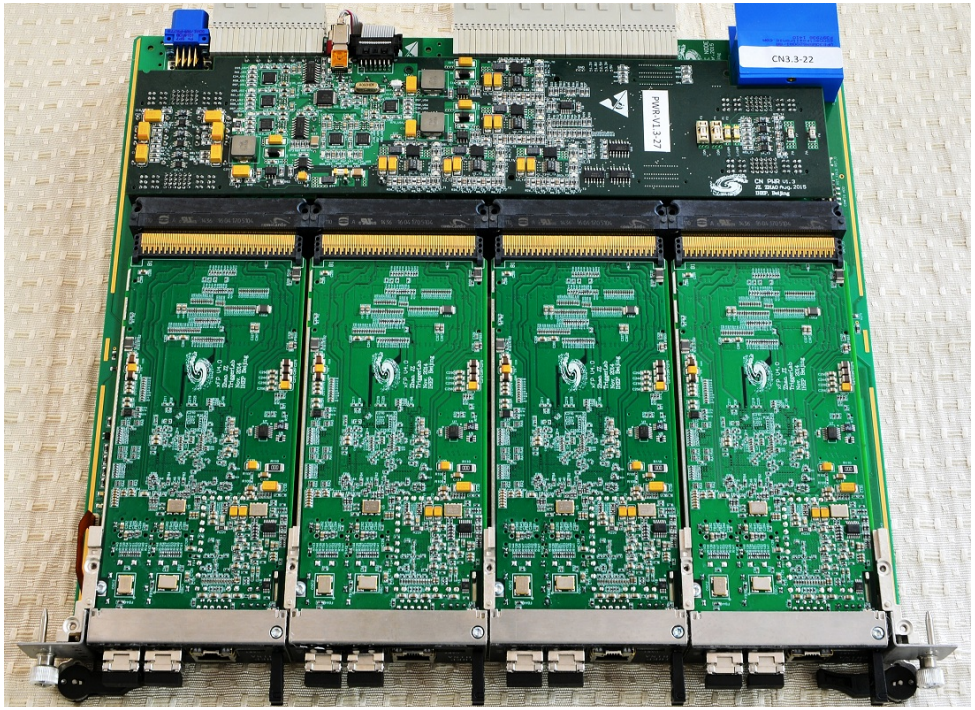
ATCA/xTCA development

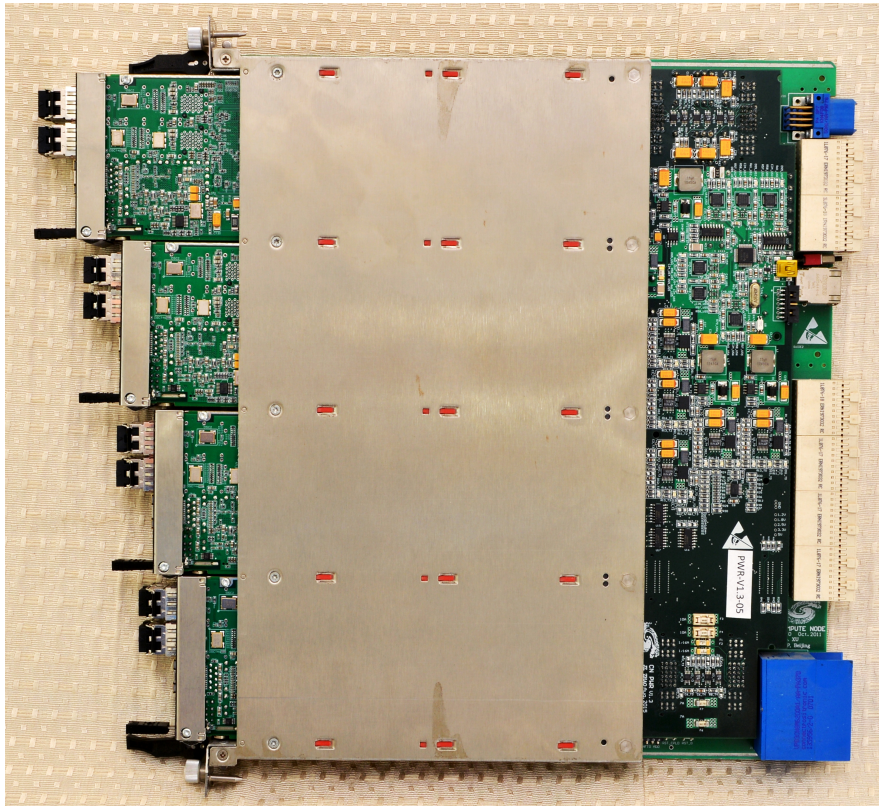
- ATCA(left)
  - Virtex 5
  - Optcal IO
  - Processor
  - Swits
- xTCA(right)
  - Carrier
  - AMC



More on xTCA Compute Node

- AMC/Carrier/Power/RTM
  - Interconnections
  - Pluggable MMC



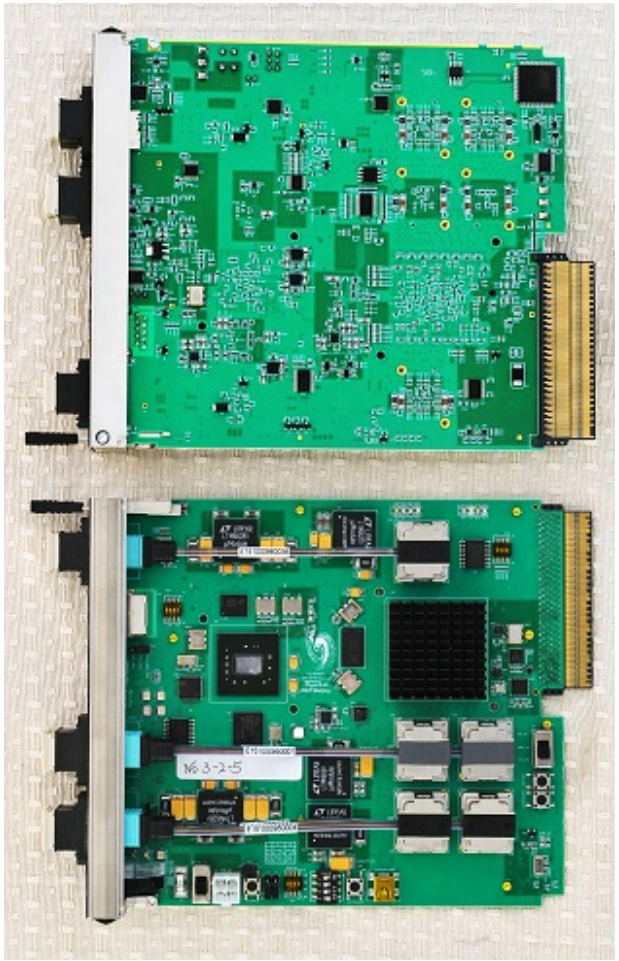


现状

- Under Design with New FPGA
  - Virtex Ultrascale
  - Higher bandwidth
    - >10 Gbps/link
    - >120 Gbps/module
    - 4G DDR4 memory

借用基金委国际合作项目开发的CPPF板
CPPF for CMS Phase I L1 Trigger Upgrade

- uTCA compliant
  - Double width AMC card
- IO
  - Inputs : **Four** 12ch MiniPoD connectors(48)
  - Outputs: **Two** 12ch MiniPoD connectors(24)
- Processing and Control
  - FPGA
    - -- XC7VX415T-2FFG1157C(48 GTH)
    - -- XC7K70T-2FG484C
  - Flash
    - -- PC28F00AG18FE

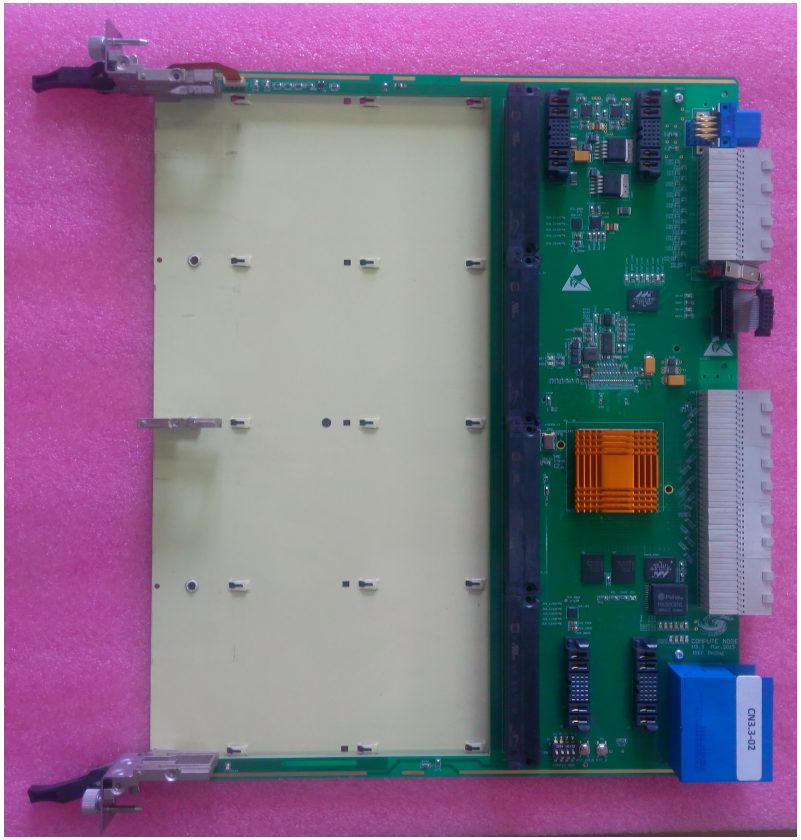


Application in Belle II/PXD

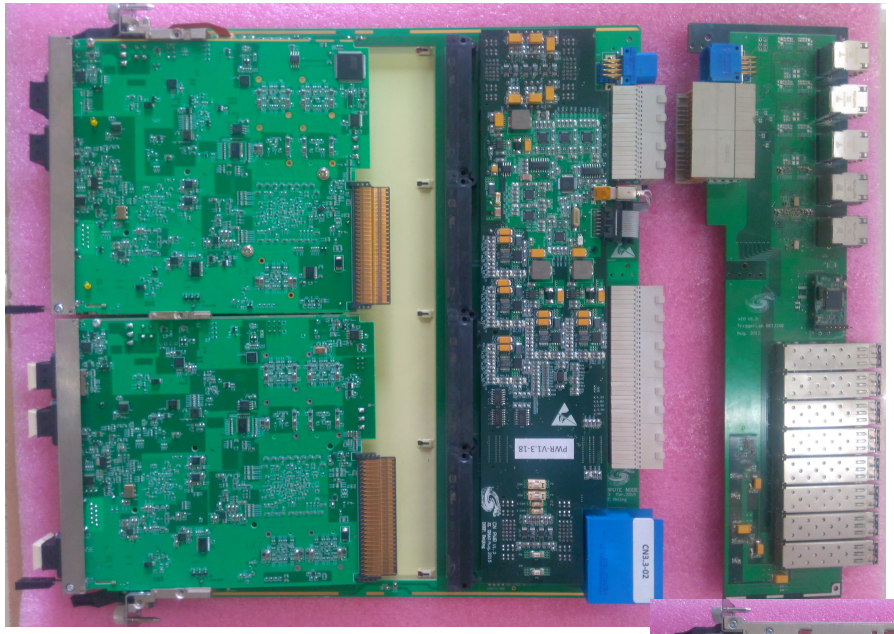
- Key Module of DAQ for Belle II/PXD
  - 8 Compute Node ,each include
    - A RTM
    - Carrier
    - 4 SW AMC
- 2 Switch
- 1 Shelf Manager
- 3 Power Modules

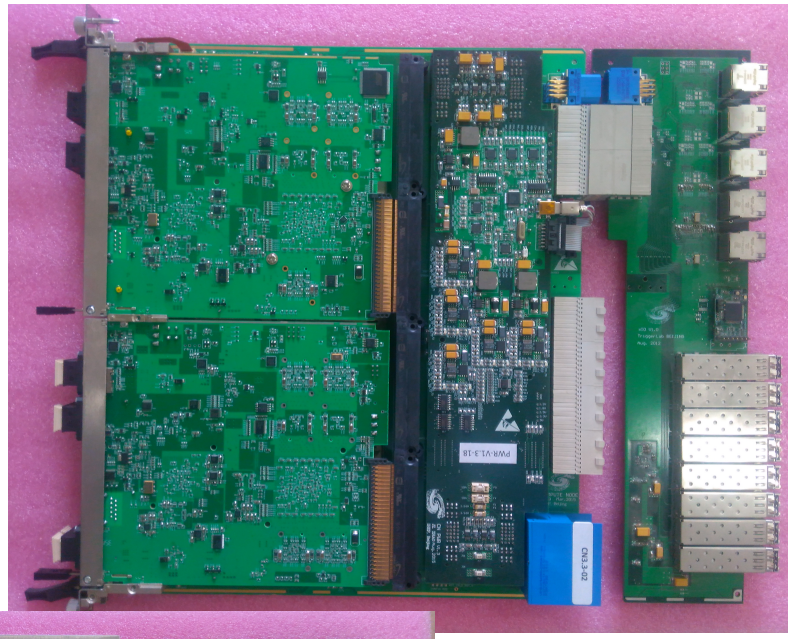
面向 PANDA和CMS Phase II 需求

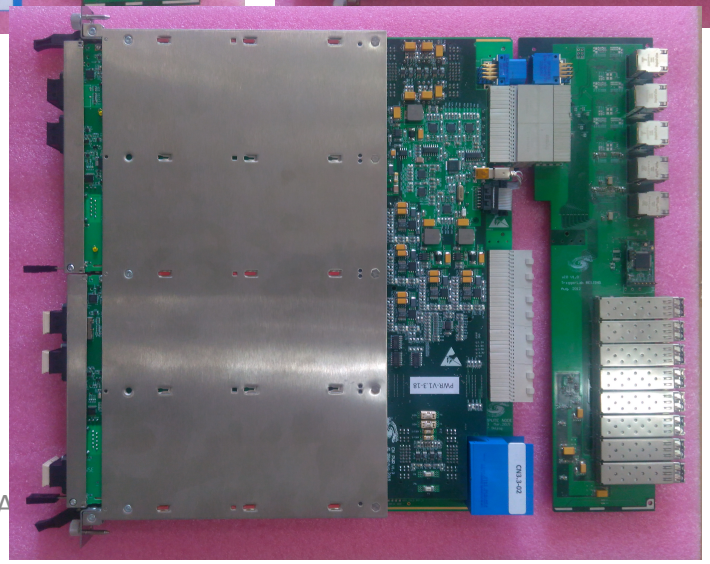
- Why ATCA/xTCA?
- xTCA Compliant
  - ATCA Carrier with Full Mess Connection
  - RTM for IO, MiniPod
  - Double Width AMC for processor
- Processors
  - Virtex 7/Kintex Ultrascale/Virtex UltraScale



已有原型设计

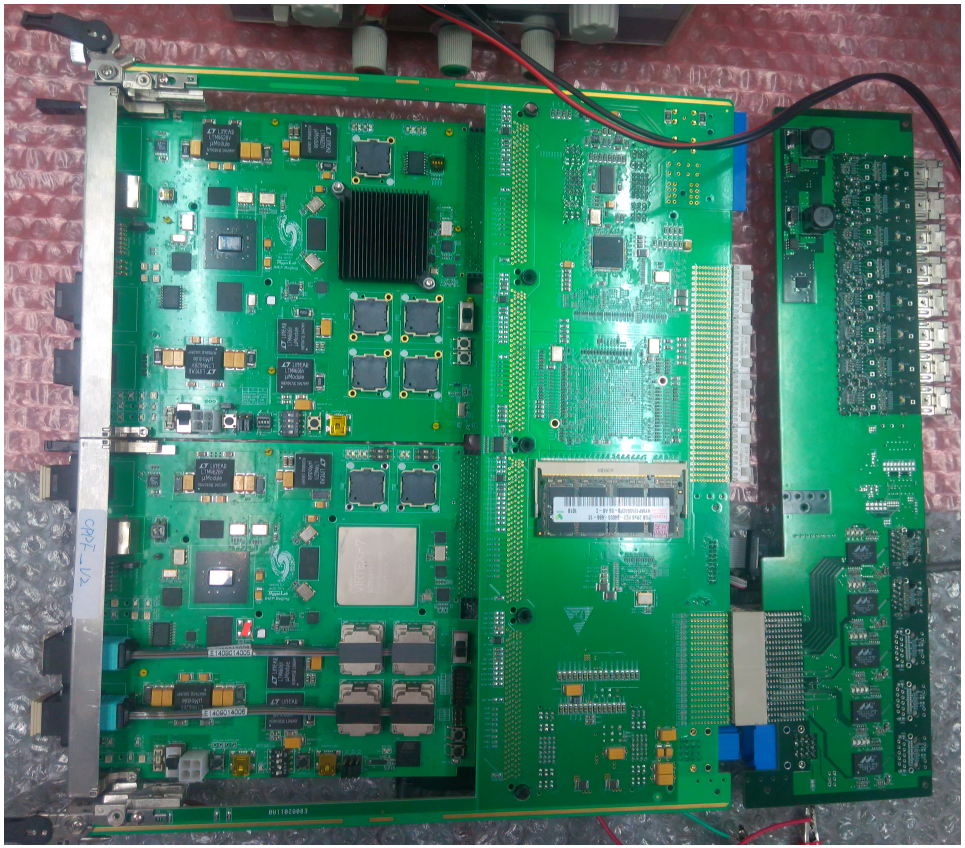






最新设计

- uTCA compliant
  - Double width AMC card
- AMC IO
  - 24 Channel/10Gbps
  - 1 ch to Switch/6Gbps
  - Flash-- PC28F00AG18FE
  - No DDR
- RTM
  - 8 Chanel/6Gbps
- Carrier Switch
  - Virtex FPGA
  - 2G DDR2



未来

- 加强与PANDA合作组的联系
- 争取经费
- 明确任务