Low-Gain Avalanche Detector for 4D Tracking

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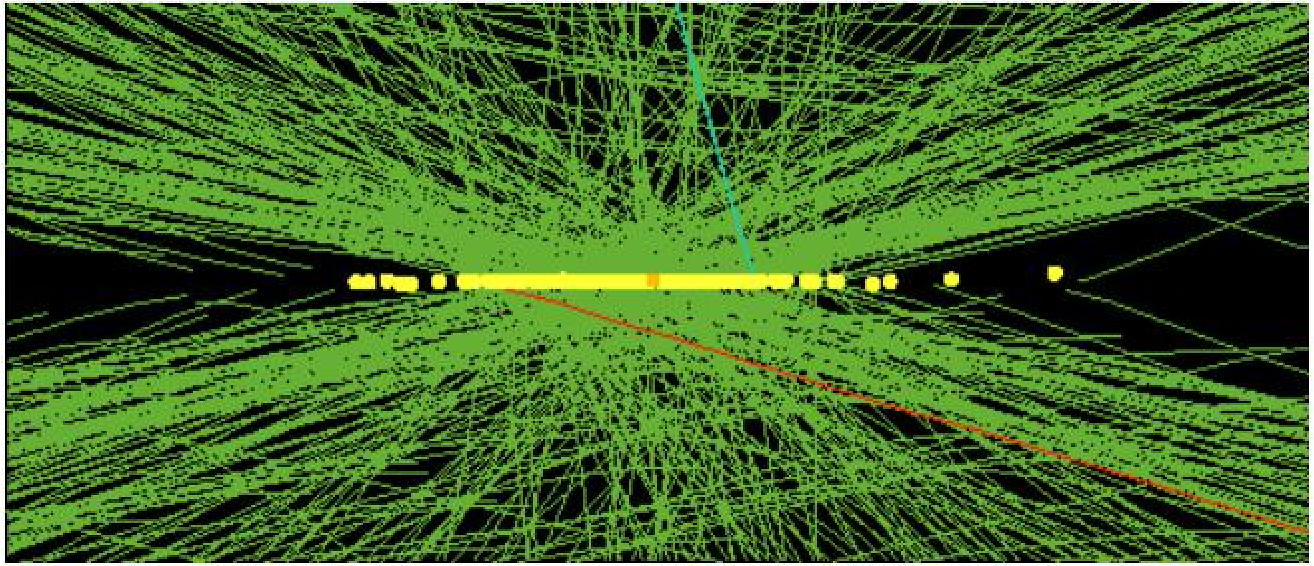
2008-09-14

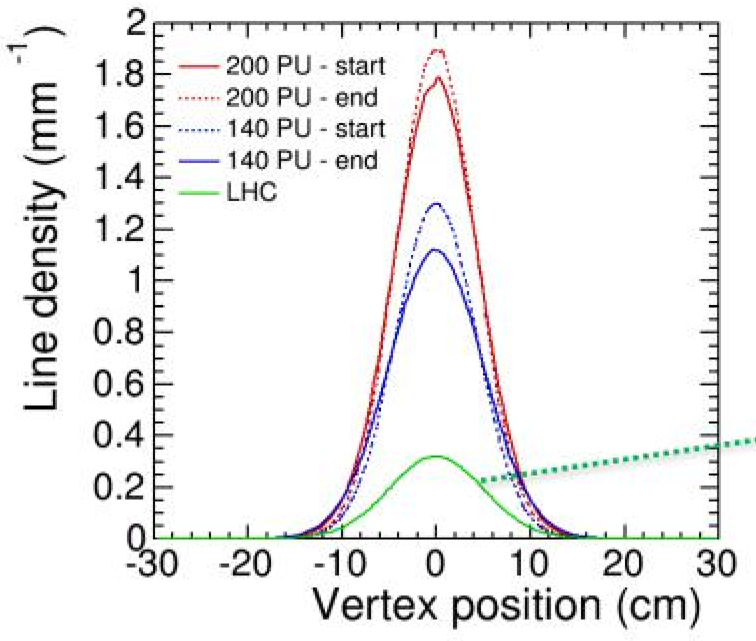
Why 4D Tracking?

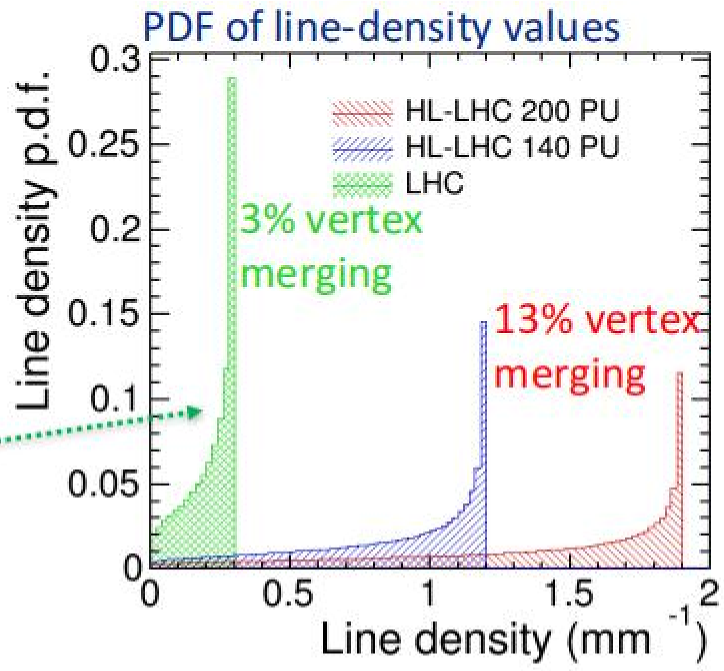


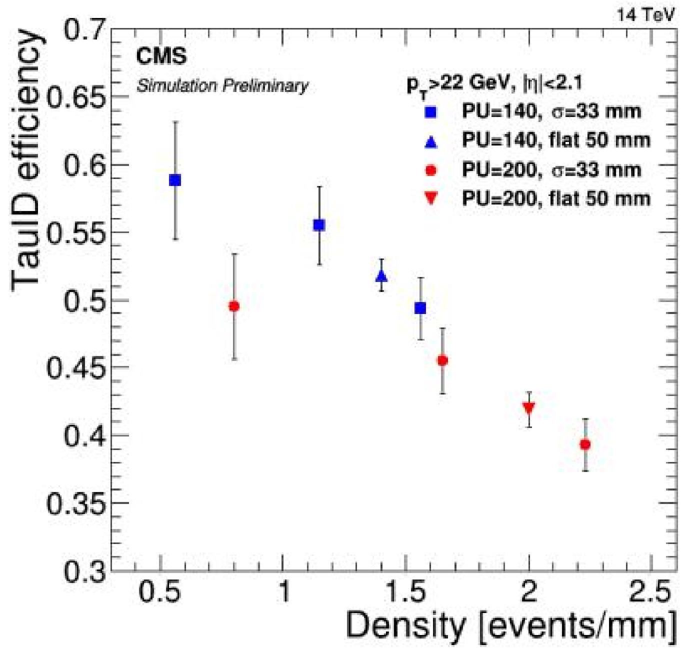
- HL-LHC environment:
  - Pileup up to 200 (180ps, 50mm)
  - Additional energy, extra jets, reducing the performance of several physics objects and particularly important for trigger
- Extended tracking coverage up to $|\eta| = 4.0$
  - Main handle against pileup
  - 5-7 vertices within tracker resolution at large $|\eta|$ (only 1/3 of the effect in the central region)

Effects of High Pileup in Reconstruction

- HL-LHC sees a substantial increase in the peak pileup line-density
- Large rate 'merged' vertices even after upgrades

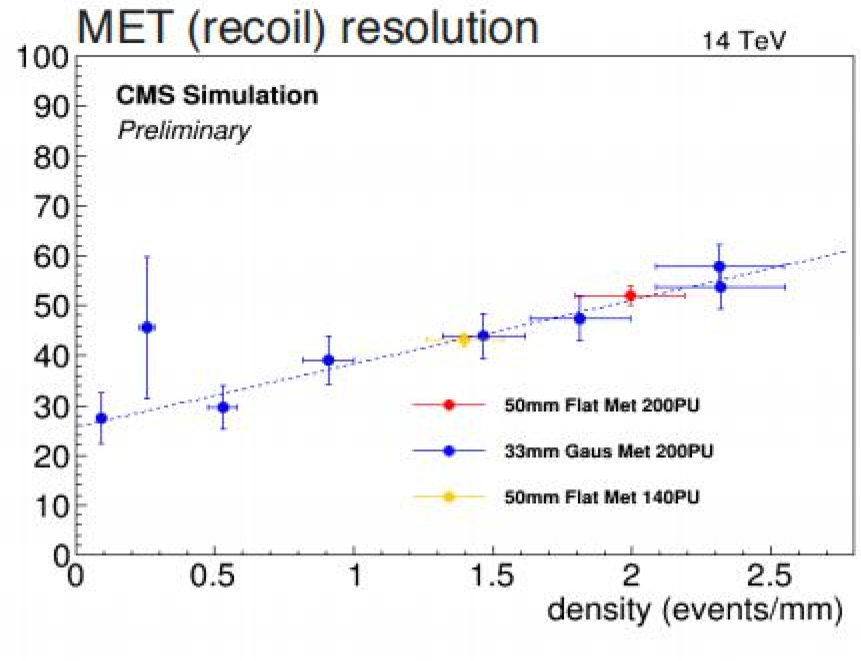


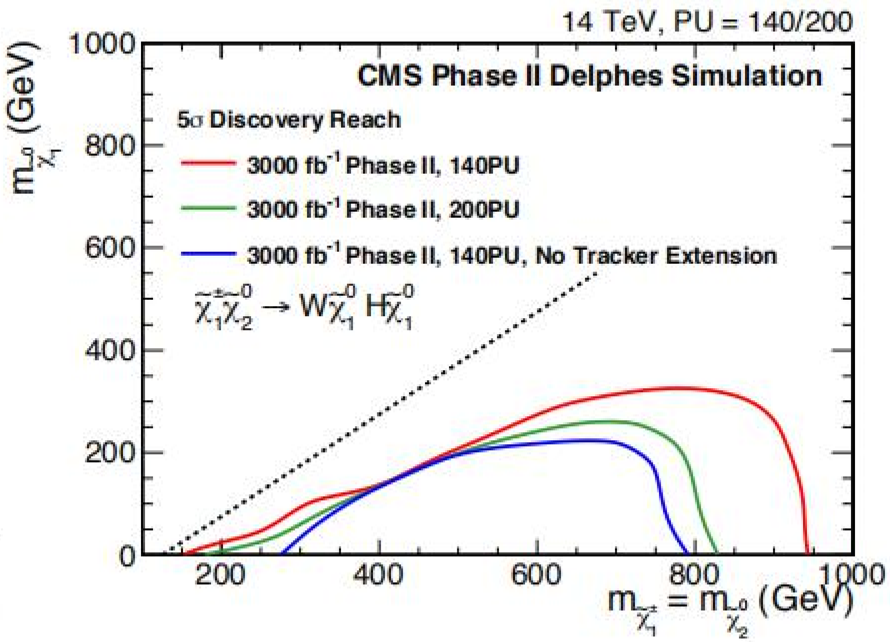




Effects of High Pileup in Analysis

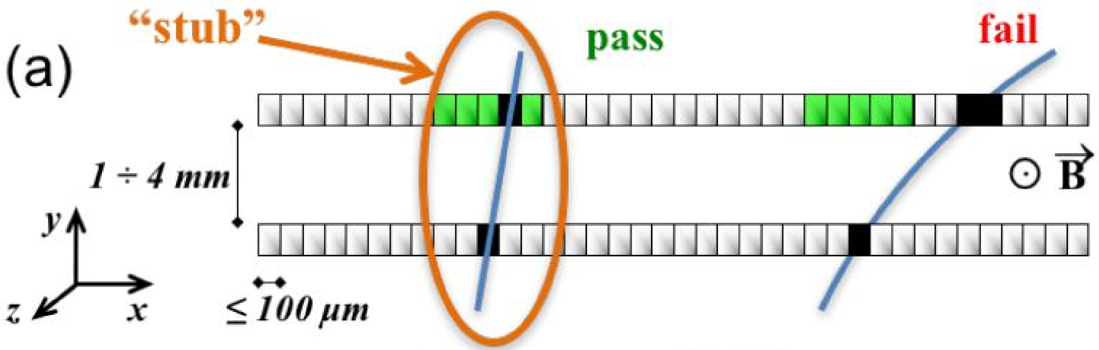
- These reconstruction and physics object impacts percolate to the analysis level



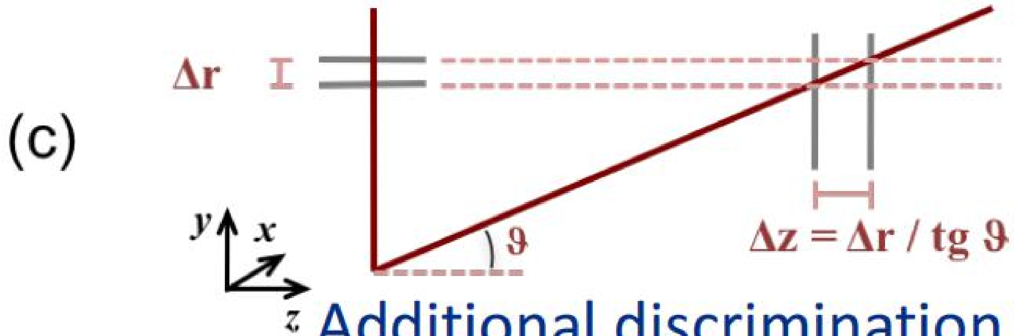


Algorithmic Effects in 4D Tracking

- Combinatorial reduction from more clean track seeds
- Could put timing into pT modules to remove fake stubs adding time coincidence cut



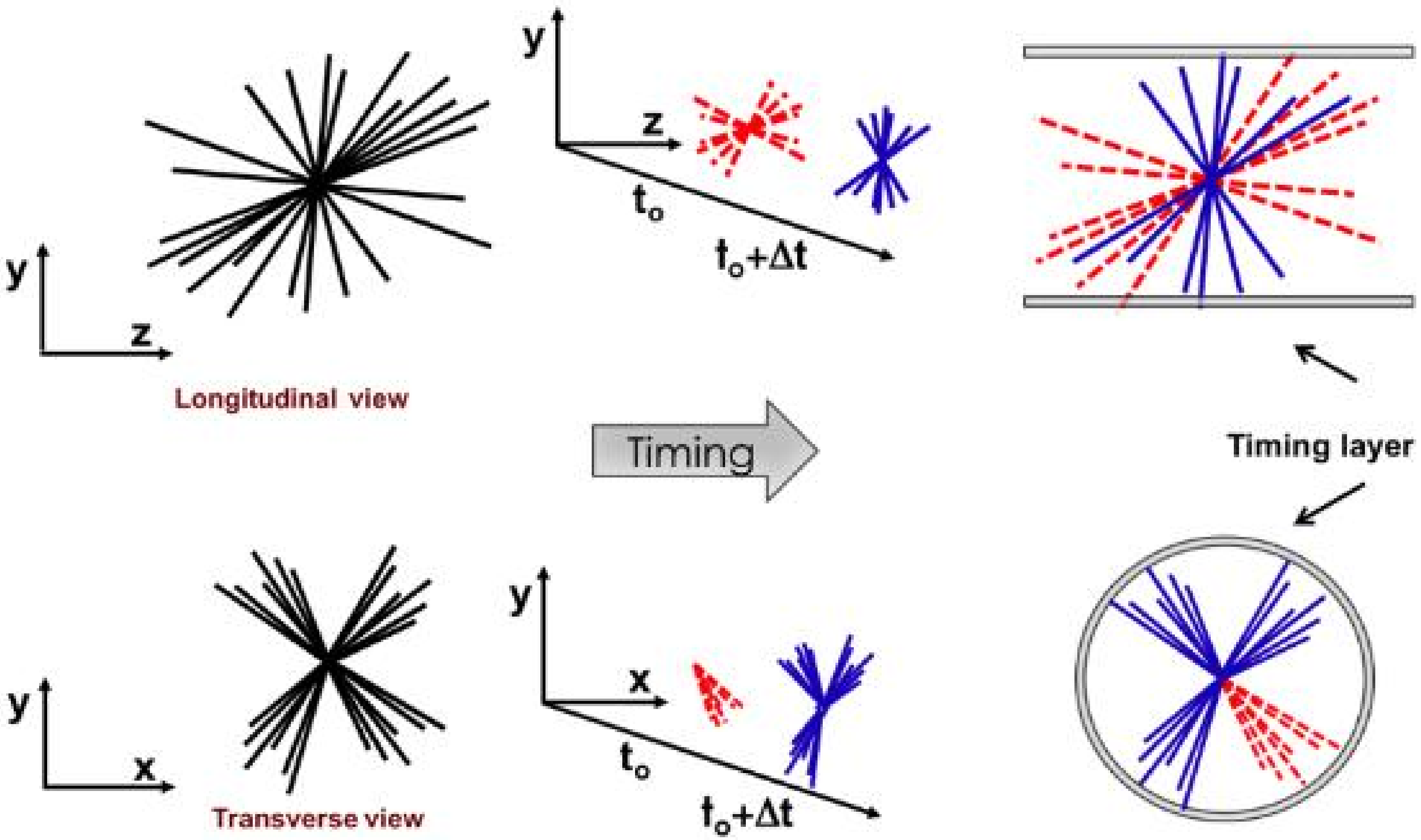
1-4mm = 3-13ps



Additional discrimination in pT module-like designs

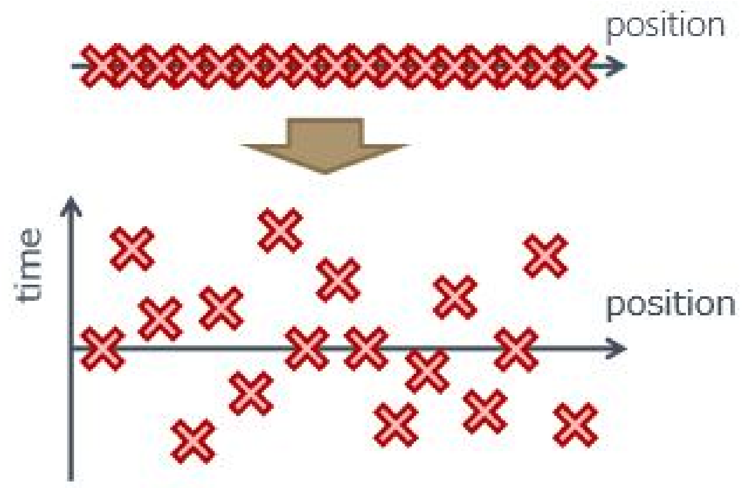
Timing in Event Reconstruction

- Timing allows distinguishing overlapping events by means of an extra dimension

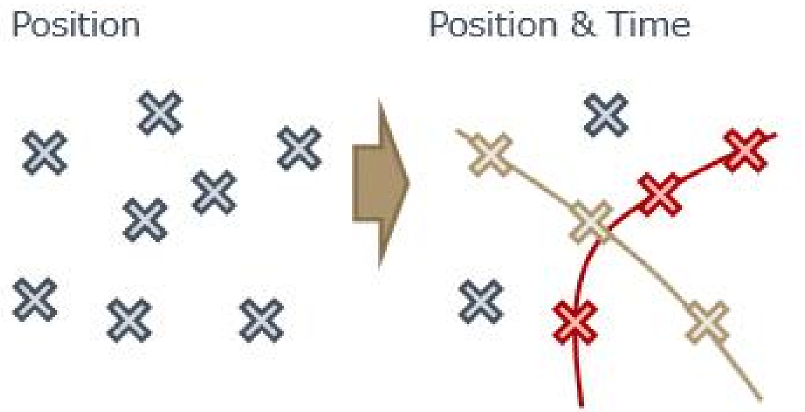


Timing in Track Reconstruction

- Massive simplification of pattern recognition, new tracking algorithms will be faster even in very dense environments

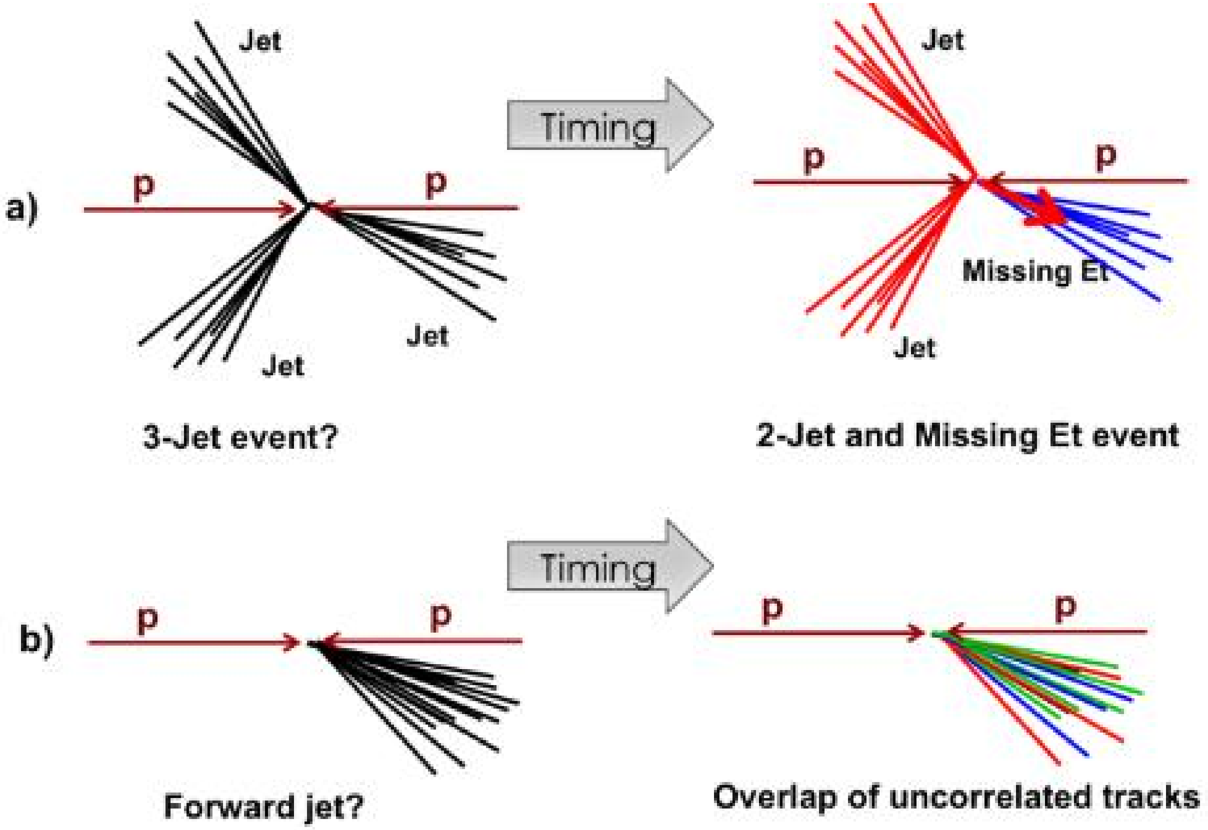


- Use only time compatible points



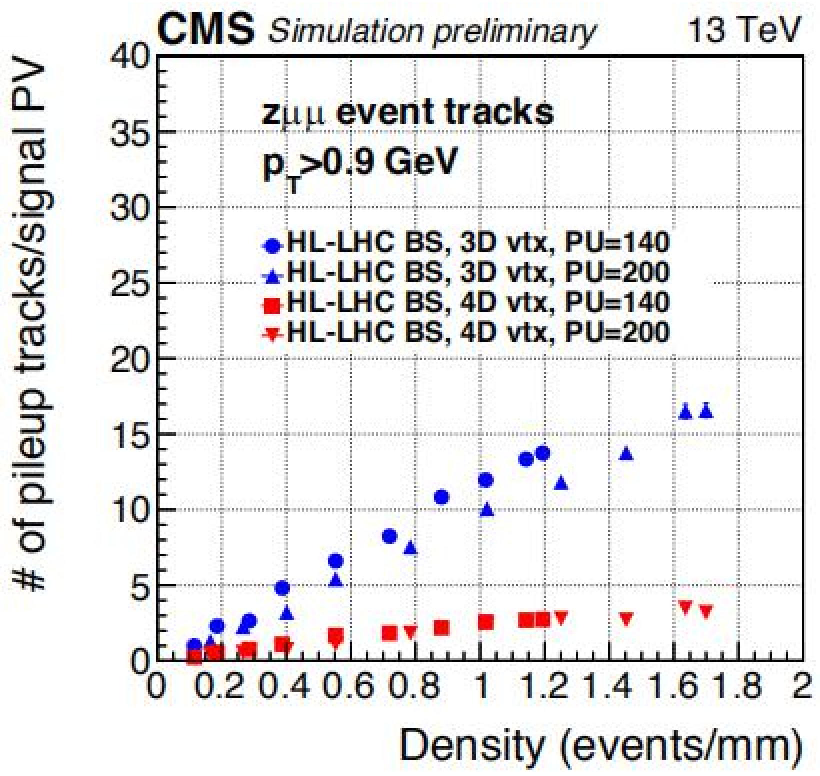
Timing at Trigger Level

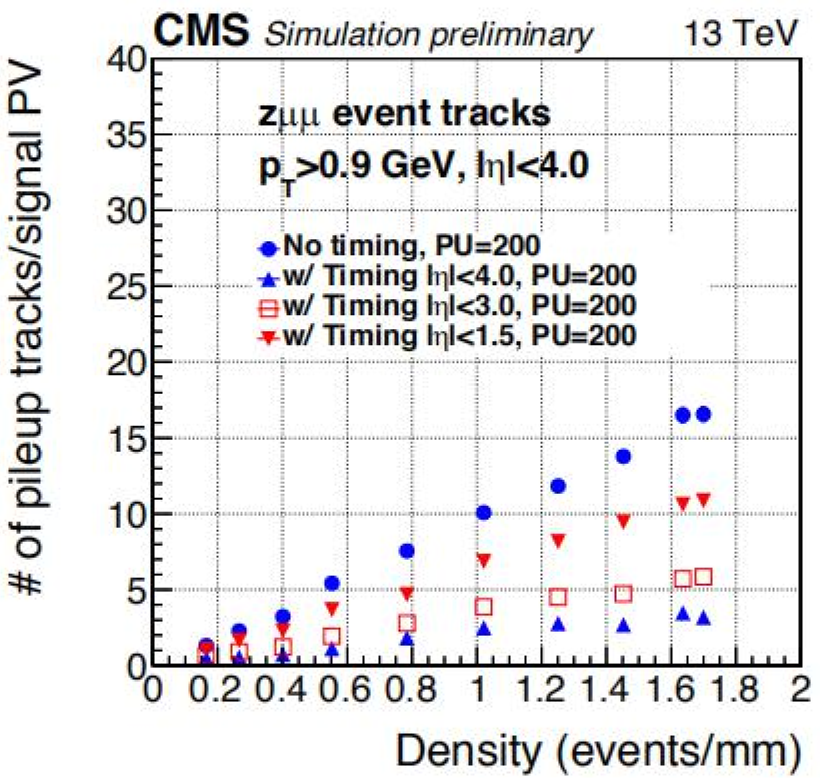
- Timing at the trigger decision allows reducing the trigger rate rejecting topologies that look similar



Effects of Timing on Track-Vertex Association

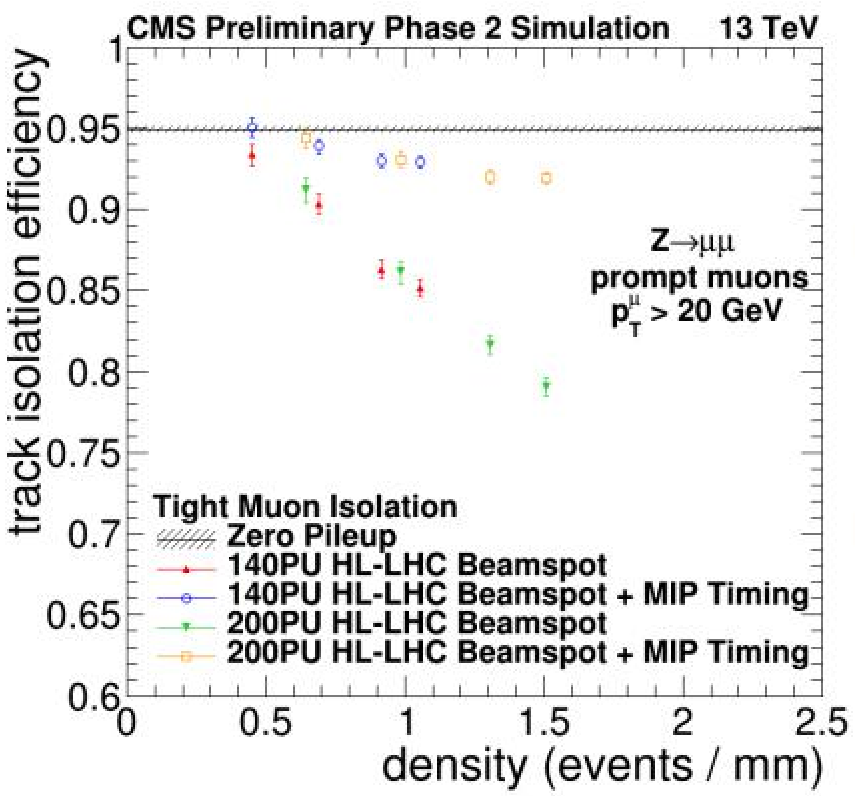
- Large improvement assuming a hermetic timing layer, total improvement scales with solid angle that is covered by the detector

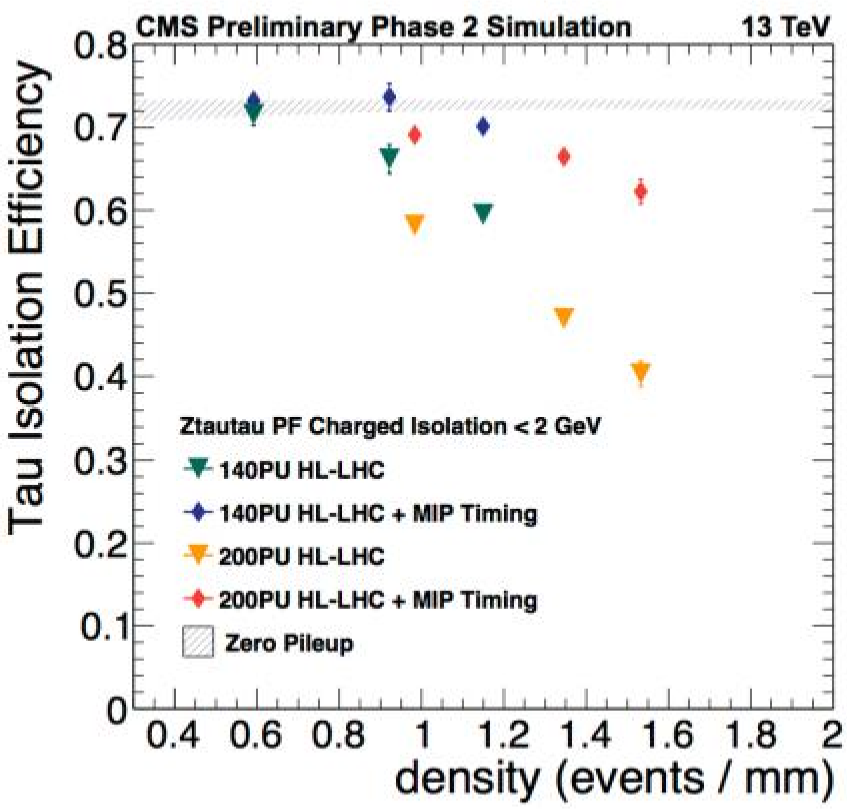




Impact of Track Timing at the Analysis Level

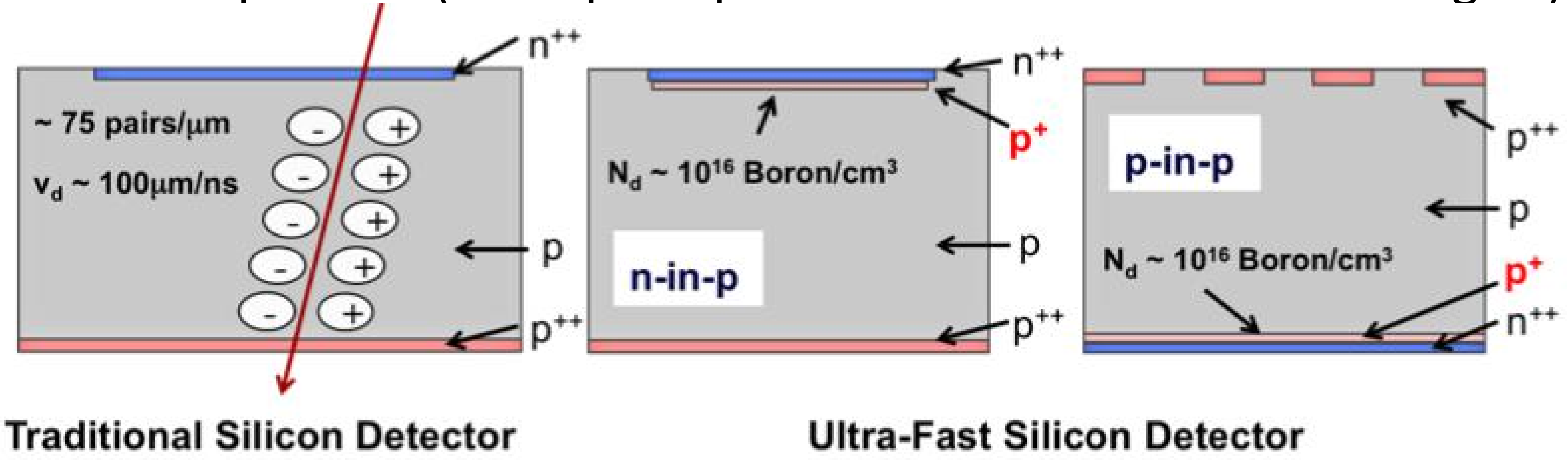
- There is a significant improvement in the efficiency.





LGAD - Ultra-Fast Silicon Detector

- Adding a highly doped, thin layer of p-implant near the p-n junction creates a high electric field that accelerates the electrons enough to start multiplication(same principle of APD but with much lower gain)



LGAD - Ultra-Fast Silicon Detector

- Why low gain?
  - Milder electric fields, possible electrodes segmentation, lower shot noise, no dark count, behaviour similar to standart Silicon sensors

- Why thin sensors?
  - Highe signal steepness, more radiation resistance, easier to achieve parallel plate geometry, smaller Landau Noise

Sensor

Silicon Sensors

- ▻ GigaTracker NA62: σ_t ~ 150 ps
- ▻ Silicon detector + SiGe HBT amplifier[1]: σ_t ~ 105 ps

+ Fine segmentation easy
+ Known technology
- Small signal

➼ Intrinsic resolution: **σ_t ~ 100 ps**

Diamond Detectors

- ▻ TOTEM Diamonds for CT-PPS ToF: σ_t ~ 100 ps

+ No leakage current
+ Radiation hard
+ Small capacitance, high mobility
- Small signal

➼ Intrinsic resolution: **σ_t ~ 100 ps**

APD (Avalanche PhotoDiodes)

+ Thin sensors (30-50 μm)
+ High signal (gain 50-500)
- Sensitive to shot noise
- Radiation resistance up to 10^{14} n_{eq}/cm^2
- Fine segmentation difficult

➼ Intrinsic resolution: **σ_t ~ 30 ps**

LGAD (Low Gain Avalanche Diodes)

+ Thin sensors (50 μm)
+ Medium-high signal (gain 10-20)
+ Shot noise under control
- Radiation resistance under investigation (within RD50 Coll.)
- Possible fine segmentation

➼ Intrinsic resolution: **σ_t ~ 30 ps**

LGAD - Ultra-Fast Silicon Detector

$$\sigma_{tot}^2 = \sigma_{Landau}^2 + \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{V_{thr}}{S/t_{rise}}\right]_{RMS}\right)^2 + \left(\frac{\mathrm{TDC}_{bin}}{\sqrt{12}}\right)^2$$

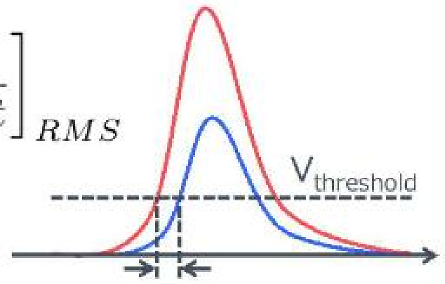
thin sensor (50 µm)

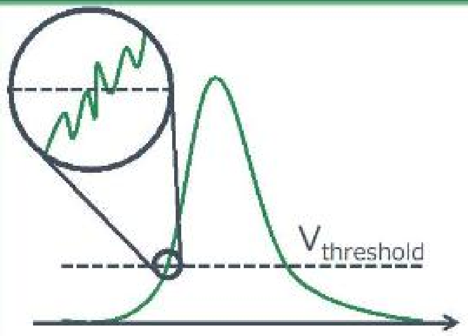
fast signals large S/N

timewalk correction with CFD small TDC bins

$$\sigma_{det}^2 = \sigma_{Landau}^2 + \sigma_{TimeWalk}^2 + \sigma_{Jitter}^2$$

$$\sigma_{TimeWalk} = \left[\frac{V_{th}}{S/t_{rise}}\right]_{RMS} \propto \left[\frac{N}{dV/dt}\right]_{RMS}$$

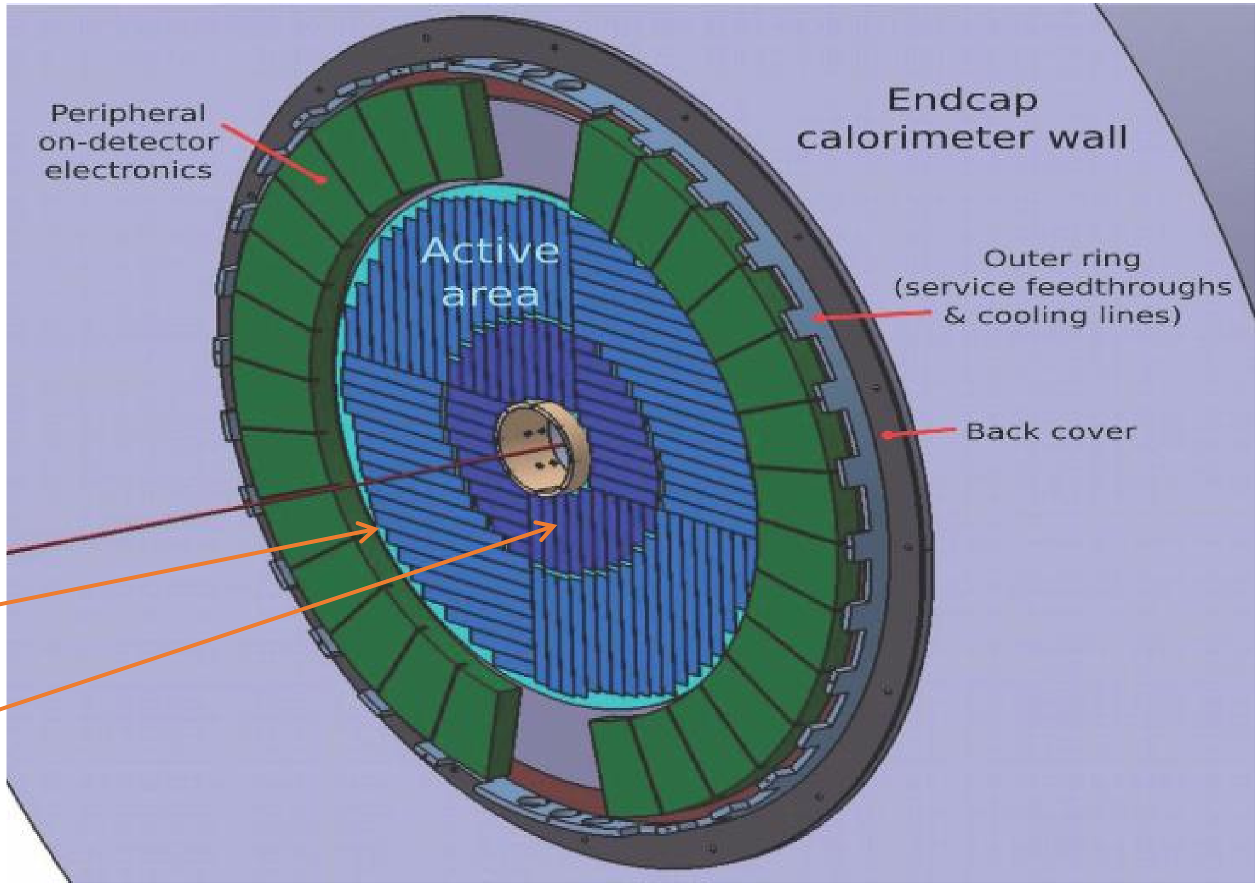




$$\sigma_{Jitter} = \frac{N}{(dV/dt)} \simeq \frac{t_{rise}}{(S/N)}$$

High-Granularity Timing Detector

- Design & Requirements
  - z = 3420-3545mm(3435-3485mm)
  - 2.4 < $|\eta|$ < 4.0 (forward region)
  - R = 110 - 1100mm (120 - 640mm)
  - Time resolution: 30ps/track
  - Pad size: 1.3 * 1.3 mm^2

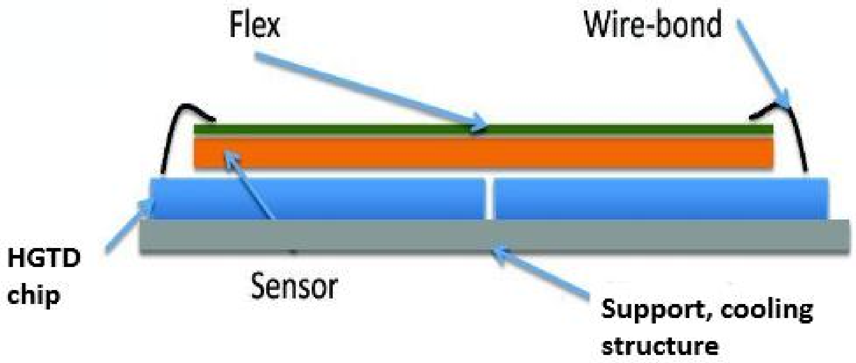


luminosity monitor

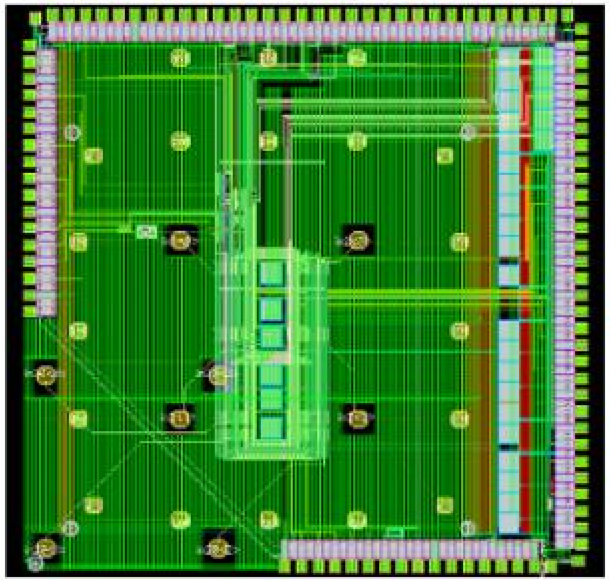
planned to be
replaced once

HGTD Preliminary Design

- 2*2 array of sensors bump-bonded to ASICs



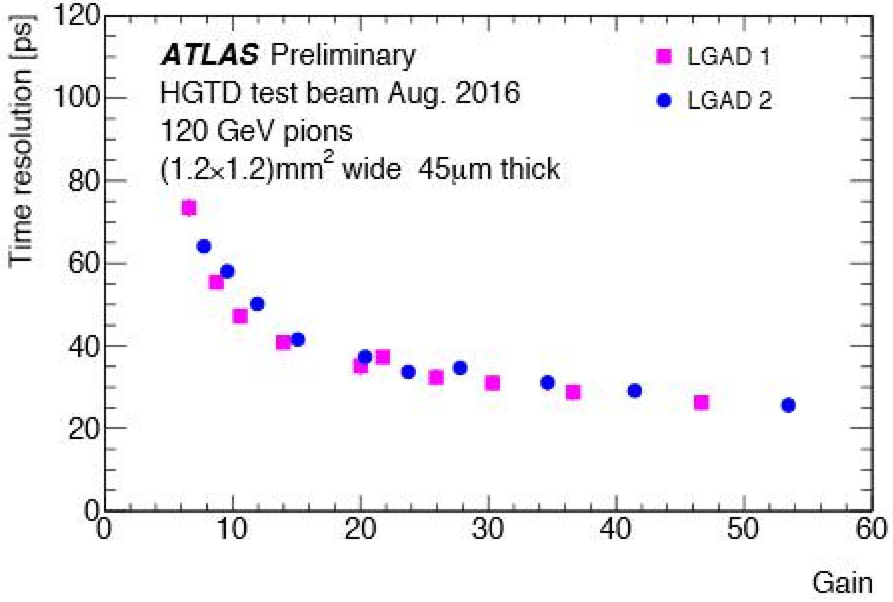
Chip layout with wire bonds in the periphery

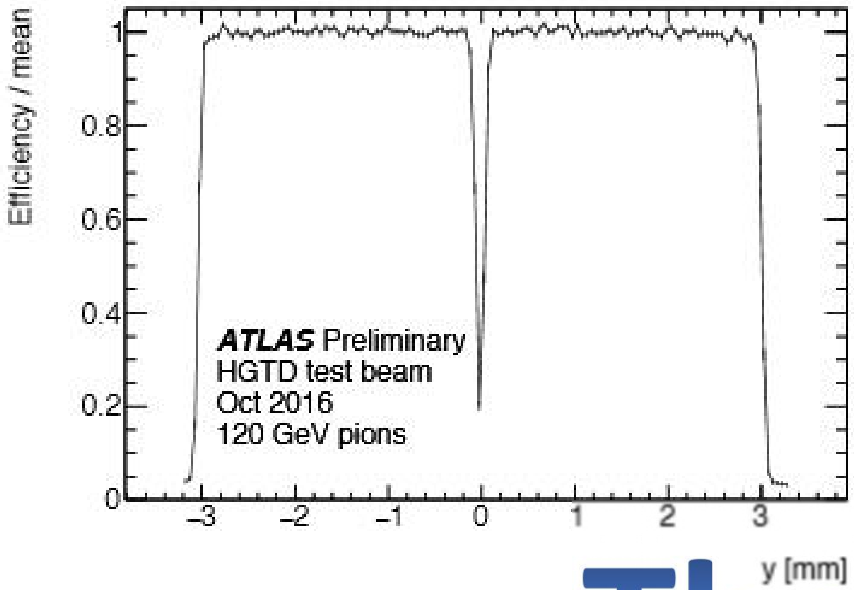


- Flex used for readout signal and voltage distribution
- Modules staggered to minimise dead areas
- 1*1mm^2 pads everywhere

Test-beam Results

- Gains up to 50, time resolution < 30ps for 1*1 mm² pads, dominated by Landau fluctuations
- Good efficiency and signal uniformity for arrays





Thanks!