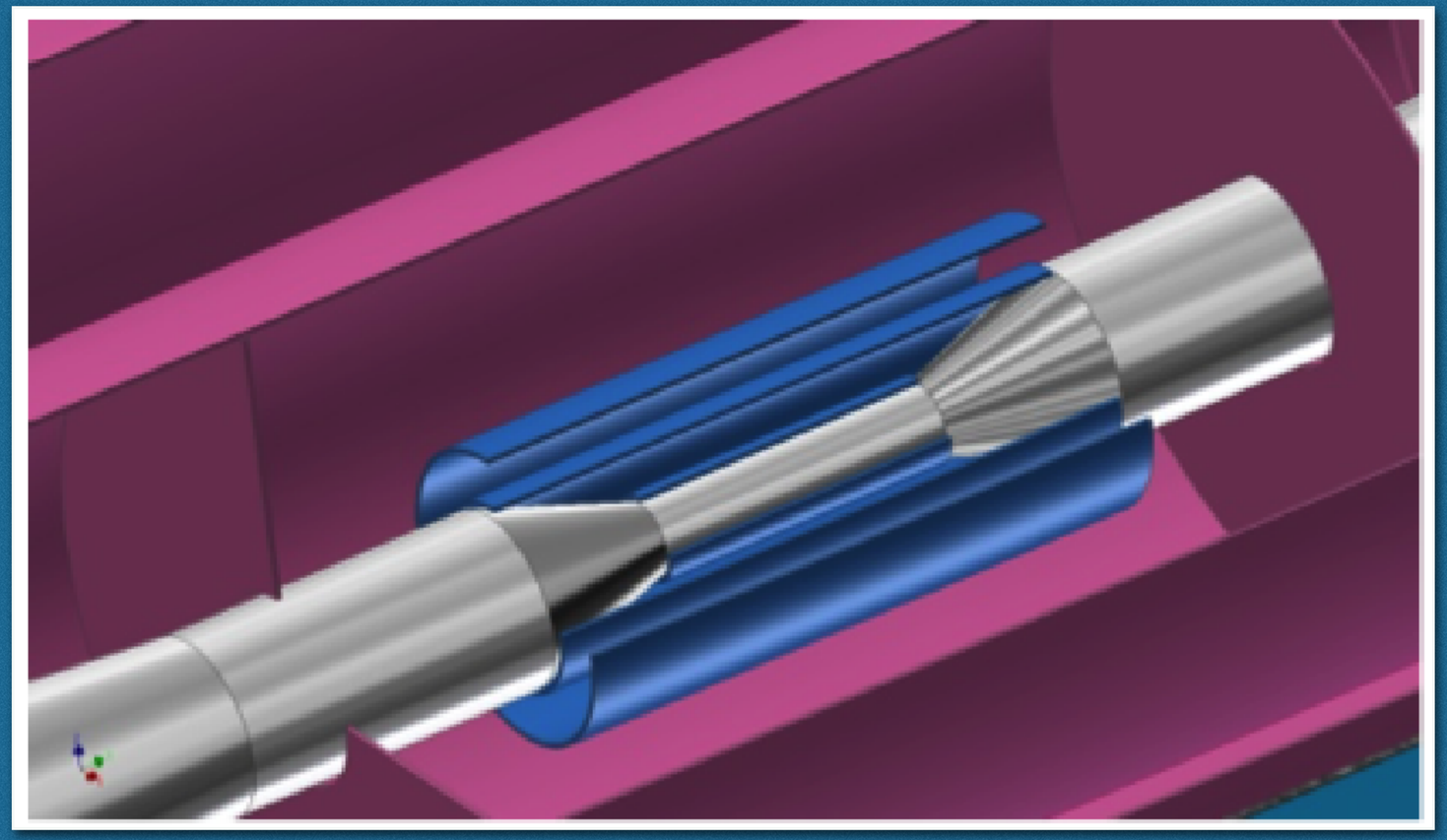
Introduction to the Pixel MOST2 Project



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Institute of High Energy Physics
Chinese Academy of Sciences

IHEP, 07 June 2018

Development and verification of key technologies for high-energy Circular Electron Positron Collider

Verification of technologies in three fronts:

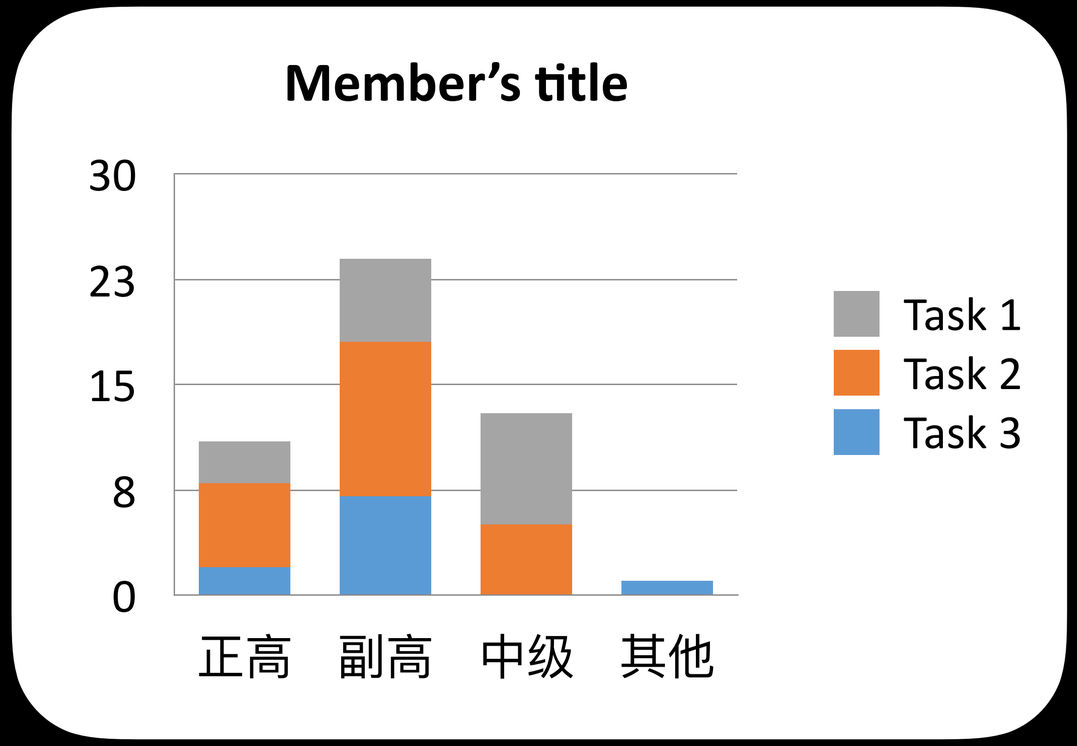
— Accelerator: Several prototypes will be produced (low-field magnets, vacuum chambers, electrostatic separator

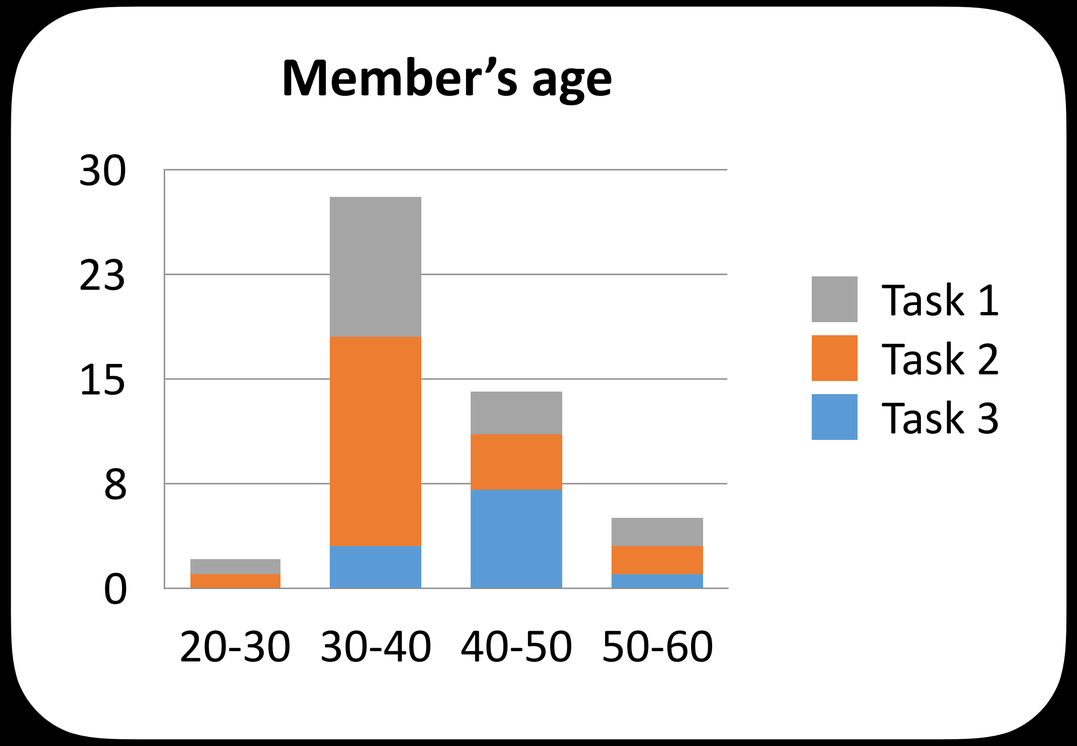
— Calorimeter: High-granularity hadronic calorimeter prototype based on Scintillator+SiPM technology

— Pixel detector: This project

Research team from China

Total members: 51, average age is 39





Pixel Task

Task 2: HEP
SDU
NJU
NWU

18 people
8 PhD, 6 Master

Task 1: IHEP

Task 3: USTC
IHEP
SJTU

Funding from MOST

	Requested M元	Granted M元	Granted M$USD
Task 1: Accelerator	10	9.74	1.5
Task 2: Pixel	12	12	1.9
Task 3: Calorimeter	10	9.71	1.5
Total	32	31.45	4.9

Additional sources of funding required

Funds do not include salaries for staff, but include a small amount for postdocs and students

MOST — Pixel project requirements

— Complete the prototype of inner silicon track detector, verify the main design indicators through test beam

- — Spatial resolution is 3-5 microns (μm);
- — Design a silicon detector with 1MRad Total ionization dose;

Interpretation of what consists a **prototype** was very much left open

Spatial resolution requirement ambiguous: point resolution, or track resolution

Vertex Detector Performance Requirements

Efficient identification of heavy quarks (b/c) and τ leptons

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\,(\mu m)$$

Intrinsic resolution of vertex detector

Resolution effects due to multiple scattering

Dominant for low-p_T tracks

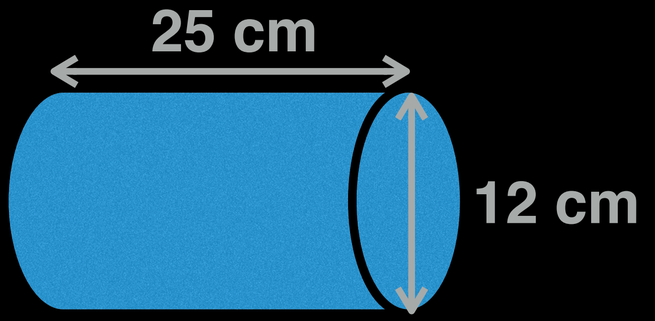
	Specs	Consequences
Single point resolution near IP:	**< 3 μm**	**High granularity**
First layer close to beam pipe:	**r ~ 1.6 cm**	
Material budget/layer:	**≤ 0.15%X_0**	**Low power consumption, < 50 mW/cm² for air cooling**
Detector occupancy:	**≤ 1%**	**High granularity and short readout time (< 20 μs)**

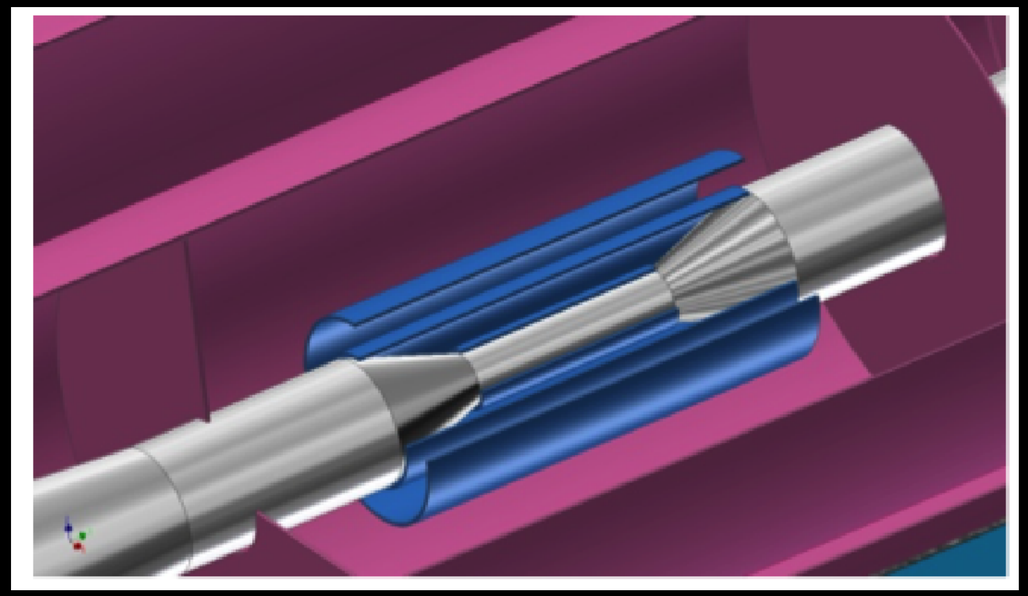
Continuous operation mode

Target: ✿ High granularity; ✿ Fast readout; ✿ Low power dissipation; ✿ Light structure

Baseline Pixel Detector Layout

3-layers of double-sided pixel sensors



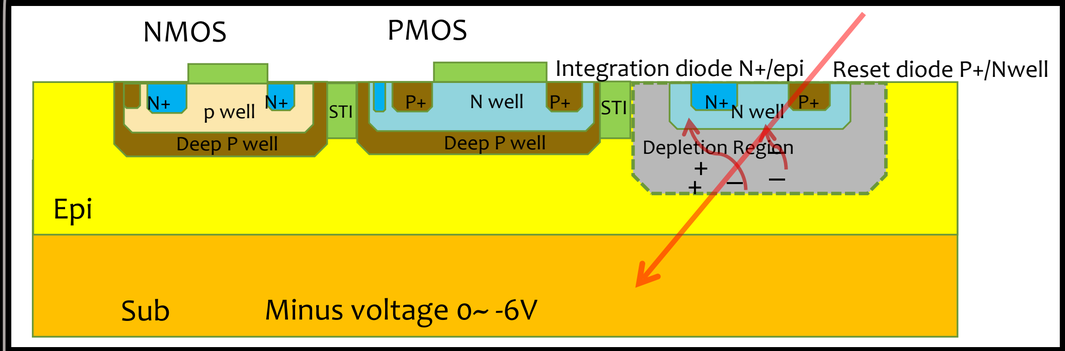


- ILD-like layout
- Innermost layer: σ_{SP} = 2.8 μm
- Polar angle θ ~ 15 degrees

Implemented in GEANT4 simulation framework (MOKKA)

		$R(mm)$	$\|z\|(mm)$	$\|cos\theta\|$	$\sigma(\mu m)$	$Readout\ time(us)$
Ladder 1	Layer 1	16	62.5	0.97	2.8	20
	Layer 2	18	62.5	0.96	6	1-10
Ladder 2	Layer 3	37	125.0	0.96	4	20
	Layer 4	39	125.0	0.95	4	20
Ladder 3	Layer 5	58	125.0	0.91	4	20
	Layer 6	60	125.0	0.90	4	20

CMOS pixel sensor (MAPS)



Integrated sensor and readout electronics on the same silicon bulk with "standard" CMOS process:
- low material budget,
- low power consumption,
- low cost …

Silicon Vertex Detector Prototype – MOST (2018–2023)

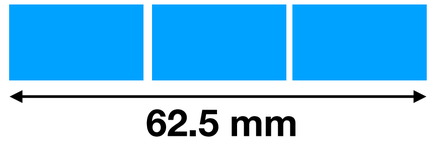
Sensor technology CMOS TowerJazz

- Design sensor with large area and high resolution
- Integration of front-end electronic on sensor chip

Benefit from MOST 1 research program

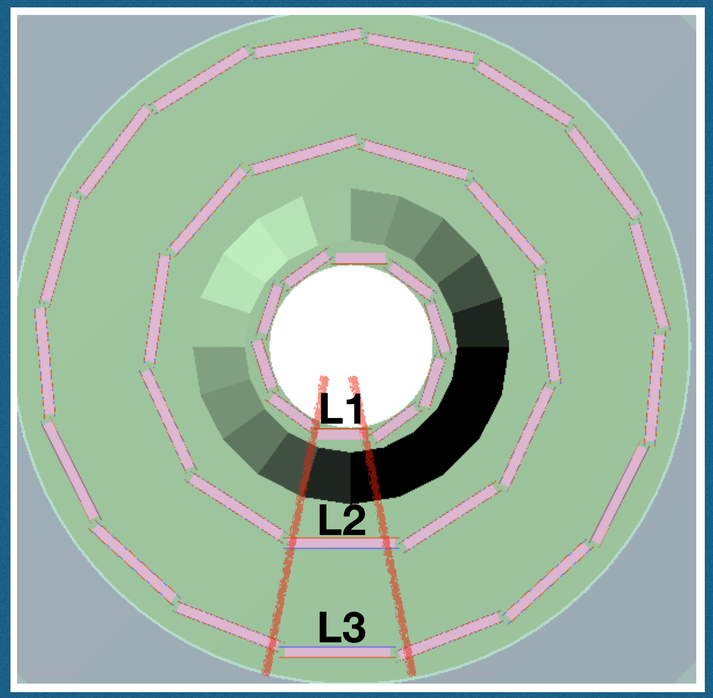
Double sided ladder

Layer 1 (11 mm x 62.5 mm)
Chip size: 11 mm X 20.8 mm



3 X 2 layer = 6 chips

3-layer sector



Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

L1
L2
L3

3-layers
same size
same chip

Goals:
1 MRad TID
3-5μm SP resolution

Integrate electronics readout

Design and produce light and rigid support structures

Silicon Vertex Detector Prototype – MOST (2018–2023)

Extended goals if manpower and technical knowledge available
Get closer to a real detector prototype

Double sided ladder

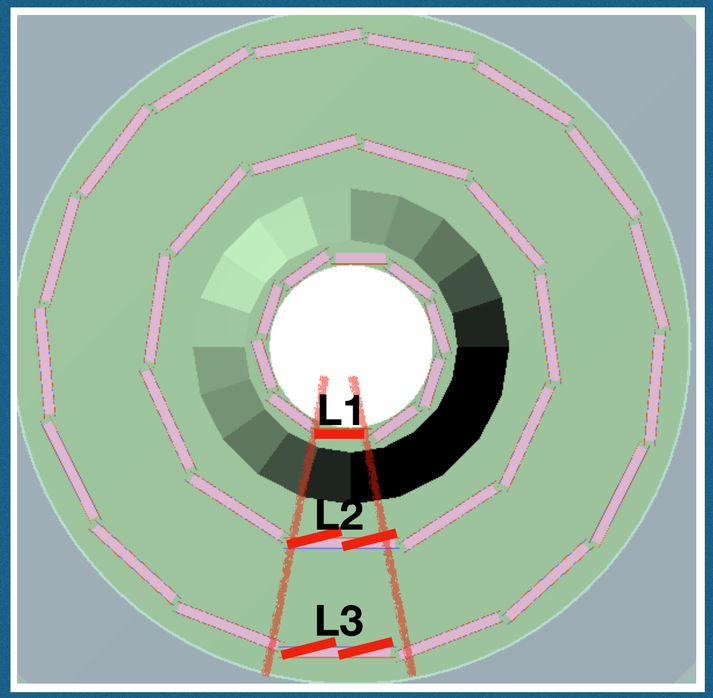
Layers 2 and 3 (22 mm x 125 mm)
Chip size: 11 mm X 20.8 mm

125 mm

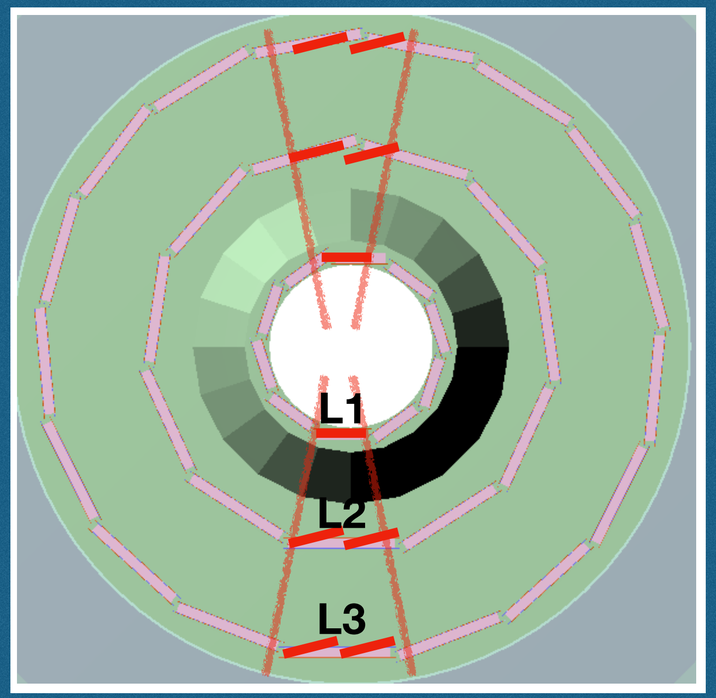
6 X 2 layer = 12 chips

3-layer sector
with multiple ladders per layer

Requires study/simulation of new layout



Full mechanical prototype
with subset of ladders instrumented/readout



International Collaboration welcome

Major Components of the Project

- Study of detector layout and mechanics ==> simulation
- CMOS sensor development (3 MPW and 1 engineering run)
- Lightweight ladder design
- Overall mechanical structure and support
  - Shipping enclosures
- MPW sensors test readout electronics
- Ladder readout electronics
- DAQ system
- Testing
  - Sensor irradiation and testing
  - Final test beam testing
- Writing documentation

Schedule — Year 1

Year	task	Assessment indicator	outcome
2018.05 | 2019.04	Task2 The mechanical support structure of the detector module and the prototype machine is preliminarily designed. The design of the front-end electronics in the sensor pixel, the preliminary design of the radiation resistance circuit device and the peripheral readout circuit of the chip are designed, and the multi project silicon wafer (MPW) flow sheet for the first sensor is submitted. The readout circuit board and data acquisition system of MPW chip are developed. In the aspect of detector system, the assembly process of detector module is formulated.	1. complete the preliminary design report of the detector module structure. 2. complete the preliminary design of the main functional modules of the sensor chip (the pixel unit of sensor and the readout module of the periphery of the chip, etc.), and complete the design report of the first sensor flow sheet	Annual report

Schedule — Year 2

2019.04 | 2020.04	Task2 The overall support structure of the detector is refined, the engineering drawing of the structure is drawn and the structure of the module is started. The first MPW chip is tested to verify its function, including the initial small dose radiation test, the integration of the pixel array and the peripheral readout circuit, and second Sub multiple wafer (MPW) wafer processing; the design of the readout electronics and data acquisition system for the detector module is started.	1. complete the preliminary design of all the functional modules on the sensor chip, and integrate the design of the functional modules to complete the design report of the second sensor chips. 2. a read-out electronics and data acquisition system for single sensor chip is developed. The first MPW chip sensor chip is tested and the test report is completed. 3. complete the preliminary design report of the readout electronics and data acquisition system of the detector module composed of multiple sensors.	Mid-term report

Schedule — Year 3

2020. 04 | 2021. 04	Task2 The structure sample of the detector module unit is processed and completed; the second MPW chip is fully tested (including a large dose of radiation test) to verify its functionality. According to the test results, the design of the peripheral digital circuit is optimized, the circuit of the front end amplifier in the pixel is corrected, the design of the radiation resistance circuit device is optimized, and the design of the function of each module is integrated, and third multiple project wafer (MPW) flow sheets are submitted and the fast verifying test is carried out after processing; the design of large area and all is designed. The functional sensor chip is prepared for large batch of engineering batch, and the data acquisition system for the read-out electronics of the whole machine system is designed.	1. the structure sample of the detector unit module is developed. 2. complete the design of the full function sensor chip and complete the design report. 3. complete the second chip test of the MPW chip and complete the test report. 4. complete the preliminary design report of the readout electronics and data acquisition system for the prototype of the detector prototype.	Annual report

Schedule — Year 4

2021. 04 | 2022. 04	Task2 At the beginning of fourth, the silicon wafer processing of large area and full function sensor chip was carried out. After the completion of the processing, the engineering batch chip was tested comprehensively. Processing the whole support structure of the detector prototype; assembling and installing the prototype of the detector; developing and debugging the data acquisition system of the prototype.	1. complete the design report of the prototype support structure of the detector prototype, and develop the whole prototype of the detector before the end of the year. 2. complete the full function sensor chip test and complete the test report. 3. develop a data acquisition system for the prototype of the detector.	Annual report

Schedule — Year 4

2022. 04 | 2023. 04	Task2 At the beginning of the fifth year, the assembly and debugging of the prototype machine were completed, the number of beam experiments were taken and the data were analyzed, and the key parameters such as the spatial resolution of the prototype machine were measured. Publish the test results and finish the task final report.	1. complete the assembly and debugging of the prototype machine. 2. through the beam experiment, the key parameters such as spatial resolution of the detector are measured. Specific indicators in accordance with the task objectives, results and assessment indicators table rules	1. final Report 2. test report and expert review and acceptance of the prototype detector. 3. paper

Project Assessment

No.	Report type	number	Submit time	public
1	Final report	1	2023.04	public
2	Annual report	3	2019.04， 2021.04，2022.04	public
3	Mid-term report	1	2020.04	public
4	CEPC detector design and test report	1	2023.04	public

EXTRA SLIDES

Silicon Tracker Detector – Baseline

CDR: Chapter 5

Not much R&D done so far

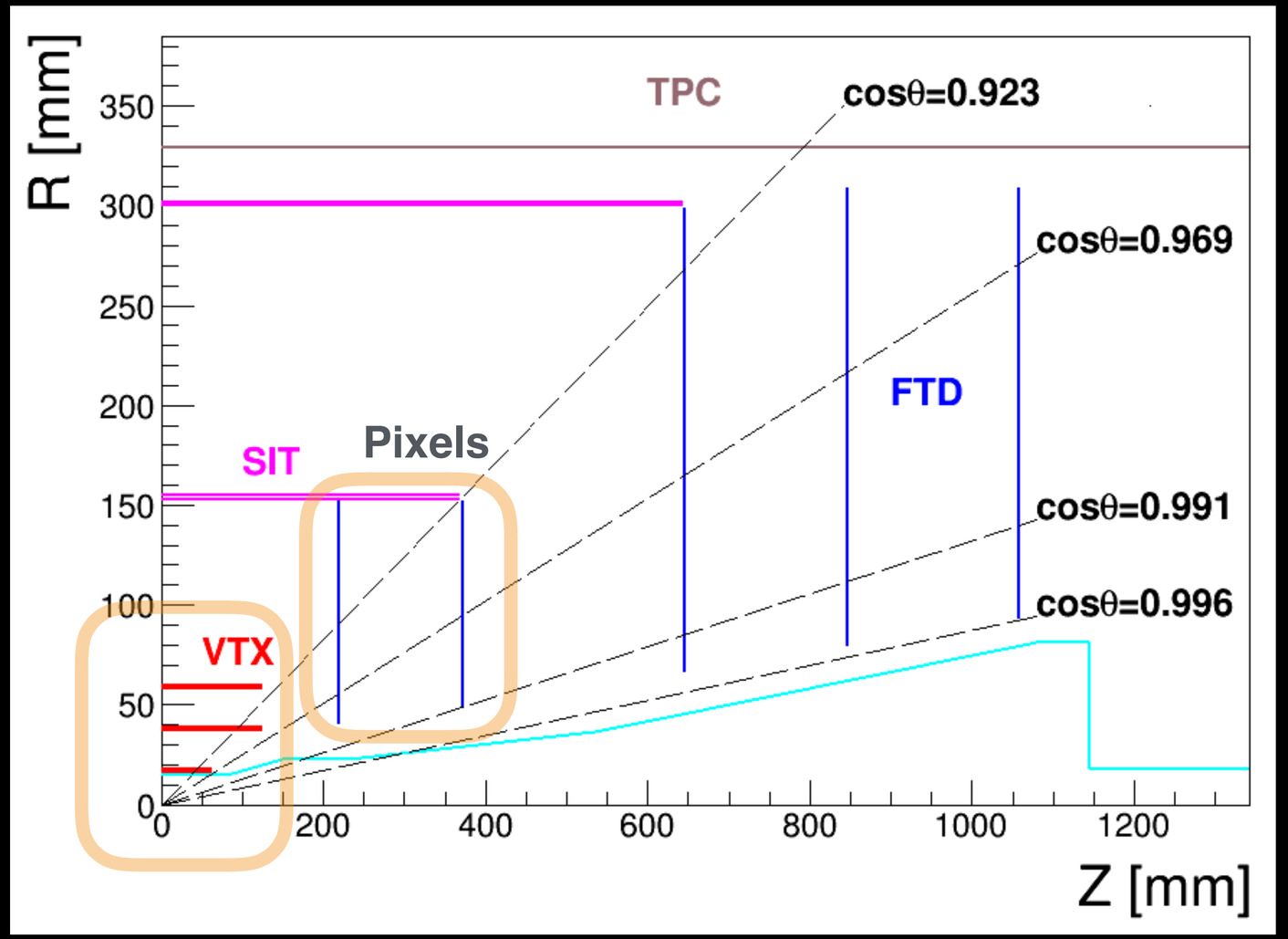
SET: r = ~1.8 m

TPC

SIT

VTX

Tracker material budget/layer: ~0.50-0.56% X/X_0

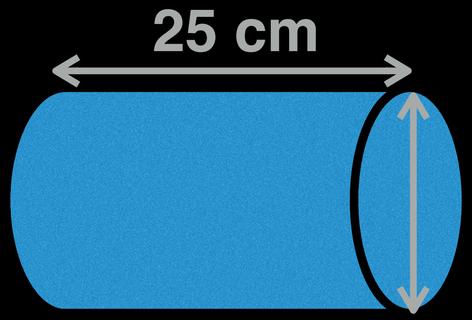


Sensor technology

1. Microstrip sensors
2. Large CMOS pixel sensors (CPS)

Power and Cooling

1. DC/DC converters
2. Investigate air cooling



ETD: z = ~2.4 m

Total Silicon area ~ 68 m^2

Beam induced backgrounds in the Vertex Detector

CDR: Chapter 10

Various sources of background studied with MC simulation:

- Radiative Bhabha scattering
- Beam-beam interactions
- Synchrotron radiation
- Beam-gas interactions

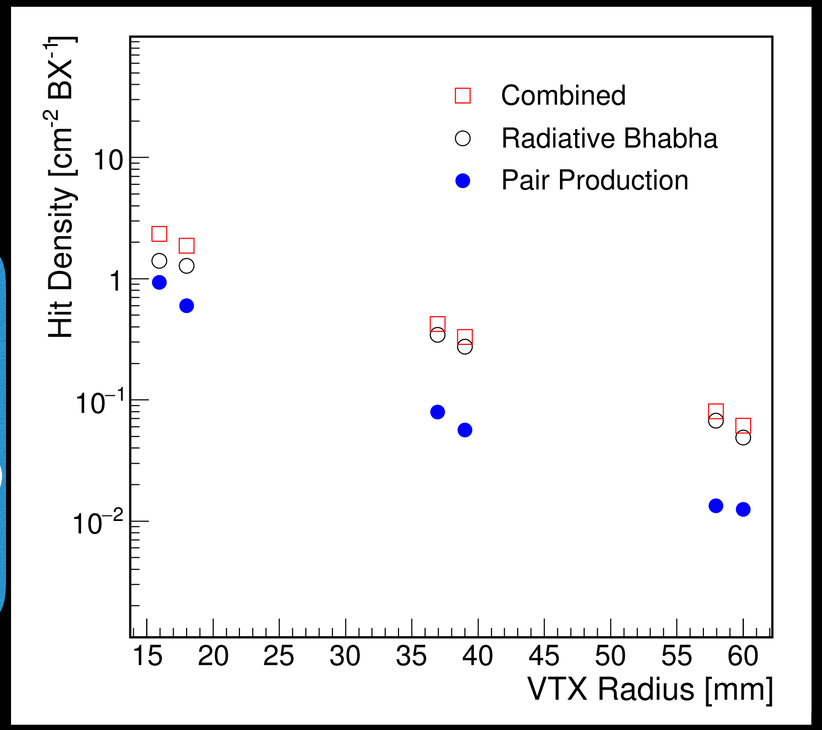
} **Studies for new configuration being finalized**

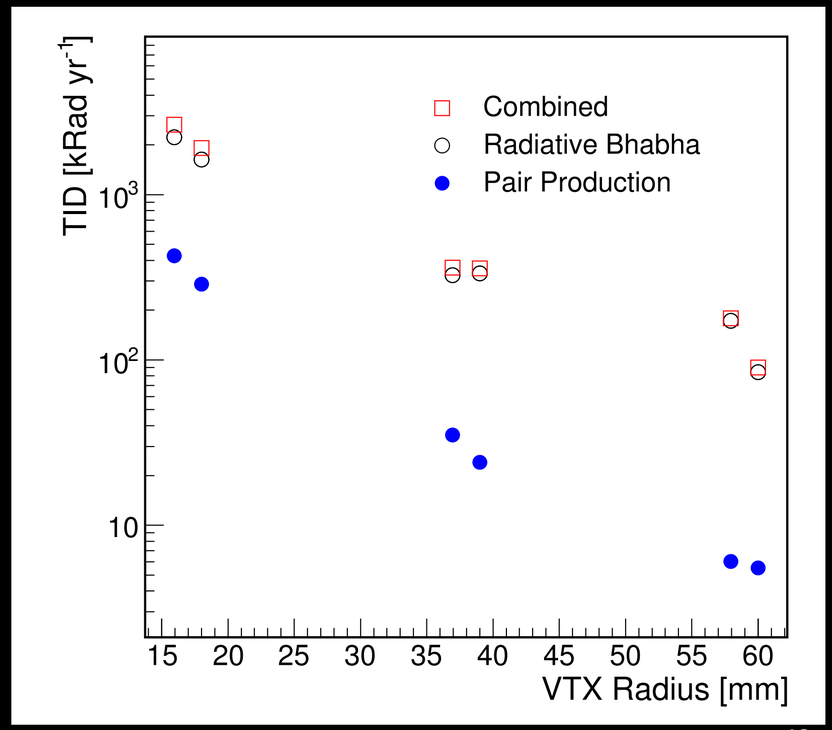
Higgs operation
(E_{cm} = 240 GeV)

Rates at the inner layer (16 mm):

Hit density: ~2.5 hits/cm²/BX
TID: 2.5 MRad/year
NIEL: 10^{12} 1MeV n_{eq}/(cm² year)

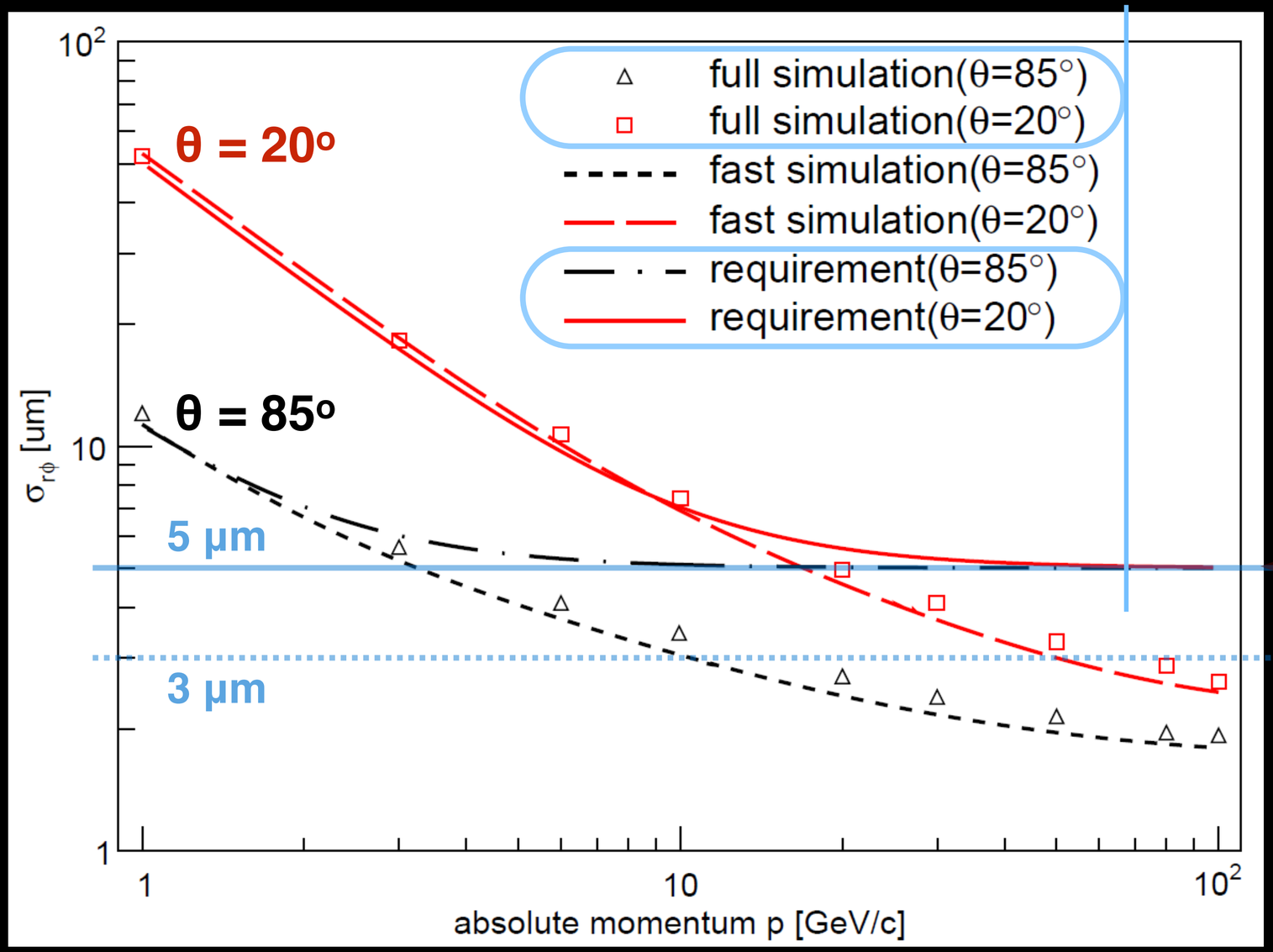
(Safety factors of 10 applied)





Performance studies: Impact parameter resolution

Transverse impact parameter resolution for single muons

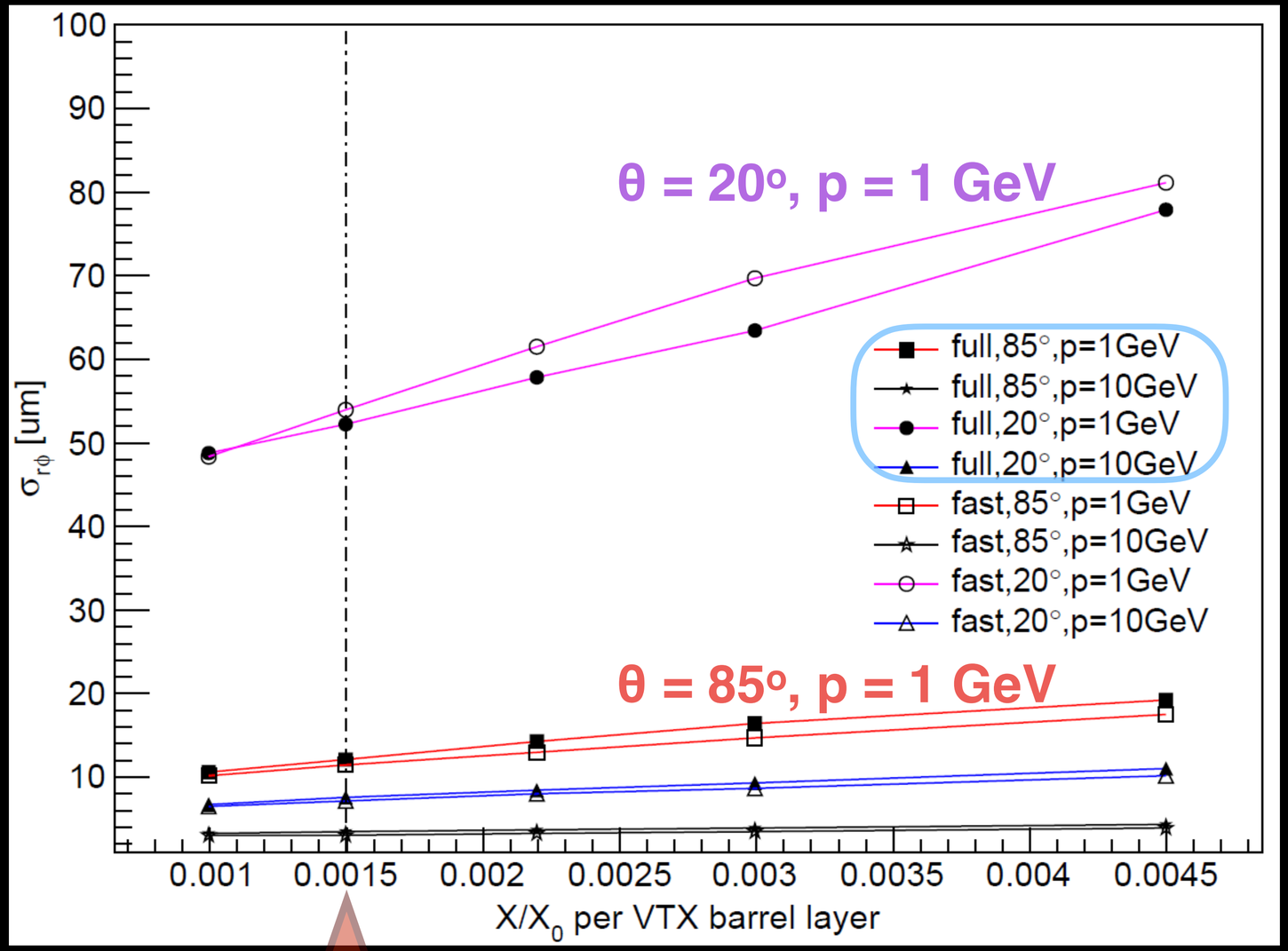


Requirement
5 μm

Impact parameter resolution goal achievable with current design

Performance studies: Material budget

Transverse impact parameter resolution for single muons



Requirement

Baseline includes very small material budget for beam pipe, sensor layers and supports ≤ 0.15%X_0

× 2 more material

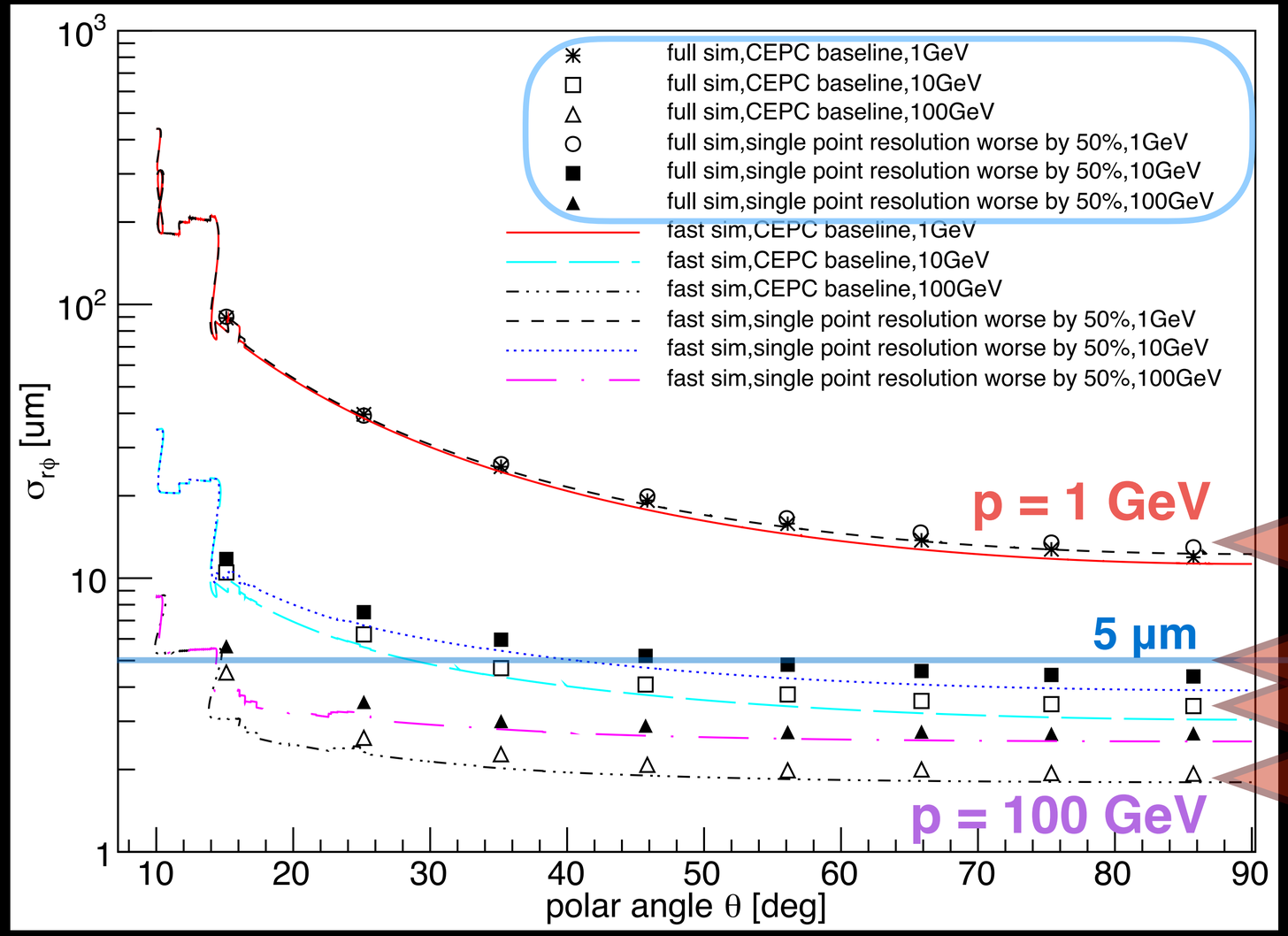
⬇

20% resolution degradation

Impact parameter resolution goal achievable but only with low material budget

Performance studies: Pixel size

Transverse impact parameter resolution for single muons



50% single point resolution degradation

⬇

50% impact parameter resolution degradation (for high-pt tracks)

Minimum degradation for low-pt tracks (dominated by multiple scattering)

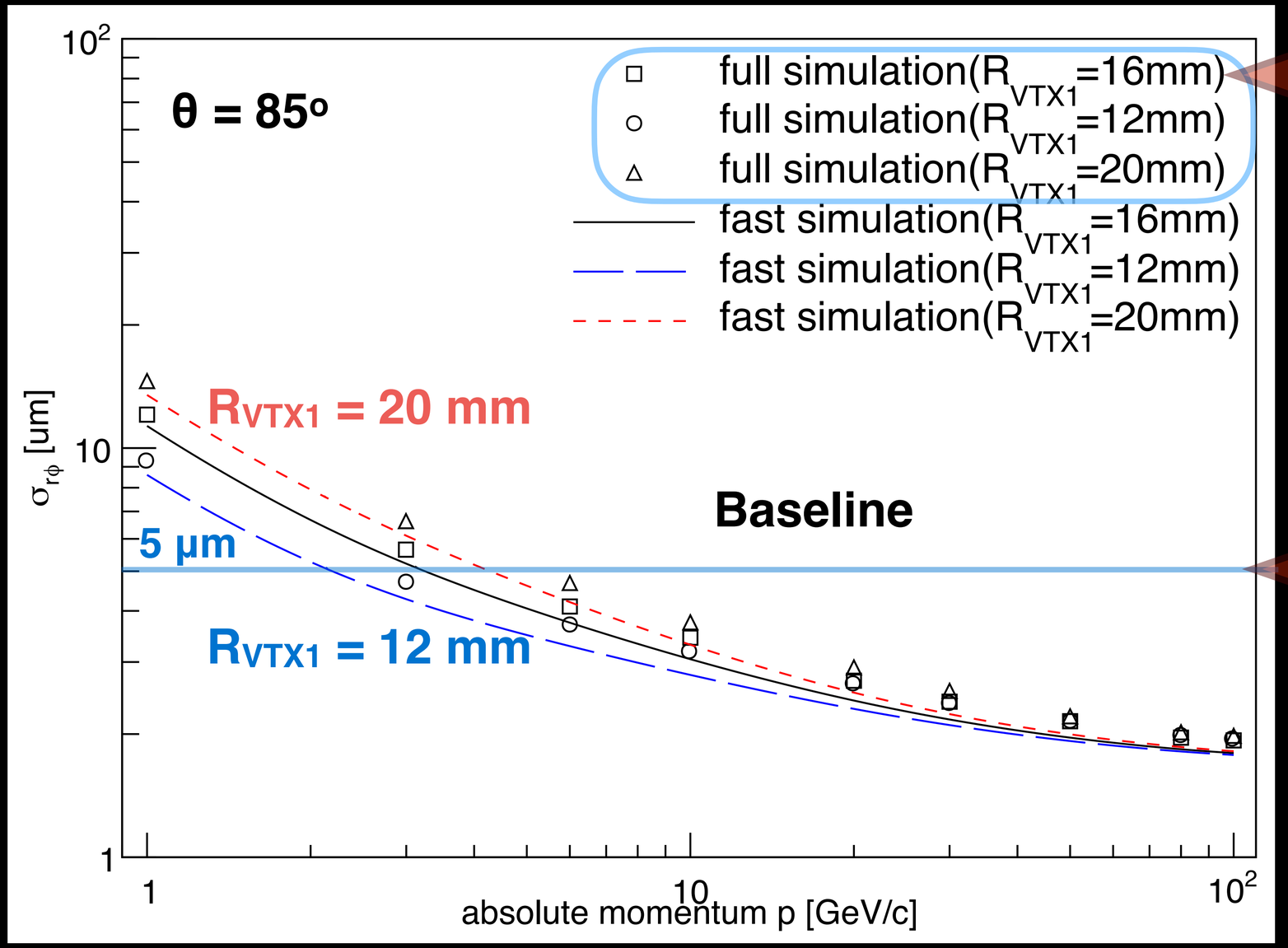
Target

Baseline **p = 10 GeV**

Baseline **p = 100 GeV**

Performance studies: Distance to IP

Transverse impact parameter resolution for single muons



Baseline

Target

Impact parameter resolution affected for low-pt tracks

Current R&D activities

- Initial sensor R&D targeting:

	Specs	Observations
Single point resolution near IP:	< 3-5 μm	Need improvement
Power consumption:	< 100 mW/cm^2	Need to continue trying to lower by a factor of 2
Integration readout time:	< 10-100 μs	Need 1 μs for final detector

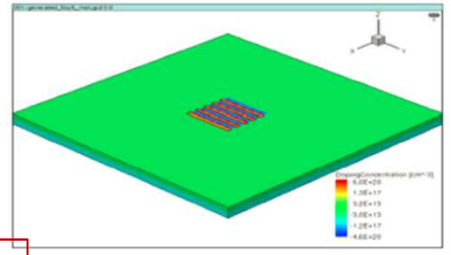
- Sensors technologies:

	Process	Observations
CMOS pixel sensor (CPS)	TowerJazz CIS 0.18 μm	Founded by MOST and IHEP
SOI pixel sensor	LAPIS 0.2 μm	Funded by NSFC

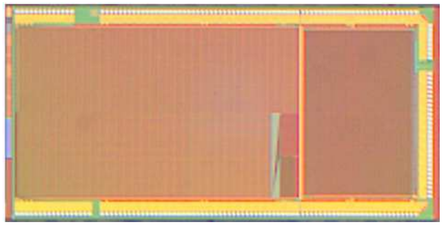
- Carry out the pixel circuit simulation and optimization, in order to achieve a CPS design with a small pixel depletion type, and try to improve the ratio between signal and noise;
- Focus on the small pixel unit design, reduce the power consumption and improve readout speed;

CMOS Pixel Sensor (CPS) R&D Activities

- **Sensor design & TCAD simulation** Y.Zhang, et al, NIMA 831(2016)99-104
  - Different sensor diode geometries, epitaxial-layer properties and radiation damage



- **First submission in Nov. 2015** Y. Zhang, Y.Zhou, et al
  - Exploratory prototype, analog pixel, rolling shutter readout mode
  - Sensor optimization and radiation tolerance study
  - sensing node AC-coupled to increase biased voltage



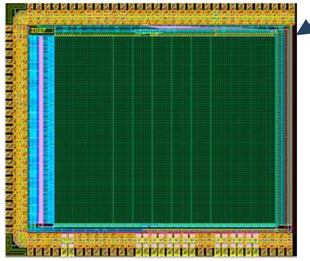
- **Second submission in May 2017**
  - Tow prototypes with digital pixels (in-pixel discriminator)
  - Tow different readout schemes: rolling shutter & asynchronous

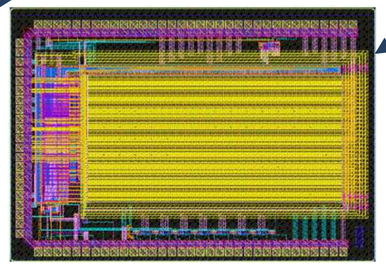
Design goals

Spatial resolution $5\ \mu m$

Integration time $< 10\ \mu s$

Power consumption $< 80 mW/cm^2$





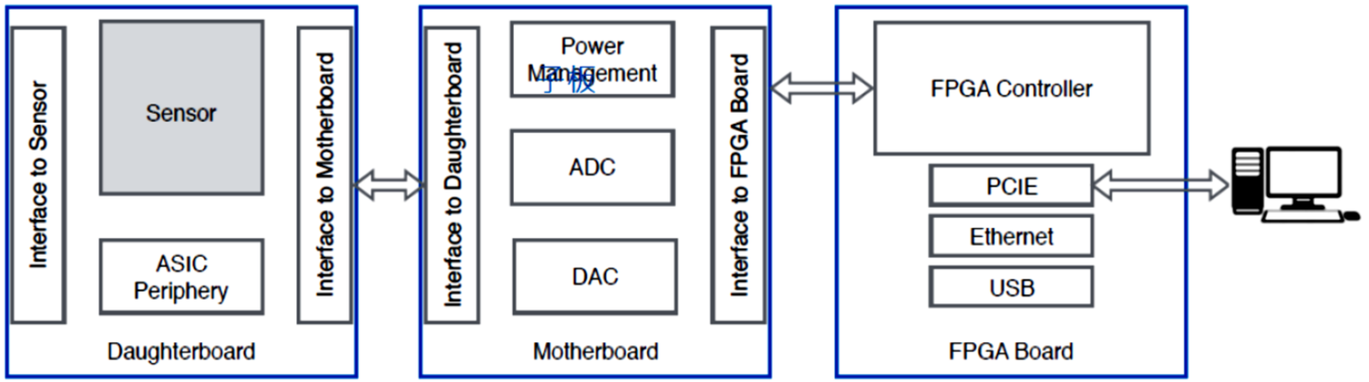
chip returned from the foundry

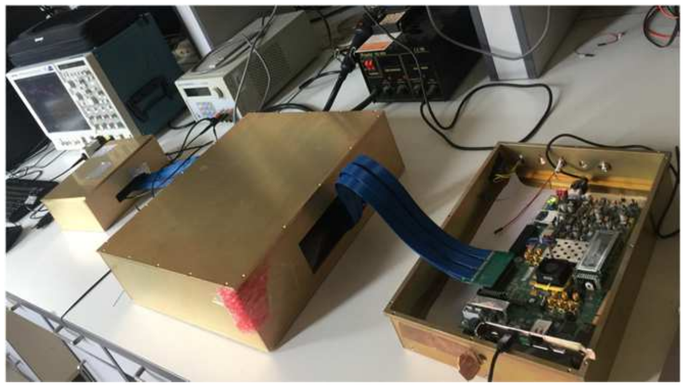
First CPS prototype characterization

- **Test system being developed**

  Prototype analog readout → Daughter-board → ADC sampling by mother-board

  - Two versions of daughter-board designed and fabricated
  - Single analog readout channel verified with oscilloscope
  - ADC debugging in progress



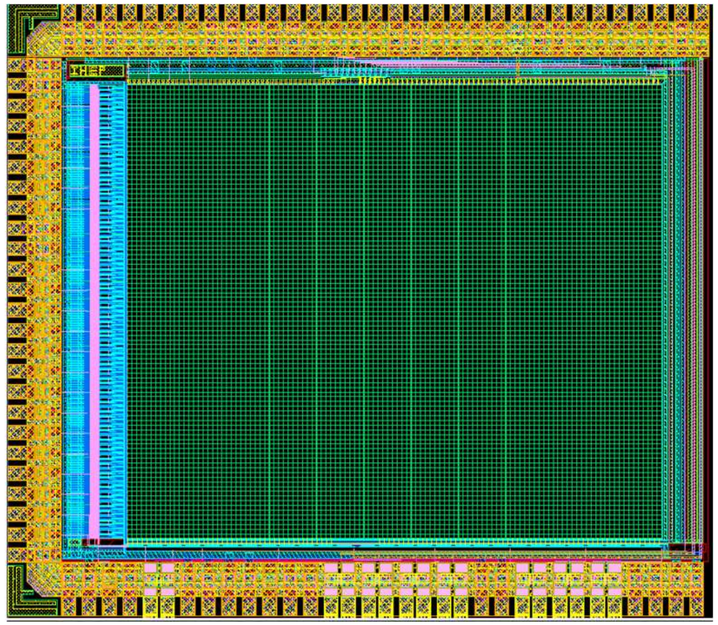


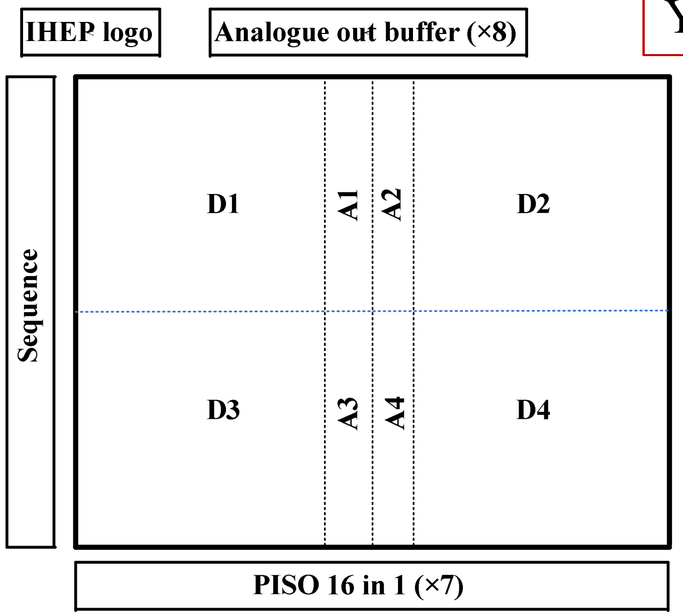
WANG Ke, WANG Na et al.

SHI Xin, Kiuchi Ryuta et al.

Second CPS submission: Rolling-shutter mode

Y. Zhou (IHEP)





Two different pixel versions:

- Pixel size: 22μm×22μm
  → 65% of ASTRAL chip
- Same amount of transistors;
- Offset cancellation technique;
- Version 2 has higher signal gain, but suffers "more" from "Latch" input voltage distortion.

Chip features:

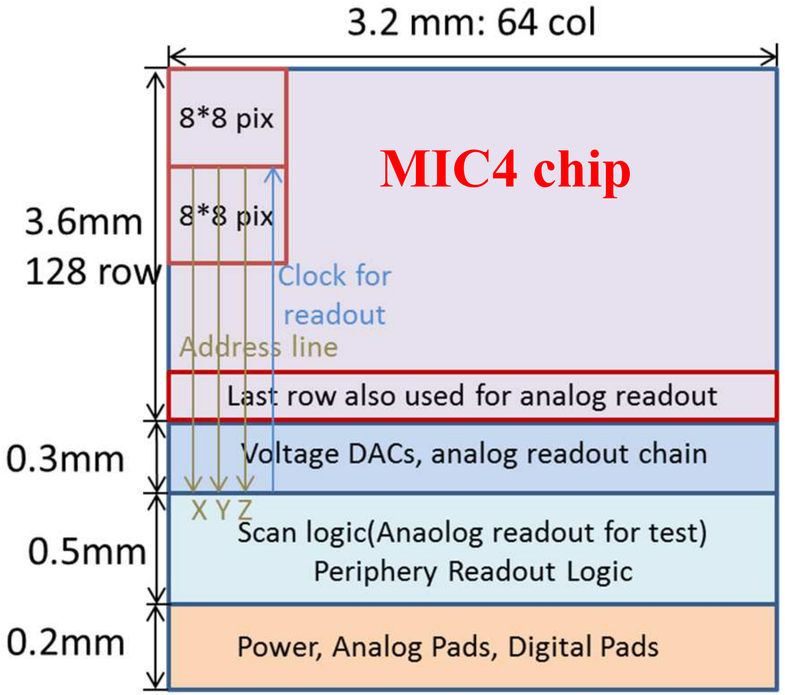
- 3×3.3 mm^2
- 96×112 pixels with 8 sub-matrix
- Processing speed: 11.2μs/frame with 100 ns/row
- Output data speed: 160 MHz
- Power: 3.7μA/pixel (14.4 mW/cm^2 @pixel matrix)

Second CPS submission: Asynchronous mode

Y. Zhang (IHEP) & P.Yang (CCNU)

front-end I: Same structure as ALPIDE chip

- ENC: 8 e^-
- Power cons.: 61 nA/pixel
- Threshold: 140 e^-
- Peaking time < 1 us
- Pulse duration < 3 μs



front-end II: CSA based front-end circuit

- Pixel size: 25 × 25 μm^2
- ENC: 24 e^-
- Power cons.: 50 nW/pixel (8 mW/cm^2 @pixel matrix)
- Threshold: 170 e^-
- Peaking time < 500 ns @ Qin < 1.5 ke^-
- Pulse duration < 9.4 μs @ Qin < 1.5 ke^-

- 3.2 × 3.7 mm^2
- 128 × 64 pixels
- Integration time: < 5 μs/10 μs
- Power consumption: < 80 mW/cm^2
- Chip periphery
  - Band gap
  - Voltage DAC
  - Current DAC
  - Matrix configuration
  - LVDS
  - Custom designed PADs

SOI pixel sensor R&D activities

- **First submission (CPV1) in June 2015**

Y. Lu (IHEP)

  - 16*16 μm with in-pixel-discrimination
  - Double-SOI process for shielding and radiation enhancement

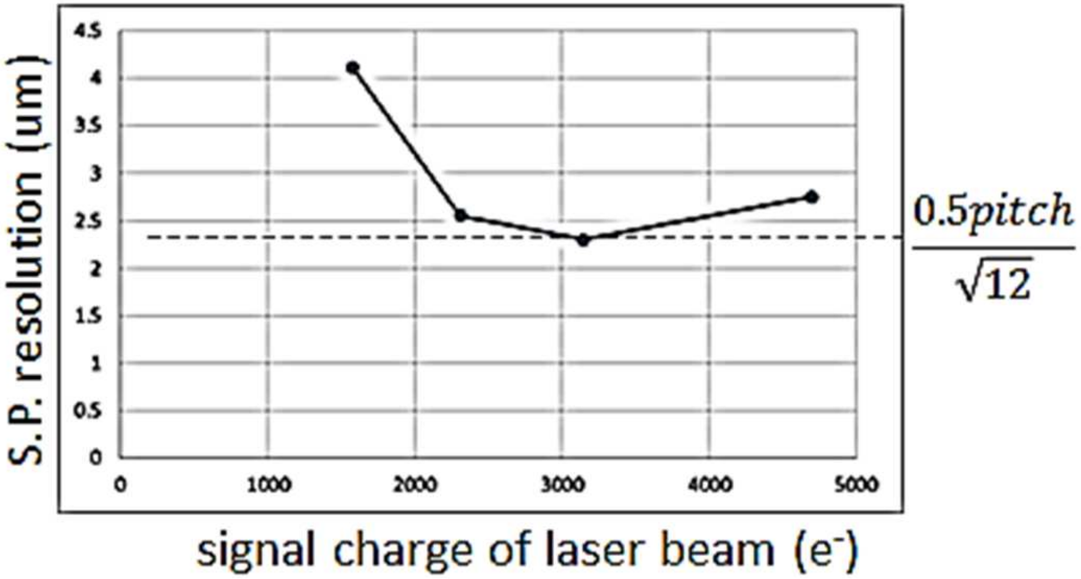
- **Second submission (CPV2) in June 2016**

Y. Lu & Y.Zhou (IHEP)

  - In-pixel CDS stage inserted
  - To improve RTC and FPN noise
  - To replace the charge injection threshold

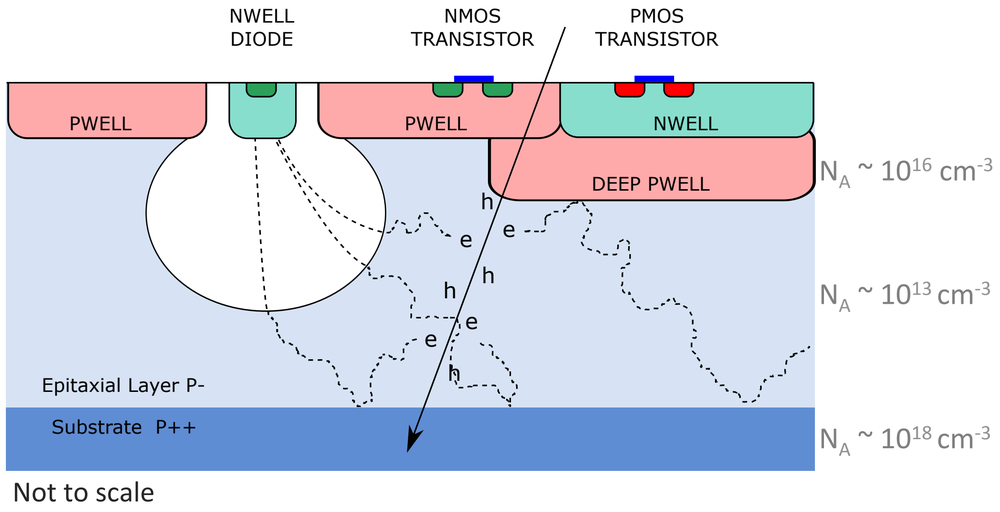
CPV2 performance

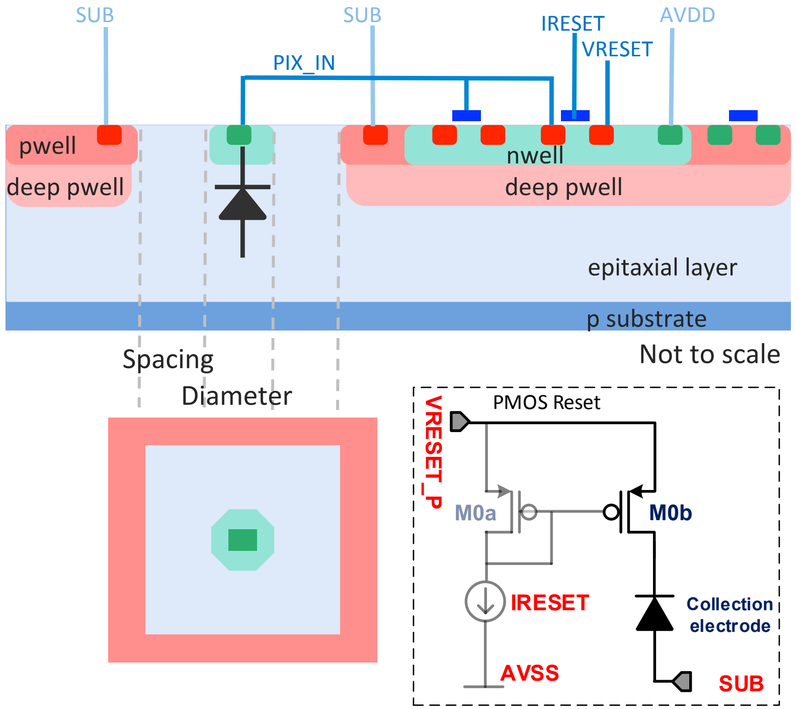
- *Thinned down to 75um thick*
- *Temporal noise ~6e$^-$*
- *Threshold dispersion (FPN) ~114e$^-$*
- *Single point resolution measurement under infrared laser beam*



Standard Pixel Sensor imaging Process (TowerJazz)

CMOS 180nm
3 nm thin gate oxide, 6 metal layers





- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18 μm to 30 μm) on p-type substrate
- Deep PWELL shielding NWELL allowing PMOS transistors (full CMOS within active area)
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (2fF) => large S/N
- Reverse bias can be applied to the substrate to increase the depletion volume around the NWELL collection diode and further reduce sensor capacitance for better analog performance at lower power

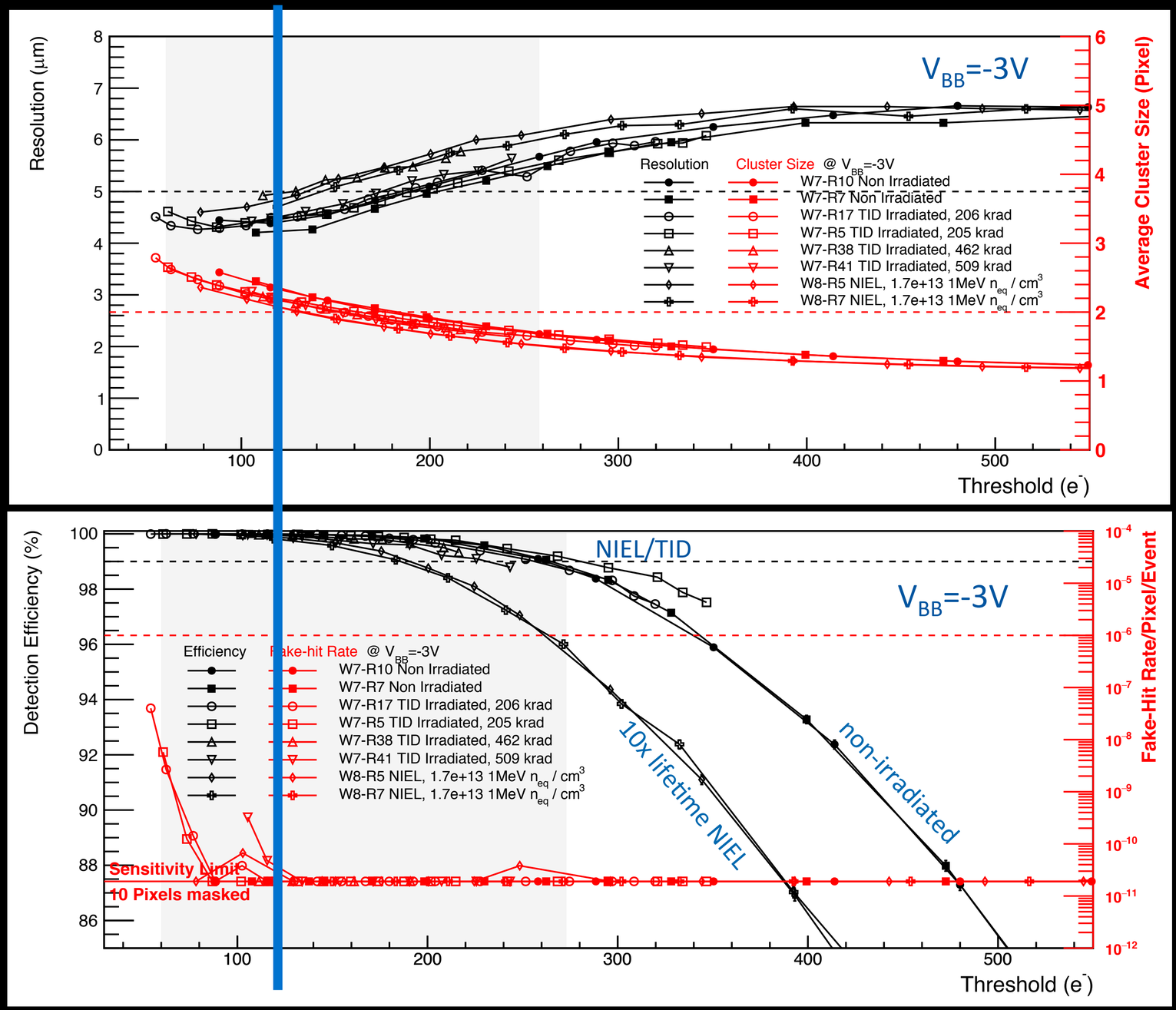
ALPIDE CMOS Pixel Sensor

	ALPIDE
Pixel dimensions	26.9 μm × 29.2 μm
Spatial resolution	~ 5 μm
Time resolution	5-10 μs
Hit rate	~ 10^4/mm^2/s
Power consumption	< ~20-35 mW/cm^2
Radiation tolerance	300kRad 2×10^{12} 1 MeV n_{eq}/cm^2

Almost OK specifications

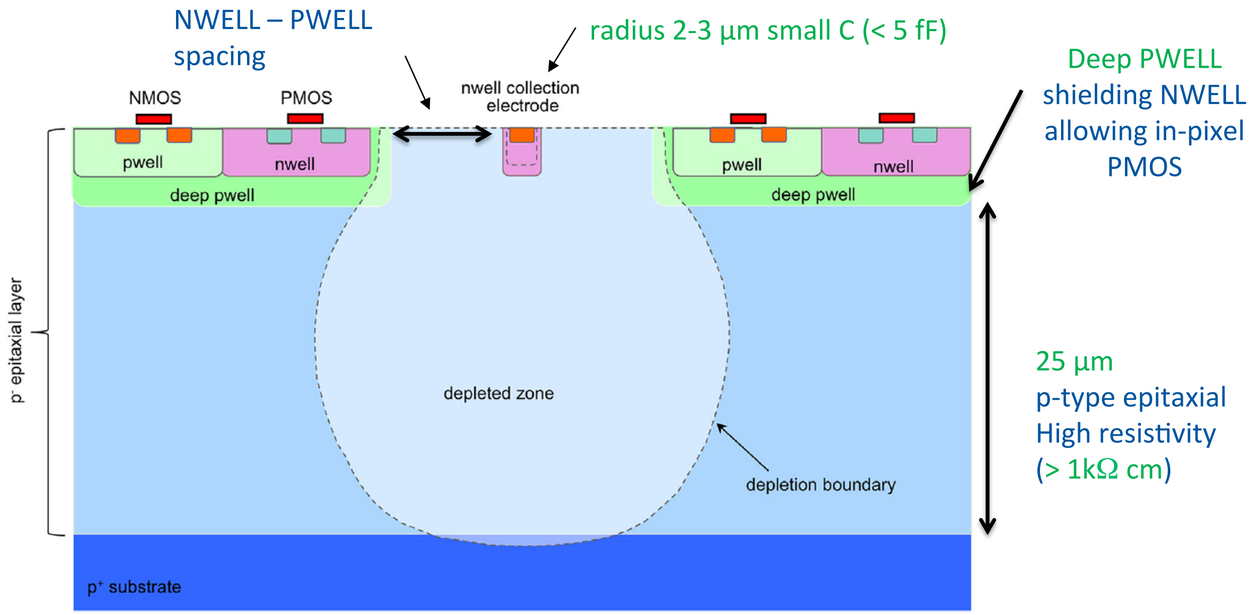
Need lower resolution

Higer radiation tolerance



ATLAS Modified TowerJazz process

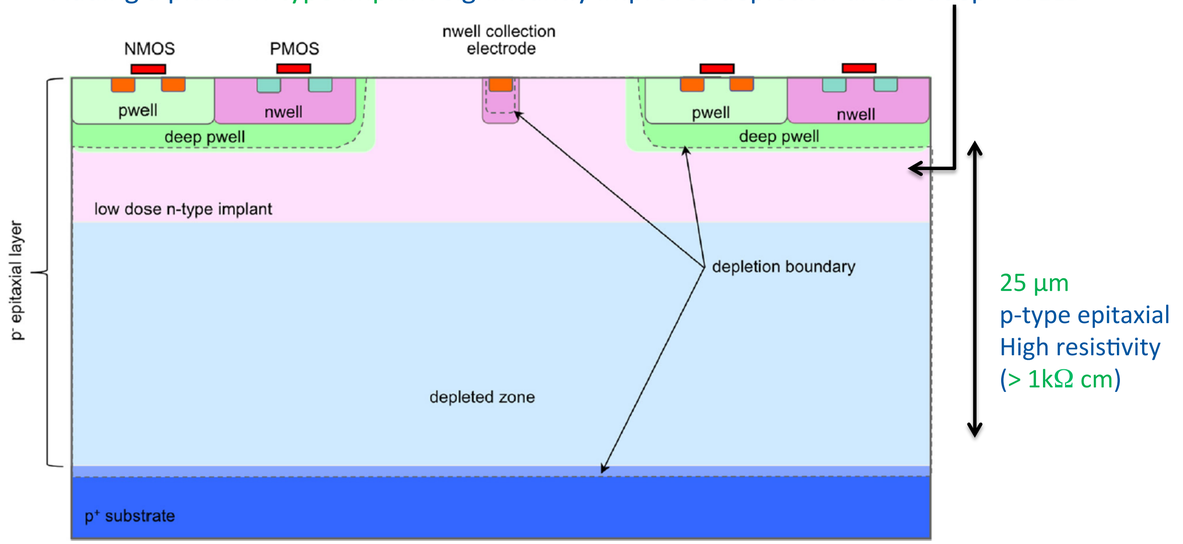
Standard process



- Reverse bias to increase depletion volume (-6 V, the sensor is not fully depleted)

Modified process

- Adding a planar n-type implant significantly improves depletion under deep PWELL



- Possibility to fully deplete sensing volume
- No significant circuit or layout changes required

W. Snoeys et al.
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Irradiation tests: 1×10^{15} n_{eq}/cm^2

Improvement of radiation tolerance by at least one order of magnitude

Ministry of Science and Technology - Funding Requests

- **MOST 1 - Funding**
  - SJTU, IHEP, THU, USTC, Huazhong Univ
  - **Silicon pixel detector ASIC chip design**
  - Time projection chamber detector
  - Electromagnetic and hadrons calorimeter
    - High-granularity ECAL
    - Large area compact HCAL
  - Large momentum range particle identification Cherenkov detector

- **MOST 2 - funding**
  - SJTU, IHEP, USTC, Shandong U., Northwestern Tech. University
  - **Pixel detector prototype**
  - Hadronic calorimeter prototype

Ministry of Science and Technology - MOST 1

- **Vertex detector**
  - Use 180 nm process
  - Carry out the pixel circuit simulation and optimization, in order to achieve a CPS design with a small pixel depletion type, and try to improve the ratio between signal and noise;
  - Focus on the small pixel unit design, reduce the power consumption and improve readout speed;
  - **Parameters:**
    - **spatial resolution to be better than 5 microns**
    - **integrated time to be 10-100 microseconds**
    - **power consumption of about 100 mW/cm^2.**