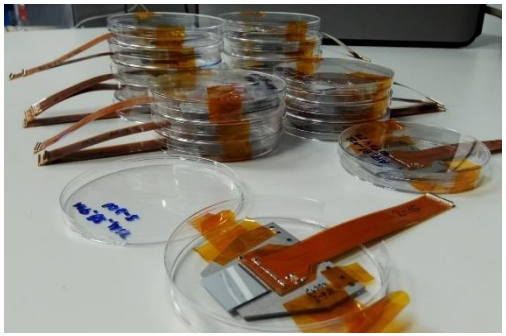
IFAE interests on MOST2

Raimon Casanova, Sebastian Grinstein

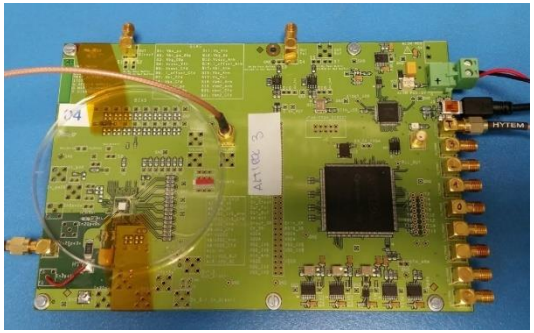
June 7, 2018

Pixels group at IFAE

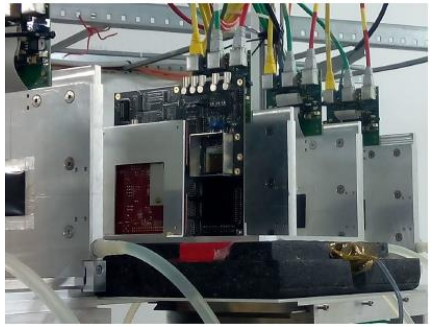
- The pixels group at IFAE is lead by Prof. **Sebastian Grinstein.**
- Strong background on pixel assembly and characterization for ATLAS:
  - **IBL:** 3D sensor technology qualification for IBL (innermost pixel layer), fabrication of 50% of sensors at CNM-Barcelona.
  - **APF:** built the ATLAS Forward Proton tracker fully at IFAE (3D sensors from CNM-Barcelona), leading role in AFP tracker installation and operation.
  - **Low Gain Avalanche Diodes (LGADS):** characterization of devices developed by CNM for the High Granularity Timing Detector (HGTD). Full module assembly in-house.
  - **3D pixels for the HL-LHC**: Qualified small pitch 3D sensors. Now baseline technology for innermost layer.
  - **R&D activities on depleted CMOS:** Participated in design of H35demo (AMS), full characterization before and after irradiation of monolithic matrices by IFAE. Investigating LFoundry.



AFP Modules (bump-bonding at IFAE)



HGTD prototype assembled at IFAE (CNM LGAD sensor)



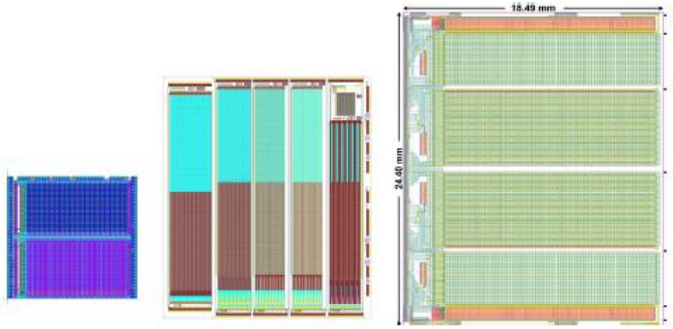
H35demo testbeam at DESY (IFAE)

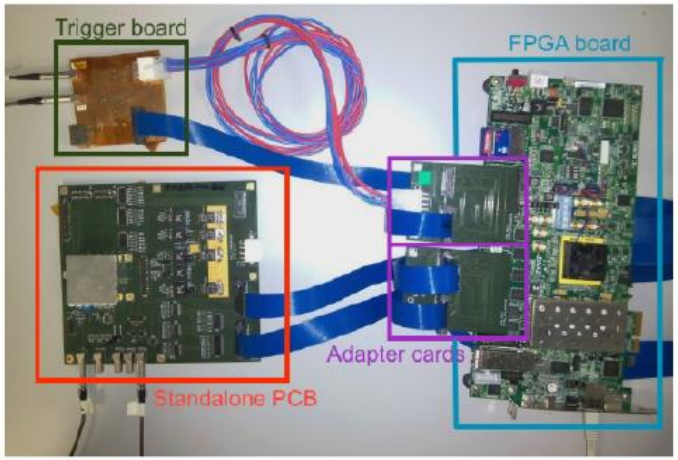
Pixels group at IFAE

- Members:
  - 3 postdocs
  - 6 Ph.D. students
  - 1 senior ASIC designer
  - 2 electronics engineers
  - 1 technician
- IFAE's workshop facilities:
  - clean rooms (class 1000 to 100000) 50m^2 + 30m^2 clean room.
  - services: chip assembly, bump bonding, wire bonding, flip-chip, device inspection, packaging systems.

ASIC design

- **ASIC team:**
  - Senior ASIC designer: Raimon Casanova
  - 1 Ph.D. student: Tinaya Wu (collaboration with CNNU)
- **Manpower:** 1.5 FTE
- IFAE is participating on monolithic pixel developments in AMS and LFoundry.
- **ASIC design experience:**
  - More than 18 years on analog/digital circuit design.
  - Technologies: 0.8µm, 0.35µm, 0.25µm, 0.18µm, 150nm, 130nm, 90nm and 65nm.
- **IFAE's interests on MOST2:** participate on the ASIC development:
  - Pixel analog/digital
  - Full chip modelling
  - Other blocks if needed (periphery)

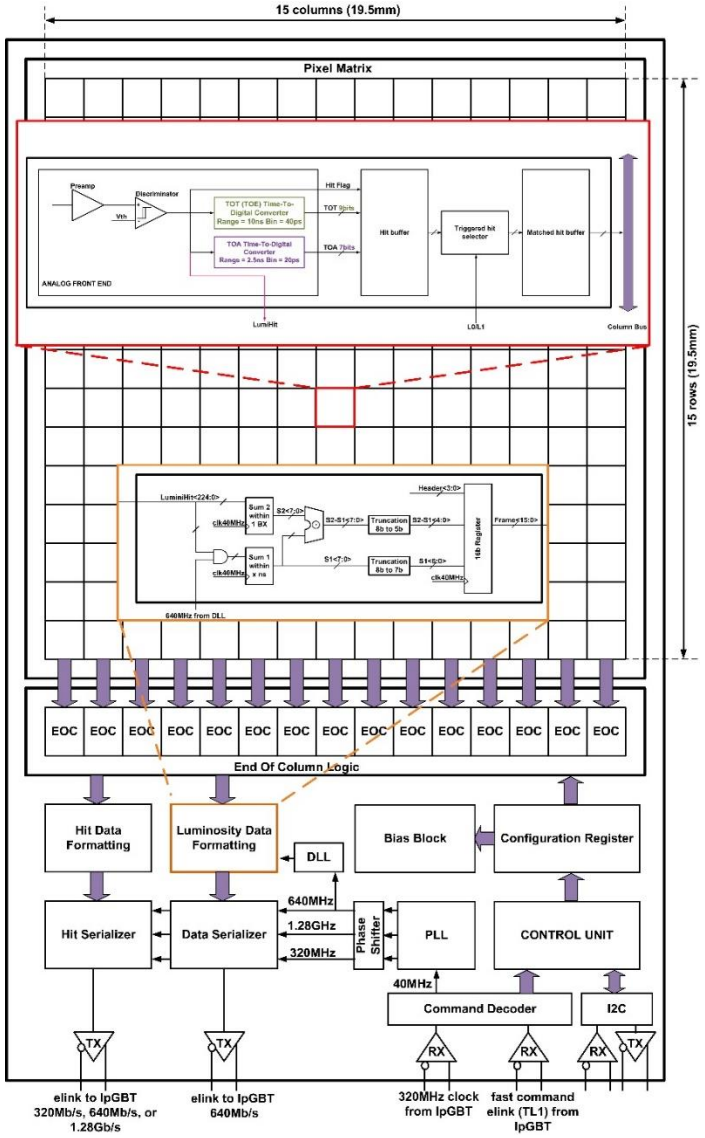




IFAE readout system

Backup slides

ALTIROC2



- ALTIROC2 chip to readout a 15 x 15 pixel matrix of LGADs.
- 130nm CMOS process
- IFAE's contribution: digital electronics + verification

ALTIROC2's UVM verification environment