MOST project midterm review

Development of Low power front-end ASIC for CEPC-TPC

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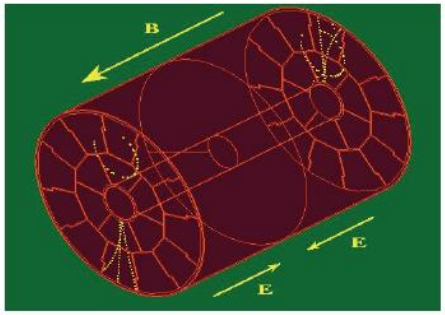
Outlines

- Introduction
- Progress
  - Analog front-end
  - SAR ADC
- Summary and future plan

CEPC-TPC

- Time projection chamber: main tracker for CEPC



Momentum resolution at B=3.5T	$\delta(1/pt) \approx 10^{-4}$/GeV/c TPC only
δ_{point} in rΦ	<100μm (avg for straight-radial tracks)
δ_{point} in rz	≈0.4~1.4mm (for zero – full drift)
Inner radius	329mm
Outer radius	1800mm
Half length	2350mm
TPC material budgt	≈0.05X_0 including the outer field cage in r <0.25X_0 for readout endcaps in z
Pad pitch/no. padrows	≈1mm×4~10mm/≈200
2-hits resolution in rΦ	≈2mm (for straight-radial tracks)
Performance	>97% efficiency for TPC only (pt > 1GeV/c) >99% all tracking (pt > 1GeV/c)

- Requirement for the front-end electronics
  - Analog front-end, including preamplifier and shaper
  - Waveform sampling ADC in 10b and 20-40MSPS
  - Continuous working, no power pulsing ⟹ Low power consumption

Total number of channels		**~1 Million per endcap**
AFE	ENC	500 e
	Gain	10 mV/fC
	Peaking time	160 ns
ADC	Sampling rate	20-40 MSPS
	Resolution	10 bit
Buffer latency		~50 μs
Data readout rate		20 Gb per event w.o. zero compression
Power consumption		<10 mW per channel
Area		< 6 mm^2 per channel, incl. cooling

- Current TPC readout ASICs

	PASA/ALTRO	AFTER	Super-ALTRO	SAMPA
TPC	ALICE	T2K	ILC	ALICE upgrade
Pad size	4x7.5 mm^2	6.9x9.7 mm^2	1x6 mm^2	4x7.5 mm^2
Pad channels	5.7 x 10^5	1.25 x 10^5	1-2 x 10^6	5.7 x 10^5
Readout Chamber	MWPC	MicroMegas	GEM/MicroMegas	GEM
Analog Front-end				
Gain	12mV/fC	18 mV/fC	12-27 mV/fC	20/30 mV/fC
Shaper	CR-$(RC)^4$	CR-$(RC)^2$	CR-$(RC)^4$	CR-$(RC)^4$
Peaking time	200 ns	100 ns	30-120 ns	80/160 ns
ENC	385 e	1000 e	520 e	482 e @ 180ns
Waveform Sampler				
Method	ADC	SCA	ADC	ADC
Sampling frequency	10MSPS	25MSPS	40MSPS	20MSPS
Dynamic range	10bit	10bit	10bit	10bit
Power consumption	32mW/ch	6.2-7.5mW/ch	47.3mW/ch	8mW/ch
CMOS Process	250 nm	350 nm	130 nm	130nm

The CEPC MOST Project

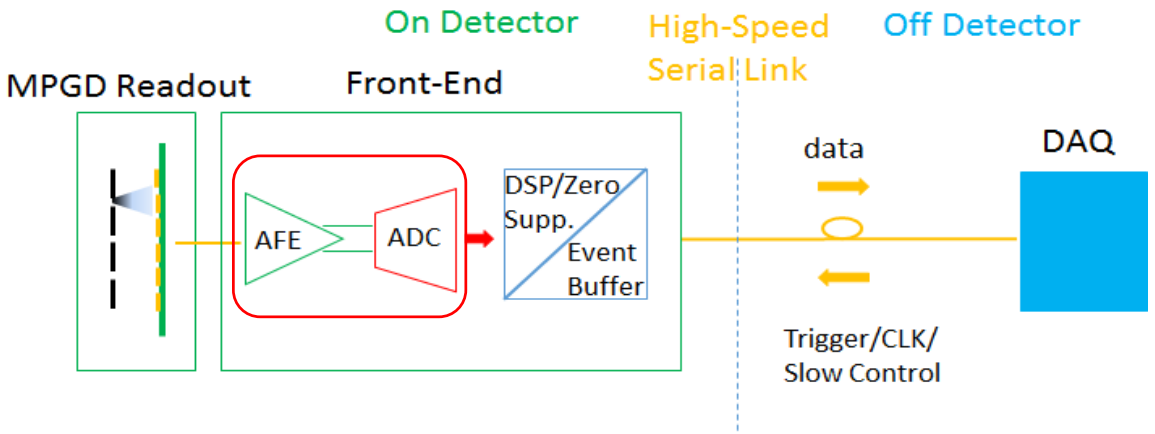
- R&D on key detector technologies
- PI: Haijun Yang
- Duration: 2016/7 – 2021/6
- Total Budget: 15.28M, 1.6M for TPC readout ASIC

国家重点研发计划
课题任务书

课题名称：	探测器关键技术预研
所属项目：	高能环形正负电子对撞机相关的物理和关键技术预研究
所属专项：	大科学装置前沿研究
项目牵头承担单位：	清华大学
课题承担单位：	上海交通大学
课题负责人：	杨海军
执行期限：	2016 年 07 月 至 2021 年 06 月

Objective

- Develop a low power and highly integration front-end ASIC in 65 nm CMOS
- Each channel consists of the analog front-end (AFE) and a SAR ADC in 10b and up to 40 MSPS
- Less than 5 mW per channel

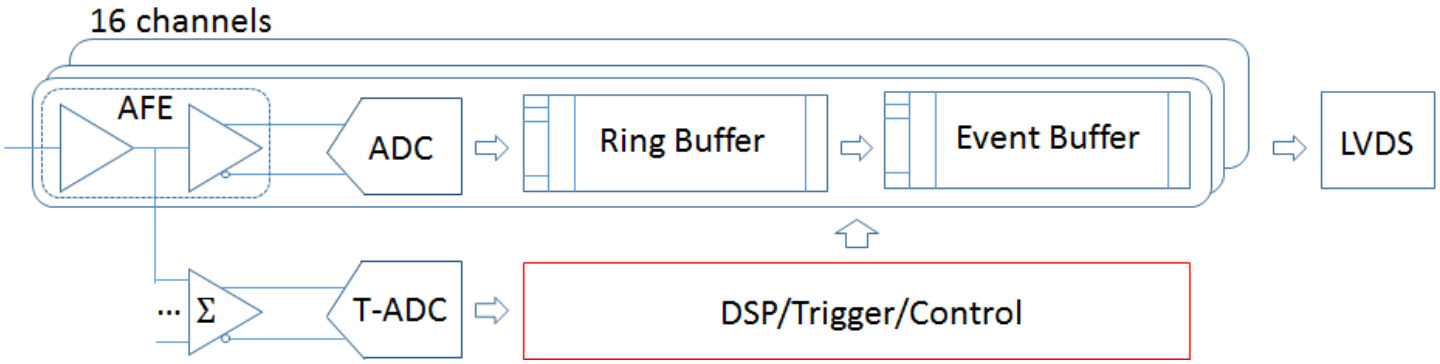


Group members

- ASIC designers:
  - TU-DEP: Zhi Deng, Wei Liu, Feng Liu, Xinyuan Zhao
  - TU-IME: Fule Li, Xian Gu (graduated)
- Other people involved:
  - IHEP: Huirong Qi's group (Spec.)
  - TU-DEP: Yulan Li (Spec.), Hui Gong(DAQ and testing), Yuyan Huang

Progress: Architecture

- The first phase supported by the MOST project is to develop a 16 channel front-end TPC readout ASIC
- Three prototype chips will be designed for the first MPW run:
  - Analog Front-end: 3-5 channels of CSA+CR-RC shaper
  - Single channel low power SAR-ADC
  - 3 channels of AFE+ADC

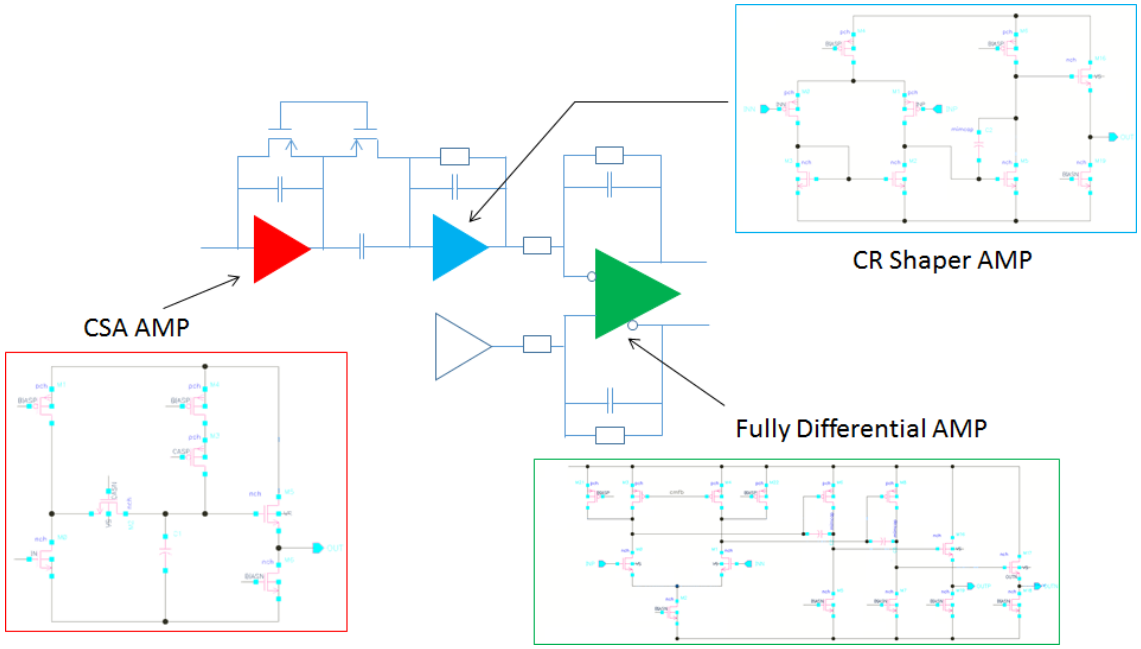


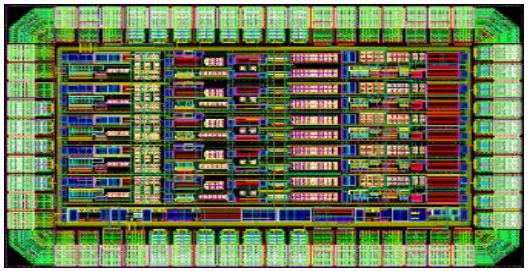
Progress: Specifications

AFE	
Signal Polarity	Negative
Detector Capacitance	5-20 pF
Shaper	CR-RC
Shaping Time	160 ns
ENC (Equivalent Noise Charge)	<500 e @ 10pF
Dynamic Range	120 fC
Gain	10 mV/fC
INL (Integrated Non-Linearity)	<1%
Crosstalk	<1%
Power Consumption (AFE)	<2.5 mW/ch
ADC	
Input Range	-0.6V ~ 0.6V diff.
Resolution	10 bit
Sampling Rate	40 MSPS
DNL	<0.65 LSB
INL	<0.6 LSB
ENOB	>9 bit @ 2MHz
Power Consumption (ADC)	<2.5 mW/ch
Process	65 nm CMOS

Progress: AFE chip

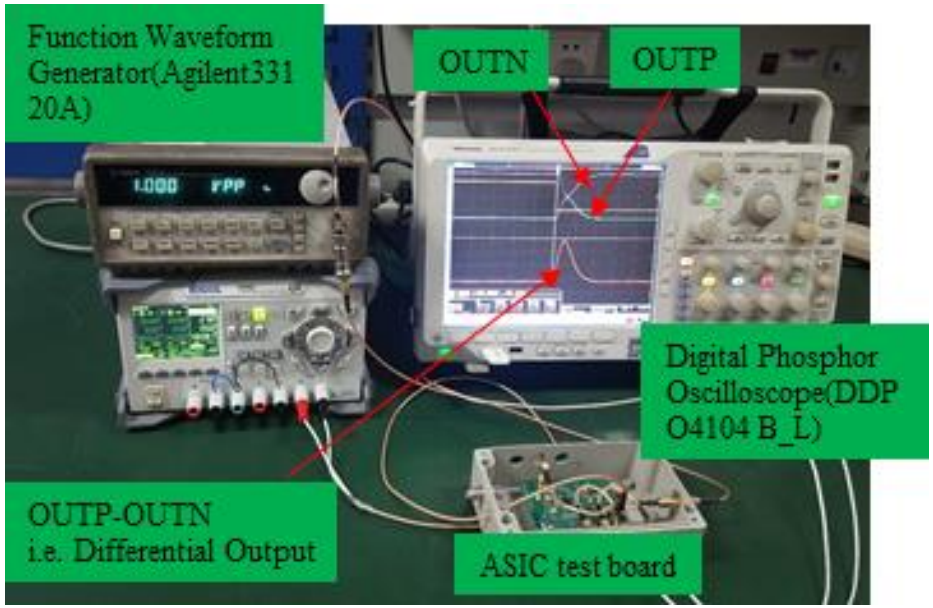
- Schematics and layout

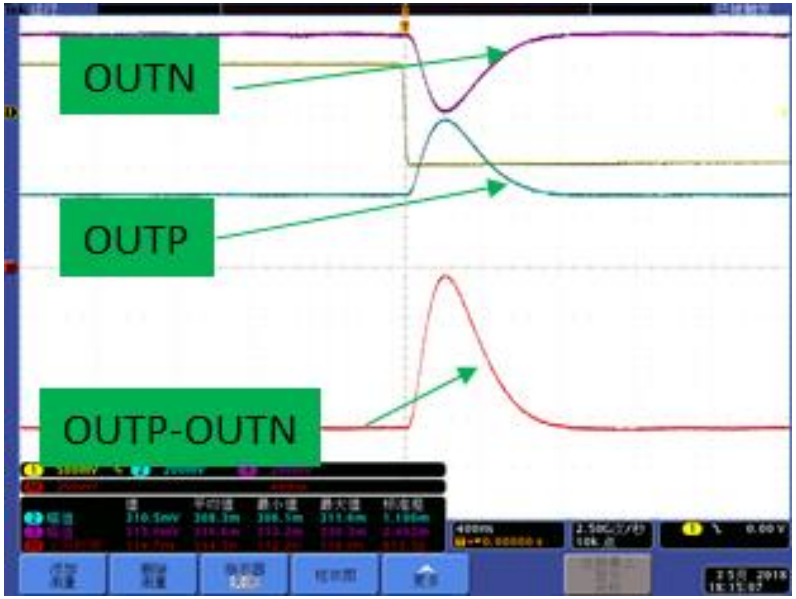




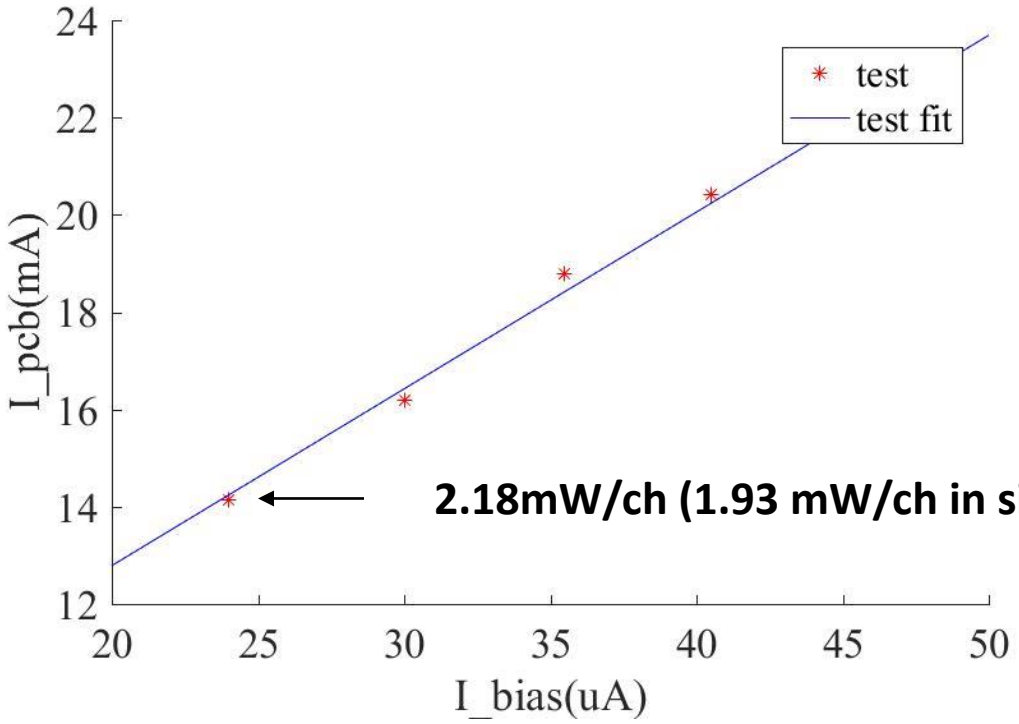
1320um x 838um

- Test results: setup and transients



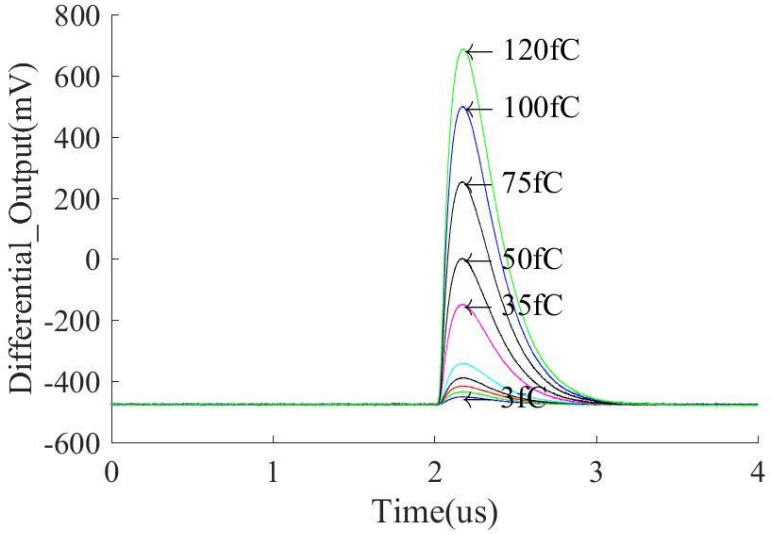


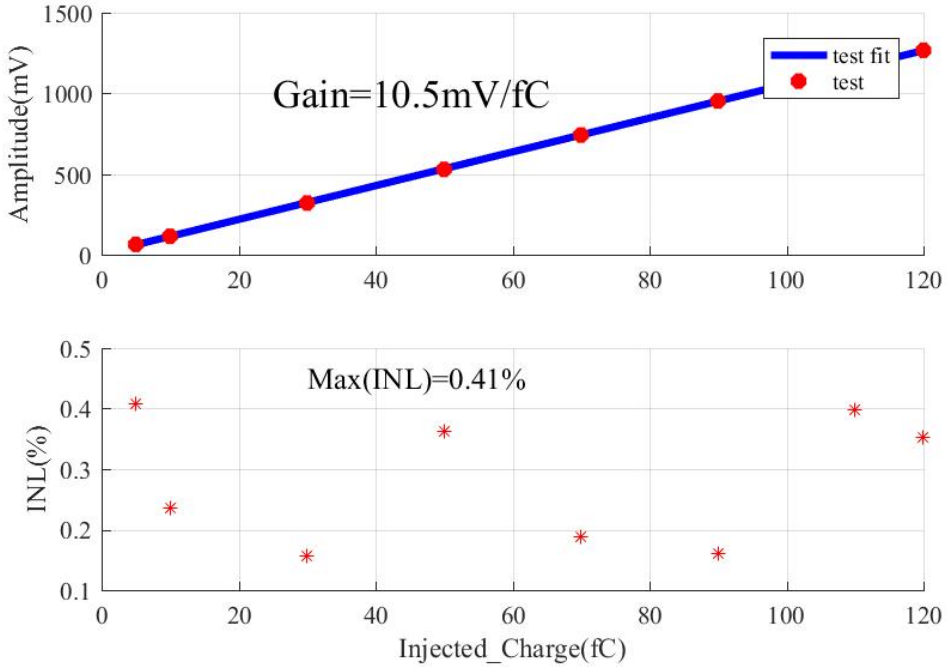
- Power consumption



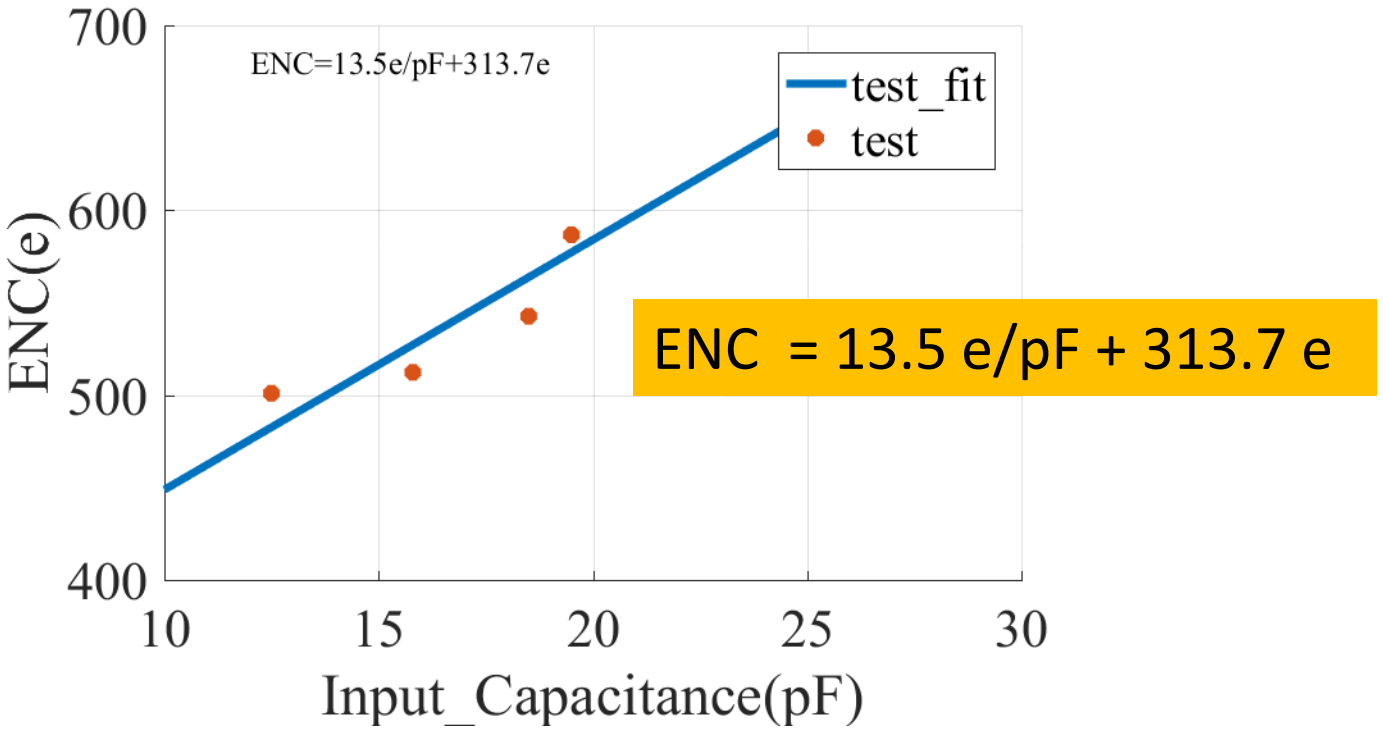
2.18mW/ch (1.93 mW/ch in simulation)

- Linearity


Differential_Output(mV)
Time(us)
120fC
100fC
75fC
50fC
35fC
3fC


Amplitude(mV)
Gain=10.5mV/fC
test fit
test
INL(%)
Max(INL)=0.41%
Injected_Charge(fC)

- ENC noise



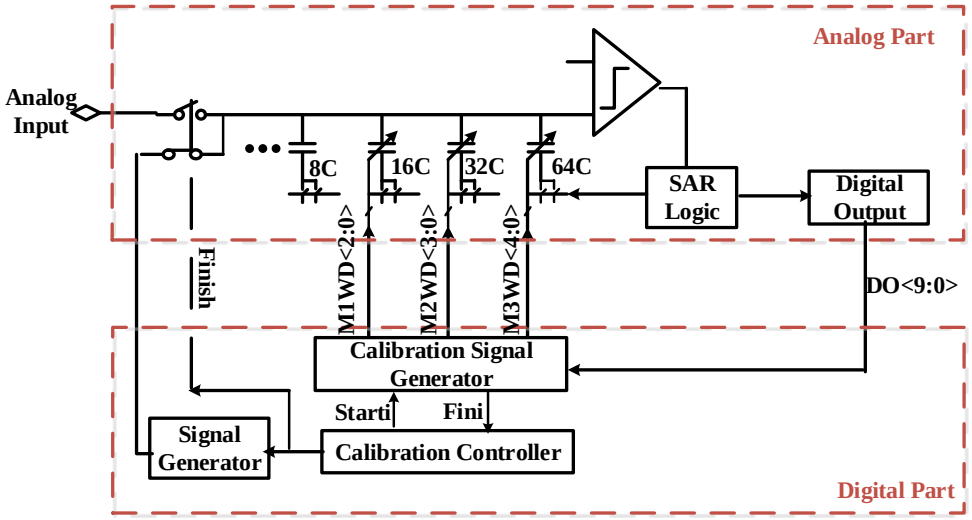
ENC = 13.5 e/pF + 313.7 e

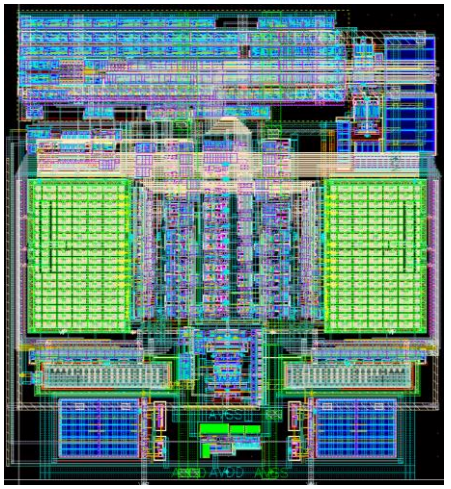
- AFE test summary

	Specifications	Test Results
Gain	10mV/fC	10.5mV/fC
Dynamic Range	120fC	>120fC
INL	<1%	0.41%
Power consumption	2.50mW/ch	2.18mW/ch
ENC	500e @ 10pF	448e @ 10pF
Xtalk	<1%	<0.36%

Progress: SAR ADC

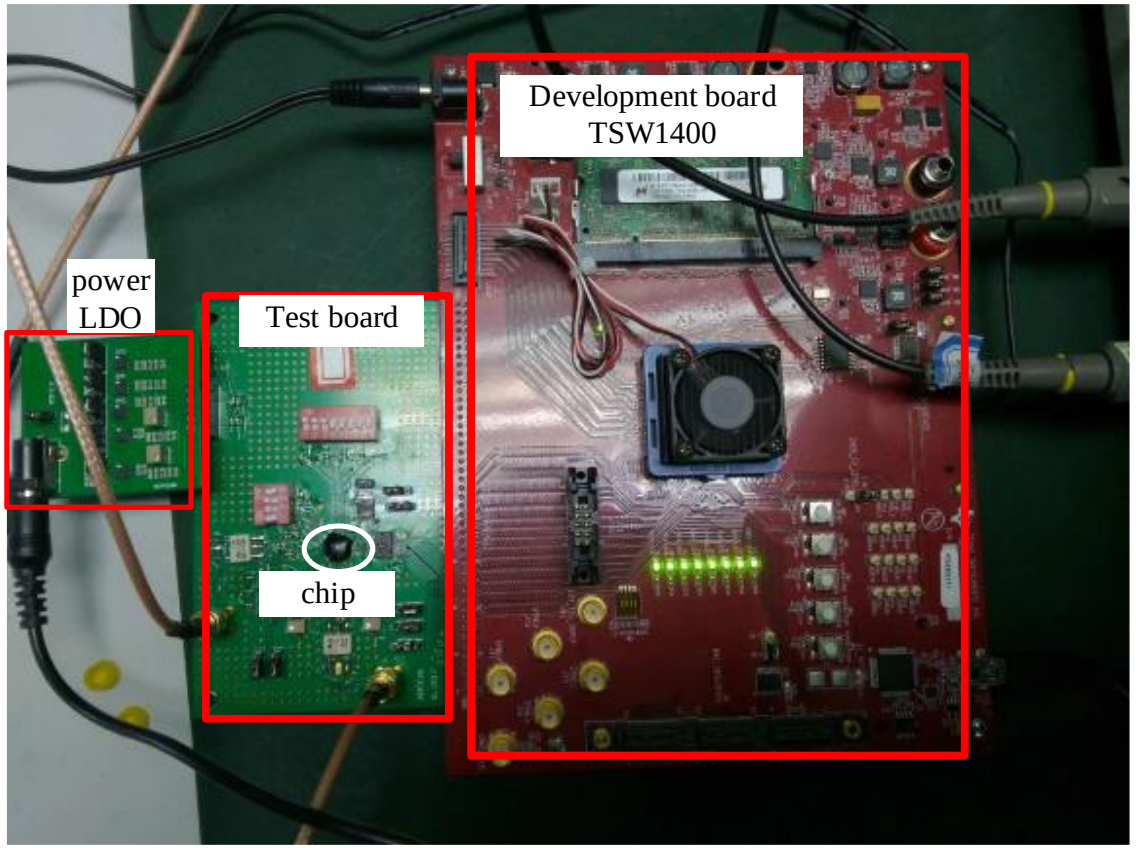
- Schematics and layout





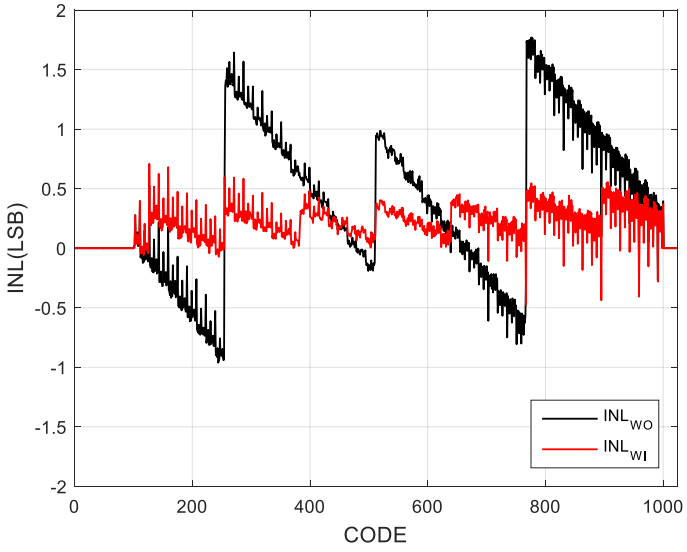
90um x 97um

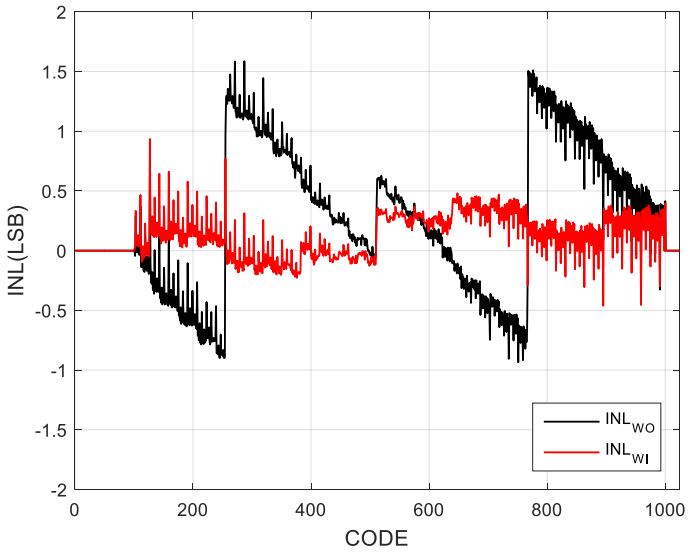
- Test setup
  - TSW1400EVM



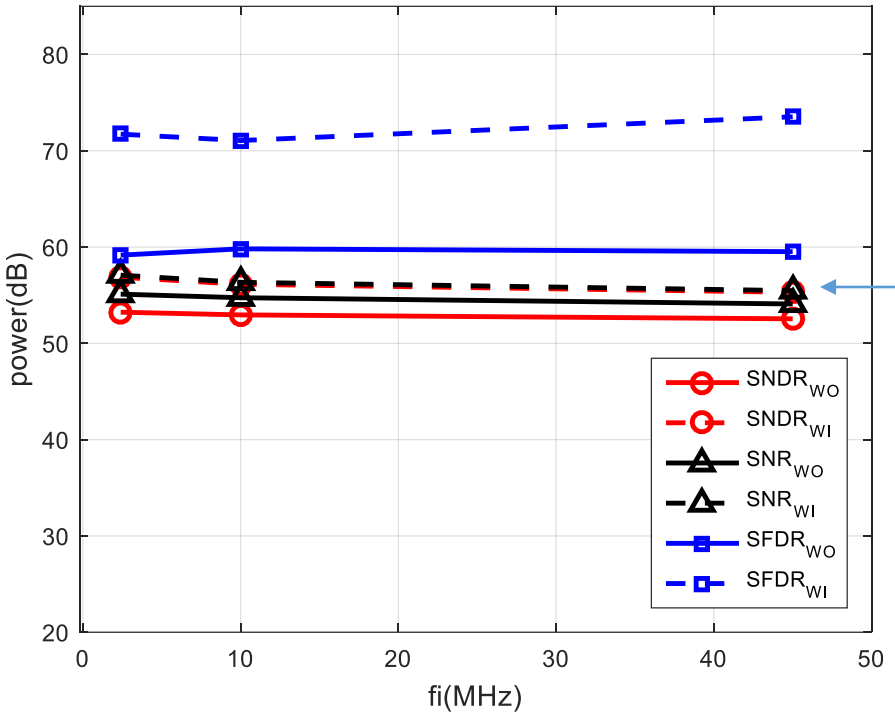
- Linearity @ 50MSPS, 2.4MHz sine input

Chip NO.	Without Cali.		With Cali.	
	SNDR (dB)	SFDR (dBc)	SNDR (dB)	SFDR (dBc)
1	54.0	61.4	57.2	79.4
2	53.2	59.2	56.9	71.7





- SNDR @ 50 MSPS sampling rate

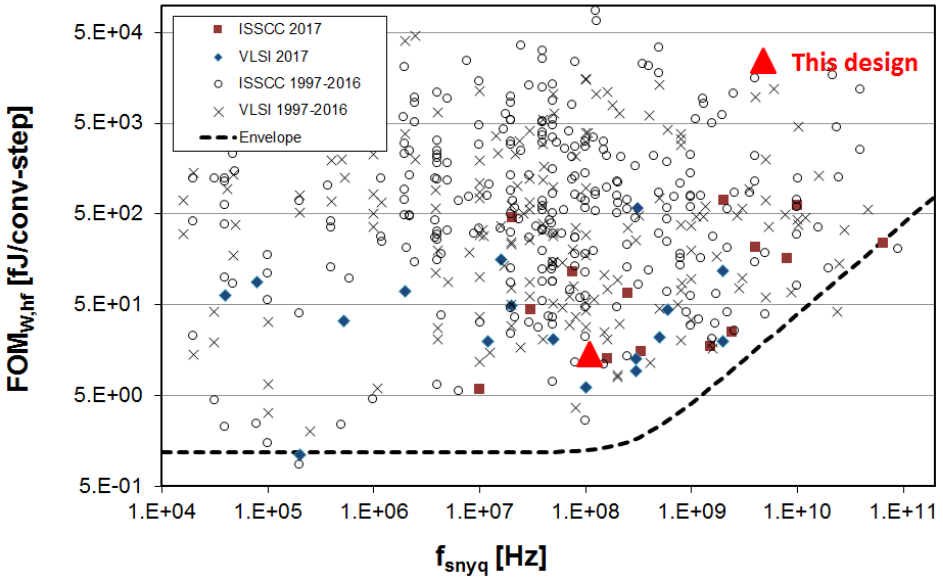


57 dB, ENOB = 9.18bit

- The power consumption

Module name	Power (mW)
The whole chip	4.0
Reference buffer module	0.25
SAR ADC Core Module	1.0
Other modules (CLK gen.)	2.75

FOM=21.3fJ/conv.



B. Murmann, ADC Performance Survey 1997-2017, [Online].Available: http://web.stanford.edu/~murmann/adcsurvey.html

- SAR ADC test summary

	Specifications	Test Results
Sampling rate	40 MSPS	50 MSPS
Resolution	10 bit	10 bit
INL	<0.65 LBS	<0.5 LSB
DNL	<0.6 LSB	<0.5 LSB
ENOB	>9 bit	9.18 bit
Power consumption	<2.5 mW/ch	1 mW/ch

Summary

- Low power front-end ASICs have been developed to meet the stringent requirements of CEPC TPC readout by:
  - Using advanced 65 nm CMOS process
  - Adopting circuit structure with minimized analog circuits such CR-RC shaper and SAR ADC
- The test results of our first run prototype chips showed good performances fully meeting the specifications, including the analog front-end and SAR ADC chips

Future plan

- More tests on:
  - More quantities of chips
  - The AFE+ADC chip
  - Mounted with detectors
  - Radiation hardness (~1krad TID for CEPC-TPC)
- One more MPW run supported
  - A 16-channel demo chip