ALICE ITS Upgrade

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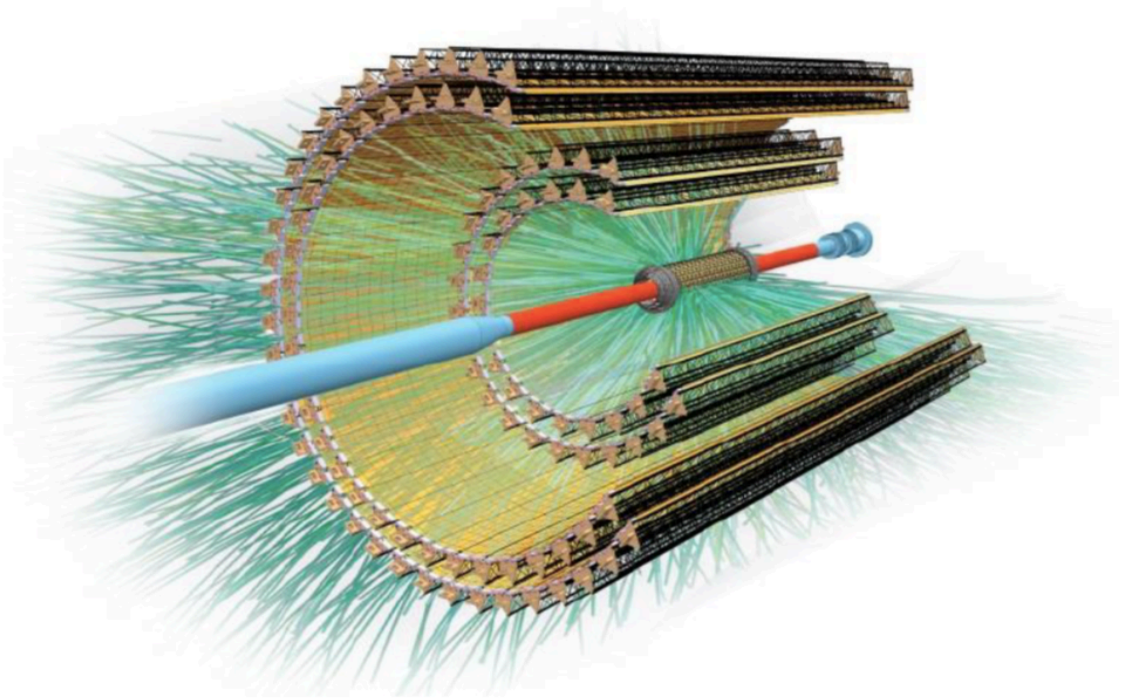
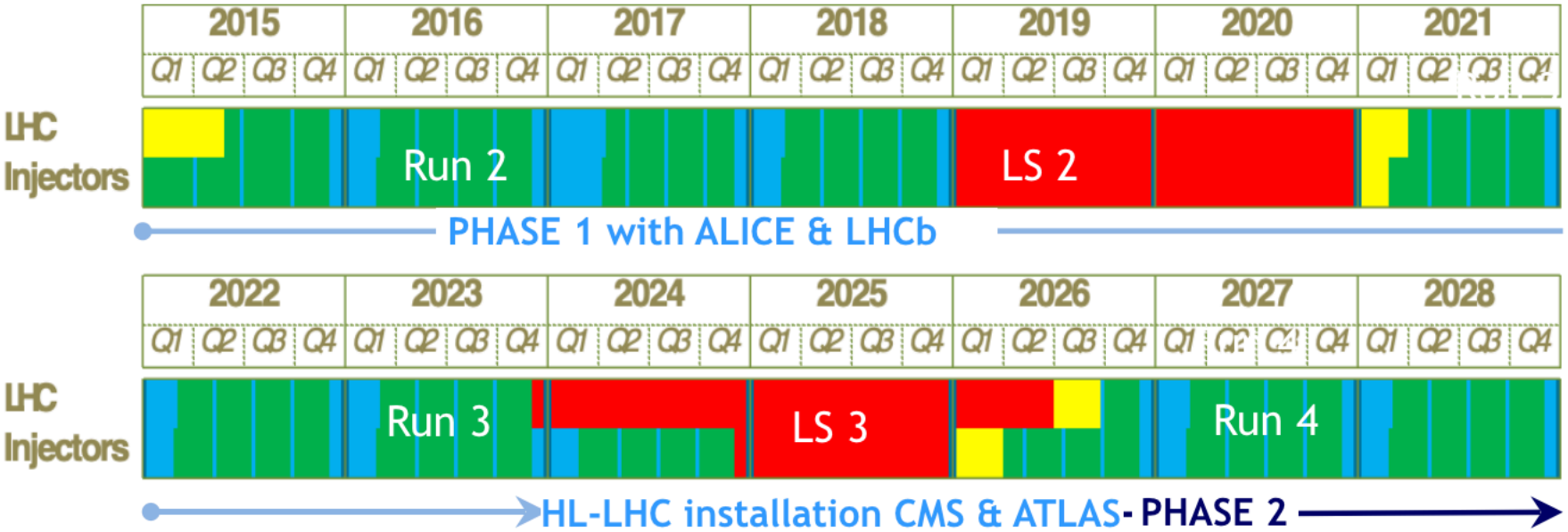


Outline

- Motivation
- ALICE ITS upgrade
  - ✓ Pixel Chip
  - ✓ Production
  - ✓ CCNU effort
- Summary and outlook

LHC program

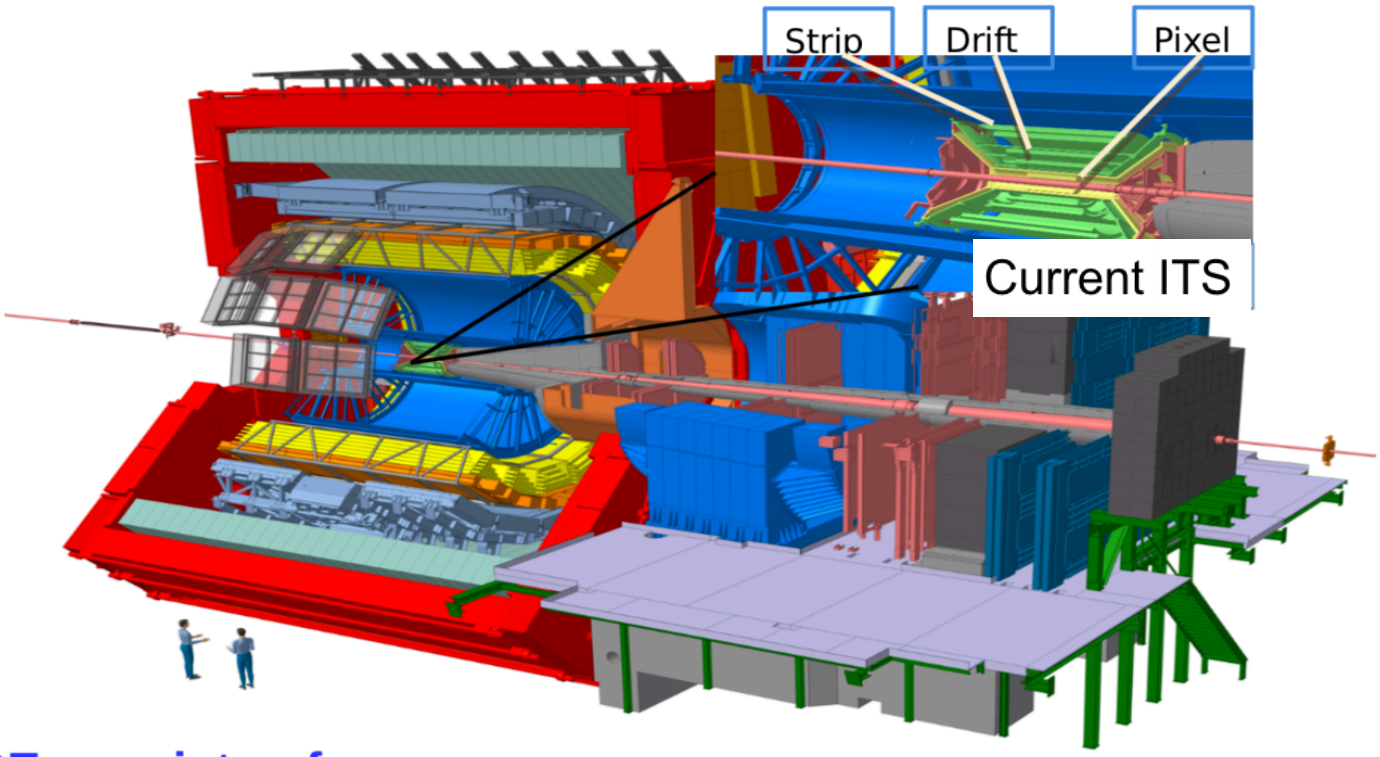


- The LHC heavy-ion program will extend to Run 3 and Run 4
  - ➡ phase I: ALICE and LHCb (2019~2020)
  - ➡ phase II: CMS and ATLAS (2024~2026)

- Goal of ALICE upgrade
  - ➡ readout of Pb-Pb interactions > 50 kHz
  - ➡ Integrated luminosity > 10 nb^{-1}

Current ALICE Detector

ALICE - dedicated heavy-ion experiment at the CERN LHC
- studies properties of strongly interacting matter (quark–gluon plasma)



Current ITS

r_{in} = 3.9 cm r_{out} = 43 cm
6 silicon detector layers:
2 hybrid pixel (**SPD**), 2 silicon drift (**SDD**), 2 silicon strip (**SSD**)

SPD thickness (X/X_0):
1.14% per layer
Readout rate: ~**1kHz** (ITS,TPC)

ALICE consists of
- central barrel,
- forward muon spectrometer,
- several dedicated detectors for triggering and event characterization.

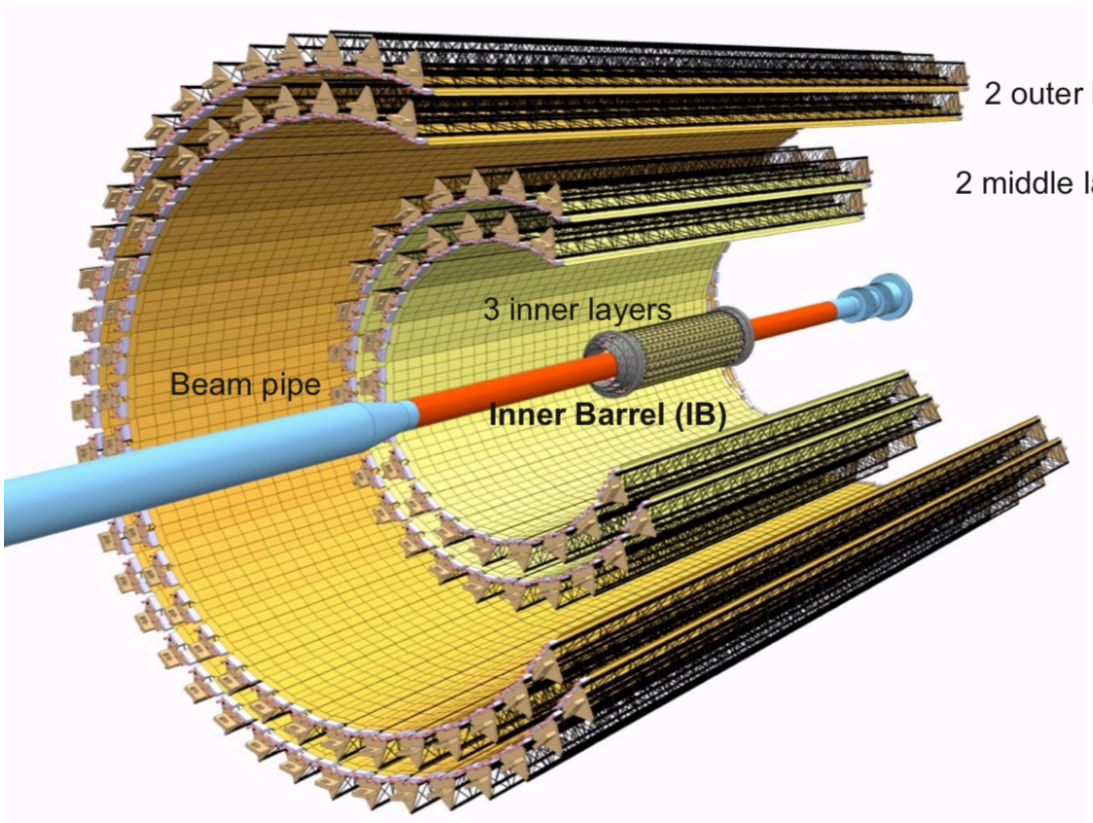
Motivation

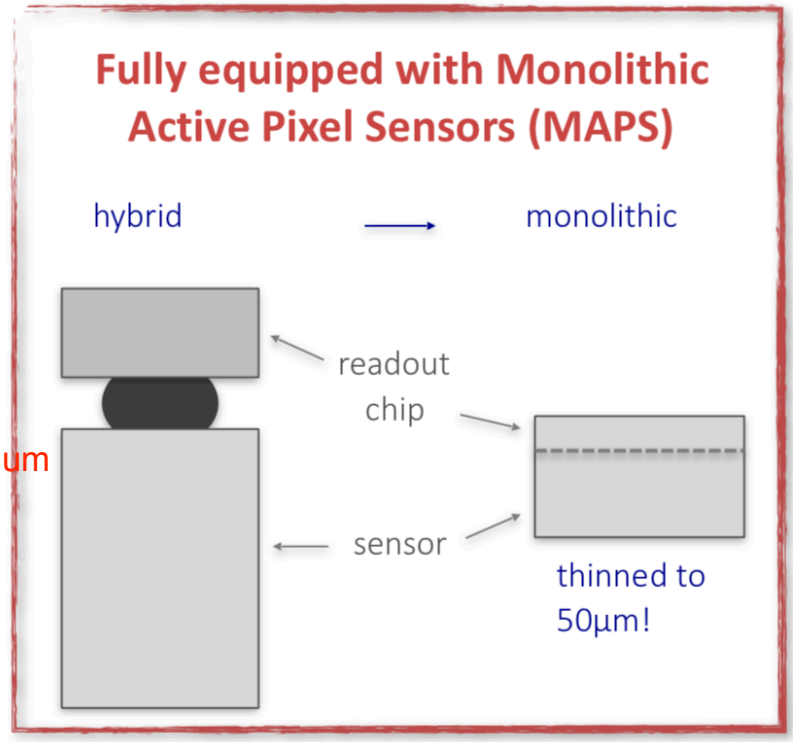
- Max readout Pb-Pb interactions rate ~ 500 Hz
- integrated luminosity ~ 0.1 nb^{-1} ☹
- Present limits:
  - charm difficult for $p_t \rightarrow 0$ (background is too large)
  - resolution not sufficient for charmed baryons (Λ_c $c\tau$= 60 μm)
  - Λ_b impossible in Pb-Pb collisions (insufficient statistics and resolution)
  - indirect B measurement via electrons;
  - ….

Requirements:

Increase vertex resolution and tracking efficiency
Increase readout rate capabilities

New Inner Tracking System





- 7 layers
- 12.5 Gigapixels
- Binary readout
- ~ 10 m^2 active surface

New ITS Performance

1. Improve impact parameter resolution by a factor of ~3

- Get closer to IP (position of first layer): 39mm ➡22mm
- Reduce material budget: X/X_0 /layer: ~1.14% ➡~ 0.3%
- Reduce pixel size
  - currently 50mm x 425mm
    monolithic pixels ➡ 27μm x 29μm

2. Improve tracking efficiency and p_T resolution at low p_T

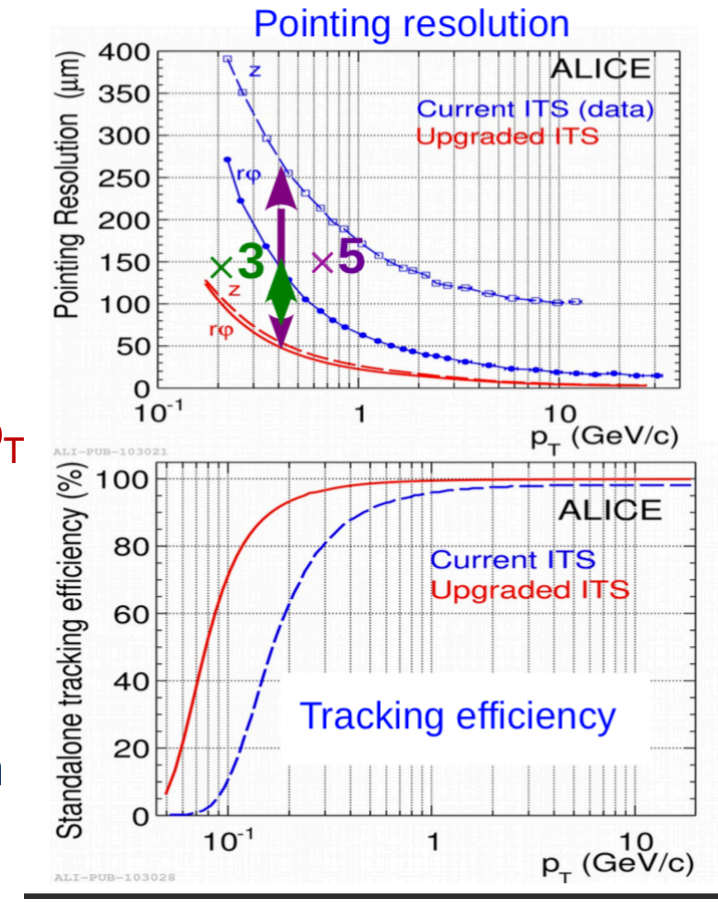
- Increase granularity: 6 layers ➡ 7 layers

3. Fast readout

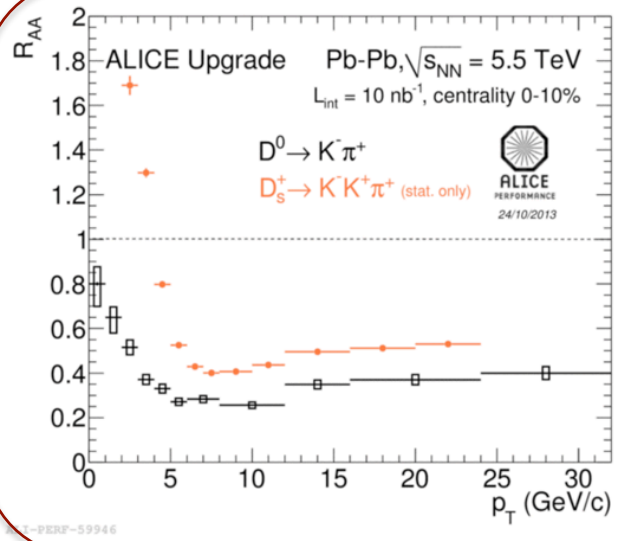
- readout of Pb-Pb interactions at > 100 kHz and pp interactions at ~ 400 kHz (currently limited at 1kHz with full ITS and ~3kHz without silicon drit)

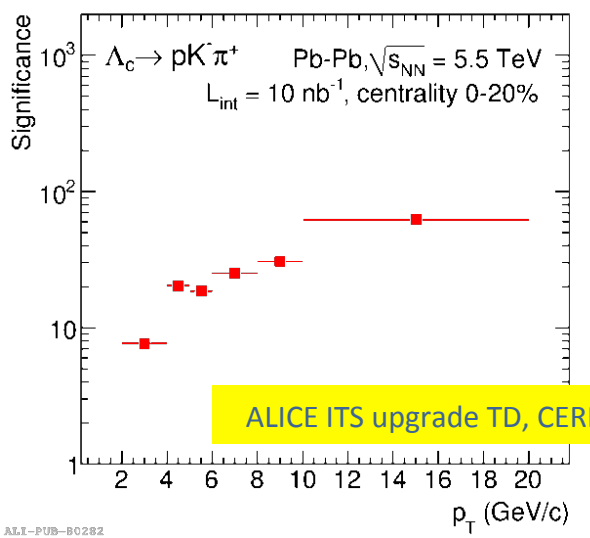
4. Fast insertion/removal for yearly maintenance

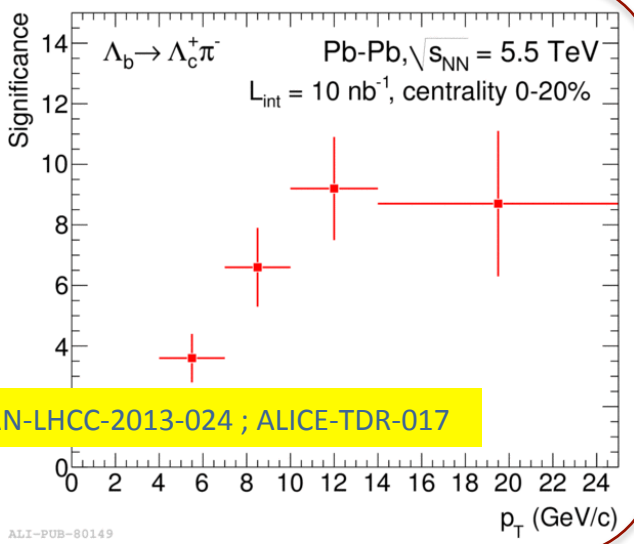
- possibility to replace non functioning detector modules during yearly shutdown



New ITS Performance

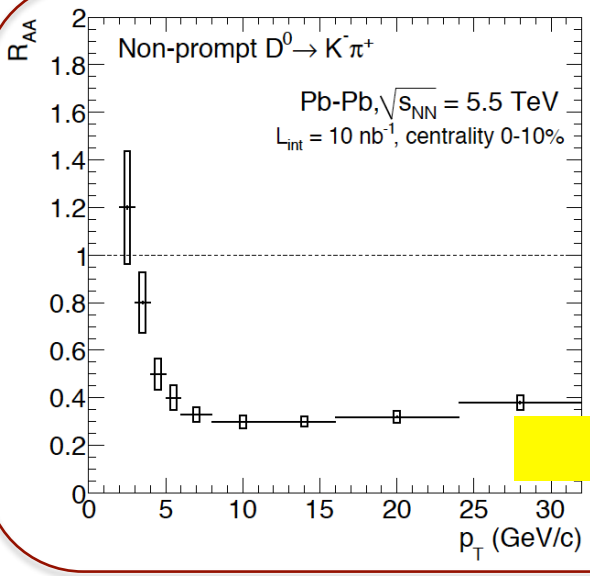


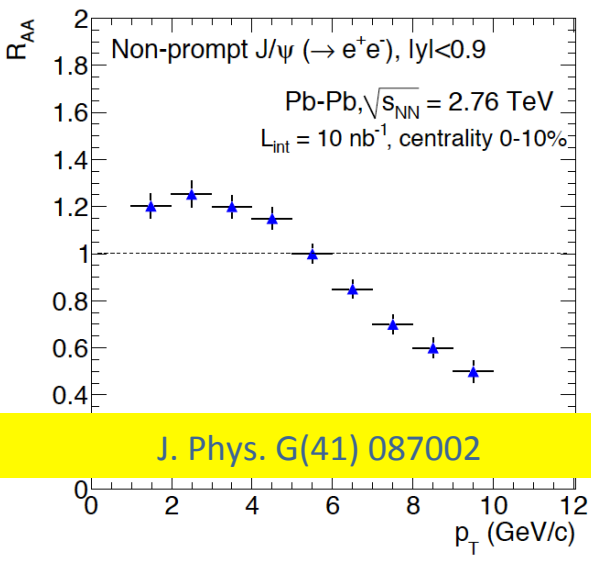


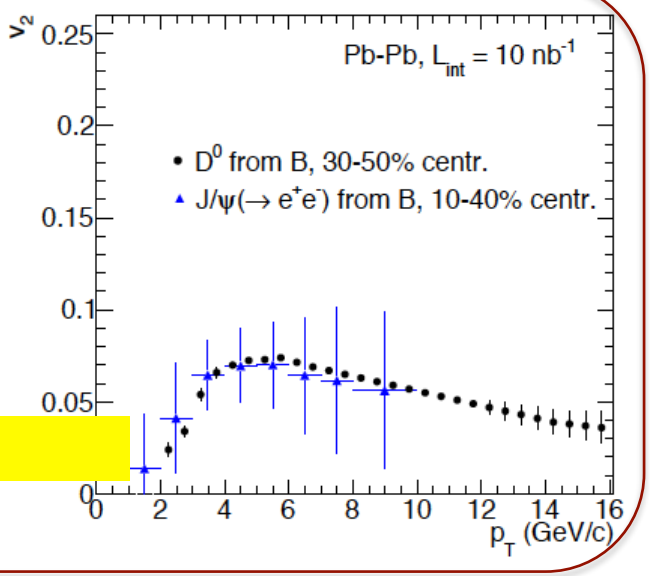


ALICE ITS upgrade TD, CERN-LHCC-2013-024 ; ALICE-TDR-017

(1) Precision measurements on charm physics; (2) open-bottom physics accessible







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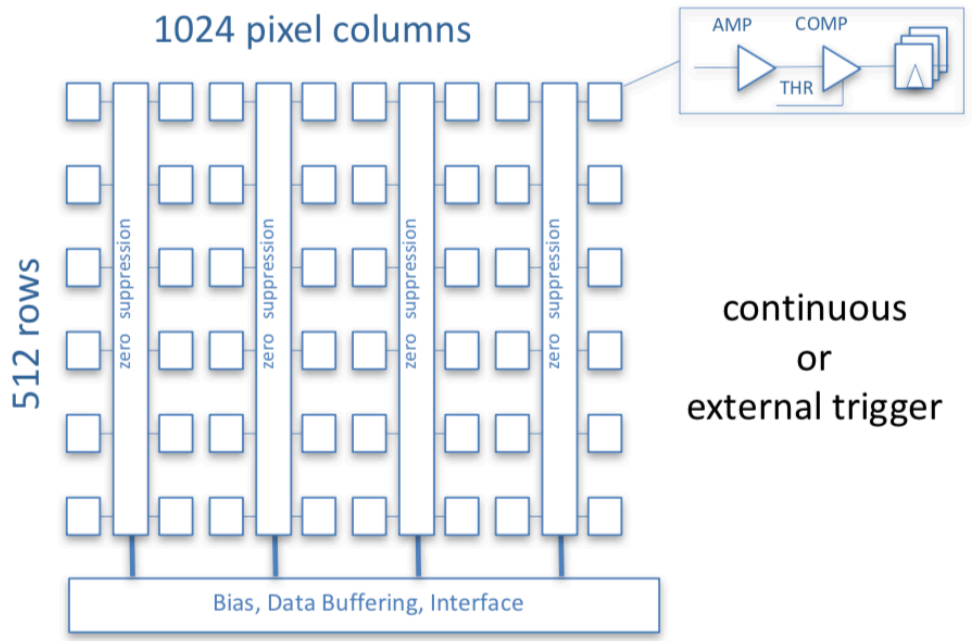
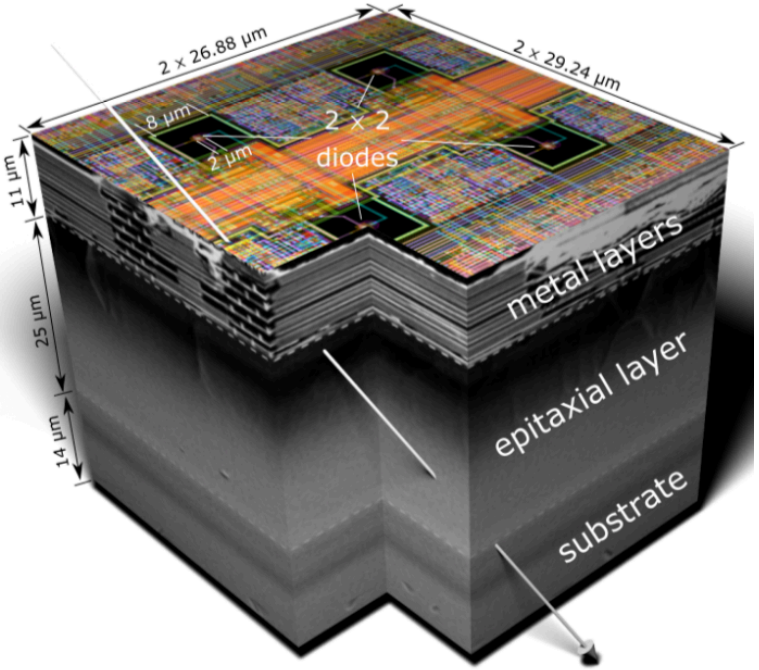
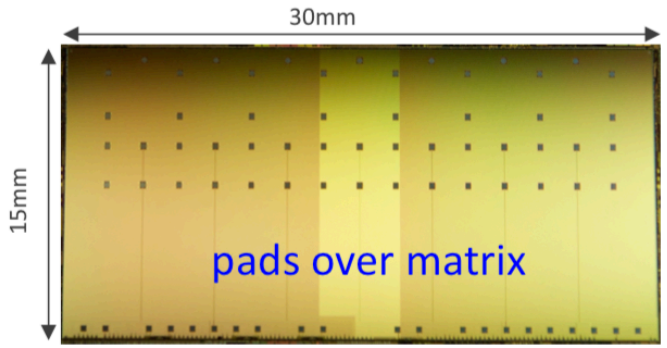
ALIPIDE pixel chip



continuous
or
external trigger

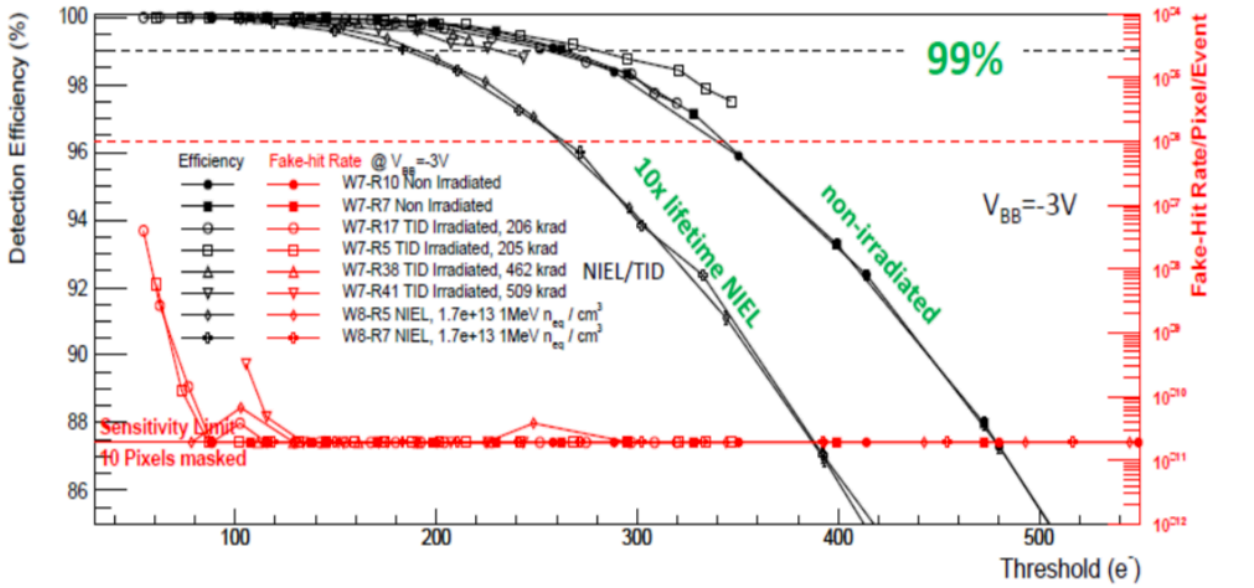


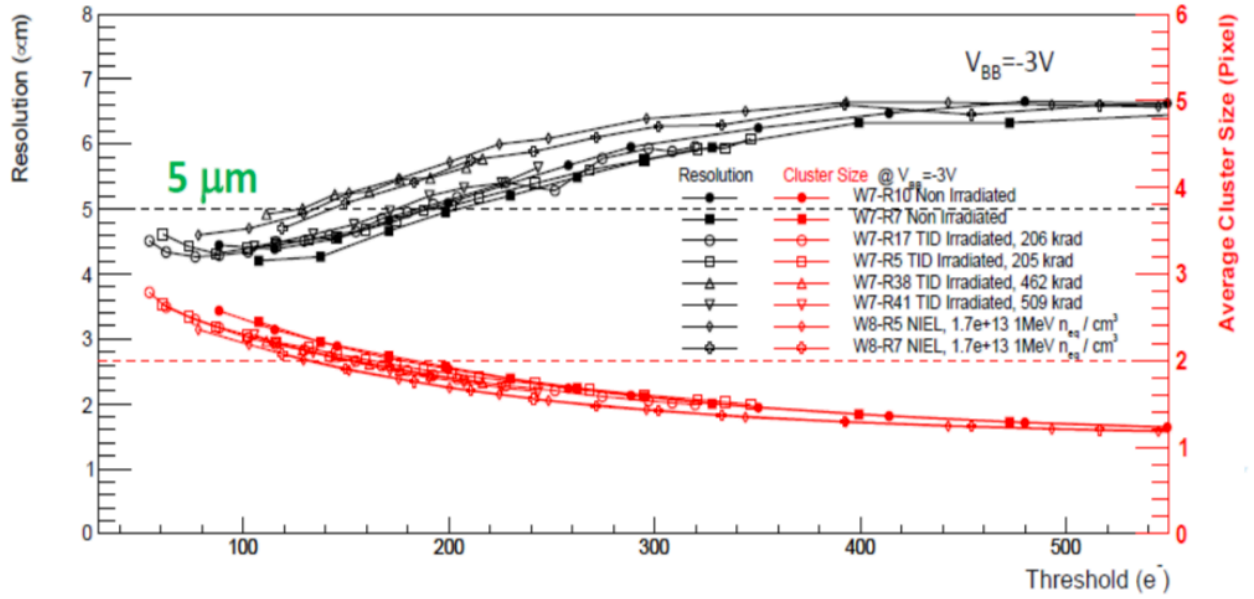
ALPIDE (ALICE PIxel DEtector)
(IB: 50 µm thick; OB: 100 µm thick)



- ✓ 130,000 pixel/cm^2
- ✓ Spatial resolution: ~5 µm (3-D)
- ✓ Integration time: < 10 µs
- ✓ Max particle rate: 100 MHz/cm^3
- ✓ Fake-hit rate: ~10^{-10} pixel/event
- ✓ Power: ~ 300 nW/pixel

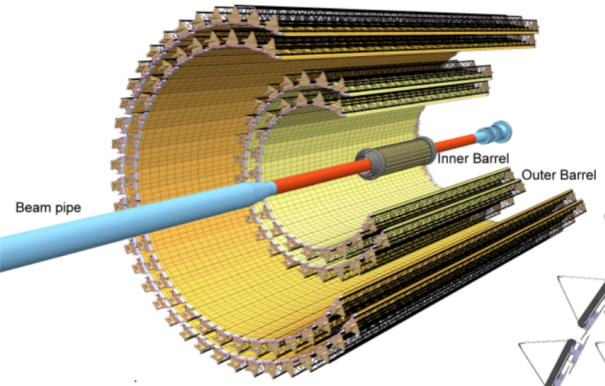
Chip Performance

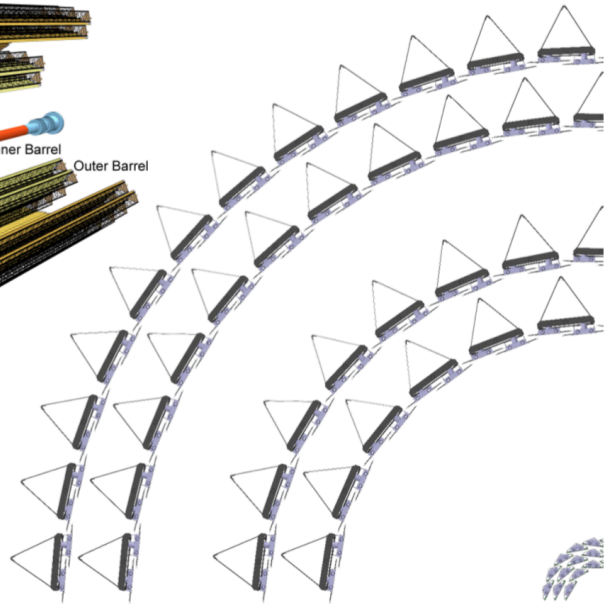




- Detection efficiency stays at 100% over wide range of threshold value
- Fake-hit rate is below 10^{-11} /pixel/event (requirement 10^{-6})
- Average cluster sizes vary between 1 and 3 pixels (for MIPs)
- Resolution of ~5µm at a threshold of 200 electrons
- Irradiated chips (NIEL/TID) show no degradation in resolution/efficiency

New ITS Layout

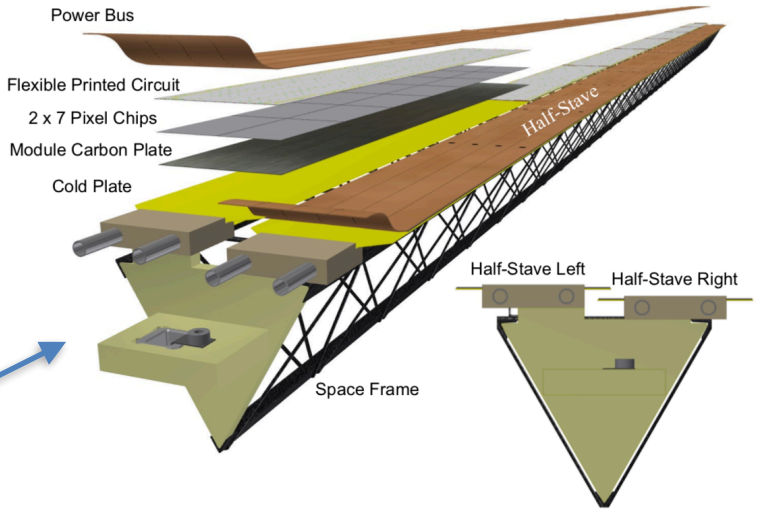




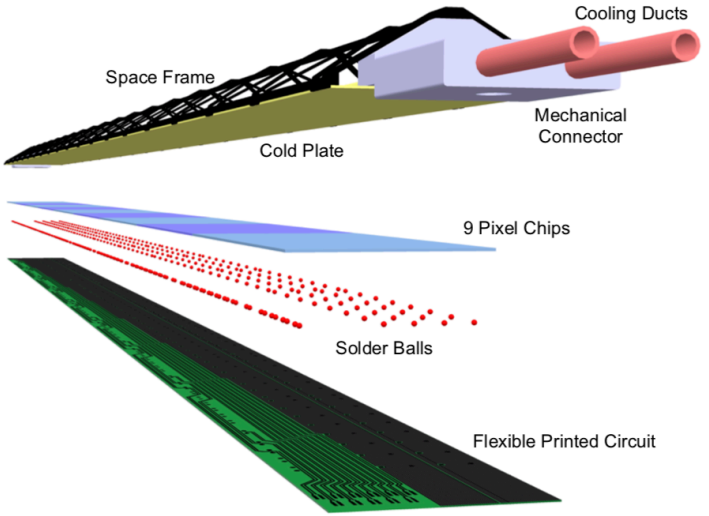
➔ The ITS is constituted by :
- 7 layers: 3 (IL), 2 (ML), 2 (OL)
- 192 Staves: 48 (IL), 54 (ML), 90 (OL)

Layer #	6	5	4	3	2	1	0
N. of Stave	48	42	30	24	20	16	12

Outer Barrel (OB)

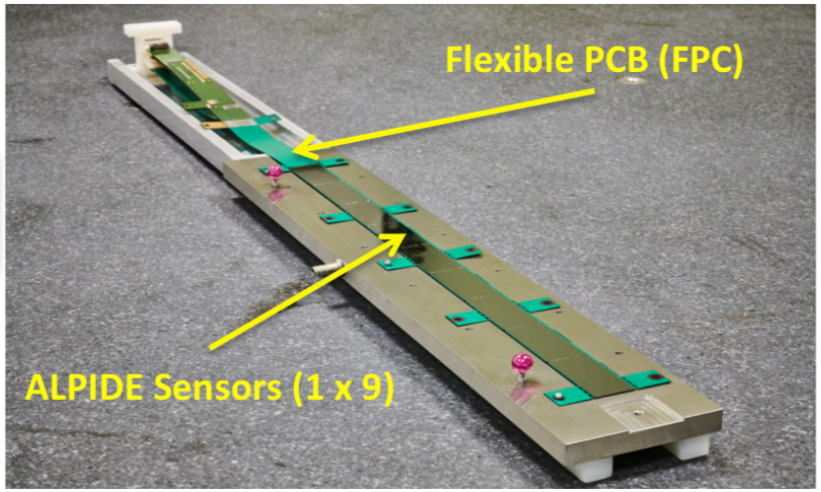


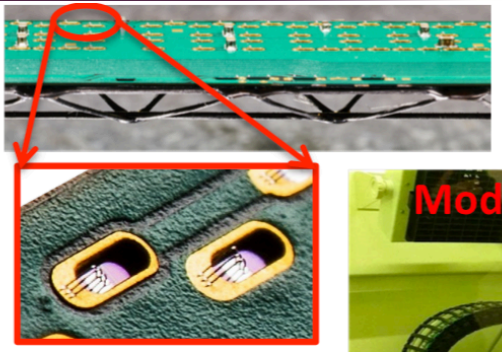
Inner Barrel (IB)



Construction -Inner Barrel

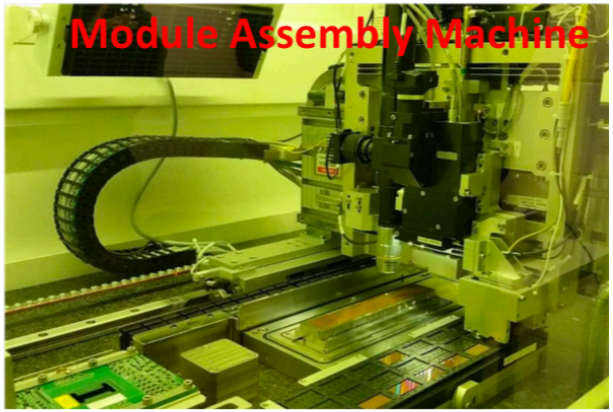
Module Assembly



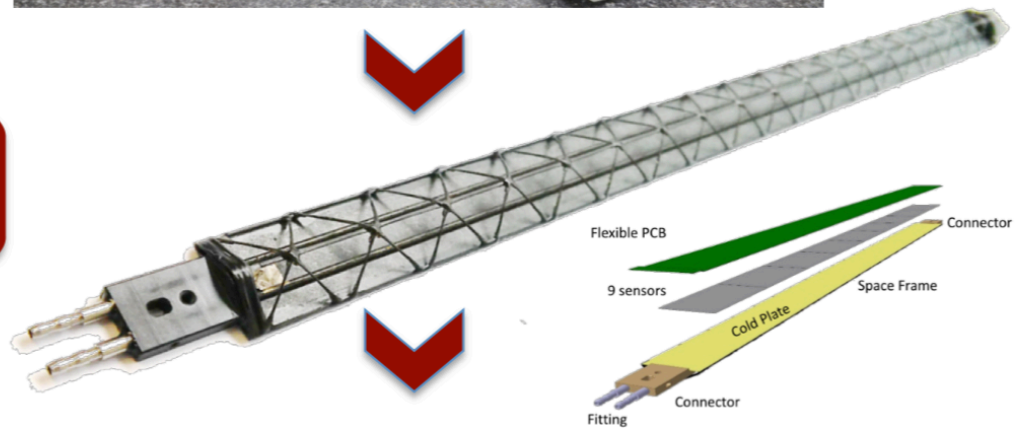


HIC: Hybrid Integrated Circuit
(IB: 9 chips + FPC; OB: 14 chips + FPC)

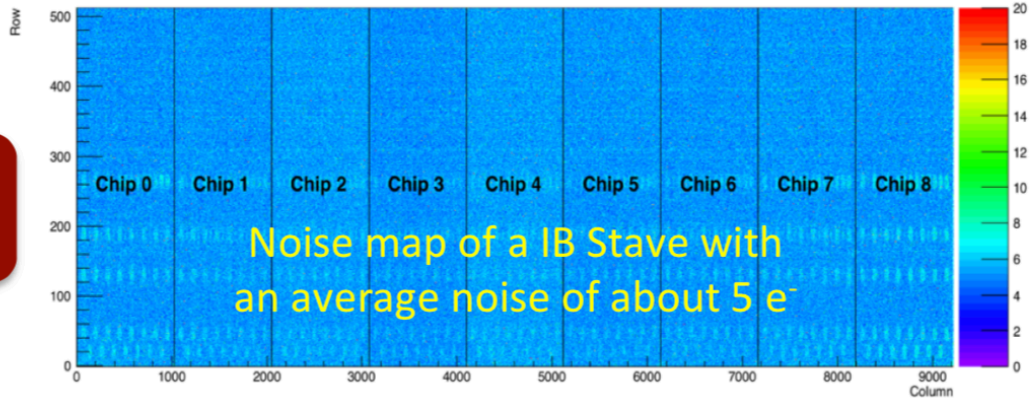
ALICIA:



Stave Assembly



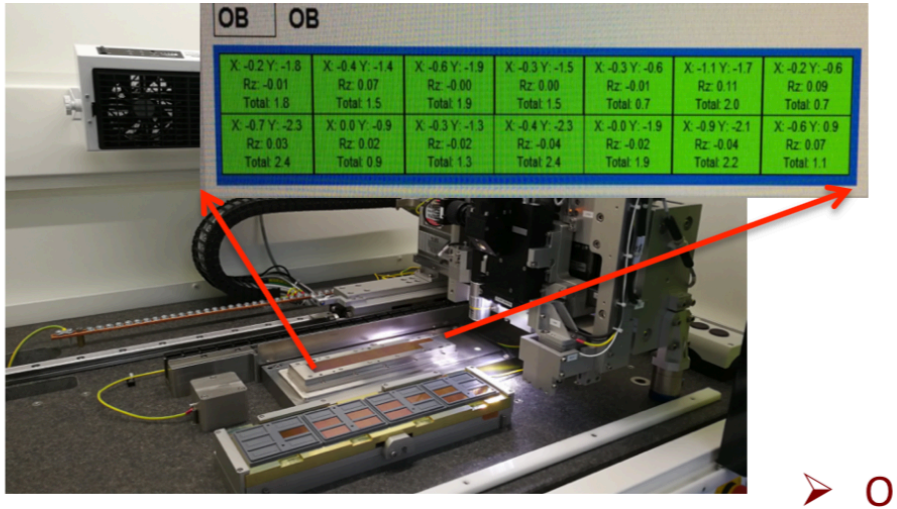
Testing

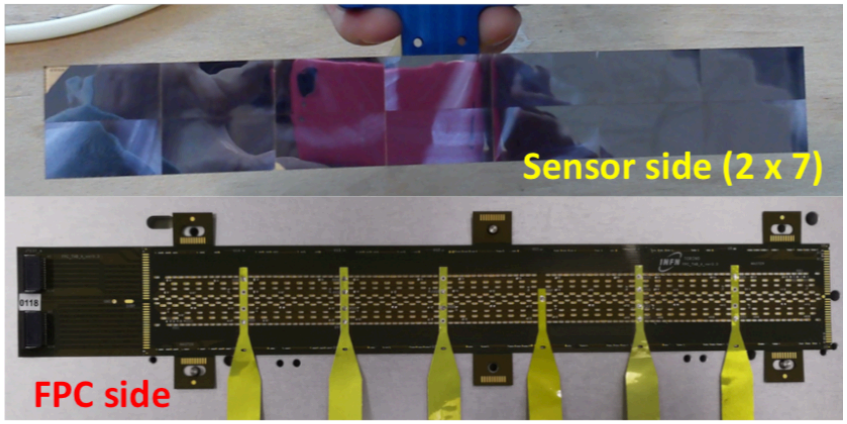


- **Required production quantity**
  - 120 HICs (48 staves per Inner Barrel, 2 Inner Barrels, plus spares)
- **Sensor alignment in a custom designed Module Assembly Machine (ALICIA):**
  - 5 μm precision chip placement
  - 6 machines were installed at HIC construction sites (IB: CERN; OB: Bari, Liverpool, Pusan, Strasbourg, Wuhan)
- **HIC/Stave testing**
  - using dedicated test setup
  - classification scheme according to the results of various functional tests

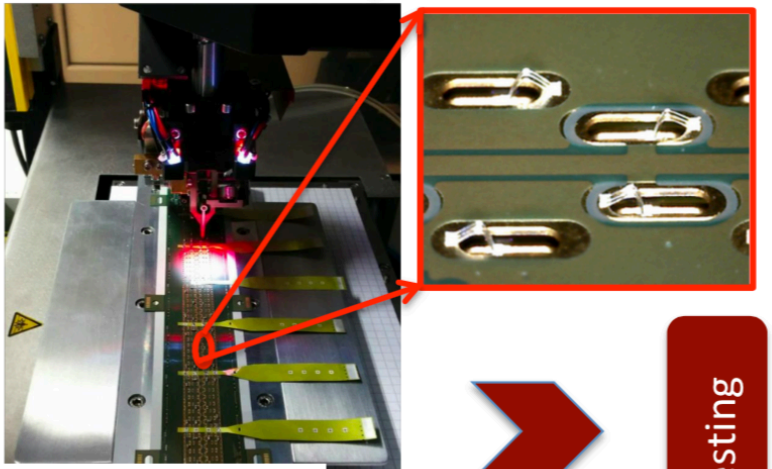
Construction -Out Barrel

Chip Alignment





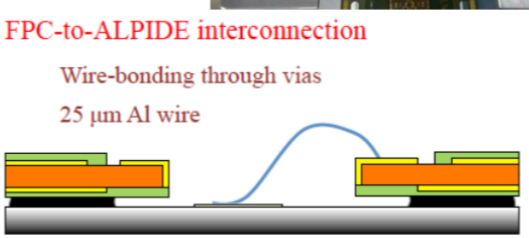
Wire Bonding



FPC-to-ALPIDE interconnection

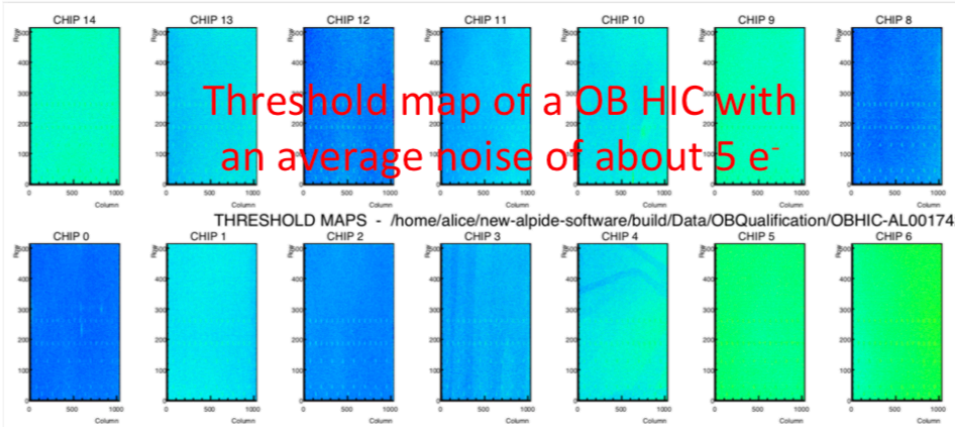
Wire-bonding through vias

25 μm Al wire



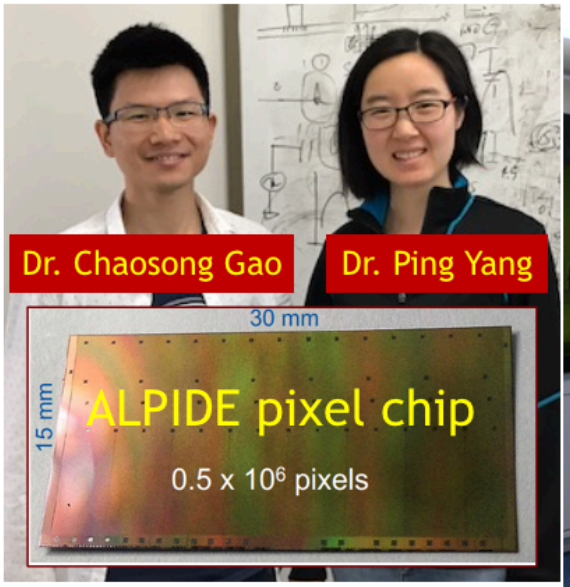
Testing

- OB HIC Production
  - 1692 HIC modules required
  - 5 HIC production sites: Bari, Liverpool, Strasbourg, Wuhan, Pusan
  - Target rate: 2 HICs per day per site

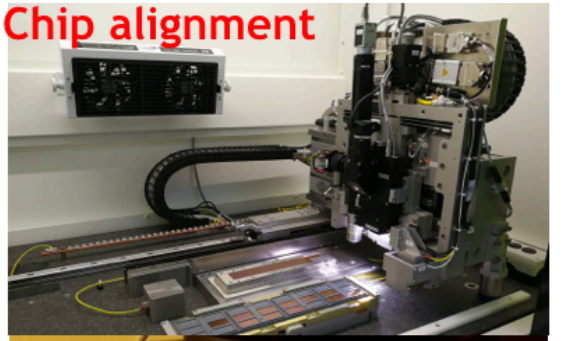


Threshold map of a OB HIC with an average noise of about 5 e⁻

CCNU Effort


Dr. Chaosong Gao
Dr. Ping Yang
30 mm
15 mm
ALPIDE pixel chip
0.5 x 10⁶ pixels

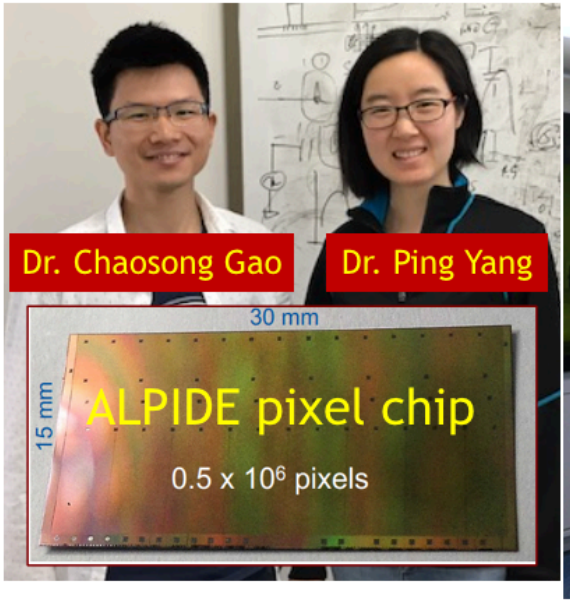

ALICE/ITS OB HIC Assembly Team（CCNU）:
Biao、Jun、Daming、Kai、Peipei、Wenjing

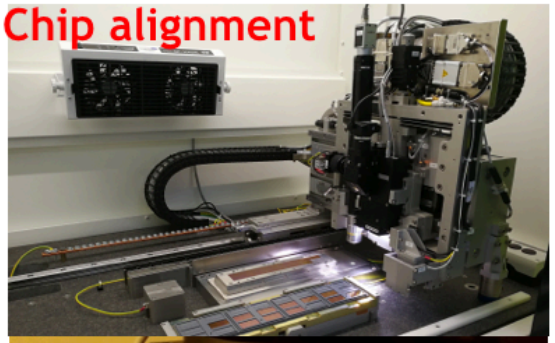

Chip alignment


Chip-FPC interconnection


storage
(chip tray, HIC box,
FPC box)
ALICIA
F&K G5
Delvotec
Endurance test box
Pull test machine
Clean room @ ISO6

CCNU Effort





- Efforts on ALPIDE chip design since 2012
- Take charge of 20% ALICE/ITS OB HIC module assembly & test (~7500 ALPIDE chips)
- Pre-series production started in Dec. 2017
- Series production started in April, 2018, and scheduled to be completed in May, 2019
- As so far, around one half HIC modules have been constructed and tested
- Long-term plan: (1) ALICE ITS calibration and alignment; (2) open-bottom production at LHC

Summary and Outlook

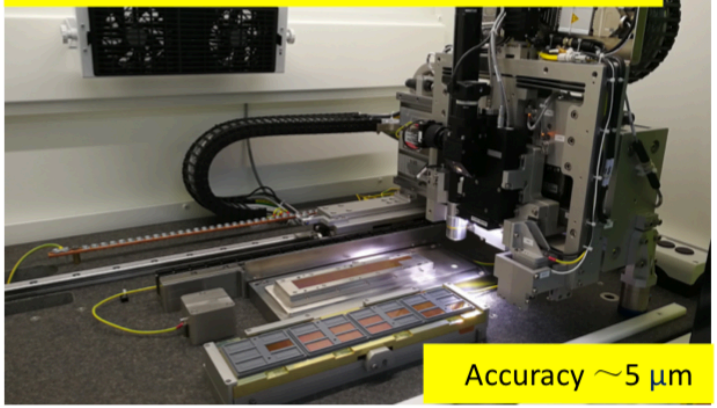
- ALICE Inner Tracking System will be upgraded in LS2(2019~2020)
  - ✓Improve vertex and tracking performance
  - ✓Enable Pb-Pb collision readout rate at 50 kHZ
- The ALPIDE pixel chip show good performance
  - ✓Low fake-hit rate and integration time
  - ✓High pixel integration density
- CCNU involves ALICE ITS upgrade
  - ✓ Chip design
  - ✓ Detector construction
  - ✓ Commissioning and heavy flavor physics in the future

BACK UP

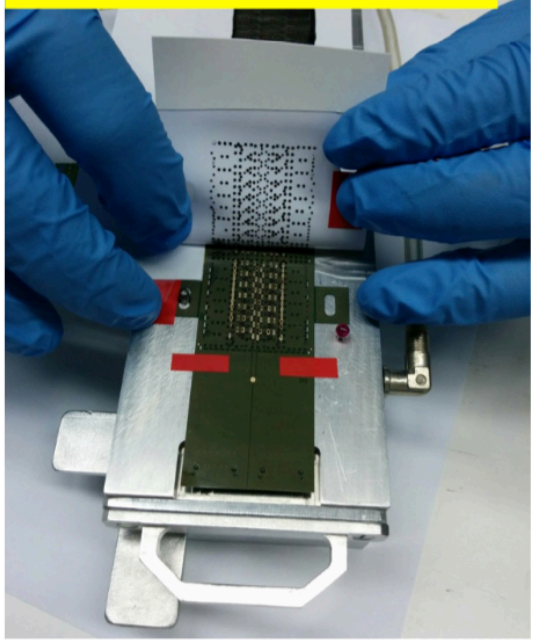
Production

HIC Assembly Procedure

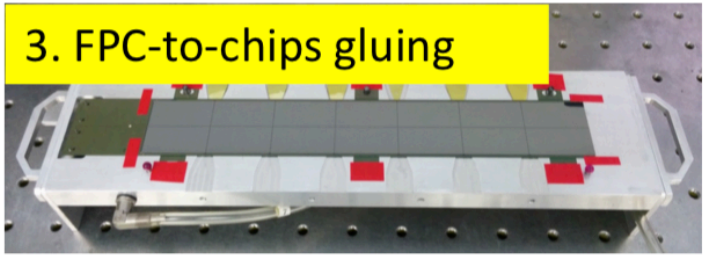
1. Chip Alignment with MAM



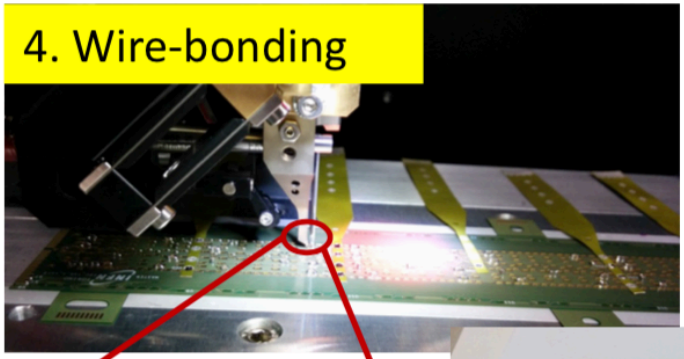
2. Glue spread on FPC

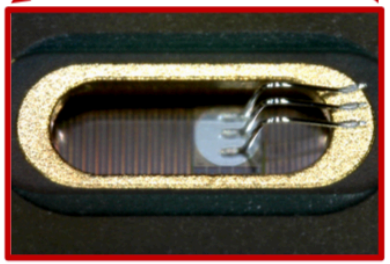


3. FPC-to-chips gluing

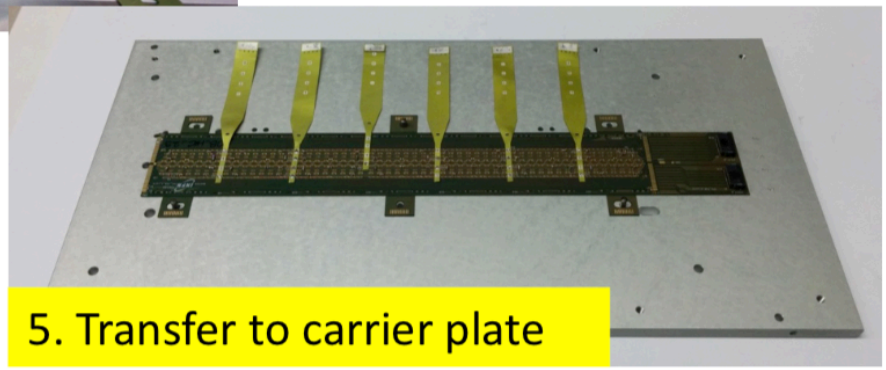


4. Wire-bonding

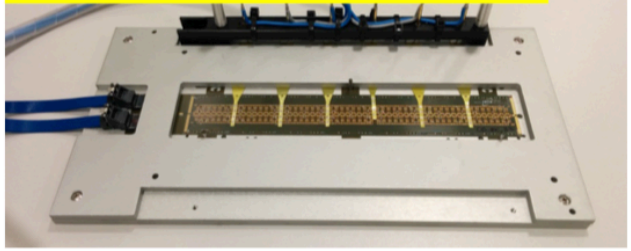




5. Transfer to carrier plate



6. Characterization test



7. Endurance test