The test of the SciFi Tracker electronics for the LHCb upgrade

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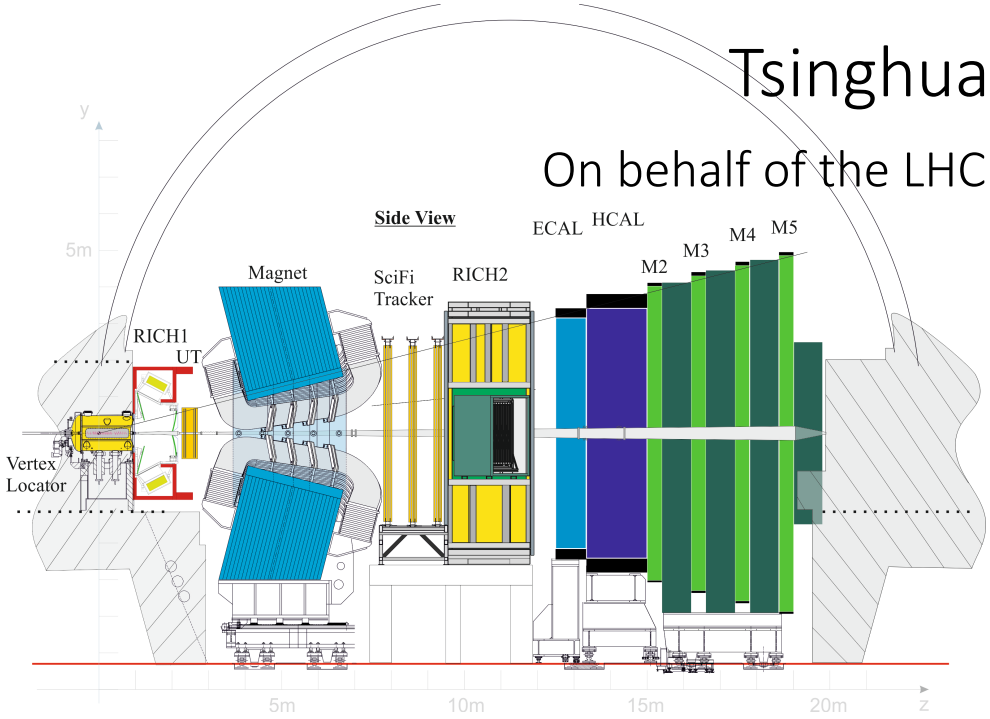
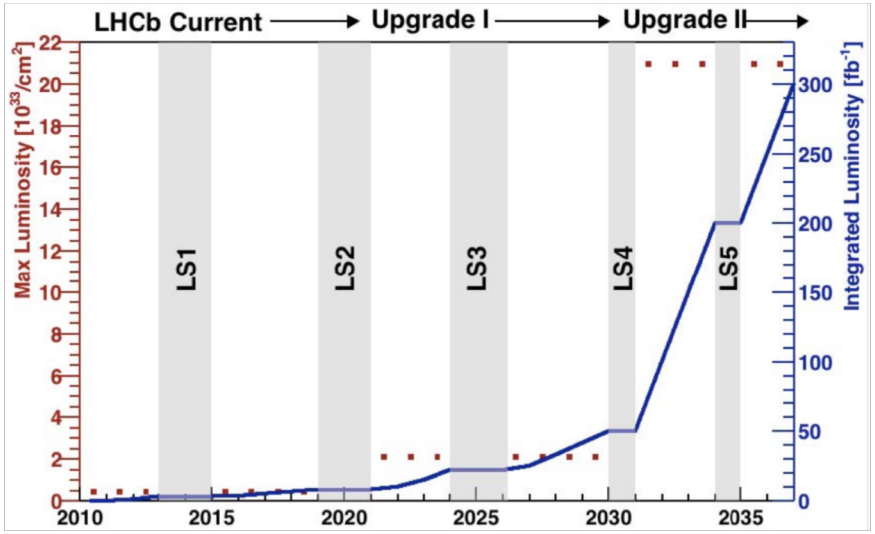
On behalf of the LHCb collaboration



LHCb Physics

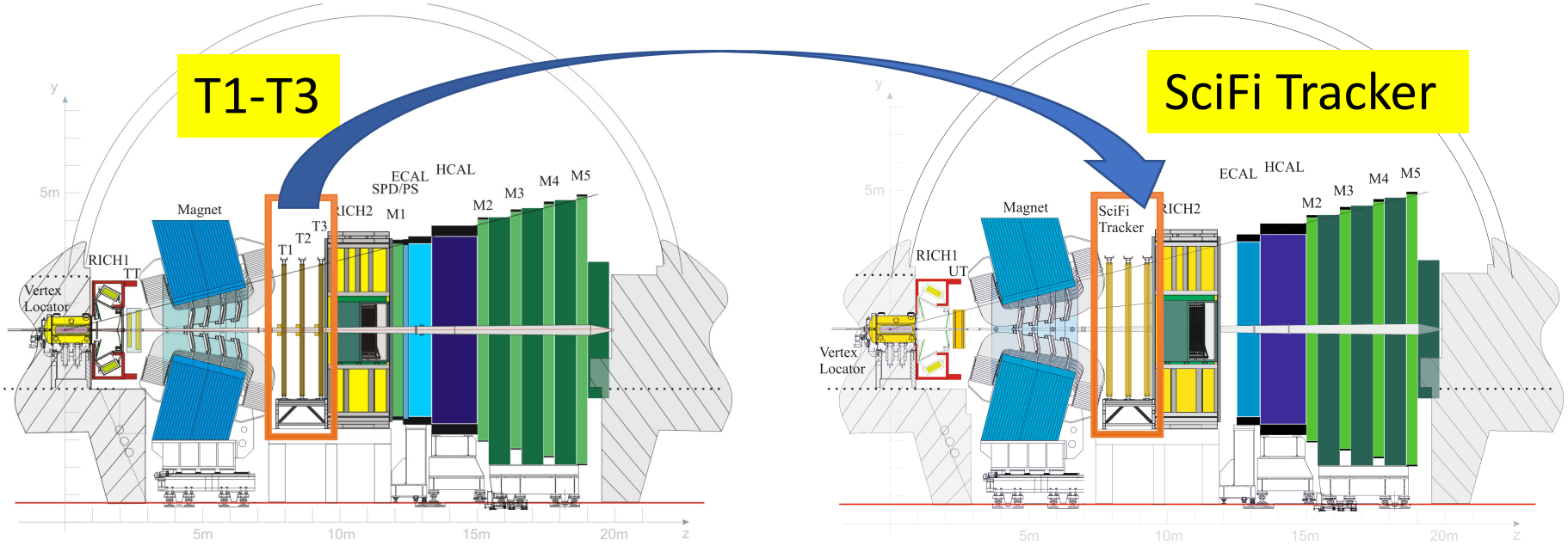
- Indirect search for New Physics via precision measurements of CKM, CP Violation and Rare Decay
- QCD + EW precision measurements at large rapidity
- Hadron spectroscopy
- Direct search of new particles beyond SM
- Heavy-ion physics



- Many measurements are limited by statistics
- $\int \mathcal{L}\,\mathrm{d}t = 9\ \mathrm{fb}^{-1}$ in Run1+Run2
- Need to upgrade: higher statistics and better performance

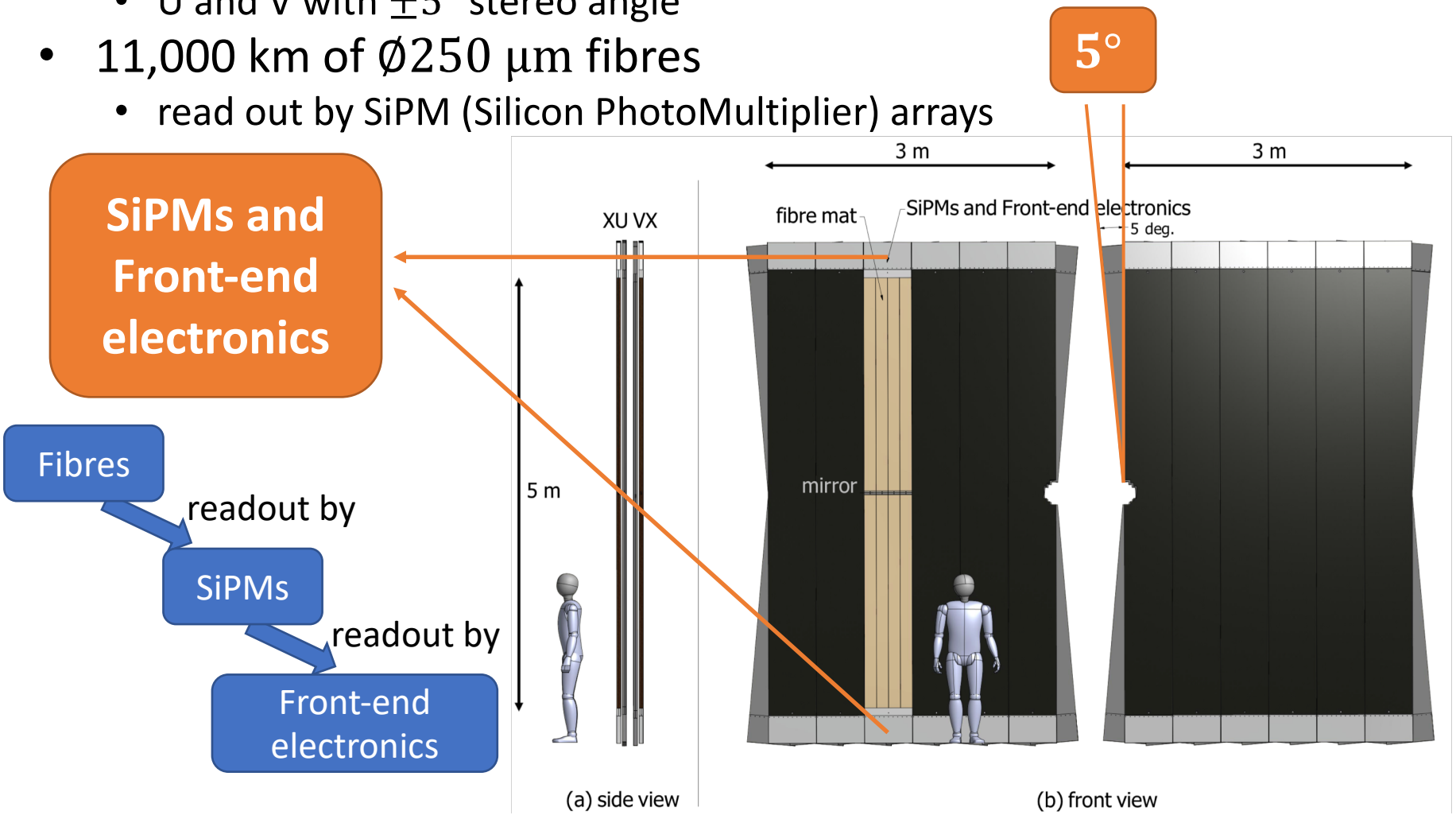
The LHCb Upgrade

- The goal of the Upgrade is to run the LHCb detector
  - At a luminosity of $\mathcal{L}_{\mathrm{inst}} = 2\times10^{33}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$, 5 times higher than that for the current detector ➔ $\int \mathcal{L}\,\mathrm{d}t = 50\ \mathrm{fb}^{-1}$ in Run3+Run4
  - With 40 MHz readout, software trigger only
- For the tracking system, the current T1-T3 stations will be fully replaced by the Scintillating Fibre (SciFi) Tracker system



SciFi Tracker

- 3 tracking stations with 4 individual planes (X-U-V-X) for each
  - U and V with $\pm 5°$ stereo angle
- 11,000 km of $\emptyset 250\ \mu m$ fibres
  - read out by SiPM (Silicon PhotoMultiplier) arrays



Front-end Electronics

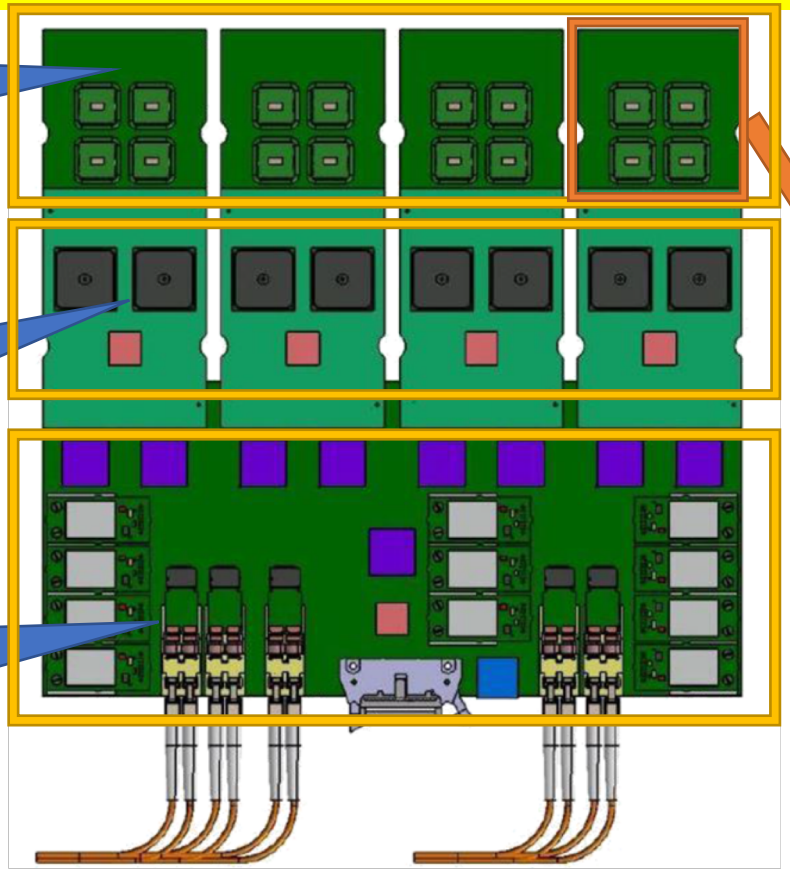
- PASIFIC Carrier Board designed by Tsinghua & Heidelberg
- ASIC and Carrier Board Quality Assurance (QA) system developed by Tsinghua

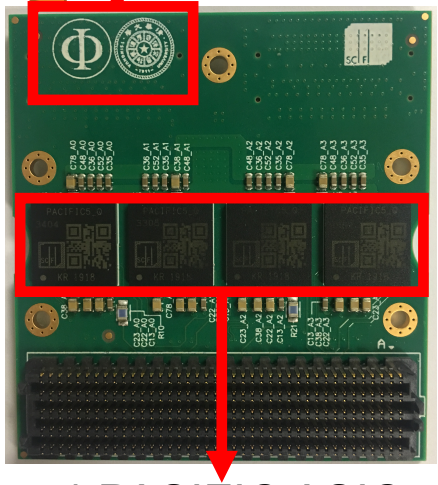
Signals from SiPMs

Digitized by the PACIFIC Carrier Board

Clusterized by the Cluster Board

Transferred to DAQ (Tell40) by the Mater Board



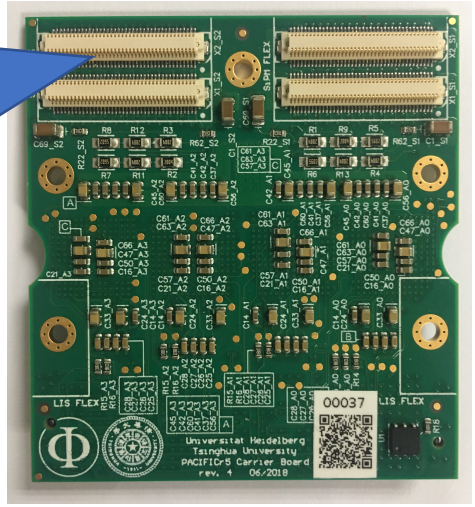


PACIFIC Carrier Board

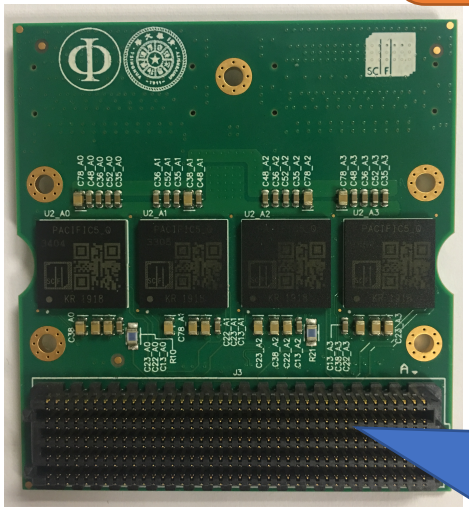
- 4 PACIFIC ASICs
  - A low Power Asic for the sCIntillating FIbre traCker
- 1 BoardID IC
  - DS2401 64-bit unique, factory-lasered silicon serial number
- 4 temperature measurement circuits
- 4 SiPM bias voltage measurement circuits

To monitor the control parameters when running the detector

4 SiPM flex cable connectors (connect to SiPM arrays)



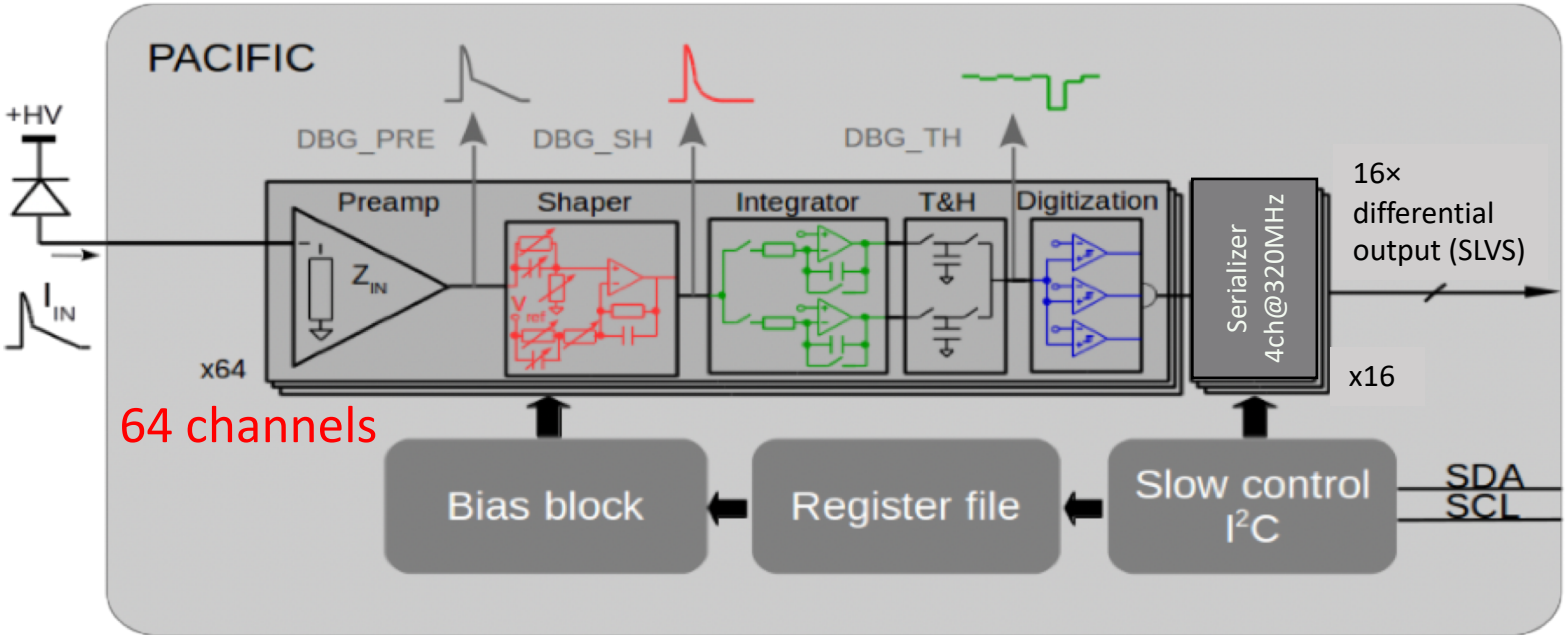
front view
of PACIFIC Carrier Board



back view
of PACIFIC Carrier Board

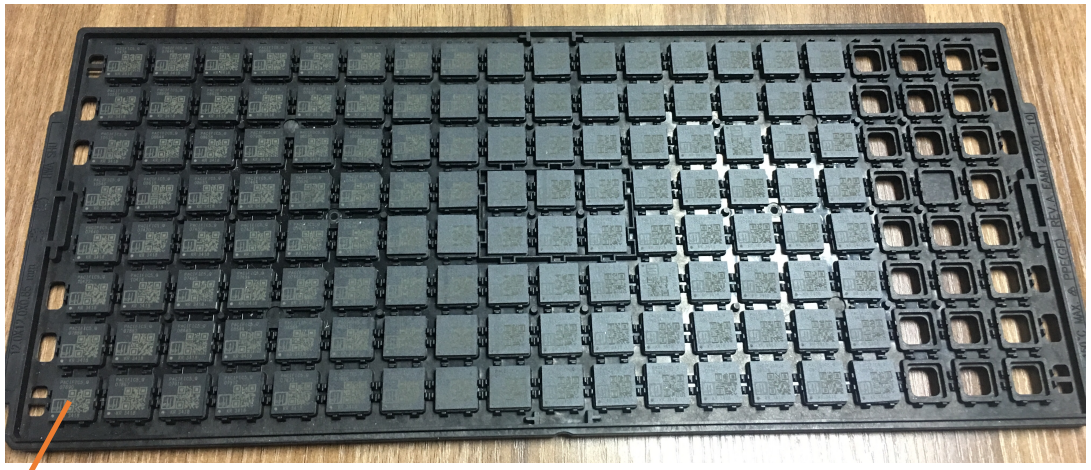
1 FMC connector (connect to the Cluster Board)

PACIFIC ASIC



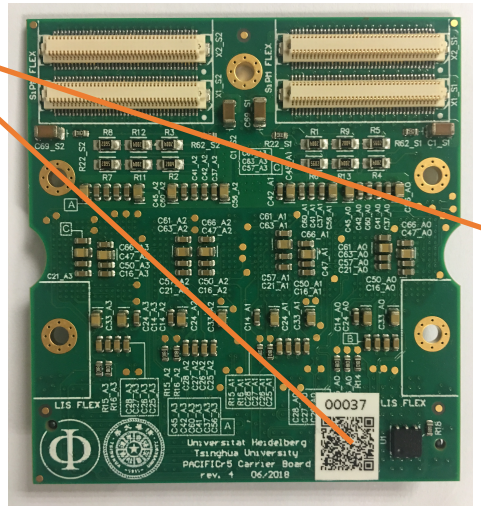
- Integrator:
  - Two interleaved gated integrators to reduce the deadtime to almost zero
  - Baselines can be tuned by a configurable block with trimDACs
- Digitization:
  - The conversion from analog to digital is based on three comparators with configurable thresholds, to effectively shrink the data bandwidth and subtract noise clusters while keeping sufficient information for tracking

PACIFIC ASIC and Carrier Board

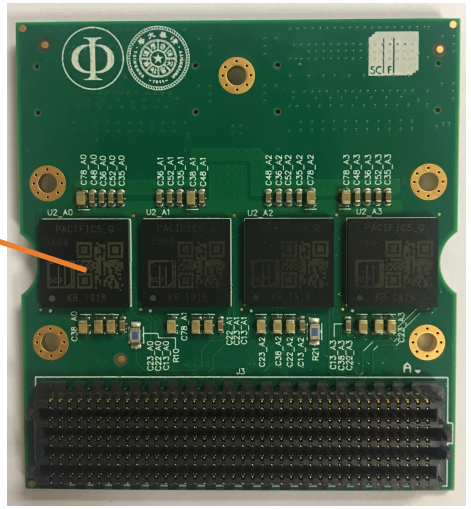


23000 ASICs to be tested
(need 8192 ASICs and +10% as space)

QR code



front view
of the PACIFIC Carrier Board

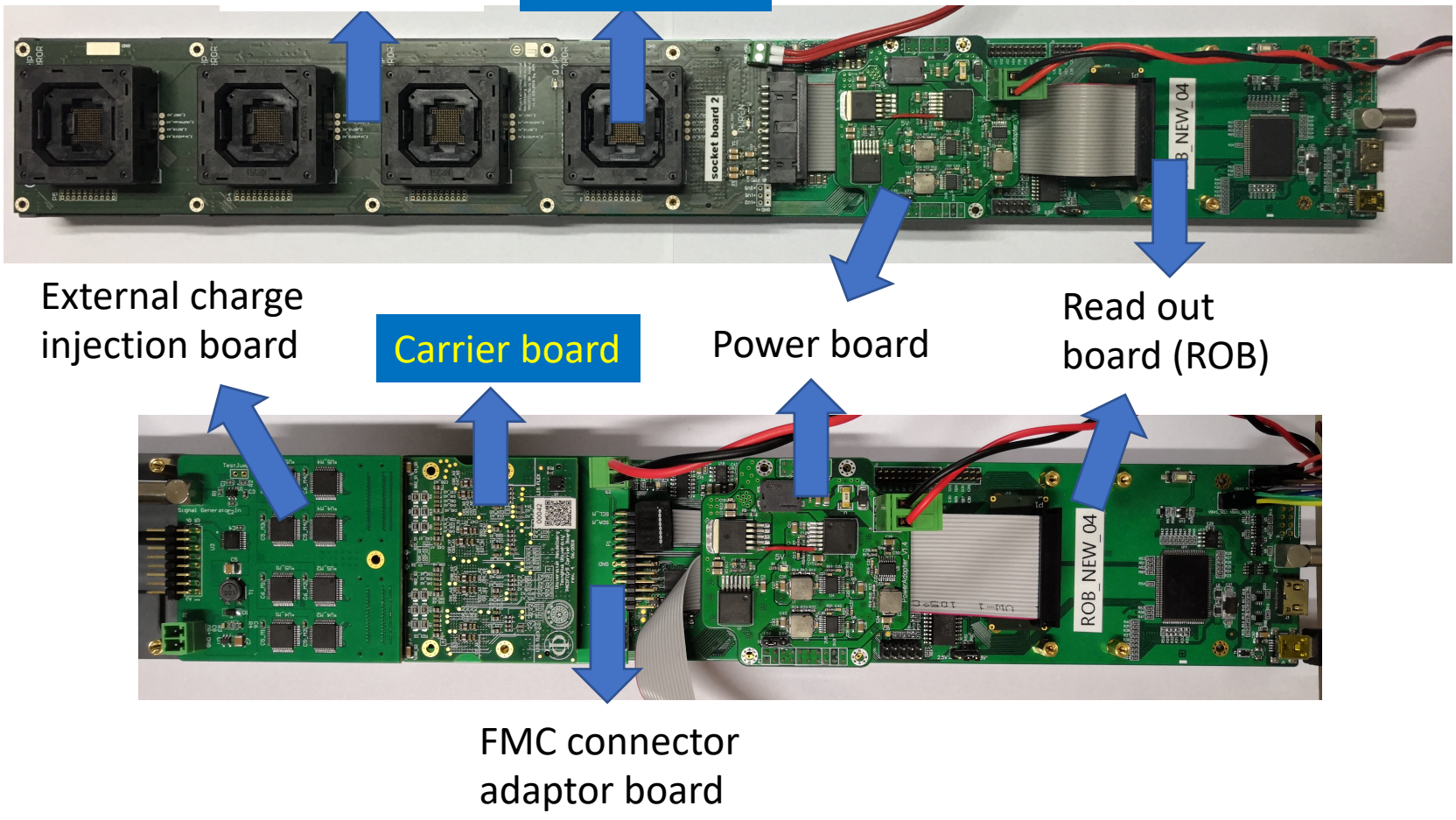


back view
of the PACIFIC Carrier Board

2500 Carrier Boards to be tested
(need 2048 Boards and +10% as space)

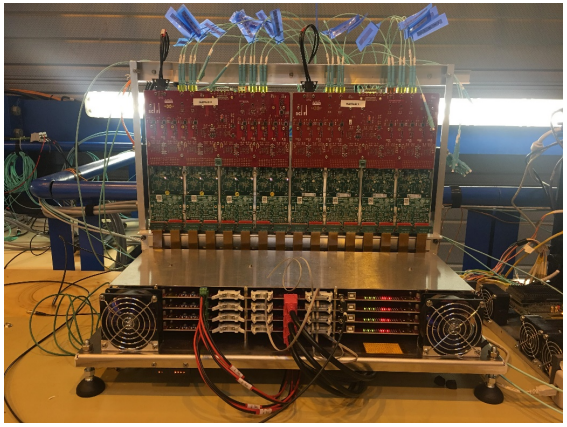
All test results are uploaded to the database

PACIFIC QA system



Production and test of Carrier Boards

- Pre-production (20 boards)
  - Tested at Tsinghua in June for SciFi detector slice test (testbeam at CERN)
- 1st production (228 boards)
  - Tested at Tsinghua in September, and delivered to CERN
  - 32 boards have been put onto Prototype C-Frame
  - The rest will be put onto 1st C-Frame of SciFi Tracker in January 2019
- Future production (2500 boards)
  - To be tested at Tsinghua and Valencia



Read-Out Box (ROB) test setup

Putting first production-version ROB onto Prototype C-Frame

PACIFIC ASIC QA routine

- Check current overflow
- Measure power consumption
- Check I^2C communication
- Check pins function
- Determine the unique operating parameters
  - Vref = +0.5V and VrefDCFB = +0.7V
- Check data output connection
- Check input connection
- Dynamic range tests of the common and local thresholds
- Threshold scan for three conditions and check baseline distributions

These two parameters will be uploaded to the database and then loaded in the Carrier Board QA

Key information, summary report (pdf file) and raw data (root file) will be uploaded to the database

Database structure for ASIC

name of the field	content	comment
Inventory	DB ID, generated once created in DB	e.g. EPB12345
Origin	Institute	
Arrived/Tested	Date for the board arriving time and test time	
initial current [mA]	ASIC current with default ASIC settings right after power on	
configured current [mA]	ASIC current after setting the correct value for Vref, VrefDCFB	
ASIC Failure	Failure type of the ASIC QA	
Vref	DAC value corresponding to Vref = +0.5V	To be loaded in Carrier Board QA
VrefDCFB	DAC value corresponding to VrefDCFB = +0.7V	To be loaded in Carrier Board QA
Summary report/Raw data	.conf/.pdf/.root	Details in latter slides
PACIFIC Boards	Link to the PACIFIC Board that carries this ASIC	To be linked in Carrier Board QA

Inventory	Origin	ID	Arrived	Tested	Location	Dimensions [mm x mm x mm]	Weight [kg]	Material composition	Comment	Initial current [mA]	Configured current [mA]	Failure	Vref	VrefDCFB	Summary report [.pdf]	Raw data [.root]	PACIFIC Boards
EPA00021	PI	PACIFIC5_Q-A2000	2018-05-26	2018-06-07						435.8	511.8	trimDAC_fails	29	8	PACIFIC5_Q-A2000.pdf 2018-06-07 22:40:22 by Xiaoxue Han	rawData_AsicQA_testsystem7_ASICID_PACIFIC5_Q-A2000.root 2018-06-07 22:40:25 by Xiaoxue Han	1
EPA00023	PI	PACIFIC5_Q-A2001	2018-05-26	2018-06-07						413.8	512.2	Working	25	7	PACIFIC5_Q-A2001.pdf 2018-06-07 22:40:29 by Xiaoxue Han	rawData_AsicQA_testsystem7_ASICID_PACIFIC5_Q-A2001.root 2018-06-07 22:40:32 by Xiaoxue Han	0

PACIFIC Carrier Board QA routine

- Check current overflow (the same as ASIC QA)
- Measure power consumption
- Read the unique 1-wire board ID
- Check I^2C communication (the same as ASIC QA)
- Check the voltage sensor
- Check pins function (the same as ASIC QA)
- Set the unique operating parameters (Vref = +0.5V and VrefDCFB = +0.7V)
- Check data output connection (the same as ASIC QA)
- Trim baselines of 64×2 integrators in each ASIC
- Check input connection with external charge injection

Key information, configure file with all parameters, summary report (pdf file) and raw data (root file) will be uploaded to the database

The configure file can be accessed later by SciFi readout system

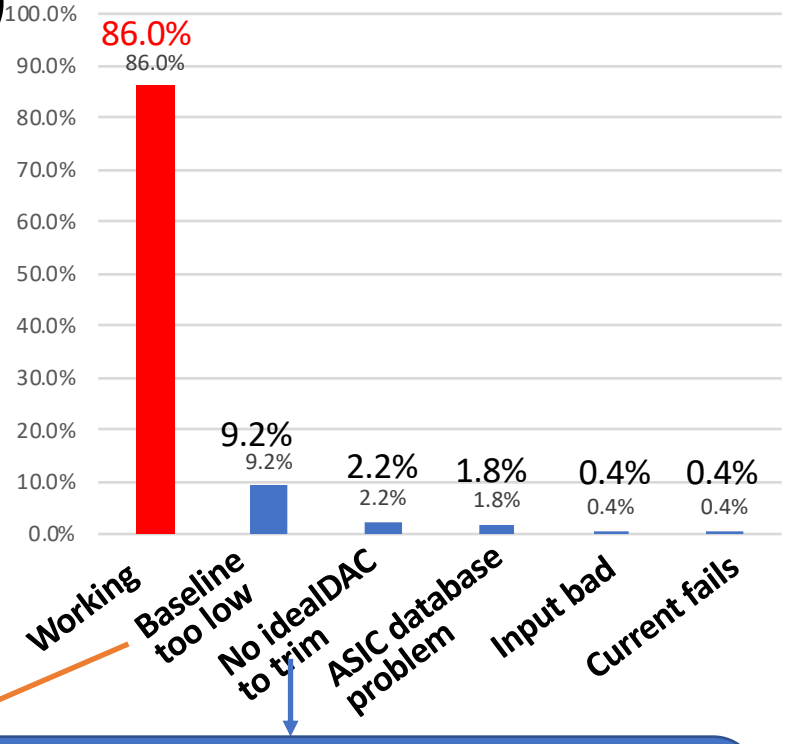
- **To make baselines of 2 integrators in the same channel almost the same (<3 DAC, ~7 mV) to avoid different efficiencies of different bunch collisions**
- **To tune baselines of as many channels as possible to be the same to reduce the charge sharing due to the variation of baselines**

Database structure for Carrier Board

name of the field	content
Inventory	DB ID, generated once created in DB
Origin	Institute
ID	Unique 1-wire ID for each board
Arrived/Tested	Date for the board arriving time and test time
Dimensions/Weight/Material composition	board dimension in mm, weight in kg and material info
initial current [mA]	board current with default ASIC setting right after power on
configured current [mA]	board current after loading the correct value for Vref, VrefDCFB
Board Failure	Failure type of the Board QA
ASIC0/1/2/3	Link to 4 ASICs in DB
ASIC Failure	Link to ASIC QA failure type automatically
Number of untrimed channels ASIC0/1/2/3	For each ASIC : number of channels that baseline difference between Top and Bottom integrators > 2.5
max_abs(T-B) ASIC0/1/2/3	For each ASIC: maximum baseline difference between Top and Bottom
Ideal_ASIC0/1/2/3 [charge1_DClevel]	For each ASIC: the target tuned value for the baseline, when chargeInjection = enable, chargeAmp = 1
Number of uniform channels ASIC 0/1/2/3	For each ASIC: after trimDAC tuning, total number of channels which baseline = ideal±2.5, T-B <2.5
Config file/Summary report/Raw data	.conf/.pdf/.root

Carrier Board test results

- 228 Carrier Boards (1st production)
  - 196 Boards working
  - 32 Boards failed
    - 21 for the baseline is too low
    - 5 for they cannot find the ideal DAC to trim
    - 4 for ASIC database problems
    - 1 for input bad
    - 1 for current fail



After trimming, the baseline of any channel is too low, possibly out of the range (0-255 DAC), difficult to calibrate

The trim margin (overlap of the trim ranges) of two integrators inside one channel is too small

Tune ASIC QA criteria for future test

- More stringent ASIC QA criteria can increase the yield of working Carrier Boards in future production
  - Discard "baseline too low" ASICs in ASIC QA:
    ➔ To reduce "baseline too low" boards in Board QA
  - Discard "small trim margin" ASICs in ASIC QA:
    ➔ To reduce "no idealDAC to trim" boards in Board QA
  - Discard "large baseline variation" ASICs in ASIC QA:
    ➔ To reduce the charge sharing due to the variation of baselines
- The new criteria will select around 75% good ASICs
- A yield of more than 90% working Carrier Boards is expected

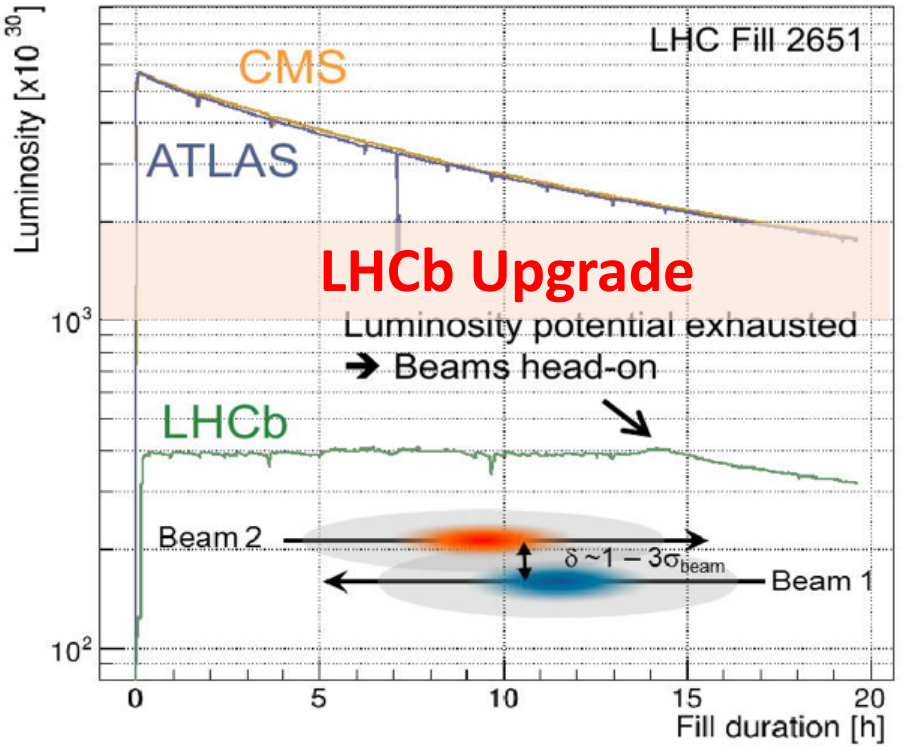
Summary

- Scintillating Fibre (SciFi) Tracker is designed for LHCb upgrade
  - 40 MHz readout, software trigger only
- The first several batches of ASICs and Carrier Boards have been produced and tested
  - The yield of working Carrier Boards is 86%
  - The ASIC QA criteria are tuned for future test based on the Carrier Boards test results
  - 32 Carrier Boards have been put onto Prototype C-Frame
- 23000 ASICs are being tested now in Barcelona
- 2500 Carrier Boards will be tested in Tsinghua and Valencia next year

Thank you

Backup

How to increase the LHCb statistics significantly?

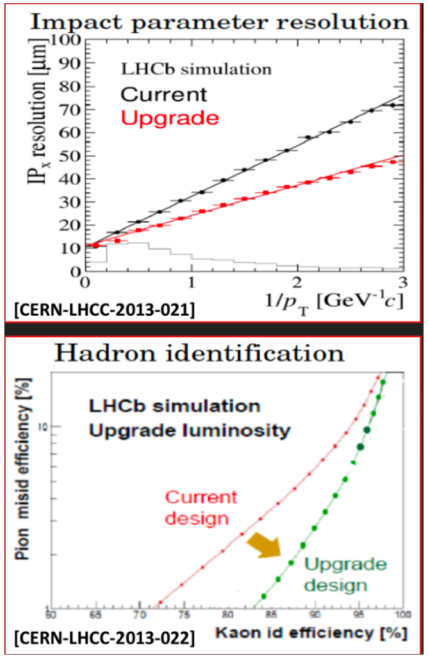


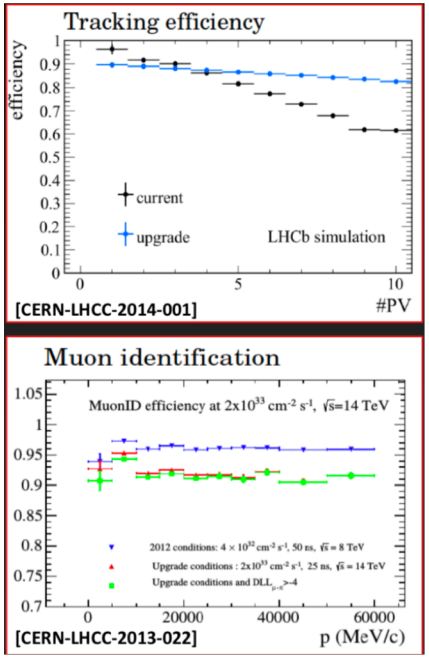
- **LHCb up to LS2 (2018)**
  - **Running at levelled luminosity of $\sim 4\times10^{32}\ \mathrm{cm^{-2}s^{-1}}$, pile-up~1**
  - **First level hardware trigger running at event rate ~1 MHz**
  - **Record ~12 kHz (0.6 GB/s)**
- **LHCb Upgrade I (2021-)**
  - **Increase luminosity to a levelled $1-2\times10^{33}\ \mathrm{cm^{-2}s^{-1}}$, pile-up~5**
  - **Run fully flexible and efficient software trigger up to 40 MHz**
  - **Record with 2-5 GB/s**

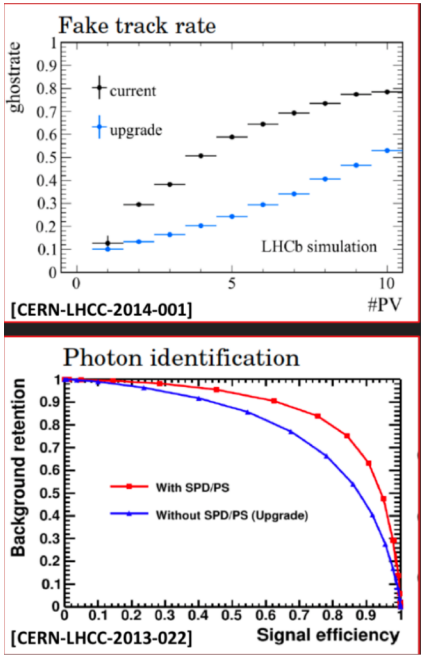
The most severe bottlenecks:
- **Hardware trigger limited to ~ 1 MHz**
- **Tracking reconstruction**

Expected detector performance

- Compare upgraded LHCb with current LHCb in upgrade condition
  - Resolution improved, efficiency increased, fake rate decreased

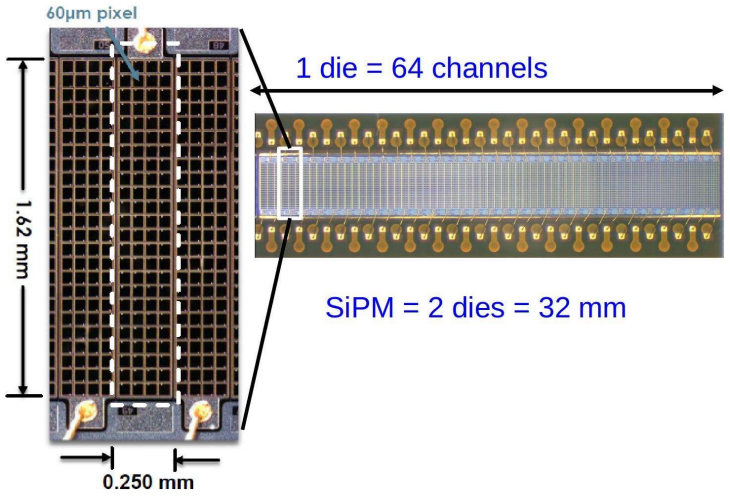


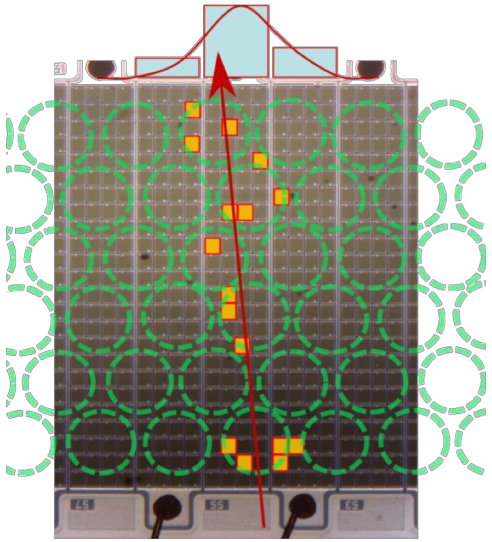




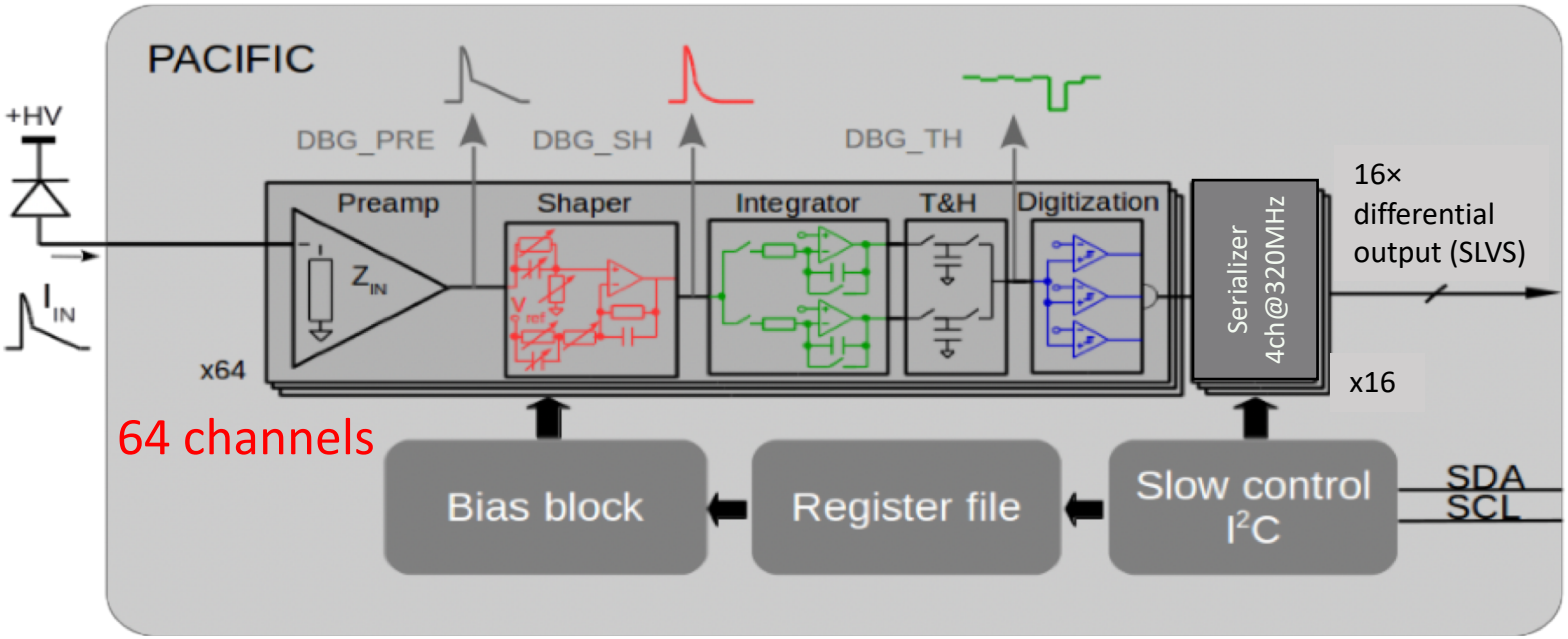
SiPM arrays

- 4 SiPM arrays per fibre mat
- 64 + 64 channels per array (2 dies)
- 96 pixels per channel
- Signal generation
  - The photons produced along the trajectory of the particle are propagated to the fibre end and further to the SiPM
  - Each pixel can detect one photon
  - The signal amplitude per channel is proportional to the total number of fired pixels
  - The position can be calculated with a weighted mean value of the channel signal





PACIFIC ASIC



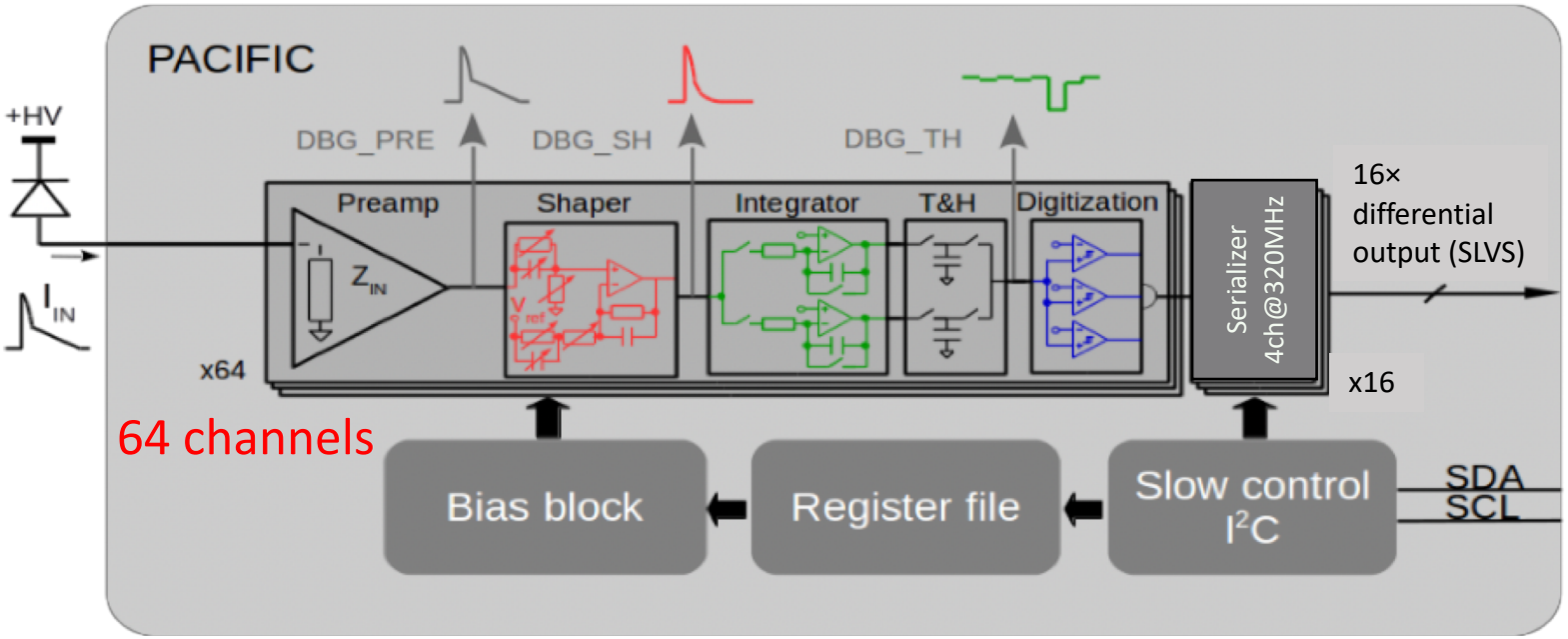
- Pre-amplifier:

It has a double feedback loop that sets the desired DC voltage at the input node and keeps at the same time a low input impedance over a broad bandwidth

- Shaper:

It has a function to reduce the peak duration of the signal to integrate as much signal as possible in the minimum time

PACIFIC ASIC



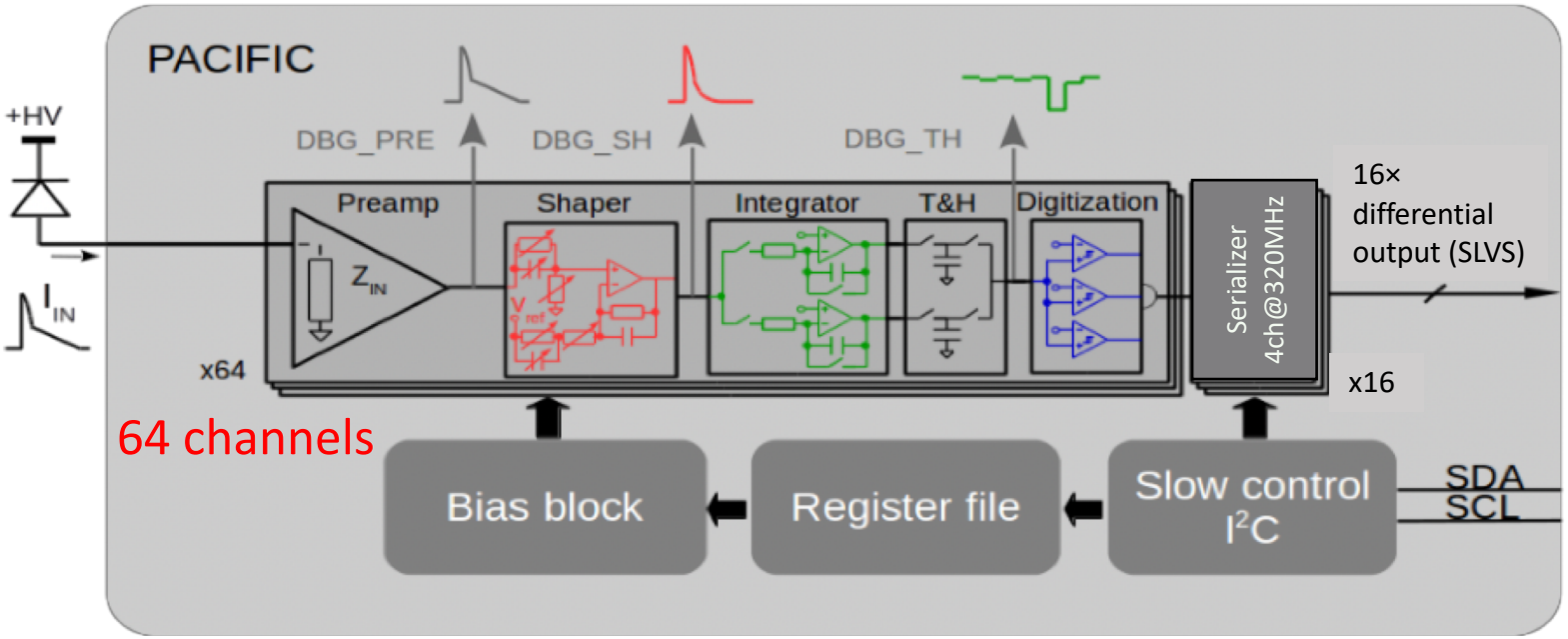
- Integrator:

It is formed by two interleaved gated integrators (top and bottom) switching at half the system clock frequency (20MHz), allowing to reduce the dead time almost to zero

- Offset trim:

A configurable block with trimDACs allows to individually fine tune the DC voltage of each integrator (2 per channel)

PACIFIC ASIC



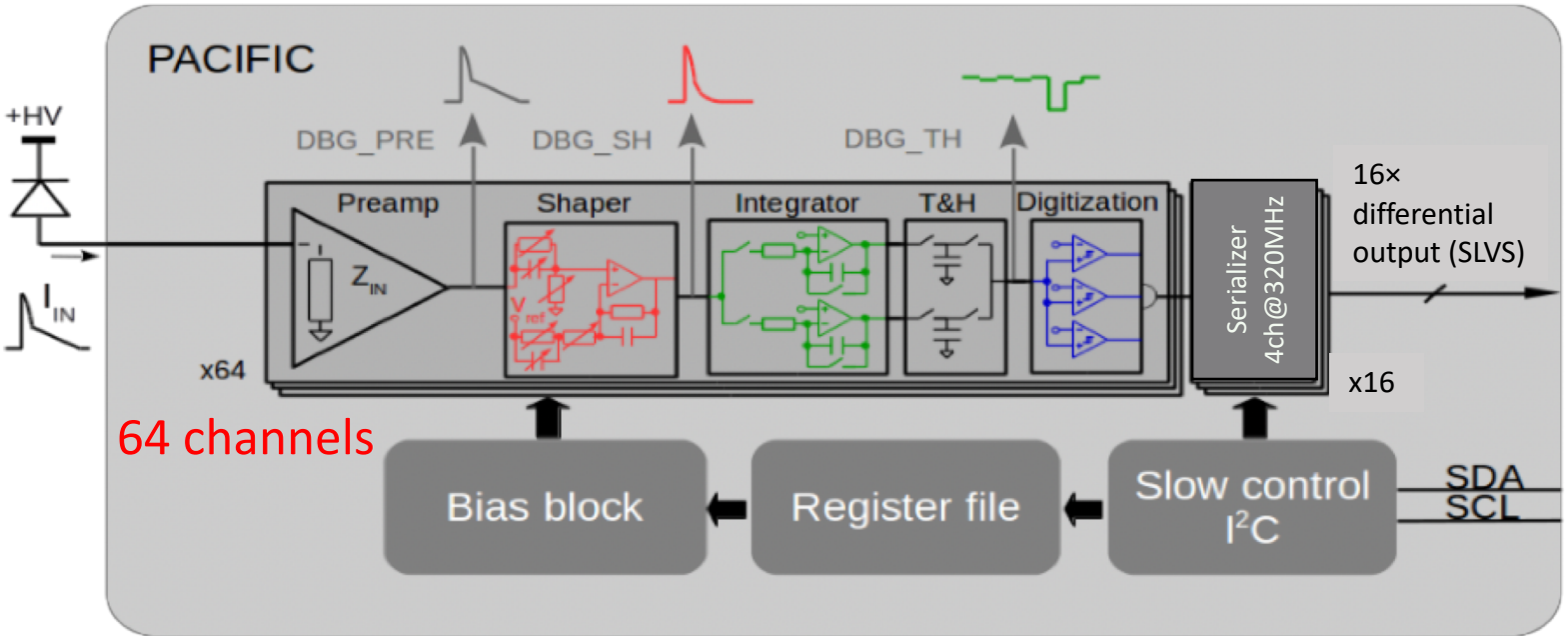
- Track and Hold:

Two single ended track and hold circuits based on gated capacitors are used to mix the two signals and keep the output stable between clock edges

- Digitization:

The conversion from analog to digital is based on three comparators with configurable thresholds

PACIFIC ASIC



- Bias block and Slow control:

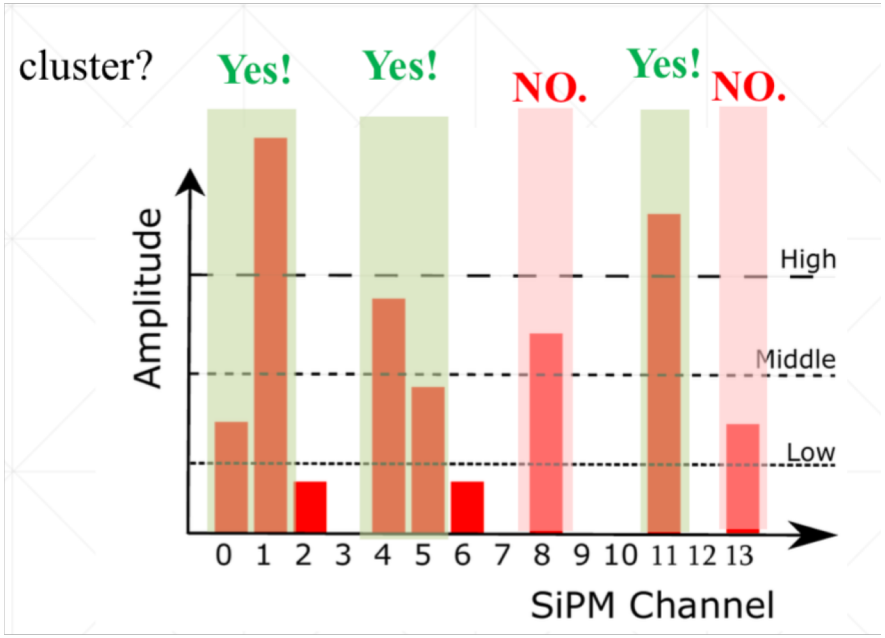
It is to set the correct operation points of the circuit and configure tunable parameters, controlled by a I^2C-standard slow control block

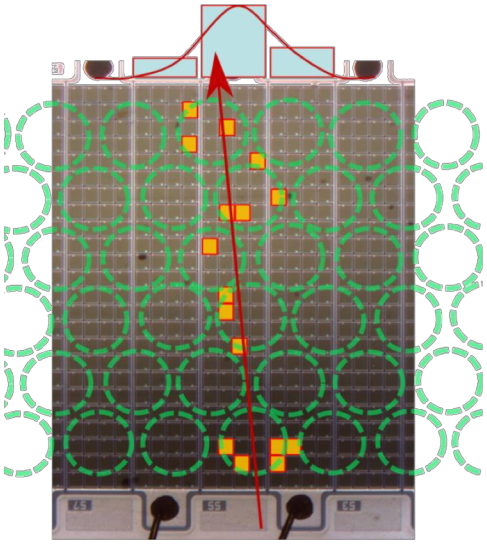
- Encoder and Serialization

It generates a bit stream at 320MHz, encoding the three outputs of each channel comparators in 2 bits and concatenating the encoded output of 4 channels

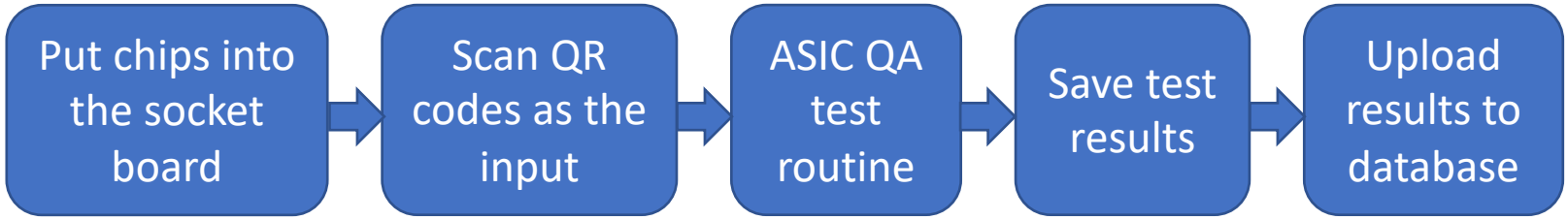
Digitization and Clusterization

- Three thresholds based on the cluster algorithm
  - **Low** threshold: noise suppression
  - **Middle** threshold: cluster candidate, need to test its neighbours
  - **High** threshold: signal channel cluster
- The cluster algorithm is executed by the FPGAs in the Cluster Boards





PACIFIC ASIC QA test flow



- Average time for testing 4 ASICs is around 6 min
- ASIC QA test routine
  - Check PACIFIC ASIC version
  - Check current overflow
  - Measure power consumption
  - Check I^2C communication
  - Check pins function
  - Determine the unique operating parameters
    - Vref = +0.5V and VrefDCFB = +0.7V
  - Check data output connection
  - Check input connection
  - Dynamic range tests of the common and local thresholds
  - Threshold scan for three conditions and check baseline distributions

ASIC QA criteria (failure type)

- Check PACIFIC ASIC version
  - If not 5q version, discard it
- Check current overflow
  - If overflow, discard it
- Measure power consumption
  - Measure initial current with default ASIC settings right after power on
  - Measure configured current after setting Vref = +0.5V and VrefDCFB = +0.7V
  - If initial or configured core current > 600mA or IO current > 1mA, mark the ASIC as current_fail
  - The criteria are determined by pre-test of about 100 ASICs and checked by formal tests
- Check I^2C communication
  - If I^2C communication doesn't work, mark the ASIC as I2C_fail

ASIC QA criteria (failure type)

- Check pins function
  - If the pin doesn't work, mark the ASIC as nRESET_bad, LDINIT_bad, ERR1GEN_bad, REFRESH_bad, DISACLK_bad or SYNC_bad

Pin name	Type	Description
nRESET	Digital in	General digital reset
LDINIT	Digital in	Forces configuration registers to load the initial values hardcoded in the slow control logic
ERR1GEN	Digital in	Pin to force error on digital memory (for debugging purposes)
REFRESH	Digital in	Refresh from error flags
DISACLK	Digital in	Disable of I^2C clock (to avoid noise on analog)
SYNC	Digital in	Reset for clock divider to generate integration clock (20MHz) from main system clock (320MHz)

ASIC QA criteria (failure type)

- Determine the unique operating parameters
  - Vref Scan, determine the corresponding DAC value for Vref = +0.5V and set it as the unique operating parameter
  - VrefDCFB Scan, determine the corresponding DAC value for VrefDCFB = +0.7V and set it as the unique operating parameter
  - If the step size of Vref is not in the range of [-7mv/DAC, -5.7mV/DAC], mark the ASIC as Vref_bad
  - If step size of VrefDCFB not in the range of [-7.7mv/DAC, -6.3mV/DAC], mark the ASIC as VrefDCFB_bad
  - The criteria are determined by pre-test of about 100 ASICs and checked by formal tests

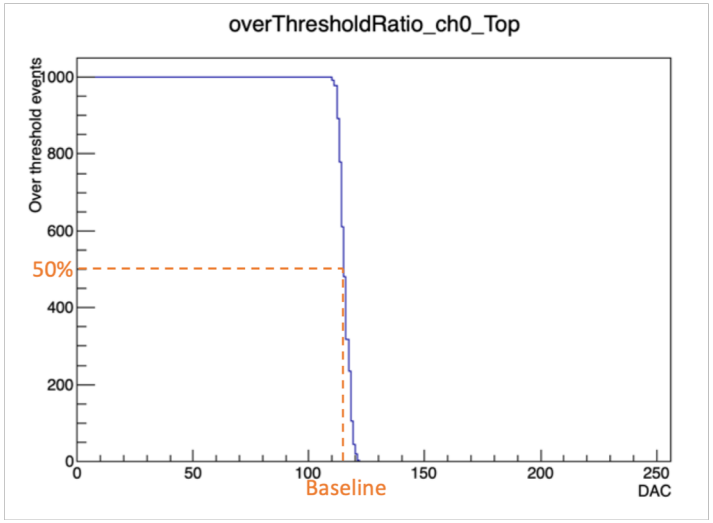
Pin name	Type	Description
Vref	Analog out	Voltage reference used for common bias, after DAC and derived from Bandgap Reference
VrefDCFB	Analog out	Reference voltage for slow feedback loop amplifier, to be decoupled with external capacitor

ASIC QA criteria (failure type)

- Check data output connection
  - If some data output doesn‘t sample 100% correctly during pattern injection, mark the ASIC as data_output_bad
- Check input connection
  - If a short or open circuit is detected at the ASIC input, mark the ASIC as input_bad
- Dynamic range tests of the common and local thresholds
  - Each ASIC (64 channels) has 3 common comparators and each channel has 3 local comparators
  - If the step size of common thresholds is not in the range of [-2.93mv/DAC, -2.25mV/DAC], mark the ASIC as commonThresholds_bad
  - If the step size of local thresholds is not in the range of [-2.93mv/DAC, -2.25mV/DAC], mark the ASIC as localThresholds_bad
  - The criteria are determined by pre-test of about 100 ASICs and checked by formal tests

ASIC QA criteria (failure type)

- Threshold scan for three conditions and check baseline distributions
  - Each channel has 2 integrators (top and bottom)
  - Prepare for trimming baselines in Carrier Board QA: set different trimDACs for 128 integrators to make there baselines almost the same
  - Use a common comparator to perform the threshold scan, get the baseline (the 50% over threshold DAC value) from the S-Curve
  - Set trimDAC = 0 (minimum), 31 (maximum), and 16 (default), get baselines of 128 integrators
  - Calculate the margin, the min value of 128 baselines when trimDAC = 31 minus the max value of 128 baselines when trimDAC = 0
  - If the margin < 4, mark the ASIC as trimDAC_fail



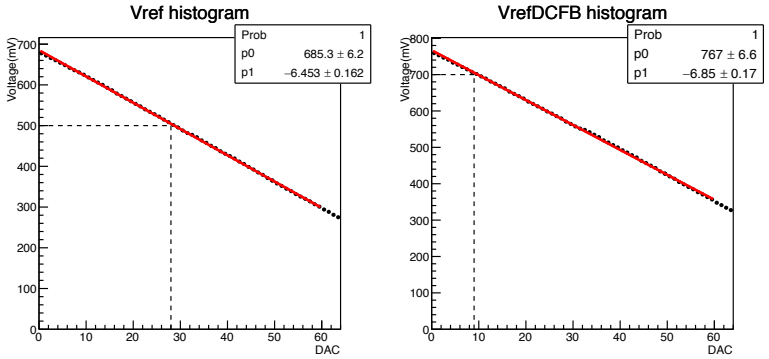
Example of a S-Curve

Output of ASIC QA

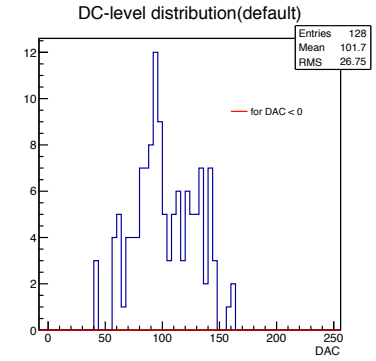
- A test log (.log) to record the results to be uploaded to the database
- A summary report (.pdf) to display histograms of Vref scan, VrefDCFB scan, step sizes of common and local thresholds and baseline distributions for three conditions
- A raw data file (.root) which stores detailed information of the test

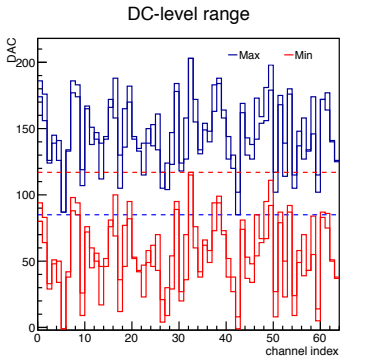
- The .pdf/.root files will also be uploaded to the database

Example of the summary report

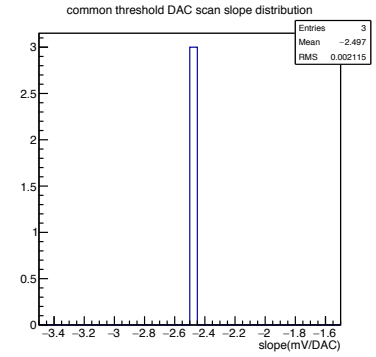


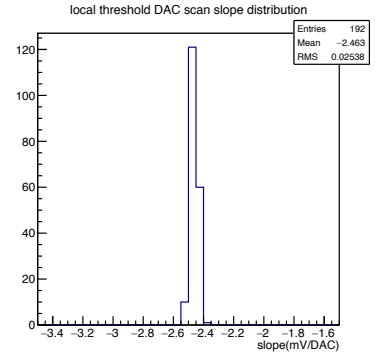
Vref scan (left) and VrefDCFB (right) scan results with linear fits





Baseline distribution with default trimDACs (left) and baseline range with max and min trimDACs (right), where the x-axis is channel index, the y-axis is DAC of baseline, and blue for max, red for min.





Step size distribution of common (left) and local (right) thresholds

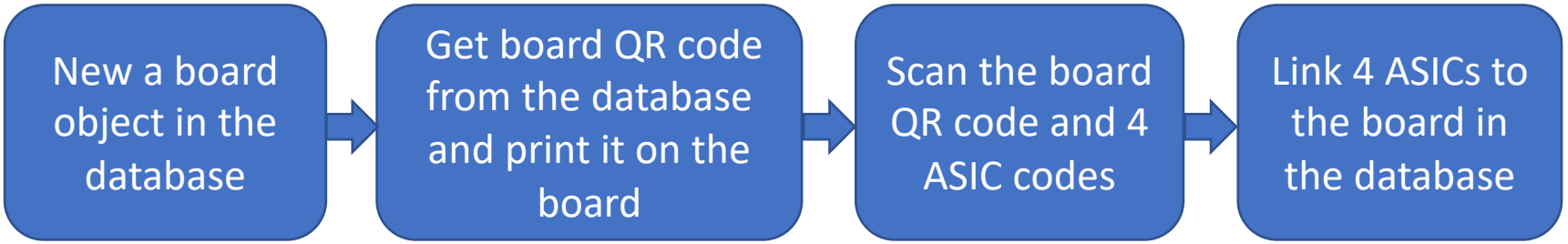
Example of the raw data

- Each ASIC has its own raw data file, with the name *rawData_ASICQA_ASICID_XXXXXXXX.root*, which contains:

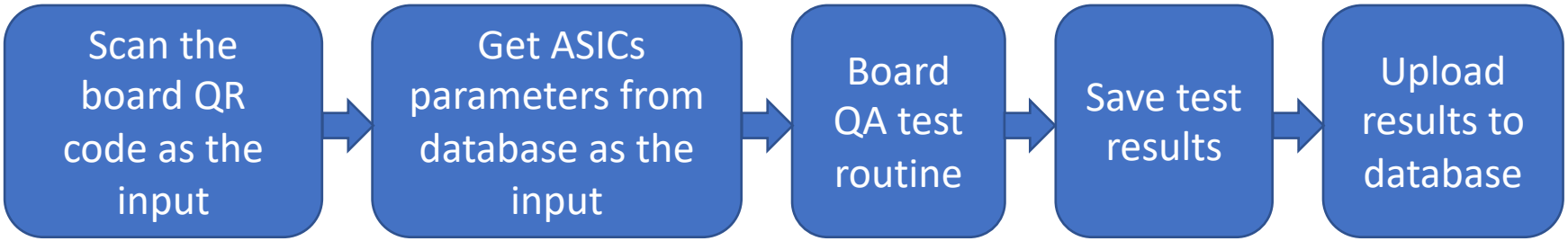
```
TFile**         rawData_AsicQA_ASICID_PACIFIC5_Q09830.root
 TFile*         rawData_AsicQA_ASICID_PACIFIC5_Q09830.root
  KEY: TH1F     Vref;1  Vref histogram
  KEY: TH1F     VrefDCFB;1      VrefDCFB histogram
  KEY: TH1F     CommonVth1;1    Common Vth1 histogram
  KEY: TH1F     CommonVth2;1    Common Vth2 histogram
  KEY: TH1F     CommonVth3;1    Common Vth3 histogram
  KEY: TDirectoryFile   localVth1;1     localVth1
  KEY: TDirectoryFile   localVth2;1     localVth2
  KEY: TDirectoryFile   localVth3;1     localVth3
  KEY: TDirectoryFile   trimDAC_minimum;1       trimDAC_minimum
  KEY: TDirectoryFile   trimDAC_maximum;1       trimDAC_maximum
  KEY: TDirectoryFile   trimDAC_default;1       trimDAC_default
  KEY: TTree    testResults;1   test results
  KEY: TH1F     commonSlope;1   common threshold DAC scan slope distribution
  KEY: TH1F     localSlope;1    local threshold DAC scan slope distribution
  KEY: TH1F     TrimMinTop;1    DC-level range
  KEY: TH1F     TrimMinBottom;1 DC-level range
  KEY: TH1F     TrimMaxTop;1    DC-level range
  KEY: TH1F     TrimMaxBottom;1 DC-level range
  KEY: TH1F     TrimDefTop;1    DC-level range
  KEY: TH1F     TrimDefBottom;1 DC-level range
  KEY: TH1F     BaselineDistribution;1  DC-level distribution(default)
```

PACIFIC Carrier Board QA test flow

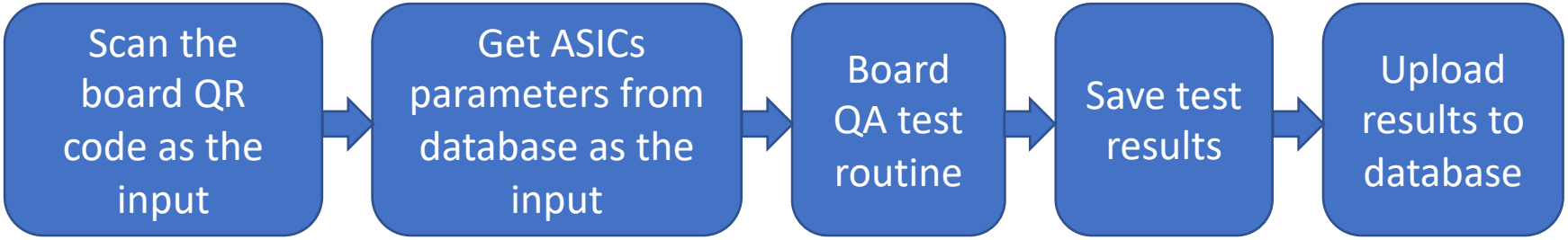
- Preparation



- Test flow



PACIFIC Carrier Board QA test flow



- Average time for testing a Carrier Board is around 8min
- Board QA test routine
  - Check current overflow (the same as ASIC QA)
  - Measure power consumption
  - Read the unique 1-wire board ID
  - Check I^2C communication (the same as ASIC QA)
  - Check the voltage sensor
  - Check pins function (the same as ASIC QA)
  - Set the unique operating parameters (Vref = +0.5V and VrefDCFB = +0.7V)
  - Check data output connection (the same as ASIC QA)
  - Trim baselines of 128 integrators in each ASIC
  - Check the baselines with local thresholds with no charge injection
  - Check input connection with external charge injection

Board QA criteria (failure type)

- Measure power consumption
  - Measure initial current of the board with default settings right after power on
  - Measure configured current of the board after setting Vref = +0.5V and VrefDCFB = +0.7V in each ASIC
  - If initial or configured core current > 2200mA or IO current > 1mA, mark the board as current_fail
  - The criteria are determined by pre-test of about 30 boards and checked by formal tests
- Read the unique 1-wire board ID
  - If the read ID = 0xfff…fff, mark the board as readID_fail
- Check the voltage sensor
  - Apply 30V on Vbias externally, check the ADC value
  - If the ADC value < 200, mark the board as voltageSensor_fail
  - This criterion is determined by pre-test of about 30 boards and checked by formal tests

Board QA criteria (failure type)

- Trim baselines of 128 integrators in each ASIC
  - Original goal: make baselines of 128 integrators the same (<3DAC, ~7mV)
  - Current goal:
    - make baselines of top and bottom integrators in the same channel the same (<3DAC, ~7mV) to avoid different efficiencies of different bunch collisions
    - make as much as possible channels have the same baselines
    - for channels having the same baselines, use common comparators to set thresholds; for the rest channels, use local comparators
  - Loop for several times to find the best trimDACs
  - When trimming, if it cannot find the ideal DAC to trim, mark the board as no_ideal_value
  - After trimming, if abs(Top-Bottom) of any channel > 2.5, mark the board as trimDAC_fail

Board QA criteria (failure type)

- Check the baselines with local thresholds with no charge injection
  - Use local thresholds to get baselines
  - After trimming, if the baseline of any channel with no charge injection < 5, mark the board as baseline_too_low, to ensure that the baseline is in the range of local comparators
- Check input connection with external charge injection
  - Select one channel to inject charge, and set the threshold for each channel to be baseline+10
  - OPEN if selected channel is under the threshold
  - SHORT if any other channel is over the threshold
  - If OPEN or SHORT, mark the board as input_bad

Output of a Carrier Board QA

- A test log (.log) to record the results to be uploaded to the database
- A configuration file (.conf) to store all parameters
  - Can be accessed later by SciFi readout system
- A summary report (.pdf) to display histograms of DC-baseline distribution after trimming
- A raw data file (.root) which stores detailed information of the test

The .conf/.pdf/.root files will also be uploaded to the database.

Example of the config file

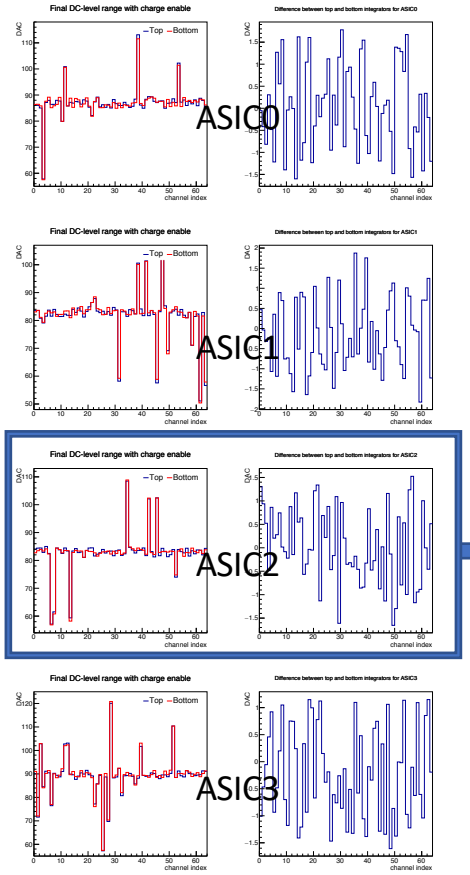
```
[BoardInfo]
BoardID=12ca1a000061
ASIC0ID=PACIFIC5_Q-A2111
ASIC1ID=PACIFIC5_Q-A2214
ASIC2ID=PACIFIC5_Q-A2084
ASIC3ID=PACIFIC5_Q-A2288

[asicID_0]
commonRegister\vth1=45
commonRegister\vth2=58
commonRegister\vth3=84
commonRegister\vrefDCFB=10
commonRegister\BLHen=true
commonRegister\THOFFen=false
commonRegister\THOFF=90
commonRegister\iDCFB=53
commonRegister\iSHGRAL=200
commonRegister\ibias=29
commonRegister\gain=3
commonRegister\ifbk=221
commonRegister\vref=29
commonRegister\irefTRIM=34
commonRegister\irefOTALP=10
commonRegister\Itxslvs=false
commonRegister\lowAtlad_PZ1=false
commonRegister\ibofHam=true
commonRegister\rlad_PZ1=5
commonRegister\cap_PZ1=11
commonRegister\capF_PZ1=false
commonRegister\rlad_PZ2=1
commonRegister\cap_PZ2=13
commonRegister\capF_PZ2=false
debugRegister\dbg_ch=false, false, false, false, false, false, false, false, false,
false, false, false, false, false, false, false, false, false, false, false, false,
false, false, false, false, false, false, false, false, false, false, false, false,
false, false, false, false, false, false, false, false, false, false, false, false,
false, false, false, false, false, false, false, false, false, false, false, false,
false, false, false, false, false, false
debugRegister\dbg_mux=0
debugRegister\dbg_en_out=false
debugRegister\synMode=false
debugRegister\dbg_en_in=false
debugRegister\dbg_Cin=false
debugRegister\dbg_adc_addr=9
debugRegister\dbg_adc_start=false
debugRegister\aLED=false
```

This file can be accessed later by SciFi readout system to obtain the parameters of this carrier board

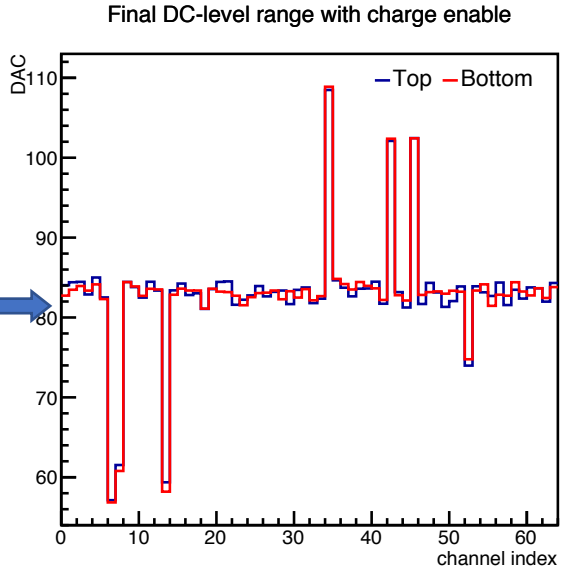
```
channelBlock_0\d_off_mux=8, 8, 8, 8, 8, 8, 8, 8
channelBlock_0\d_trim_tDAC=5, 12, 12, 6, 1, 7, 12, 11
channelBlock_0\d_trim_bDAC=1, 4, 13, 2, 2, 9, 11, 10
channelBlock_0\d_trim_tsign=true, true, false, true, true, false, false, false
channelBlock_0\d_trim_bsign=true, true, false, true, true, false, false, false
channelBlock_0\d_vth1=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_0\d_vth2=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_0\d_vth3=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_0\d_selvth=false, false, false, false, false, false, false, false
channelBlock_1\d_off_mux=8, 8, 8, 8, 8, 8, 8, 8
channelBlock_1\d_trim_tDAC=14, 9, 5, 14, 10, 3, 1, 10
channelBlock_1\d_trim_bDAC=6, 8, 1, 2, 13, 4, 11, 10
channelBlock_1\d_trim_tsign=true, false, true, true, false, false, false, true
channelBlock_1\d_trim_bsign=true, false, true, false, true, false, false, true
channelBlock_1\d_vth1=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_1\d_vth2=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_1\d_vth3=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_1\d_selvth=false, false, false, false, false, false, false, false
channelBlock_2\d_off_mux=8, 8, 8, 8, 8, 8, 8, 8
channelBlock_2\d_trim_tDAC=11, 15, 12, 9, 14, 5, 14, 6
channelBlock_2\d_trim_bDAC=2, 13, 14, 9, 0, 1, 13, 12
channelBlock_2\d_trim_tsign=true, true, false, true, false, true, false, false
channelBlock_2\d_trim_bsign=true, true, false, true, false, true, true, false
channelBlock_2\d_vth1=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_2\d_vth2=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_2\d_vth3=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_2\d_selvth=false, false, false, false, false, false, false, false
channelBlock_3\d_off_mux=8, 8, 8, 8, 8, 8, 8, 8
channelBlock_3\d_trim_tDAC=4, 15, 15, 10, 4, 8, 10, 11
channelBlock_3\d_trim_bDAC=6, 9, 9, 9, 11, 4, 14, 5
channelBlock_3\d_trim_tsign=true, true, true, false, true, false, true, true
channelBlock_3\d_trim_bsign=true, true, false, false, true, false, true, false
channelBlock_3\d_vth1=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_3\d_vth2=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_3\d_vth3=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_3\d_selvth=false, false, false, false, false, false, false, false
channelBlock_4\d_off_mux=8, 8, 8, 8, 8, 8, 8, 8
channelBlock_4\d_trim_tDAC=10, 13, 1, 11, 7, 8, 2, 4
channelBlock_4\d_trim_bDAC=11, 13, 11, 12, 8, 1, 7, 10
channelBlock_4\d_trim_tsign=true, false, true, true, false, true, false, true
channelBlock_4\d_trim_bsign=true, true, true, false, false, true, false, true
channelBlock_4\d_vth1=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_4\d_vth2=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_4\d_vth3=255, 255, 255, 255, 255, 255, 255, 255
channelBlock_4\d_selvth=false, false, false, false, false, false, false, false
channelBlock_5\d_off_mux=8, 8, 8, 8, 8, 8, 8, 8
channelBlock_5\d_trim_tDAC=14, 10, 5, 7, 9, 13, 9, 9
channelBlock_5\d_trim_bDAC=15, 13, 5, 12, 14, 12, 12, 12
channelBlock_5\d_trim_tsign=false, true, false, false, false, false, false, true
```

This example only shows the structure. Some info is omitted.

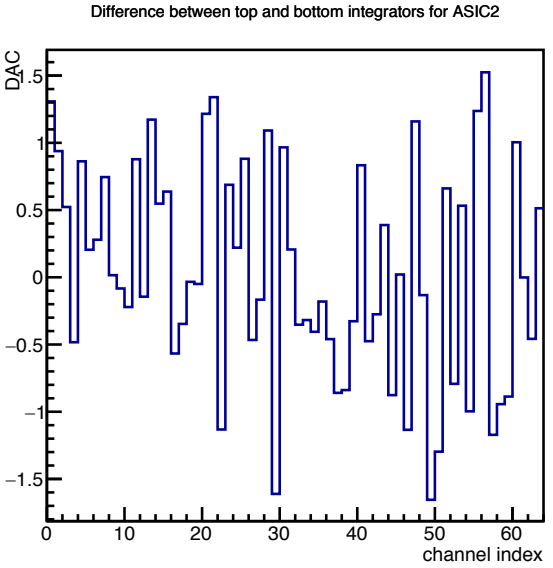
Example of the summary report



The left figure shows the baselines of 64 channels. The x-axis is channel index, and the y-axis is DAC of baseline. Blue for top integrator, and red for bottom.



The right figure shows the baseline differences between top and bottom integrators of 64 channels. The x-axis is channel index, and the y-axis is DAC of difference.



Example of the raw data

- Each board has its own raw data file, with the name *rawData_BoardQA_testsystemXX_Board_XXXXXXXX.root*, which contains:

```
TFile**         rawData_BoardQA_testsystem11_Board_4TSTHUEPB00090.root
 TFile*         rawData_BoardQA_testsystem11_Board_4TSTHUEPB00090.root
  KEY: TDirectoryFile   ASIC0;1 ASIC0
  KEY: TDirectoryFile   ASIC1;1 ASIC1
  KEY: TDirectoryFile   ASIC2;1 ASIC2
  KEY: TDirectoryFile   ASIC3;1 ASIC3
  KEY: TTree    BoardTestResults;1      Board test results
```

- In each ASIC directory:

```
TDirectoryFile*         ASIC0   ASIC0
 KEY: TDirectoryFile    trimDAC_minimum;1       trimDAC_minimum
 KEY: TDirectoryFile    trimDAC_maximum;1       trimDAC_maximum
 KEY: TDirectoryFile    trimDAC_default;1       trimDAC_default
 KEY: TDirectoryFile    trimDAC_withChargeFinal;1       trimDAC_withChargeFinal
 KEY: TDirectoryFile    trimDAC_noChargeFinal;1 trimDAC_noChargeFinal
 KEY: TTree     ASICTestResults;1       test results
 KEY: TH1F      TrimMinTop;1    DC-level range
 KEY: TH1F      TrimMinBottom;1 DC-level range
 KEY: TH1F      TrimMaxTop;1    DC-level range
 KEY: TH1F      TrimMaxBottom;1 DC-level range
 KEY: TH1F      TrimDefTop;1    DC-level range
 KEY: TH1F      TrimDefBottom;1 DC-level range
 KEY: TH1F      TrimWithChargeTop;1     Final DC-level range with charge enable
 KEY: TH1F      TrimWithChargeBottom;1  Final DC-level range with charge enable
 KEY: TH1F      TrimWithChargeDiff;1    Difference between top and bottom integrators for ASIC0
 KEY: TH1F      TrimNoChargeTop;1       Final DC-level range with charge disable
 KEY: TH1F      TrimNoChargeBottom;1    Final DC-level range with charge disable
```

Tune ASIC QA criteria for future test

- The ASIC QA criteria are tuned based on the Carrier Boards test results
  - Add baseline_too_low failure type in ASIC QA:

    When trimDAC = default value, ask the lowest baseline > 20

    ➔ To avoid “baseline too low” failure type in Board QA
  - Add small_trim_margin failure type in ASIC QA:

    Ask the trim margin in each channel > 30

    ➔ To reduce “no idealDAC to trim” failure type in Board QA
  - Add large_baseline_variation failure type in ASIC QA:

    When trimDAC = default value, ask the highest baseline – lowest baseline < 160

    ➔ To reduce the charge sharing due to the variation of baselines
- The new criteria will filter 60% ASICs