LHCb Detector Upgrade

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第四届中国LHC物理工作会议

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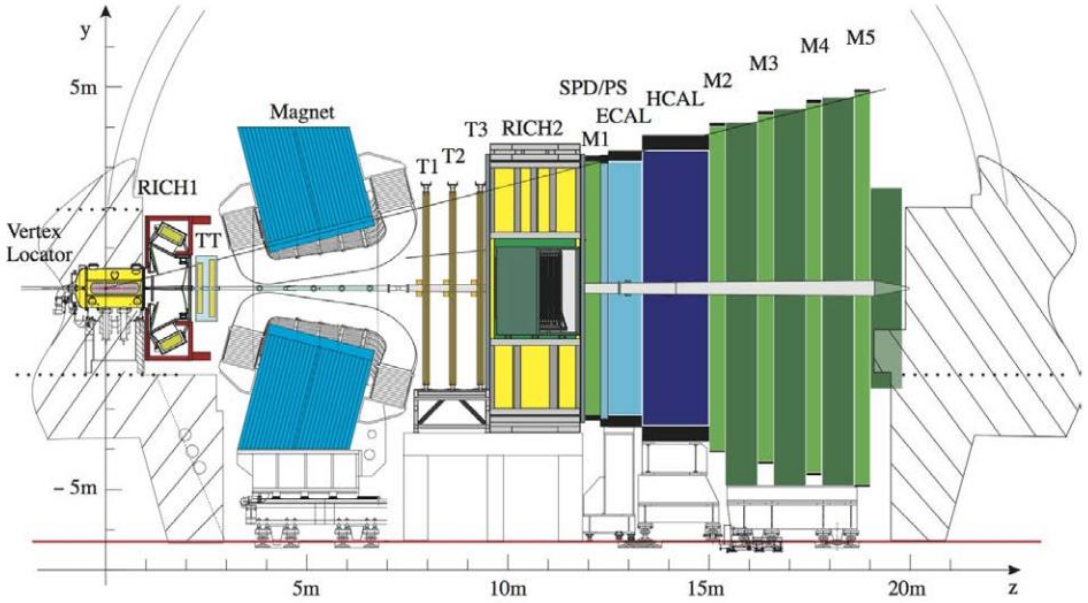
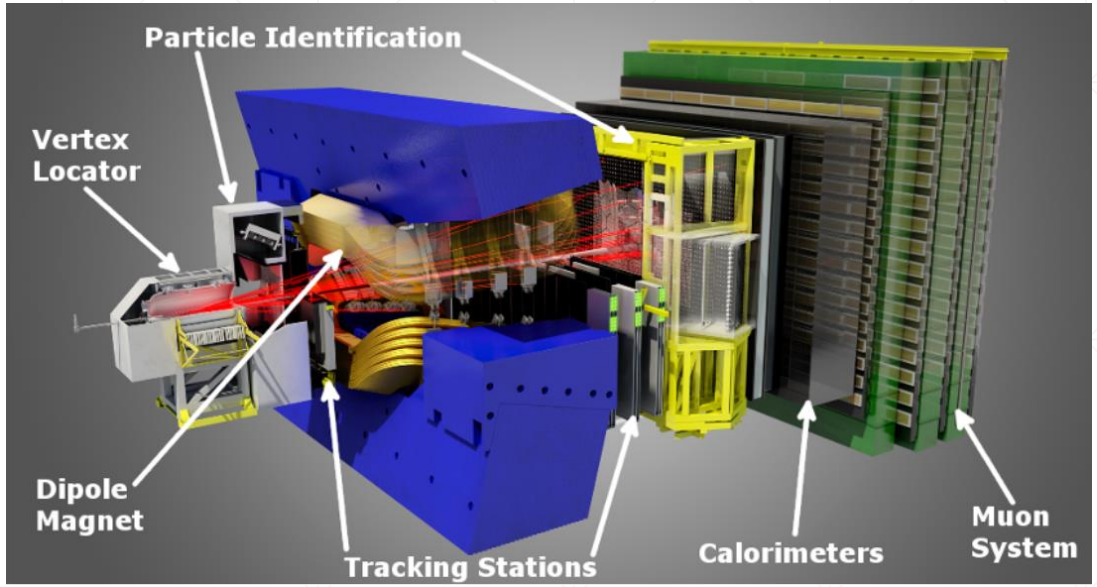
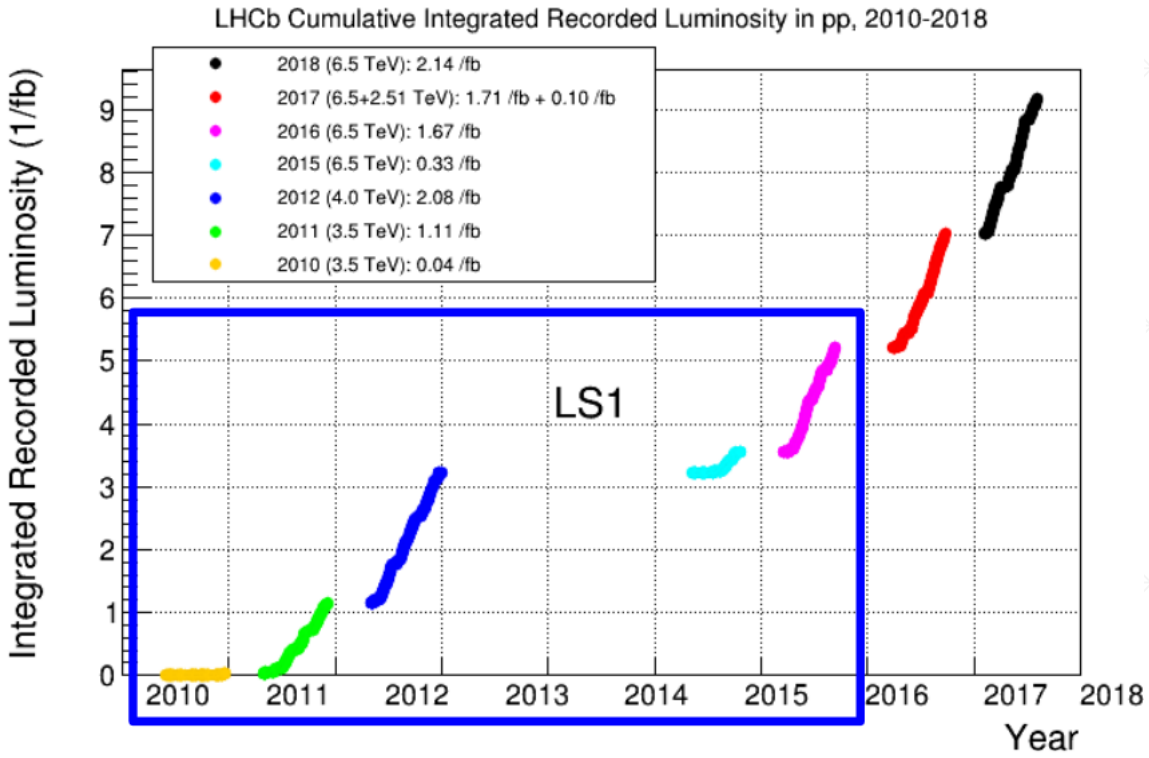
LHCb 主要科学目标与探测器



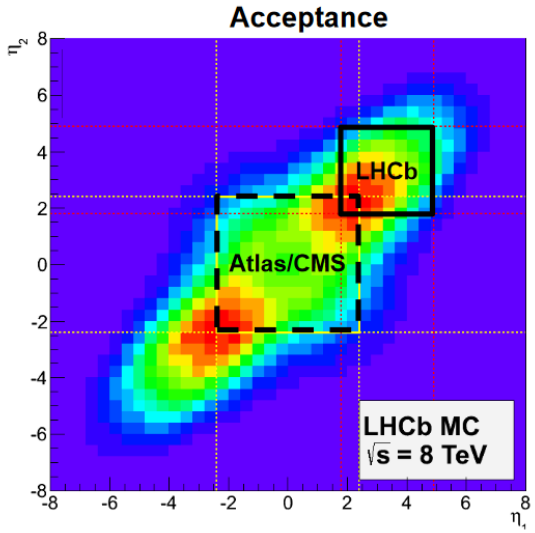


- **理解正反物质不对称：CP破坏**
- **间接发现新物理：稀有衰变**
- **理解强相互作用机制：强子性质，新强子态**
- **其它：电弱物理，重离子物理，…**

LHCb Run 2

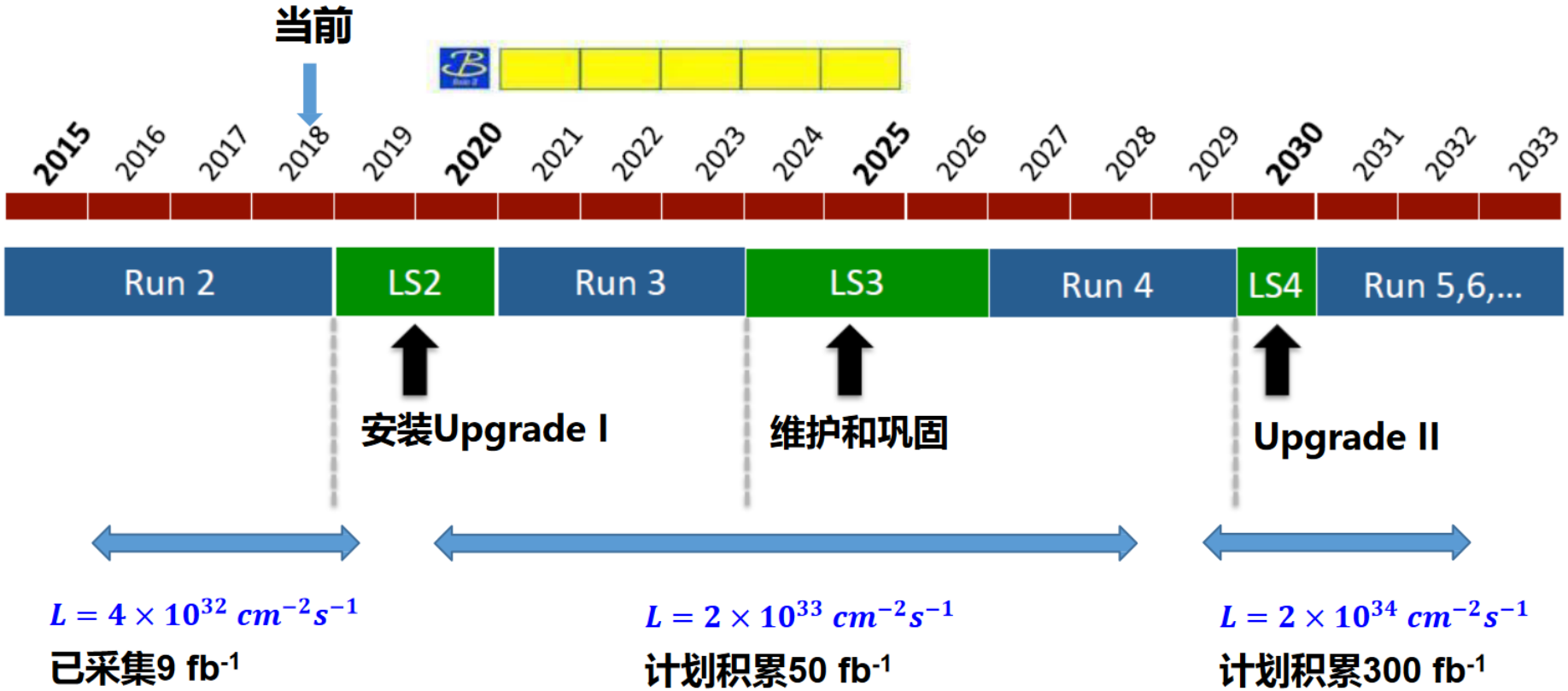


LHCb proved itself to be the Forward General–Purpose Detector at the LHC



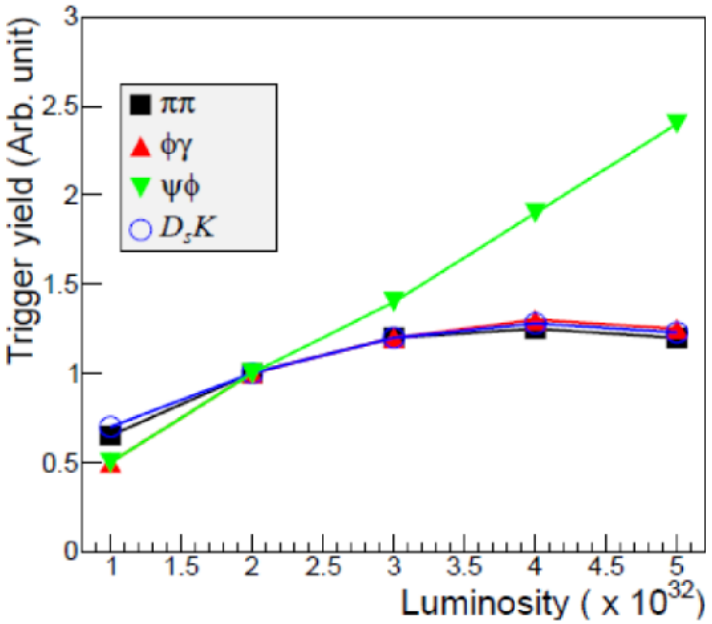
- **运行亮度达到$4 \times 10^{32}\ cm^{-2}s^{-1}$, 两倍于设计指标**
- **积分亮度超过$9fb^{-1}$**

LHCb 未来升级计划



- **Upgrade I**：中国组参与闪烁光纤径迹探测器（SciFi）电子学研发
- **Upgrade II**：希望对探测器有更大贡献，重点开展电磁量能器fast timing 所需的硅探测层研发。**需要相应的经费支持。**

LHCb Upgrade Motivation

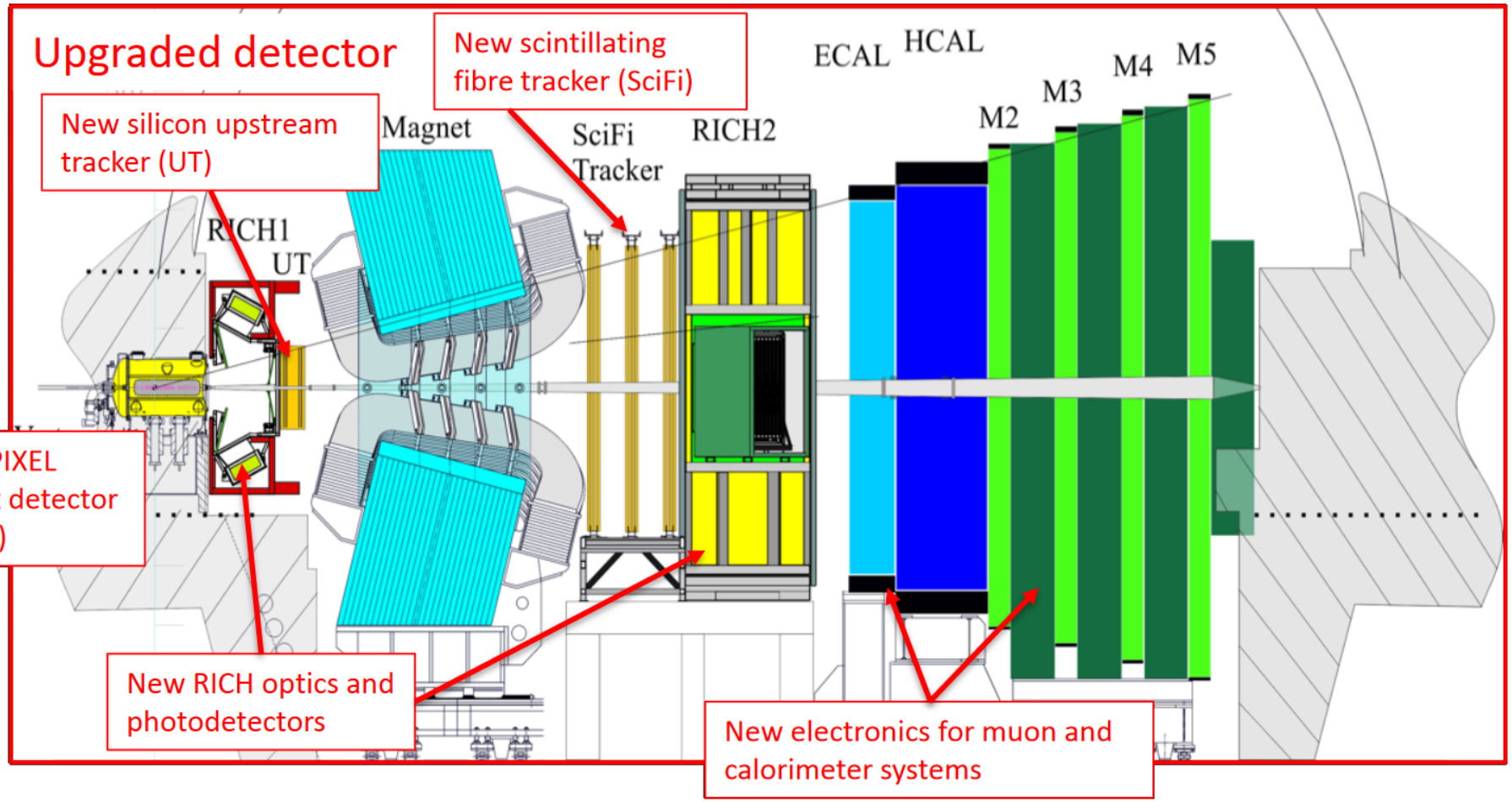


Present L0 hardware trigger (max rate 1 MHz) saturates at high luminosity for hadronic final state modes

LHCb Upgrade I, with installing in 2019-2020 (LHC LS2) and first data-taking in Run 3 (2021-2023).

- ❖ Goal: increase statistics by more than ×10
- ❖ Raise operational luminosity by factor of five to $2\times10^{33}cm^{-2}s^{-1}$
- ❖ Triggerless 40MHz readout (Full software trigger)
- ❖ Necessitates redesign of several sub-detectors and overhaul of readout (40MHz readout rate)
- ❖ Replace tracking detectors (finer granularity to cope with higher particle density)

LHCb Upgrade I



All sub-detectors read out at 40 MHz for a fully software trigger.

LHCb Upgrade I: Tracking - VELO

Current VELO:

21 layers of silicon micro-strips

→ 170 k readout channels

Inside LHC vacuum chamber

→ active area at 8.2 mm from beam

→ separated from beam only by a 300 μm thin aluminium foil

VELO Upgrade:

26 layers of silicon pixel detectors

→ 41 million readout channels

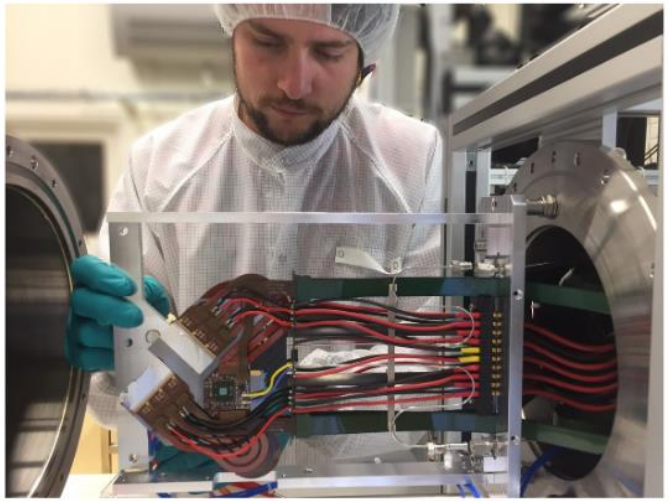
Even closer to beam

→ active area 8.2 → 5.1 mm

Even less material

→ thinner sensors (300 → 200 μm)

→ thinner aluminum foil (300 → 250 μm)



LHCb Upgrade I: Tracking - UT

Current: TT

4 layers of silicon micro-strips

→ 183 μm pitch

→ 40, 30, 20, 10 cm in length

→ 143 k readout channels

Upgrade: UT

4 layers of silicon micro-strips, but finer granularity

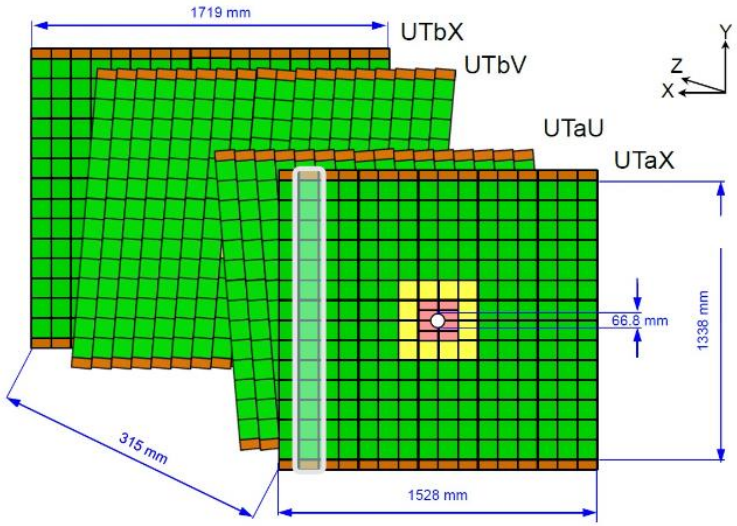
→ 190 and 95 μm pitch

→ 10 and 5 cm in length

→ 537 k readout channels

and better radiation hardness

New readout chip, compatible with 40 MHz readout scheme



LHCb Upgrade I: Tracking - SciFi

Current: IT & OT

3 stations with 4 layers each

→ silicon micro-strips in innermost region

→ straw drift tubes in outer region

→ 130 k + 54 k readout channels

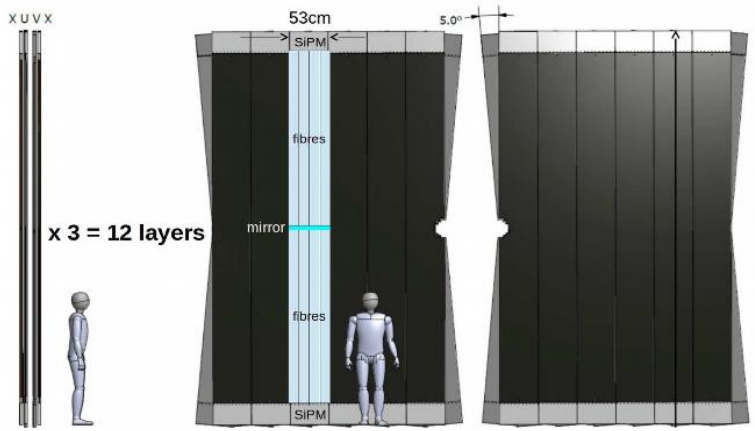
Upgrade: SciFi

3 stations of scintillating fibres

→ 2.5 m long, 250 μm diameter

→ read out with silicon photomultipliers

→ 590 k readout channels



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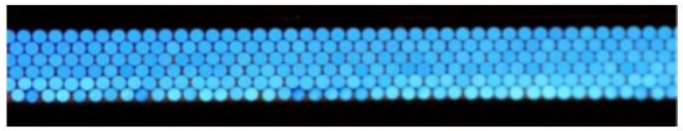
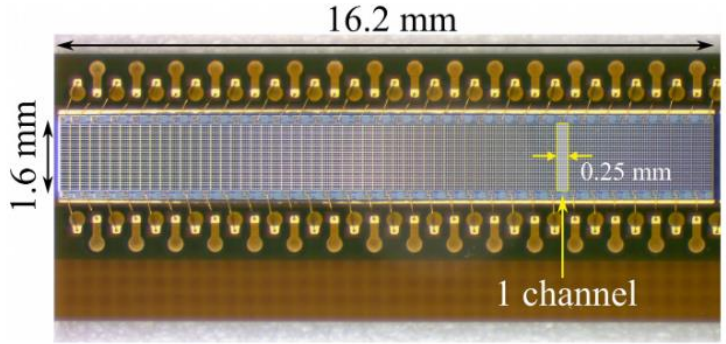




LHCb Upgrade I: PID Detector – RICH, Muon, Calorimeters

RICH:

- New photo-detectors and readout chain.
- 6x6 and 2.9x2.9 mm2 pixels multi-anode photo-multipliers (MaPMTs).
- Modified optics and mechanics to reduce RICH1 occupancy.

Calorimeters:

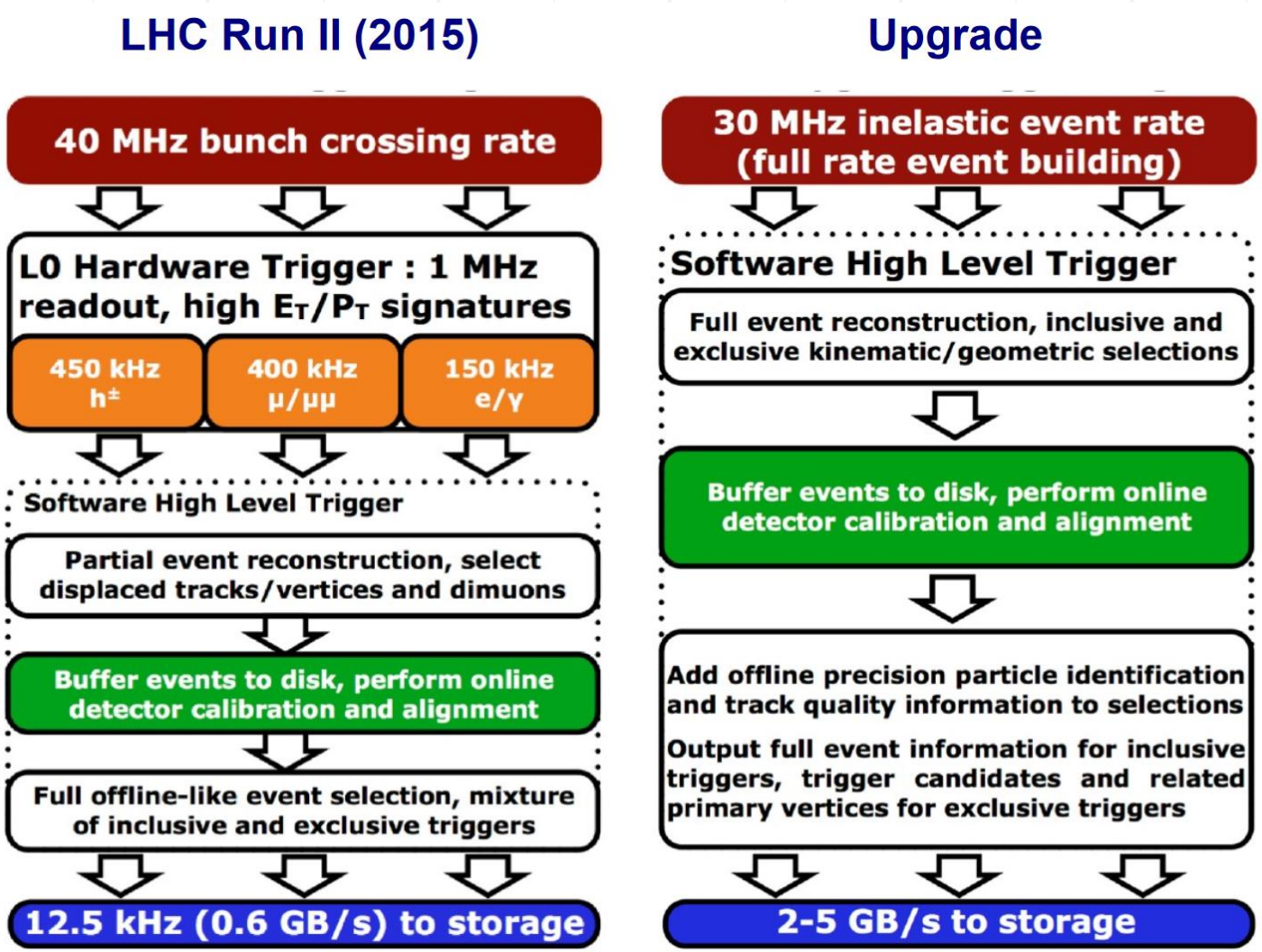
- Electromagnetic (ECAL) and hadronic (HCAL) calorimeters remain identical
- New readout electronics.
- ECAL inner modules replaced in LS3.

Muon Stations:

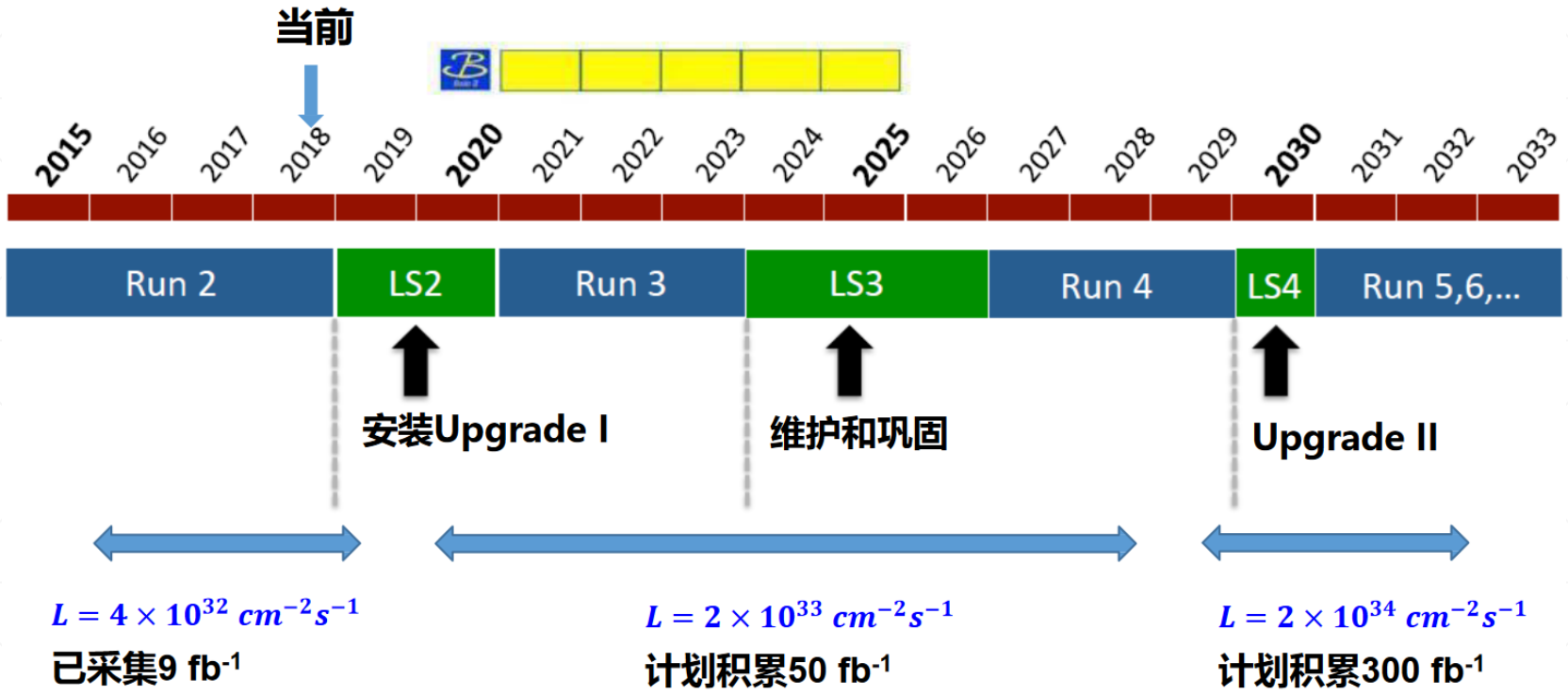
- New readout electronics and increased granularity.

RICH module equipped with MaPMTs

LHCb Upgrade I: Trigger



LHCb Upgrade II



LHCb Upgrade II, with installing in 2030 (LHC LS4).

- ❖ Raise operational luminosity by another factor of ten to 1.5-2 $\times 10^{34}cm^{-2}s^{-1}$
- ❖ Detectors with even finer granularity and with excellent timing resolution (4D resolution)
- ❖ Radiation hardness !

LHCb Upgrade II

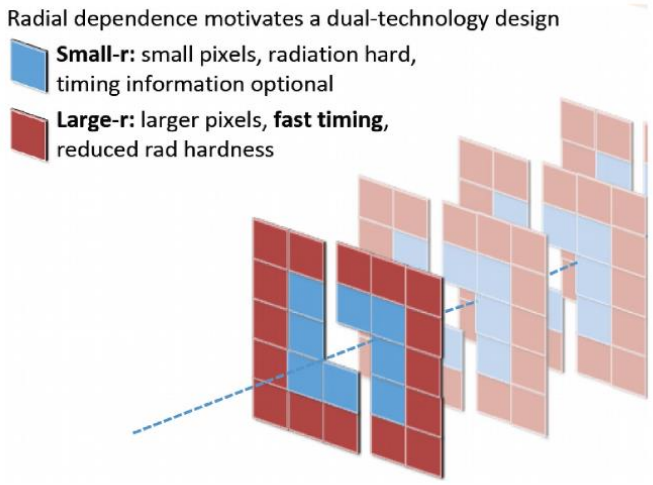
Examples of detector developments

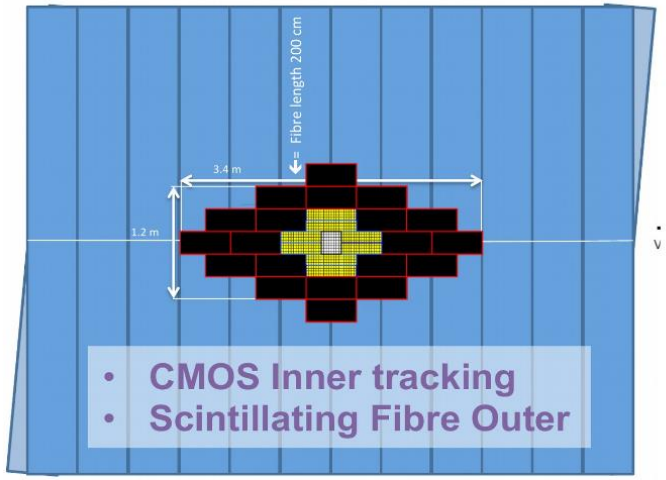
VELO: silicon pixels with timing resolution

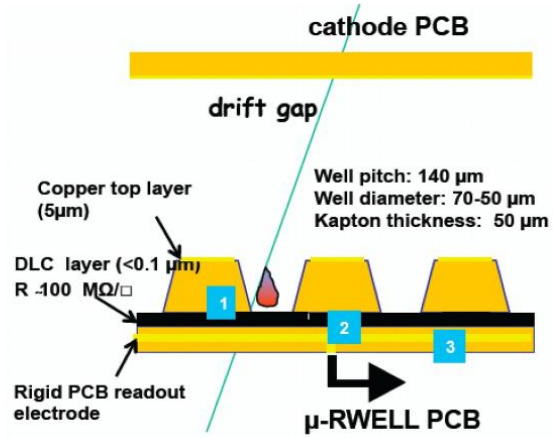
→ LGAD (Limited Gain Avalanche Detectors)

Tracking: central region with silicon
→ HV-MAPS (Monolithic Pixels)

Muon detectors: finer granularity
→ μ-RWELL







LHCb Upgrade I: SciFi

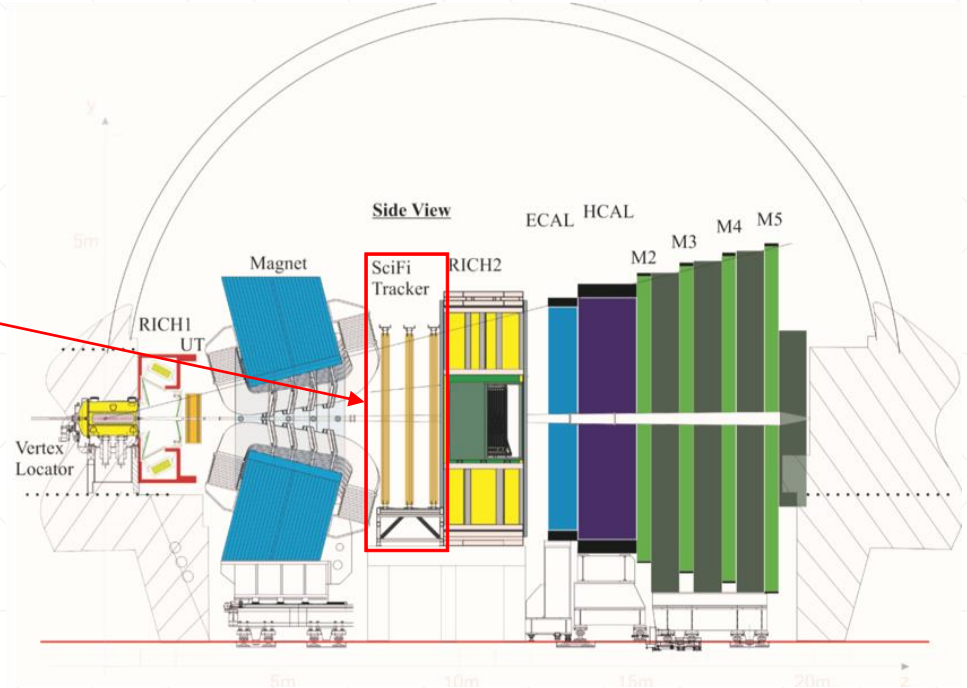
LHCb Upgrade I: SciFi

❖Goal: increase statistics by more than ×10

- ✓ Operate at $2\times10^{33}cm^{-2}s^{-1}$ → 50 fb^{-1}
- ✓ Triggerless 40MHz readout

❖Scintillating Fibre (Sci-Fi) Tracker

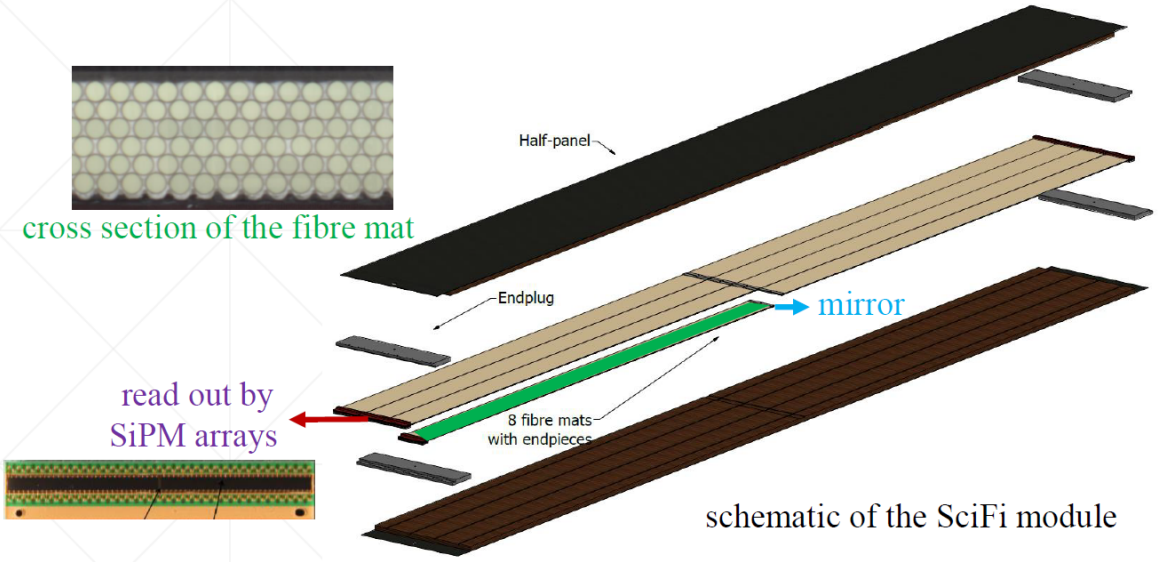
- ✓ Fast, high efficiency (~99%)
- ✓ High granularity (250μm)
- ✓ High resolution (<100μm)
- ✓ Low mass (<1% X_0/layer)
- ✓ Radiation hardness (up to 35kGy)



Schematic view of the current LHCb detector

SciFi – Fibre Mat & Module

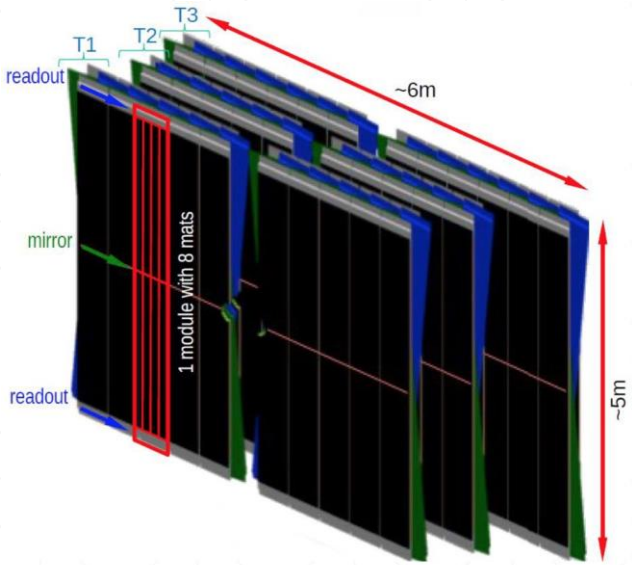
- 250μm diameter scintillating fibre wound into a 6-layer 2.4m-long fibre mat
  - ✓ one end equipped with a mirror
  - ✓ read out by 4× SiPM arrays
- 8 × fibre mat + honeycomb = sandwich-structure 0.5m × 5m module

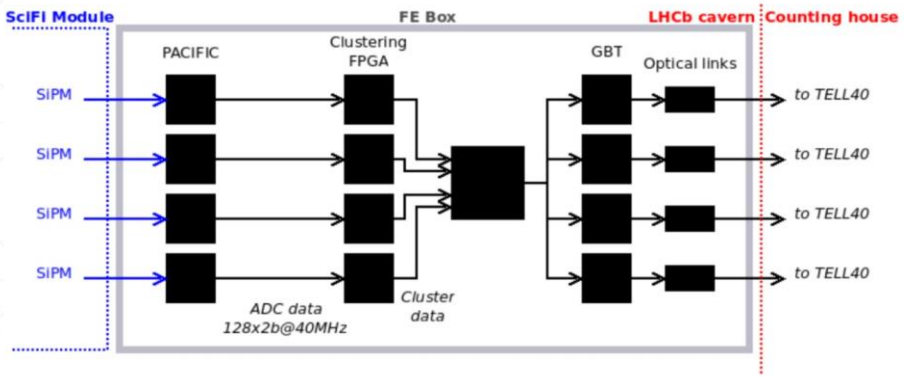


Sci-Fi readout electronics (FE)

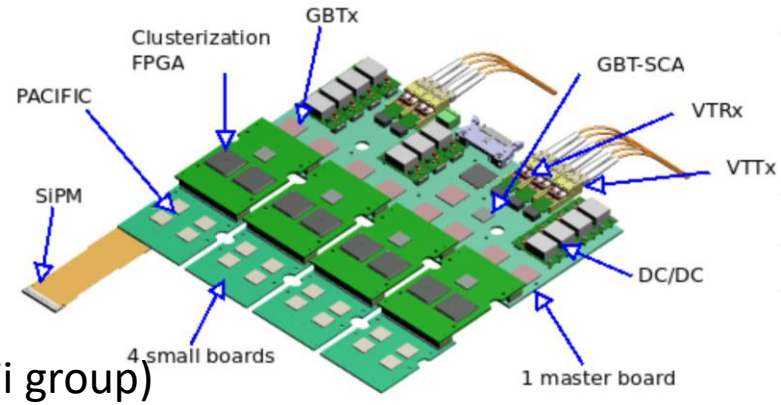
❖Tracker structure:
- ✓ 3 Tracking Stations
  - ✓ 12 detector layers (X-U-V-X, 5°)
    - ✓ 144 modules

❖Electronics design:
- ✓ ~340m^2 total active surface
- ✓ 590,000 SiPM channels
- ✓ 12,000 PACIFIC chips needed
- ✓ 2,500 Frontend Electronic Boards



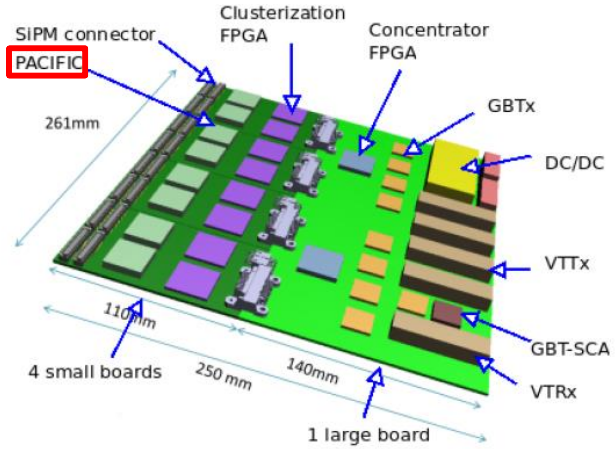


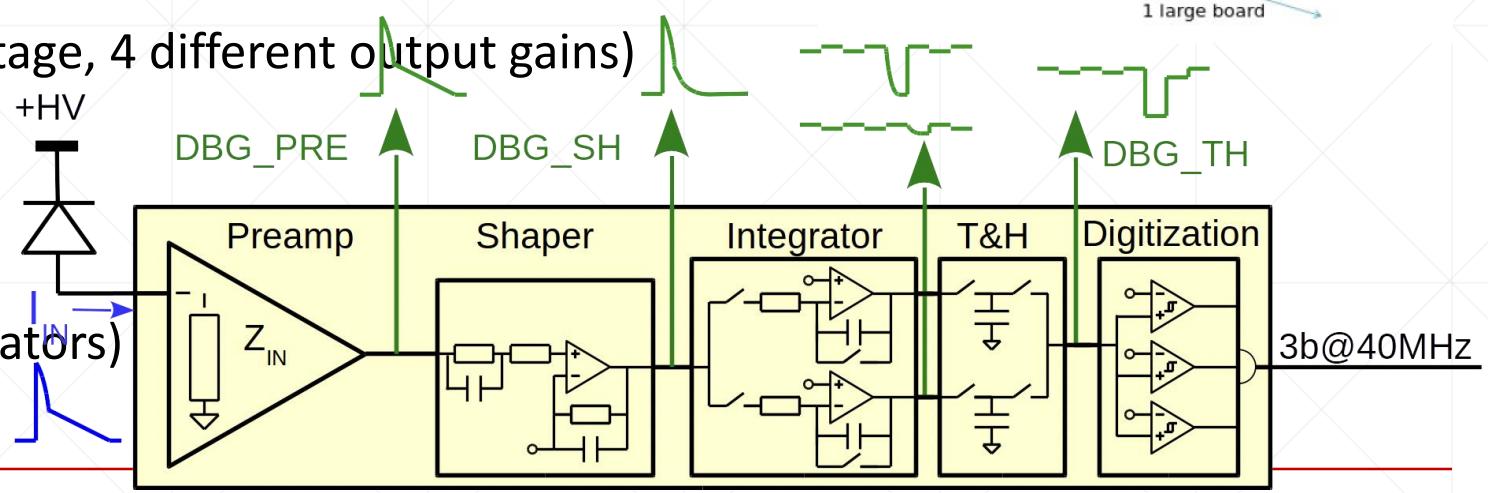
❖LHCb China Group 2016~2018:
- ✓ Co-design Sci-Fi Frontend Electronic Boards
- ✓ Manufacturing all Frontend Boards in China, testing a part
- ✓ Sci-Fi Readout Electronics Quality Assurance System (For chips and boards)
- ✓ Readout Electronics for Detector Performance Evaluation (>20 setups in Sci-Fi group)



PACIFIC5

- ❖64-channel SiPM readout ASIC for the Sci-Fi Tracker
- ❖Current mode input
- ❖Low input impedance (≈50Ω)
- ❖High Bandwidth preamplifier (≈250MHz)
- ❖Output：8bit×16pair@320MHz
- ❖Main functional blocks:
  - ✓Pre-amplifier(Current->Voltage, 4 different output gains)
  - ✓Shaper
  - ✓Offset trim
  - ✓Integrators×2 (20MHz)
  - ✓Track & Hold
  - ✓Digitization (with 3 comparators)

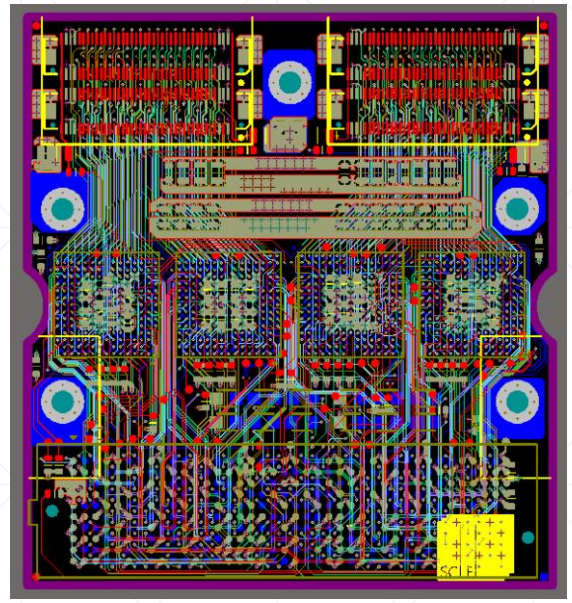




PACIFIC Carrier Board

We decided to re-optimize the routing of the PACIFIC Carrier Board

- 4 × PACIFIC ASICs (196-pin BGA packaged)
- 4 × temperature measurement circuits (voltage divider circuits with NTC , 2 for SiPMs, 2 for the ASICs)
- 4 × SiPM bias voltage measurement circuits (voltage divider circuits)
- 1 × BoardID IC (DS2401 64-bit unique, factory-lasered silicon serial number, no permanent damage up to 140Gy)
  http://radwg.web.cern.ch/RadWG/Pages/showExternal.aspx?GotoUrl=https://twiki.cern.ch/twiki/bin/viewauth/Main/TulliosPreferredPartList
- 4 × SiPM flex cable connectors (Hirose DF12(3.0)-80DS-0.5V)
- 1 × FMC connector (ASP-134602-01)



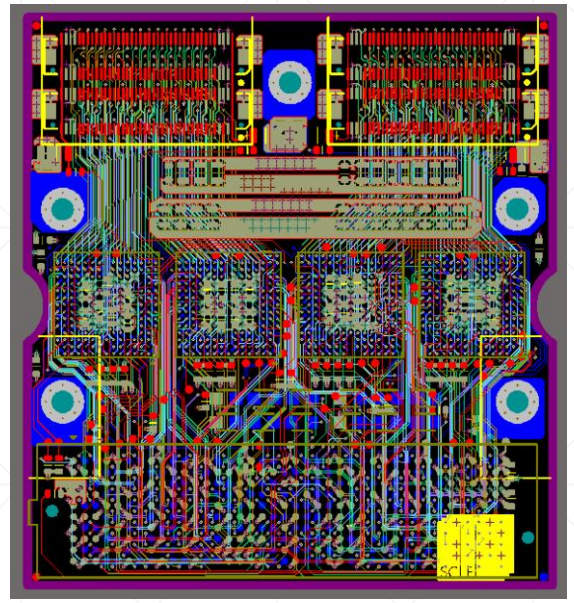
re-optimised PACIFIC Carrier Board r4

Redesign of PACIFIC Carrier Board

We decided to re-optimize the routing of the PACIFIC Carrier Board

- for a higher production yield
- more strict routing constrains, to gain some margin for the sampling window size

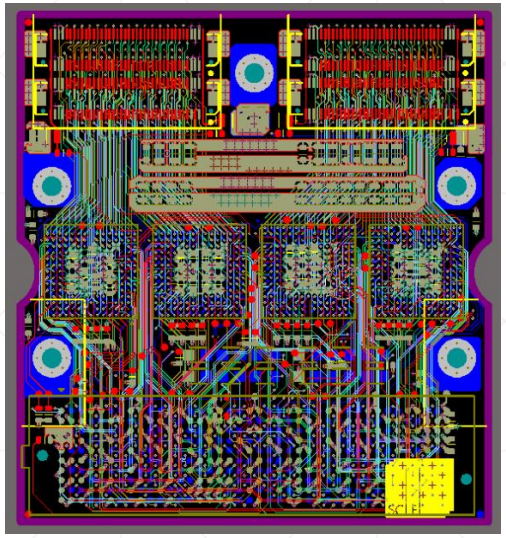
- 4 pairs of PACIFIC Clock lines (CLKIN_0~3) : routing length match < 1mm
- 4 SYNC lines (SYNC_0~3): routing length match < 1mm
- 64 pairs of data lines (DATA_0~3_X) : routing length match <3mm.
- well seperate the analog input signals and the output data lines, the CLOCK lines
- from 8-layers to 14-layers
- Calculate impedance for Halogen Free (TU-862HF), and keep thickness 1.7mm

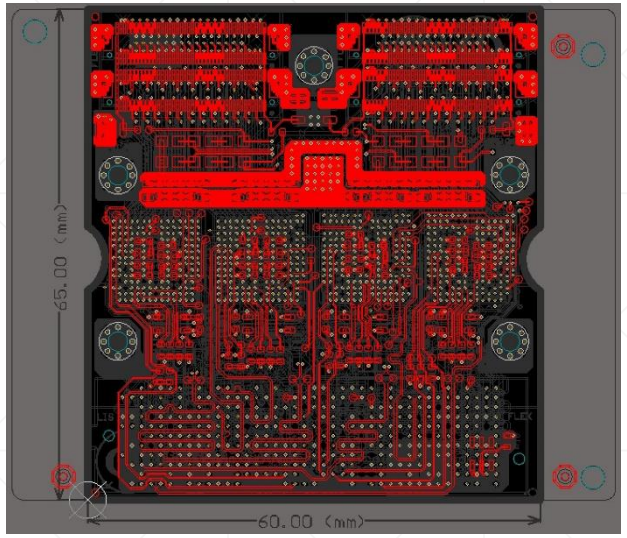


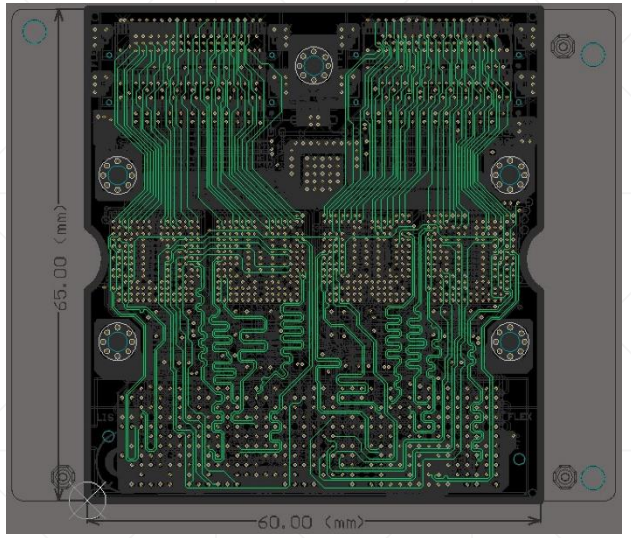
re-optimised PACIFIC Carrier Board r4

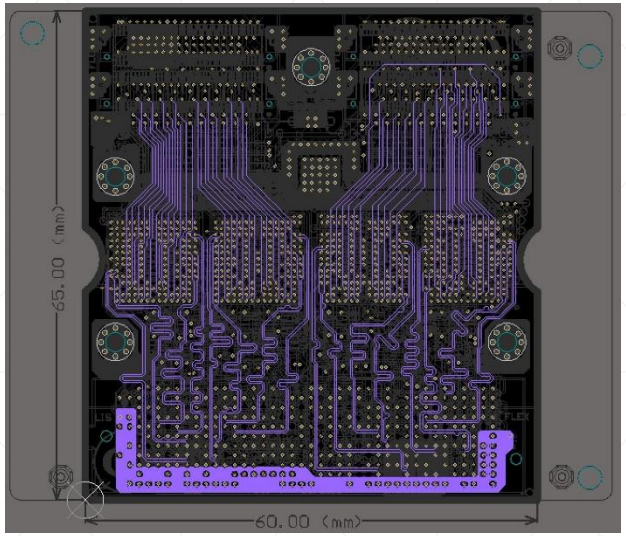
The design has been complete.
For the first 250 PACIFIC Carrier Boards, we will assemble first 10 PCBs, check with the SciFi full electronics (MB+CB) to make sure everything works fine after this optimization.

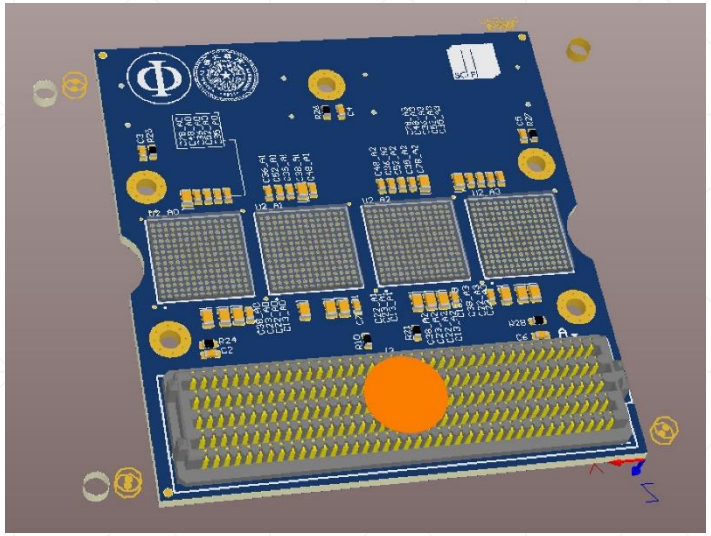
Redesign of PACIFIC Carrier Board

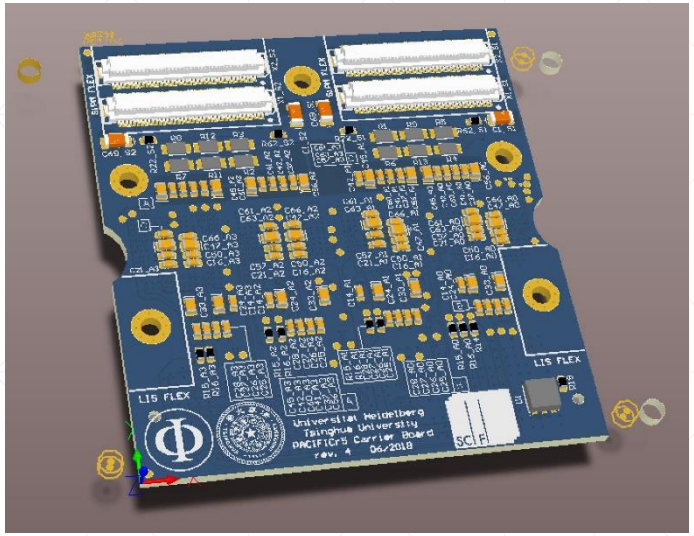




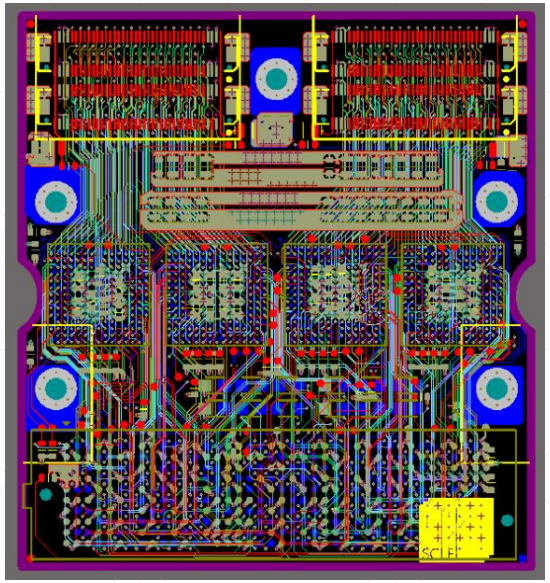


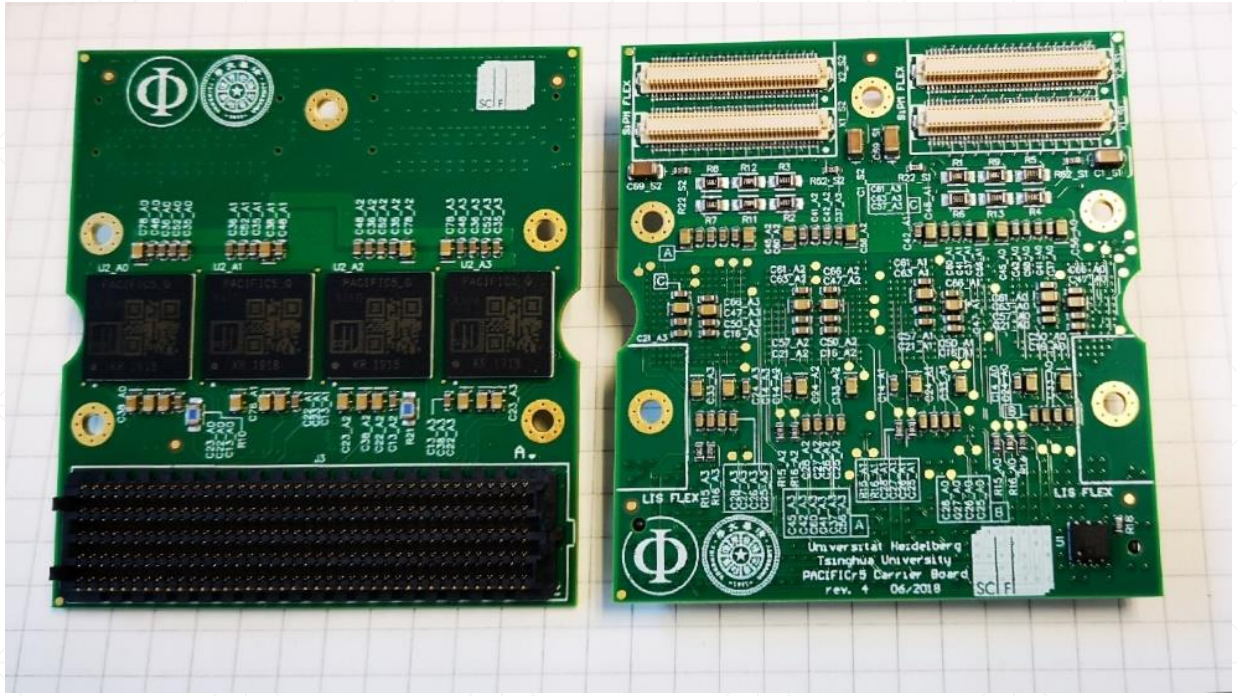






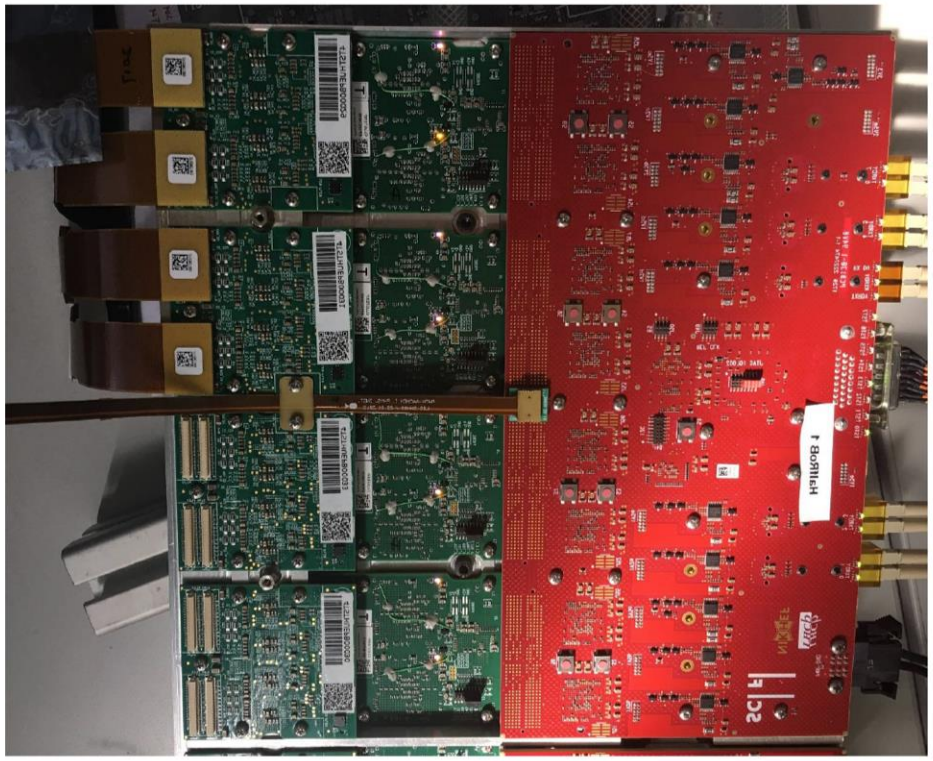
Redesign of PACIFIC Carrier Board & Mass Production





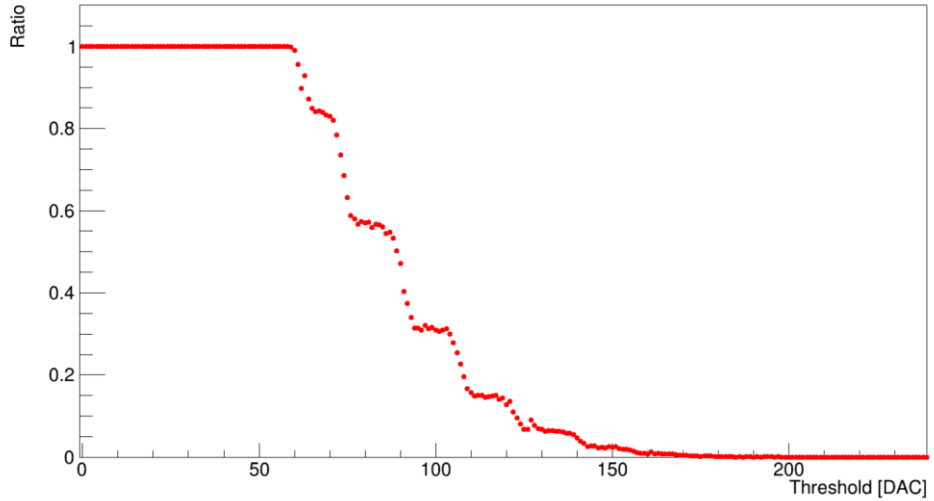
2018.09 - First 250 PACIFIC Carrier Boards finished !
(for first C-Frame of SciFi)

First Setup of SciFi C-Frame



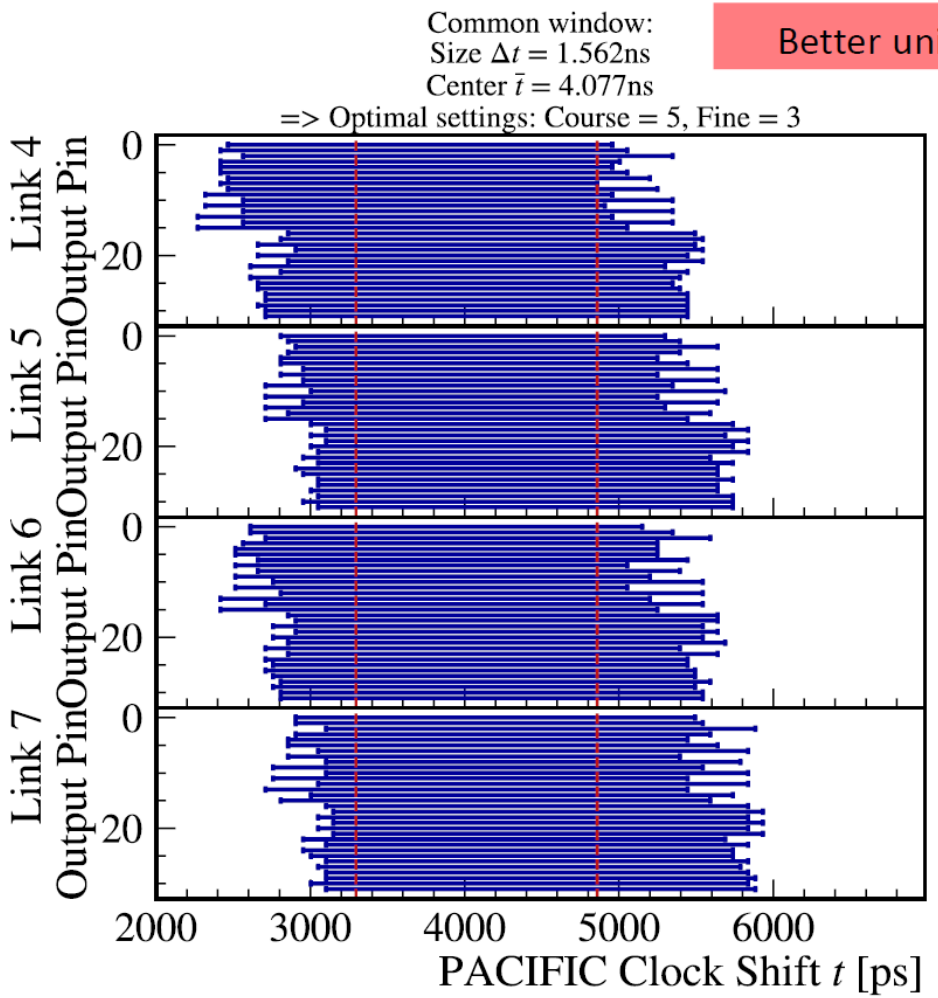
First Setup of SciFi C-Frame
(Sci-Fi milestone of 2018)

Test with SiPM + Light Injection System

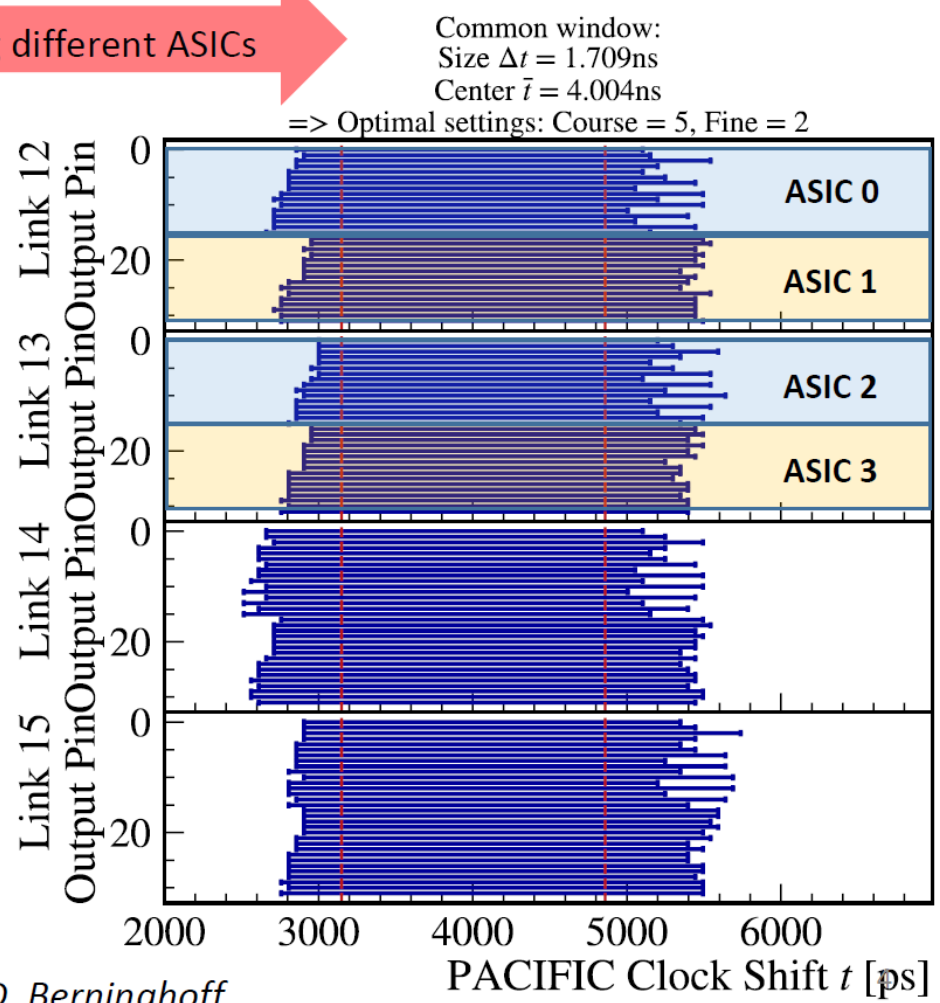


BER test with SciFi FE

- Position: Master Board 0, PBs 2+3, old design
- Position: Master Board 1, PBs 2+3, **new design**



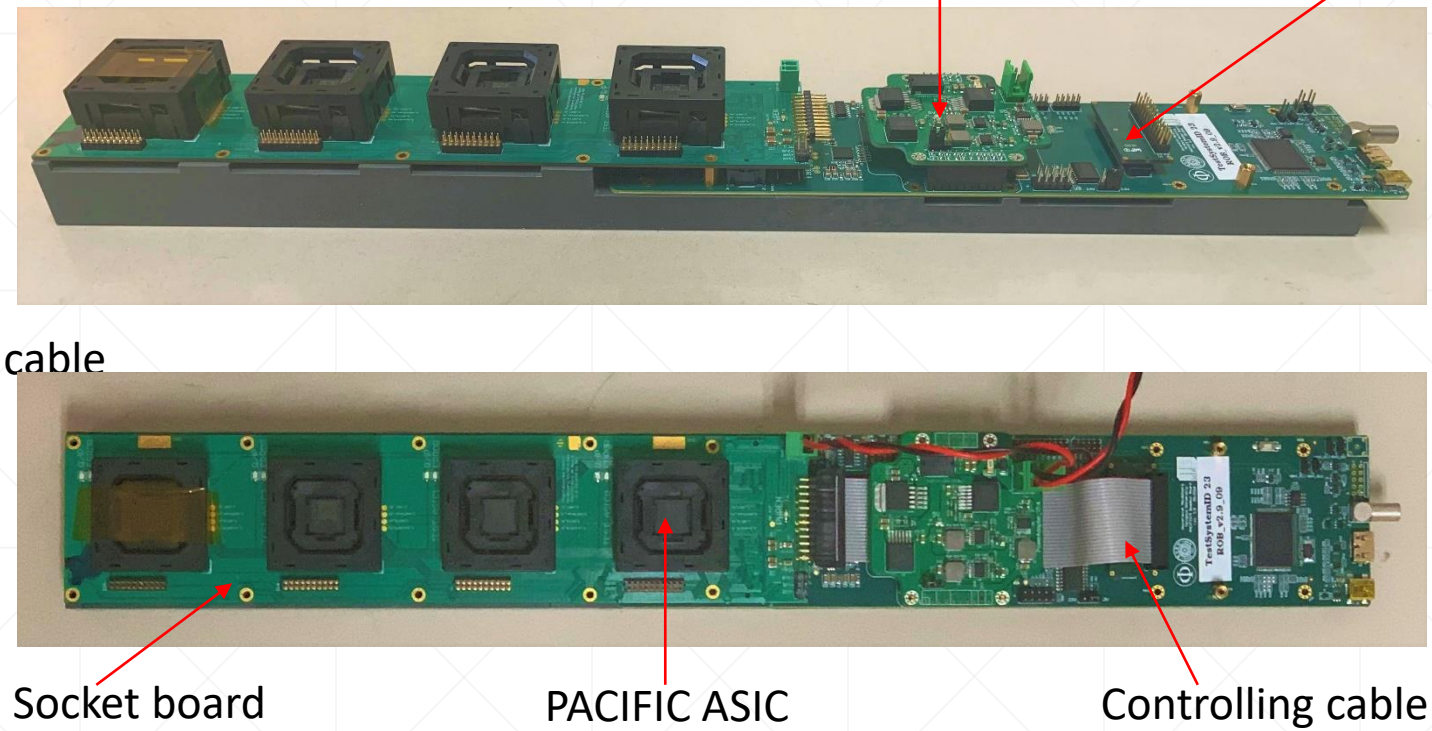
Better uniformity among different ASICs

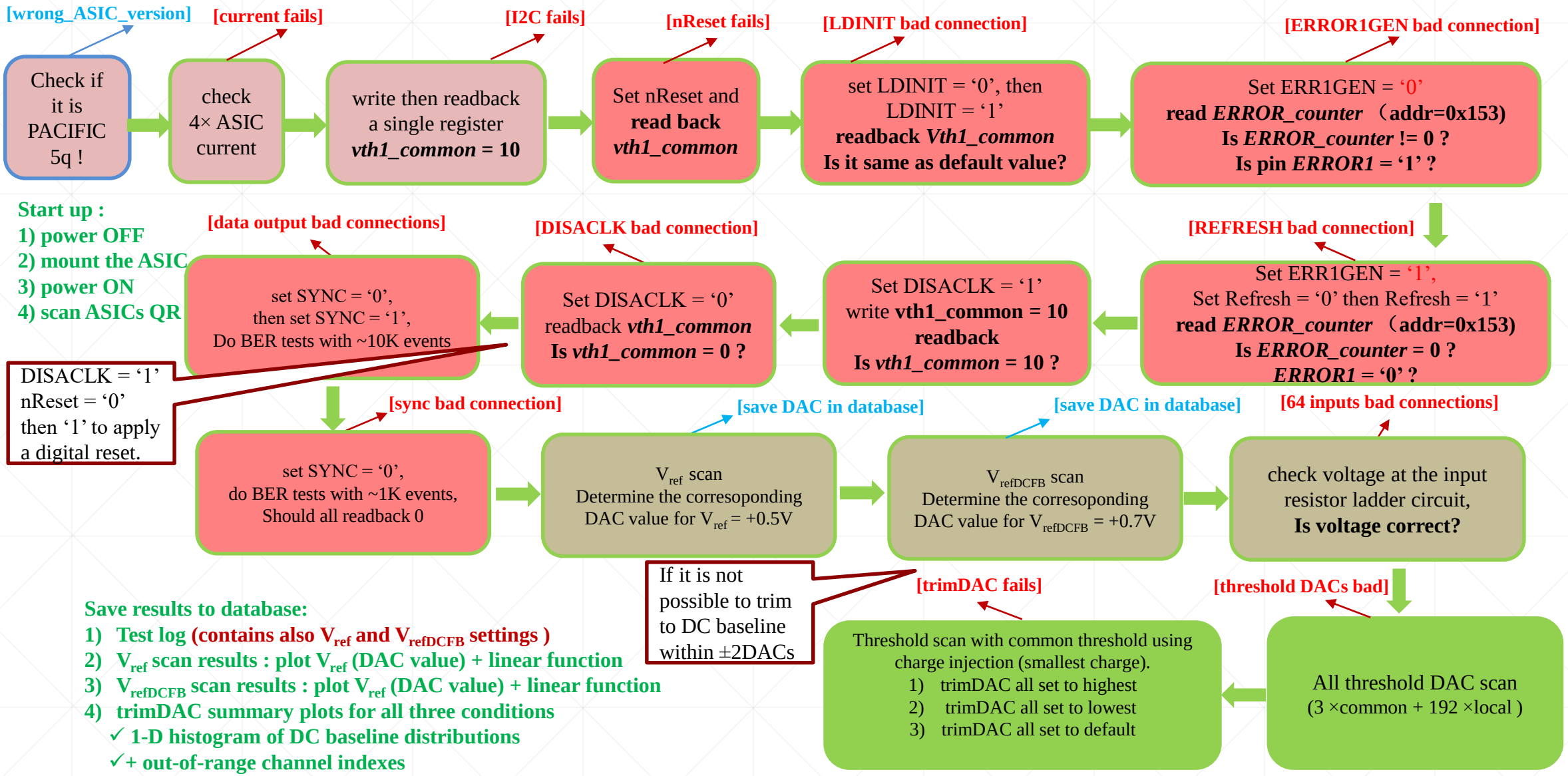


Result from D. Berninghoff

QA System for PACIFIC chips

- ❖Custom designed test DAQ (PACIFICROB): [fully tested, 4 for Heidelberg, 3 for Barcelona, 3 for Valencia]
  - ✓ Altera Cyclone FPGA (clock generation, ASIC configuration, data process, sensor readout ...)
  - ✓ precision clock conditioner to fine tune the clock for each ASIC
  - ✓ (LVDS-SLVS convertor)
  - ✓ 8-channel, 12-bit ADC
  - ✓ USB interface to PC
- ❖Socket Board:
  - ✓ 4 sockets to nip chips
  - ✓ Connected with FMC & controlling cable
- ❖DC power supply
  - ✓ Output 5V/3A at least
- ❖Linux PC
- ❖Robot arm (Barcelona)





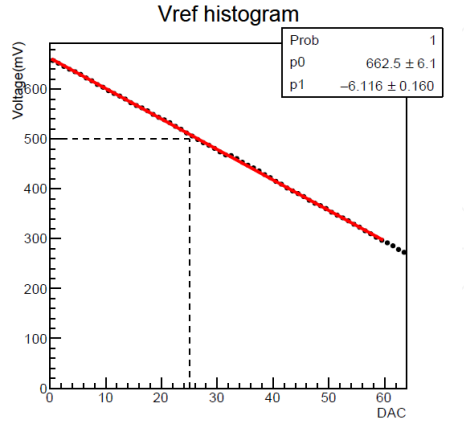
Save results to database:

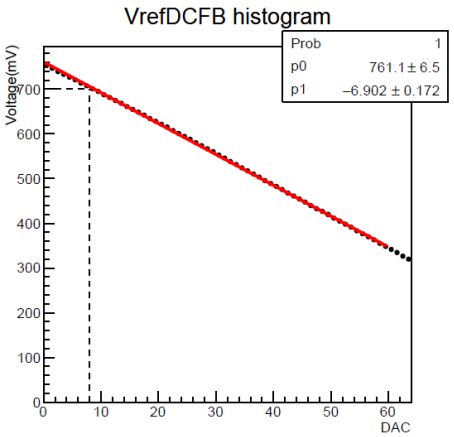
1) **Test log (contains also V_{ref} and $V_{refDCFB}$ settings)**
2) **V_{ref} scan results : plot V_{ref} (DAC value) + linear function**
3) **$V_{refDCFB}$ scan results : plot V_{ref} (DAC value) + linear function**
4) **trimDAC summary plots for all three conditions**
   - ✓ **1-D histogram of DC baseline distributions**
   - ✓**+ out-of-range channel indexes**

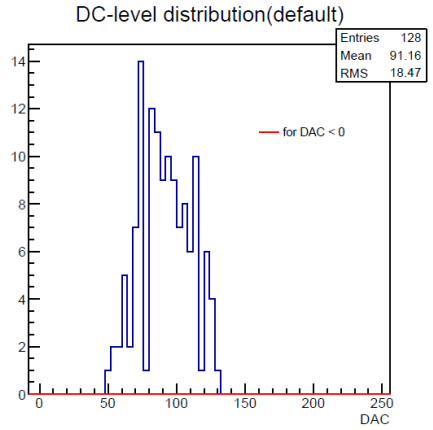
PACIFIC ASIC QA test routine

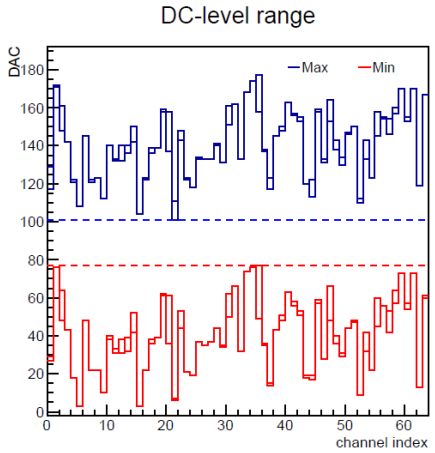
Raw data from all the scans will be save into one file to reproduce the results.

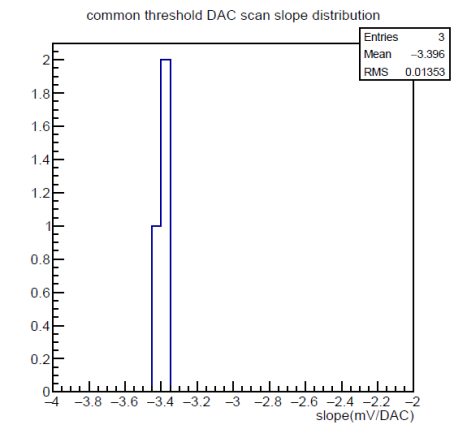
Main features of test results for one chip

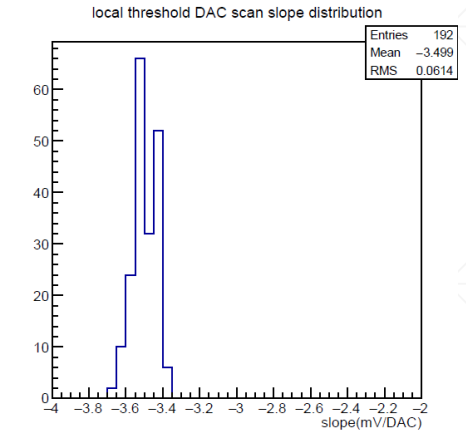






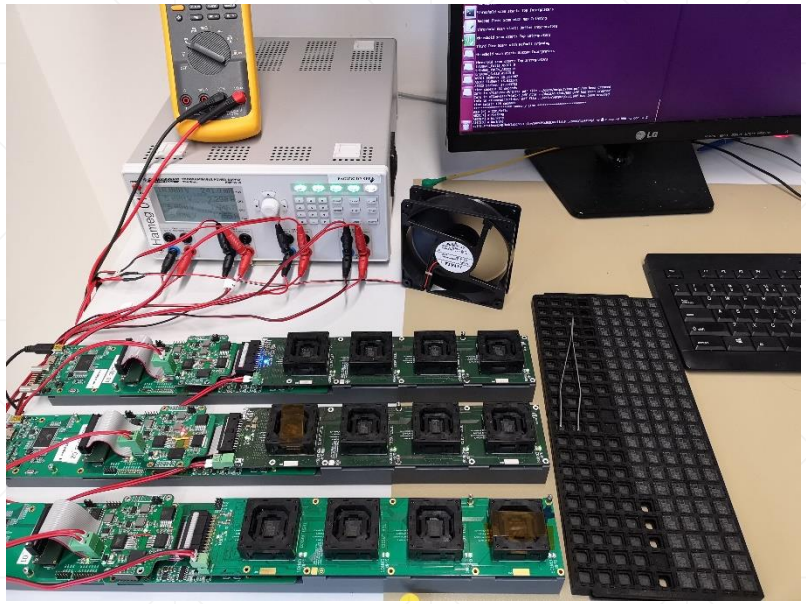




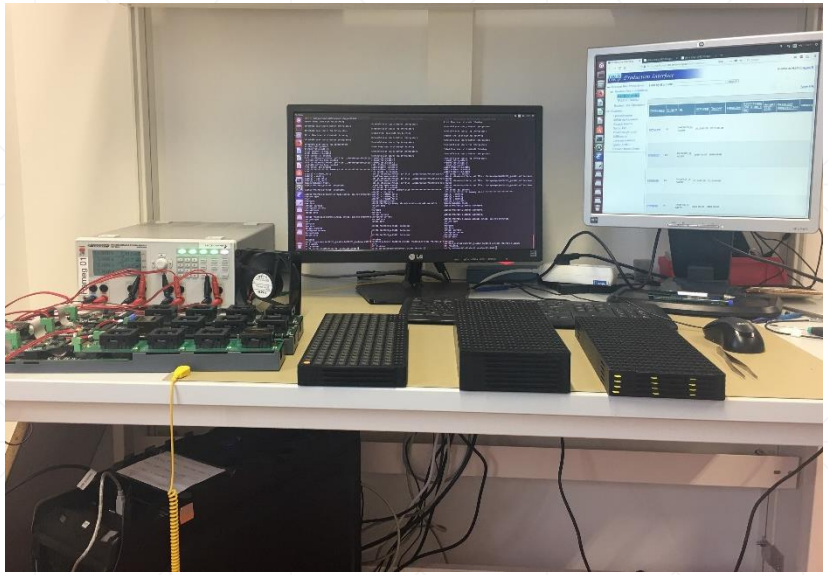


test automatically update result to DB

final check the QA test routine



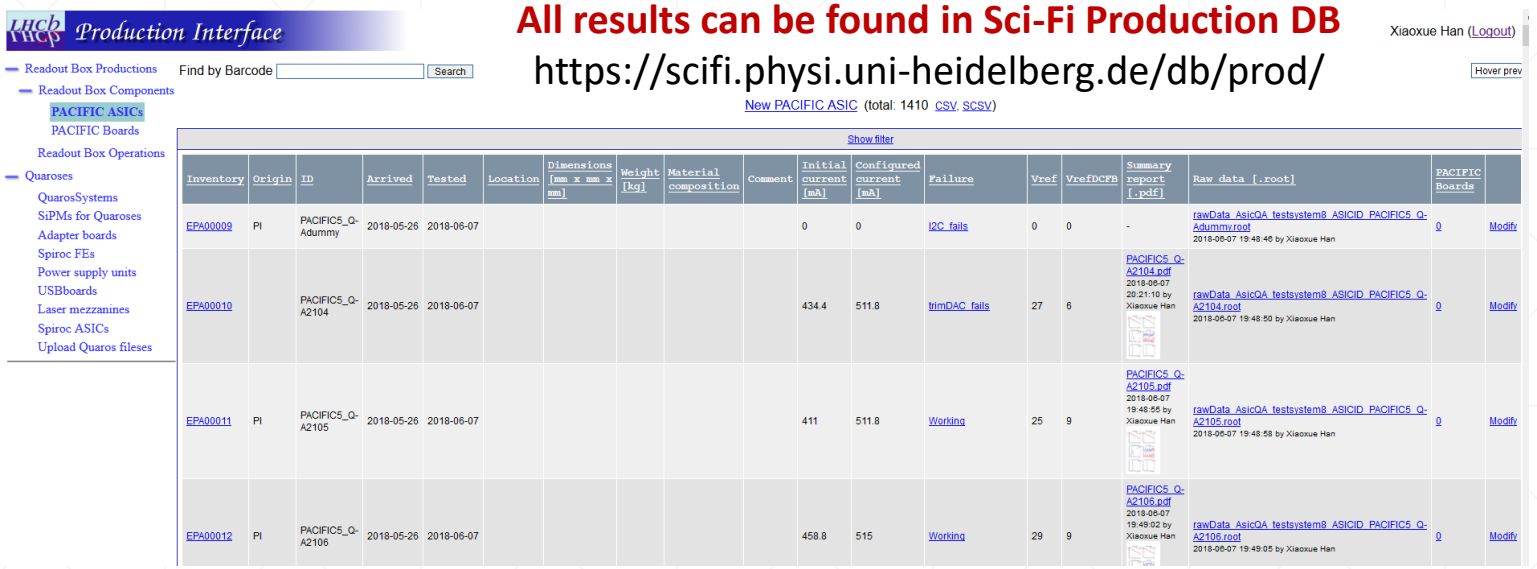
QA test running : 10 ASICs/run , ~100ASICs/hour



finish all 1st batch 1420 PACIFIC5q test

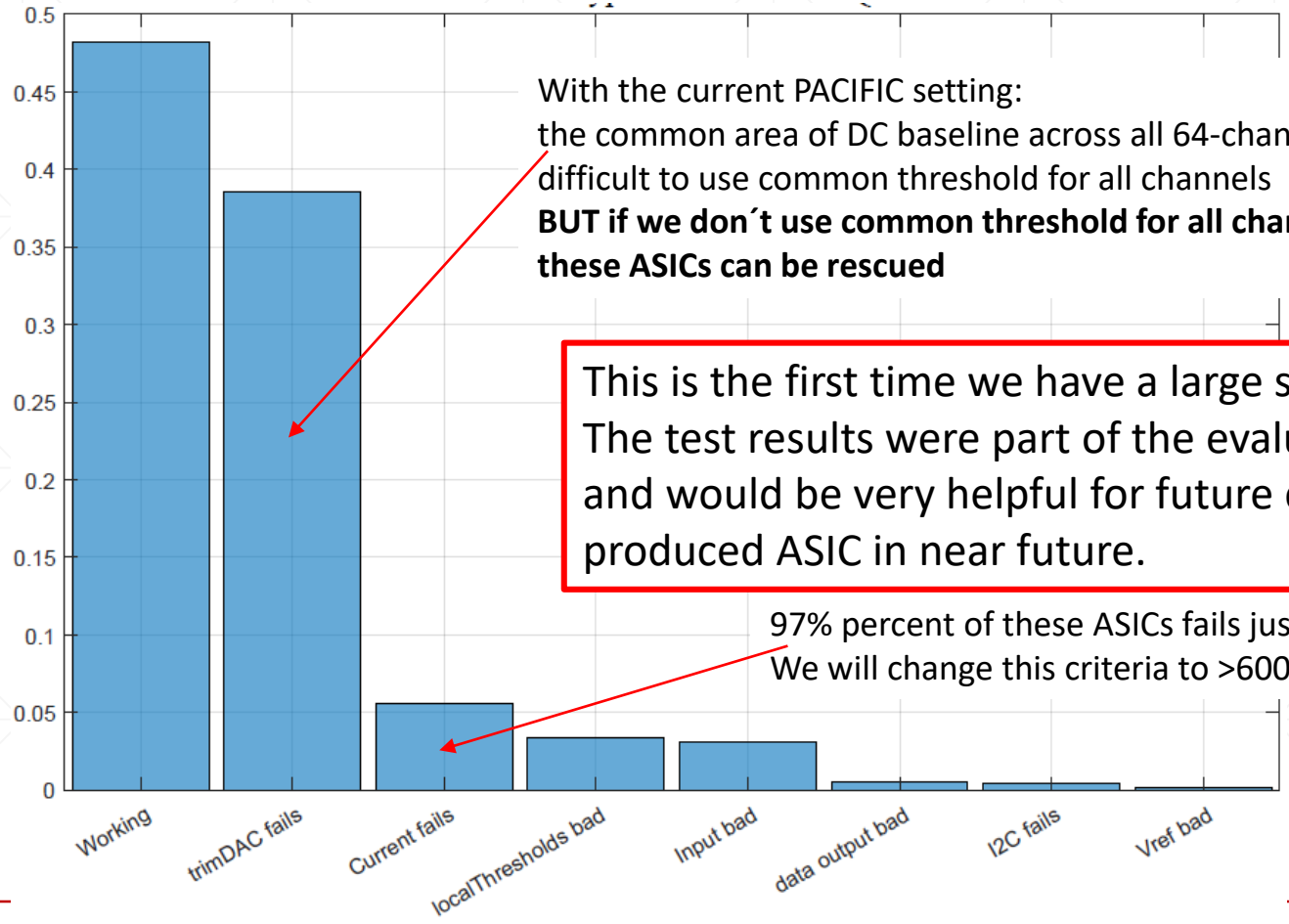
All results can be found in Sci-Fi Production DB

https://scifi.physi.uni-heidelberg.de/db/prod/



QA test for 1st batch of packaged PACIFIC5q

1st batch of 1420 chips



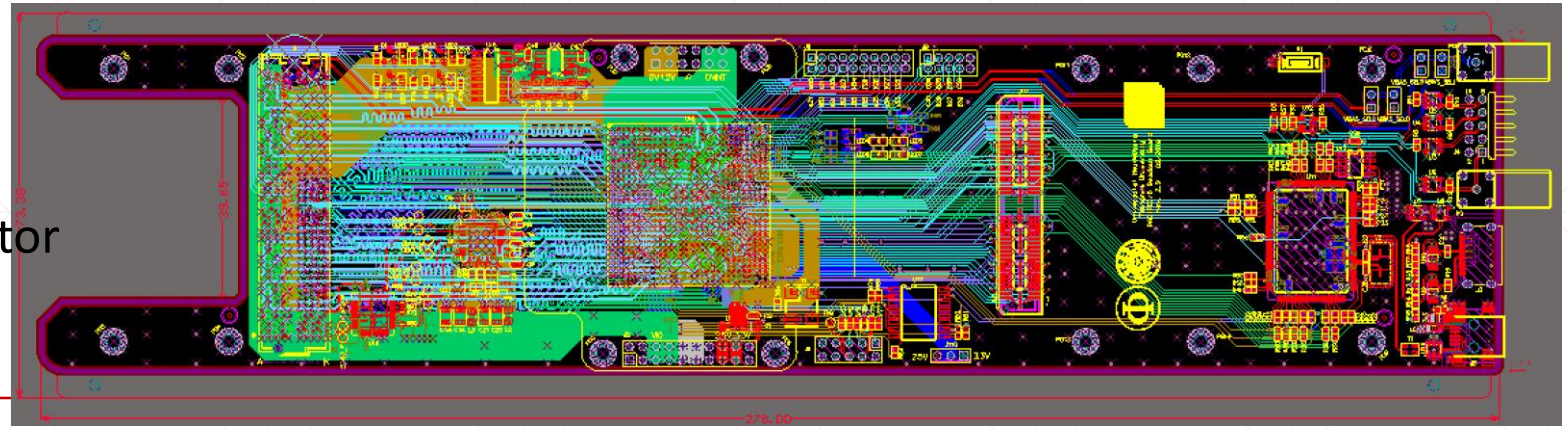
With the current PACIFIC setting:
the common area of DC baseline across all 64-channels is less than 4DACs,
difficult to use common threshold for all channels
BUT if we don´t use common threshold for all channels or tune the PACIFIC settings , these ASICs can be rescued

This is the first time we have a large statistical sample of the ASICs. The test results were part of the evaluation of the Sci-Fi electronics and would be very helpful for future classification of mass-produced ASIC in near future.

97% percent of these ASICs fails just because the initial current > 500mA
We will change this criteria to >600mA and re-measure these ASICs

QA System for Carrier Boards

- ❖Custom designed test DAQ (PACIFICROB): [fully tested, 3 for Heidelberg (delivered), 3 for Barcelona, 3 for Valencia]
  - ✓ Altera Cyclone FPGA (clock generation, ASIC configuration, data process, sensor readout ...)
  - ✓ precise clock conditioner to fine tune the clock for each ASIC
  - ✓ LVDS-SLVS convertor
  - ✓ 8-channel, 12-bit ADC
  - ✓ USB interface to PC
- ❖FMC connector intermedia board:
  - ✓ Simple pin-to-pin adapter PCBs
  - ✓ To avoid broken FMC connectors
- ❖Charge injection board
- ❖DC power supply
  - ✓ Output 5V/3A at least
- ❖Arbitrary waveform generator
- ❖Linux PC



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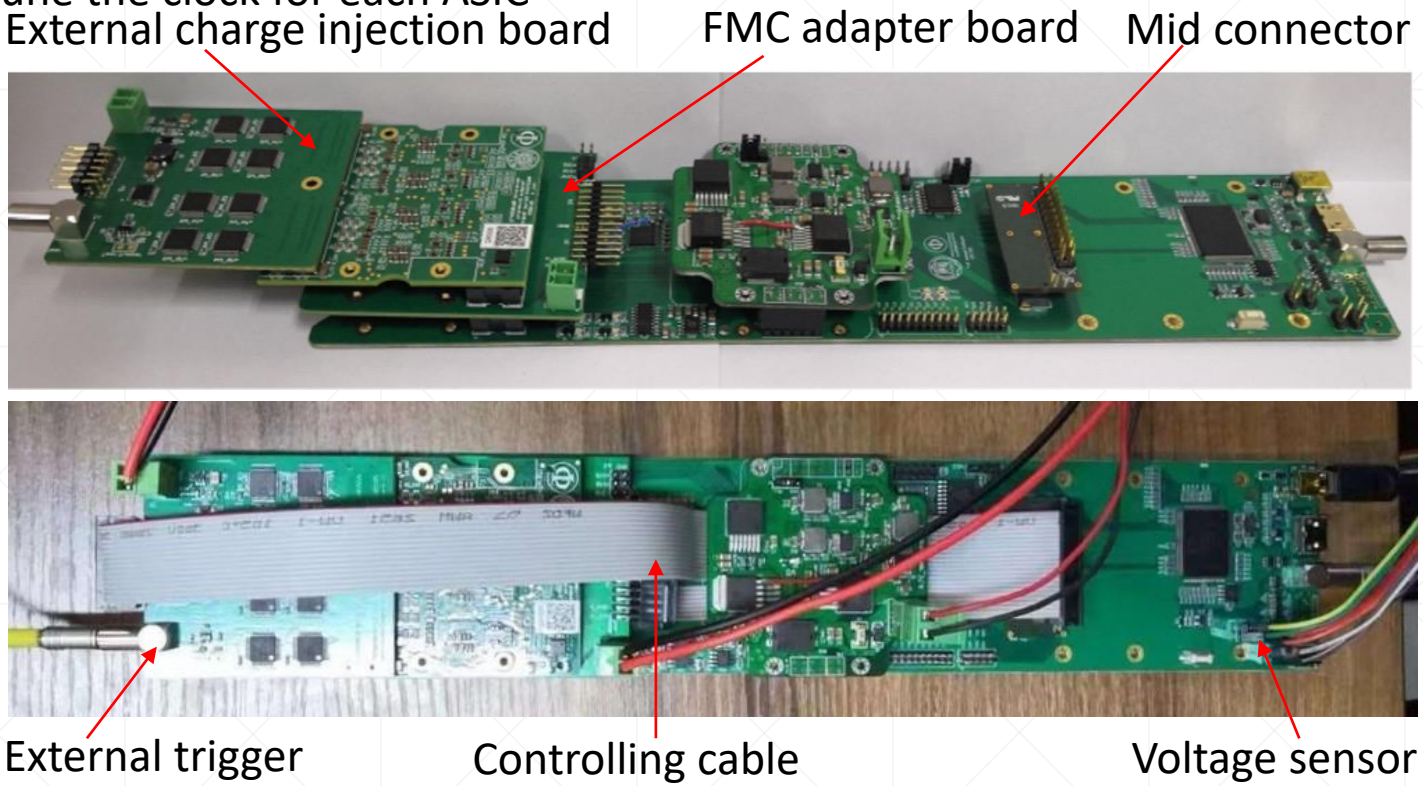
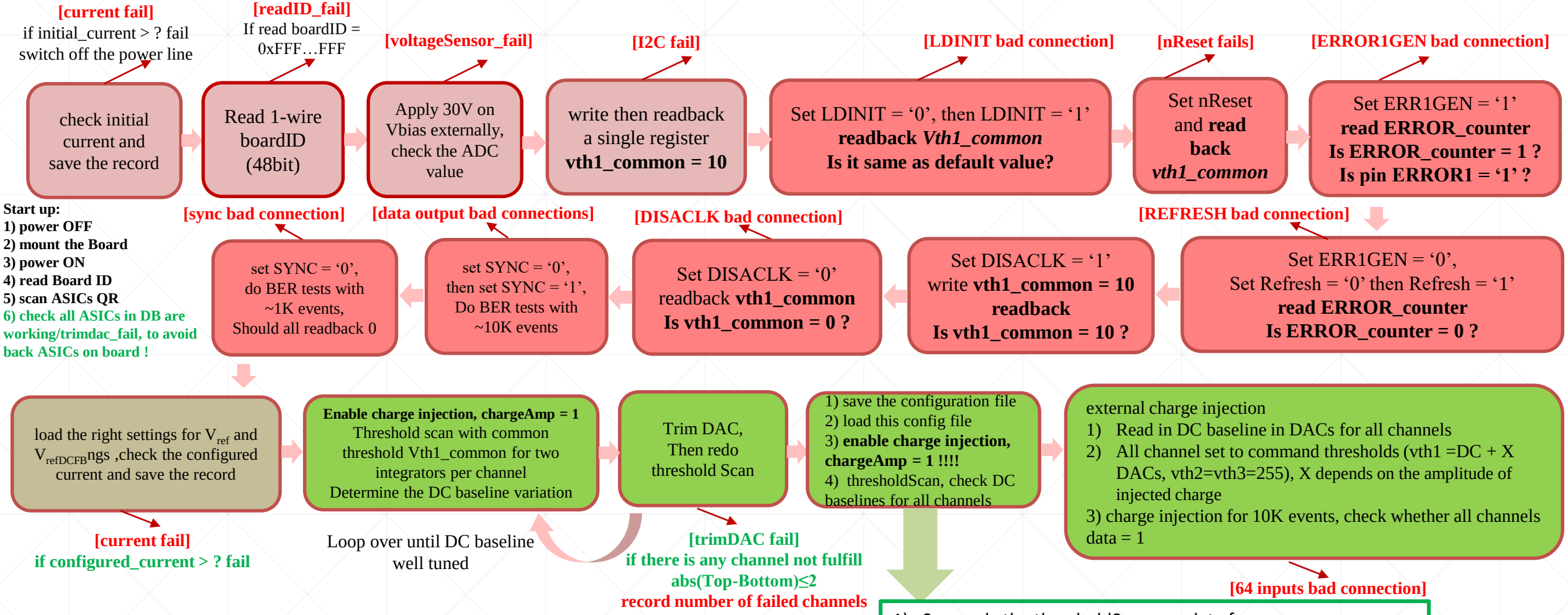


PACIFIC Carrier Board QA test routine



Save results to database:

1) test log

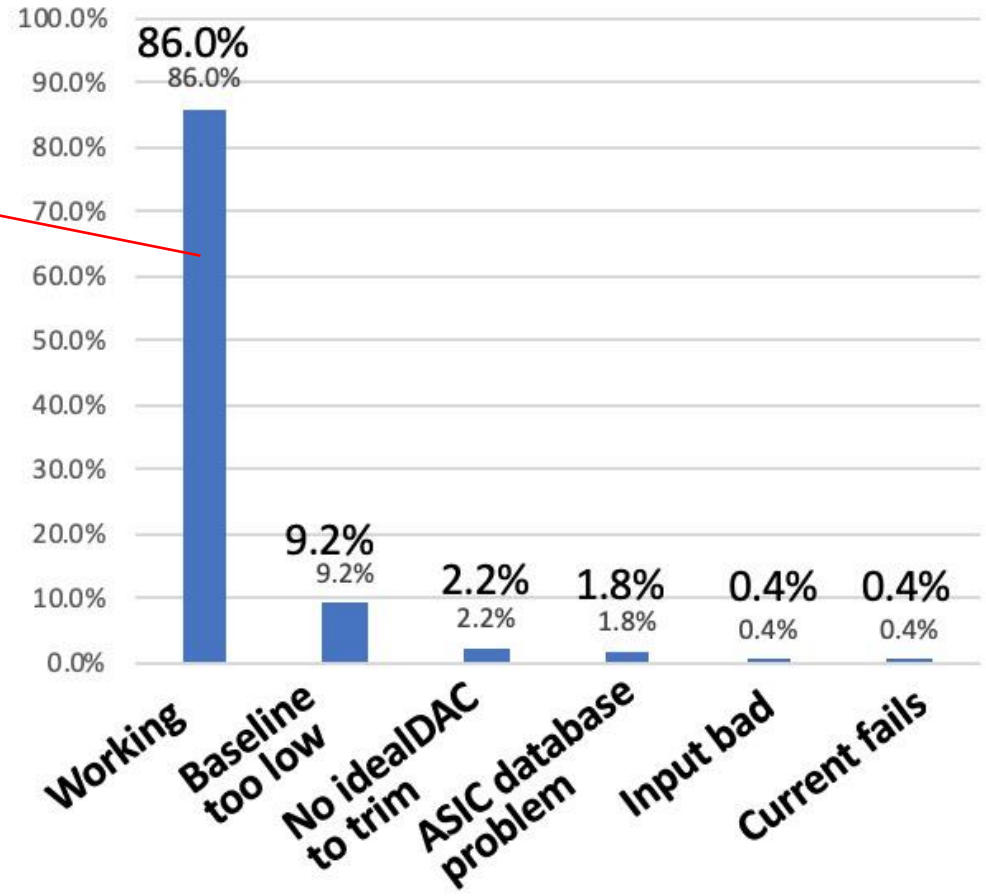
2) all parameters into a configuration file: PB_XX.conf, which can be read later by SciFi readout system.

3) after trimming DC-baseline distribution

- ✓ **1-D histogram of 0.5ratio-transition-DAC value for all channels (both Top and Bottom DAC) for each ASIC**
- ✓ **1-D histogram of difference of Top and bottom DAC within the same channel for each ASIC**

First 250 PACIFIC Carrier Boards Tested

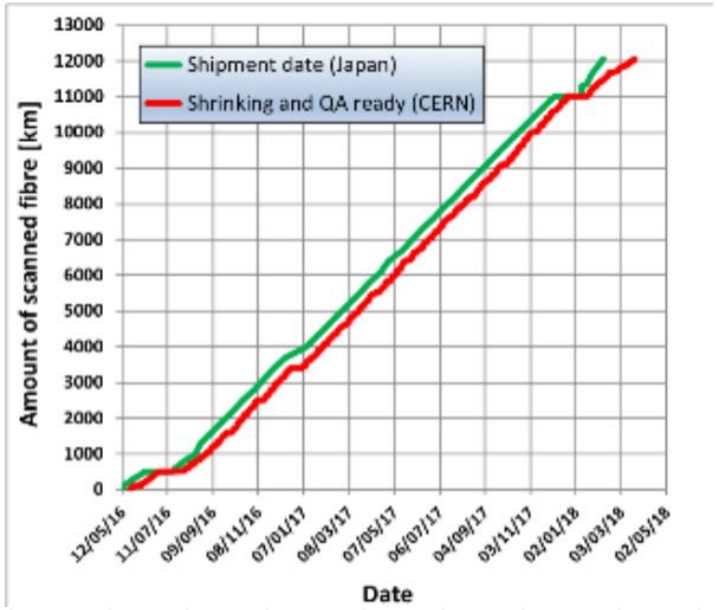
- ❖86.0% Working
- ❖14.0% Failed:
  - ✓ Baseline too low
  - ✓ No ideal DAC to trim
  - ✓ ASIC database problem
  - ✓ Input bad
  - ✓ Current fails

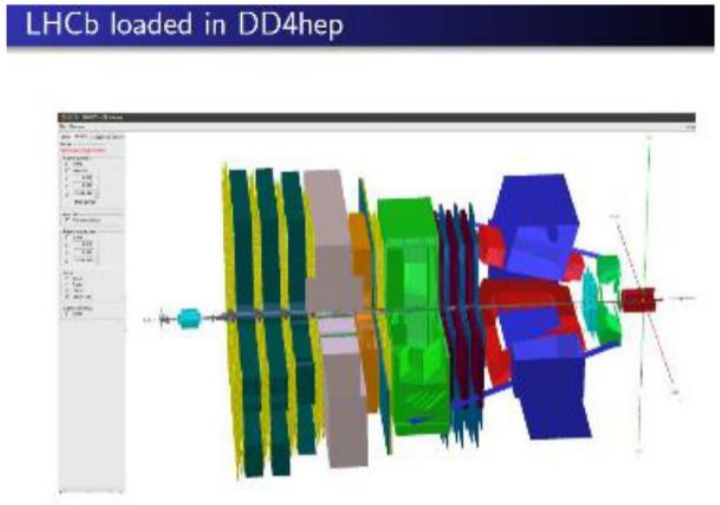


LHCb Upgrade I: SciFi

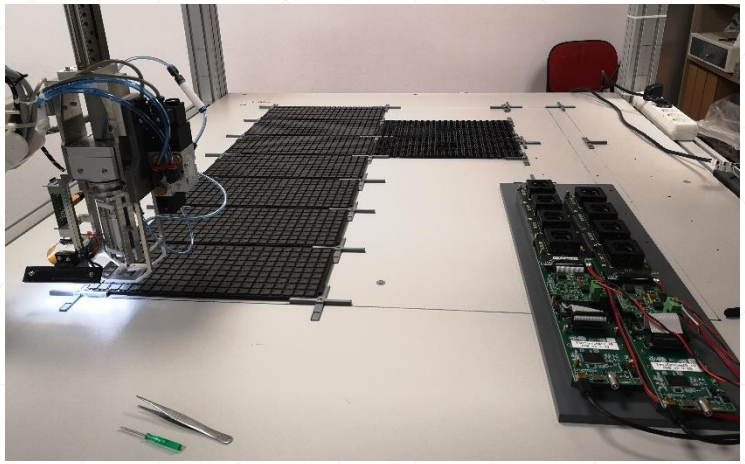
一名博士后和一名博士生分别在CERN和海德堡参加SciFi 探测器的工作

- **作为主力完成了全部闪烁光纤的质量检测（QA）**
- **负责把SciFi探测器几何描述数据库从XML 转换为DD4HEP**
- **开发SciFi 探测器监控软件**





LHCb Upgrade I: SciFi (LHCb China Group)

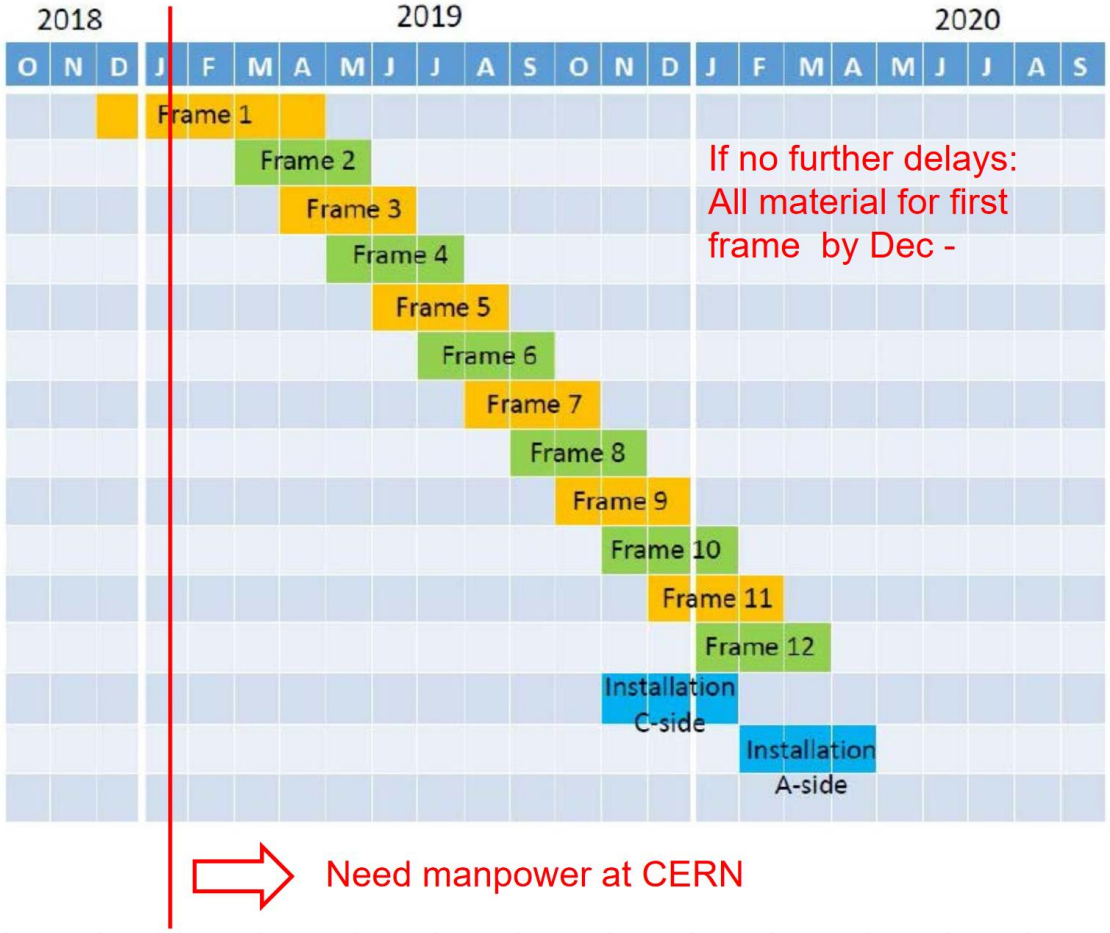


- LHCb China Group (2018) finished:
  - ✓ >1500 PACIFIC ASICs tested
  - ✓ Frontend Boards redesigned and verified
  - ✓ 250 Frontend Boards manufactured and tested in China
  - ✓ 6 Readout Electronic Quality Assurance System set up in Heidelberg, Barcelona and Valencia

- 2019 To Do:
  - ✓ ALL 12,000 PACIFIC ASICs to test (with Barcelona group)
  - ✓ ALL 2,500 Frontend Boards to manufacture in China [in progress] and to test (with Valencia group)

LHCb Upgrade I: SciFi

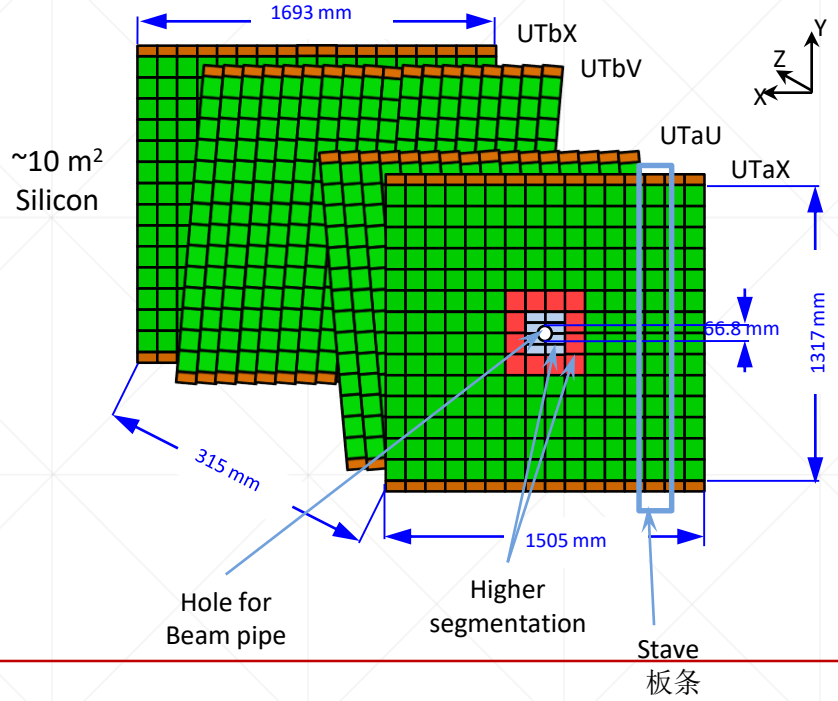
Production Schedule

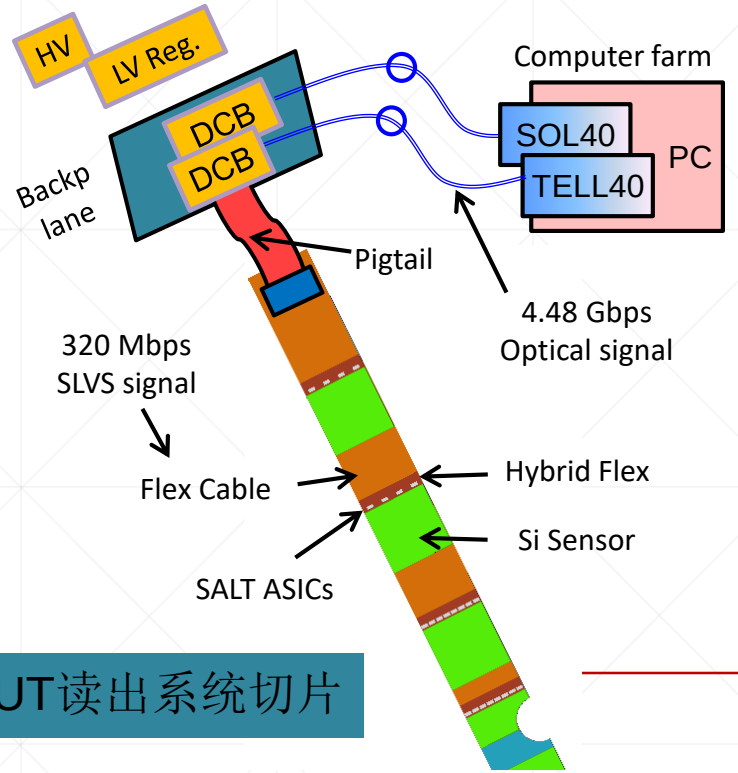


LHCb Upgrade I: UT

LHCb Upgrade I: Upstream Tracker (UT)

- 在高辐射的中心区域使用更抗辐射的n-in-p的硅微条技术，而在其余部分使用技术相对成熟价格较低的p-in-n探测器.
- 前端读出芯片(SALT)采集信号,数字化,并压缩数据,然后将电子信号传送到UT板条顶端的数据控制板(DCB); DCB收集数据,转化为光信号,输送到地表的数据收集系统.





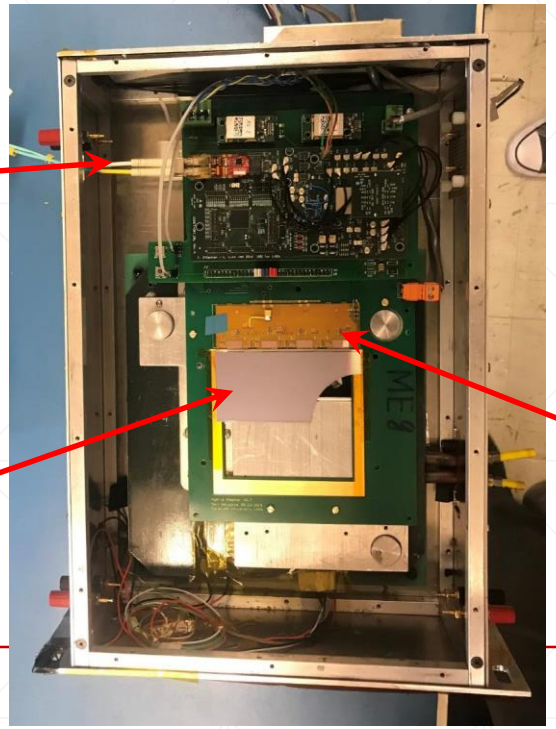
UT读出系统切片

LHCb Upgrade I: Upstream Tracker (UT)

- 在UT研发和建造过程中发挥关键作用, 协调电子学及读出系统各部件的发展。
- 测试 SALT芯片(版本2)的性能, 及纠正设计问题。
- 在10月份参加并成功领导了读出系统的第一次束流测试。

4.48 Gbps 光信号
与~300m 远的后端
读出系统通讯

硅微条探测器
条距 = 93.5 μm
条长 ~ 50 mm.



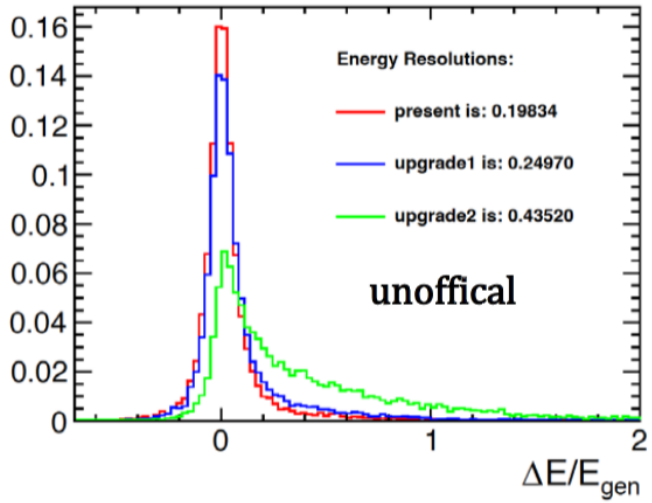
用于束流测试的
数据控制板(DCB) 样品
和UT探测器模块样品

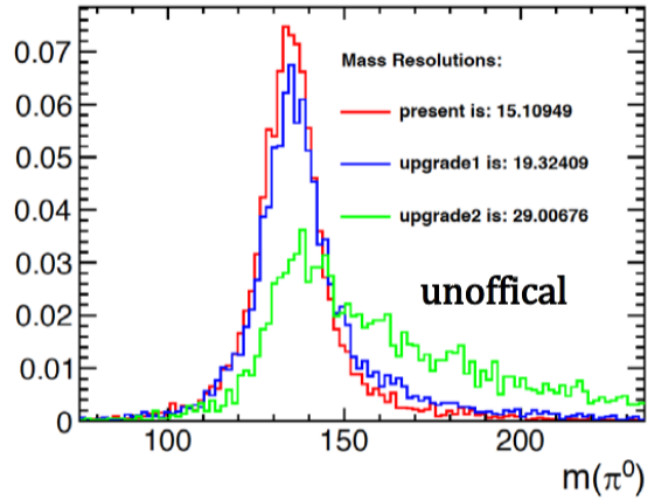
UT组自行设计的前端读
出芯片（SALT）

LHCb Upgrade II: ECAL

LHCb Upgrade II：电磁量能器升级的模拟研究

- **利用Delphes软件开展快速模拟，优化电磁量能器的设计**
  - **通过对簇射横向发展的模拟，研究光子能量分辨和π^0质量分辨**





- **通过计算机模拟，研究电磁量能器的背景粒子流**
  - **Upgrade II 本底增加，理解本底的大小、能量流分布对电磁量器的设计和性能优化至关重要**

结论：现有量能器不能满足Upgrade II 要求，需要提高颗粒度，引入时间信息。
下一步研究：高颗粒度取样型量能器 + 硅探测层用于提供快速时间测量

Thank you!

Questions?

References:

- https://cds.cern.ch/record/2630472/files/passaleva-ichep%2007.07.pdf
- https://cds.cern.ch/record/2650584/files/181206_Kruger.pdf
- https://cds.cern.ch/record/2648754/files/grauges-LHCb-NagoyaHfNPFP.pdf
- ……