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Design and Characterization of MIC4, the Monolithic Active Pixel Sensor for CEPC Vertex Detector

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The Circular Electron Positron Collider (CEPC) is proposed as a Higgs factory to produce adequate events, which is the basis for high precision measurement of Higgs boson. The vertex detector in CEPC should meet the requirement of low material budget, high spatial resolution, fast readout speed and low power consumption. The MIC4 sensor is a CMOS Monolithic Active Pixel Sensor (MAPS) being developed for the R&D activities of CEPC vertex detector. It has been implemented in the TowerJazz 180 nm CMOS Image Sensor (CIS) Process with a high-resistivity epitaxial layer. It measures 3.1 mm * 4.6 mm and features a 128 * 64 (column * row) pixel array with a small pixel pitch of 25 μm. A binary front-end circuit has been designed for a compact pixel combined with a sparisified readout circuitry. Each pixel is composed of an amplification, shaping, discrimination circuit and digital logic. To meet the requirement of high spatial resolution and fast readout speed, a new architecture of an asynchronous zero-suppression data-driven readout circuit is proposed and implemented in MIC4 chip. The periphery of the chip contains bandgap, DACs, serializer and LVDS providing bias for the front-end circuit and transmitting the address data of hit pixels off chip. The preliminary tests show that all the blocks of the chip are functional. The front-end features a peaking time of below 1 μs, a duration time of less than 3 μs, a charge threshold of about 223 e- and an Equivalent Noise Charge (ENC) of 6.2e-. Further tests on the mismatch of the pixel and the high speed readout link are under preparation and we will get the conclusion soon.

Type

Parallel talk

Sessions (parallel only)

Detector performance and upgrade

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