Progress and Status of CMS Trigger Upgrade

Zhen-An LIU on behalf of CMS Team

CLHCP Workshop 2018

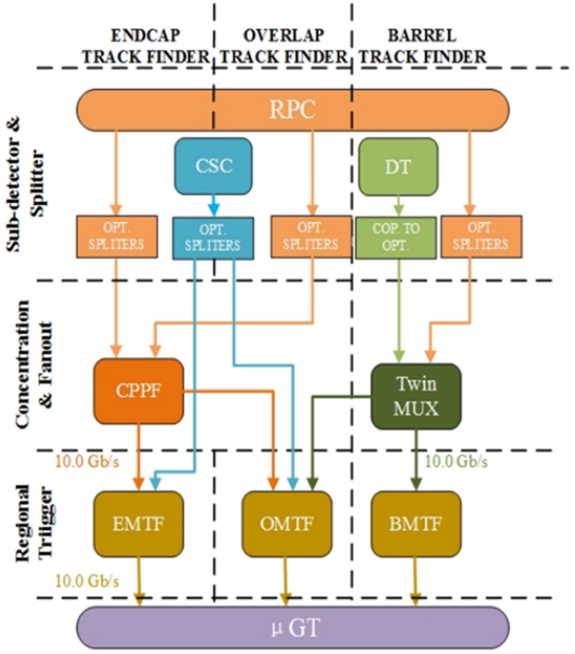
Huazhong Normal Uni., Wuhan

2018年12月19-22 日

Outline

- Progress on Current Trigger System
- Requirement of P2 RPC Backend(BE) Electronics
- Status of R&D
  - First CMS Prototype for RPC BE
  - Further Development
  - New Trigger Requirement
  - Meeting DTH
  - iRPC solution case
- Summary

Progress on Current Trigger System



CMS China-Group had designed and Constructed the CPPF system in CMS L1 Trigger Phase I upgrade which started running since May 2017. In 2018 more works done on CPPF System

Layer 1

1. **On-call Service by China Group: Libo, Ahmad/Siying-Pengcheng/Jingzhou/Zhen-An close collabration home/broad**

Layer 2

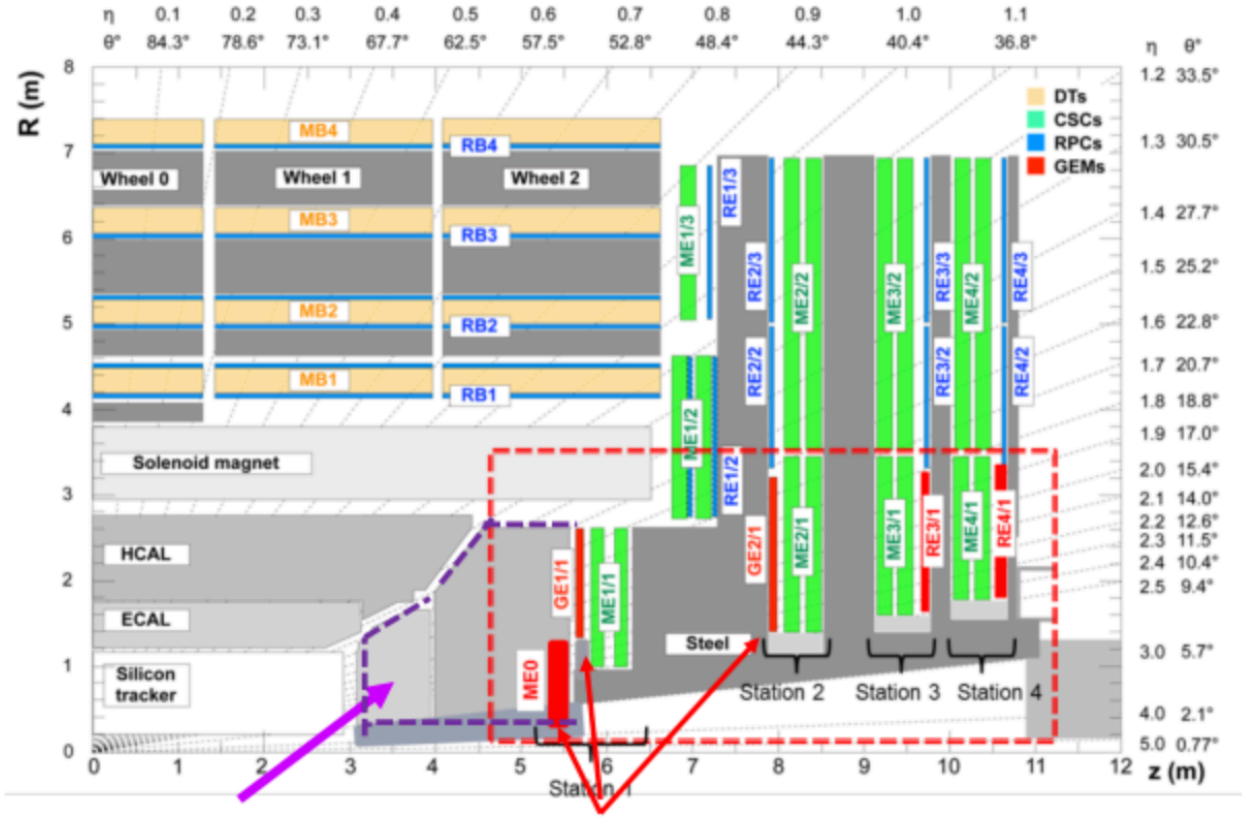
2. **CPPF Emulator + Unpacker Software Devlopment by Libo**

Layer 3

3. **CPPF data validation by Libo**
4. **CPPF board firmware IPBUS Builder by Pengcheng**
5. **CPPF Test Manager Security software by Hanjun/Pengcheng**
6. **CPPF DQM by Guangyi/Mingshui/Zhen-An**

China Activities inn CMS Phase II Upgrade

- **中国组拟承担CMS phase II 升级任务**



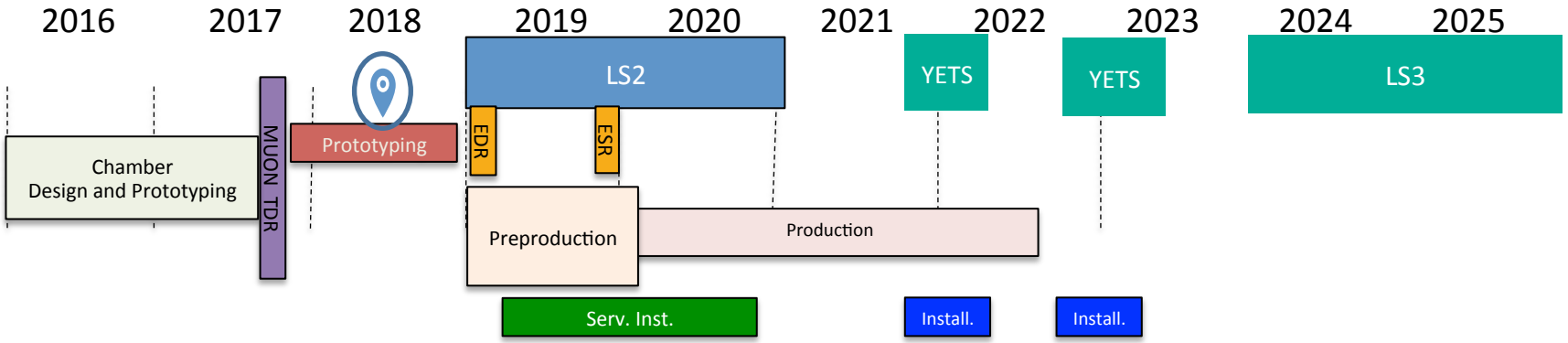
端部量能器升级
高能所

端盖μ触发探测器升级
北京大学, GEM

缪子backend
电子学及触发 高能所

RPC BE3.1/4.1 Backend Electronics

RE3/1 and RE4/1



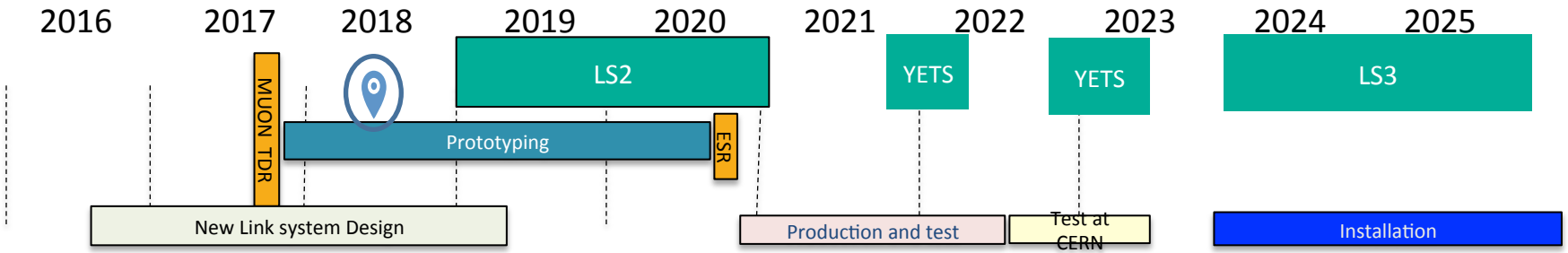
1. Prototype+Joint Test electronically

2. Integration MTCA system

3. Migration to ATCA if neccesary and possible

RPC Upgrade Schedule/New DAQ Backend

New Link System/New RPC DAQ



1. ATCA Prototype

2. ATCA/TTC-DAQ protoT

3. Final ATCA

4.Production

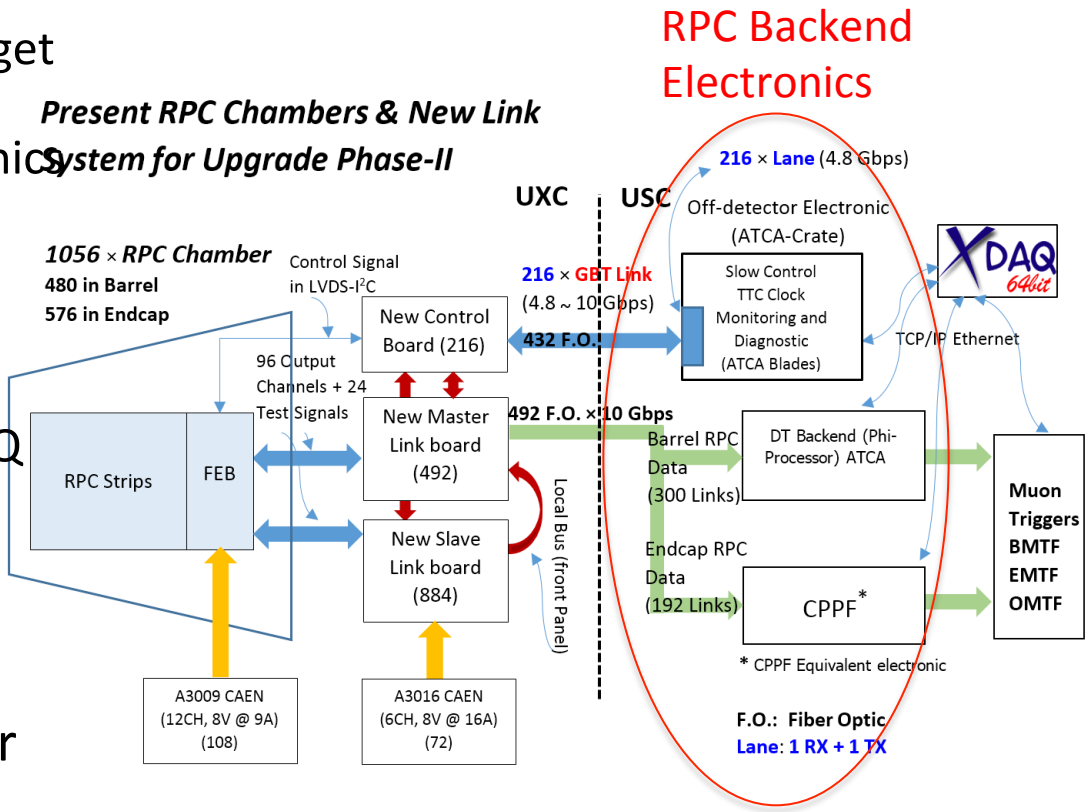
5.Integration

Challenges in Phase II Upgrade

- Electronics/trigger/DAQ borders less clear
- More General purpose module design
- Less types of modules
  - 5 types in Phase I (uTCA)
  - Lesser in Phase II ?
  - ATCA Compliant
- General Purpose Backend Electronics?
  - Fast Control(TCDS/TTC/TTS)
  - DAQ of FEE
  - Layer1 trigger for primitives?

Requirement of P2 RPC Backend(BE)

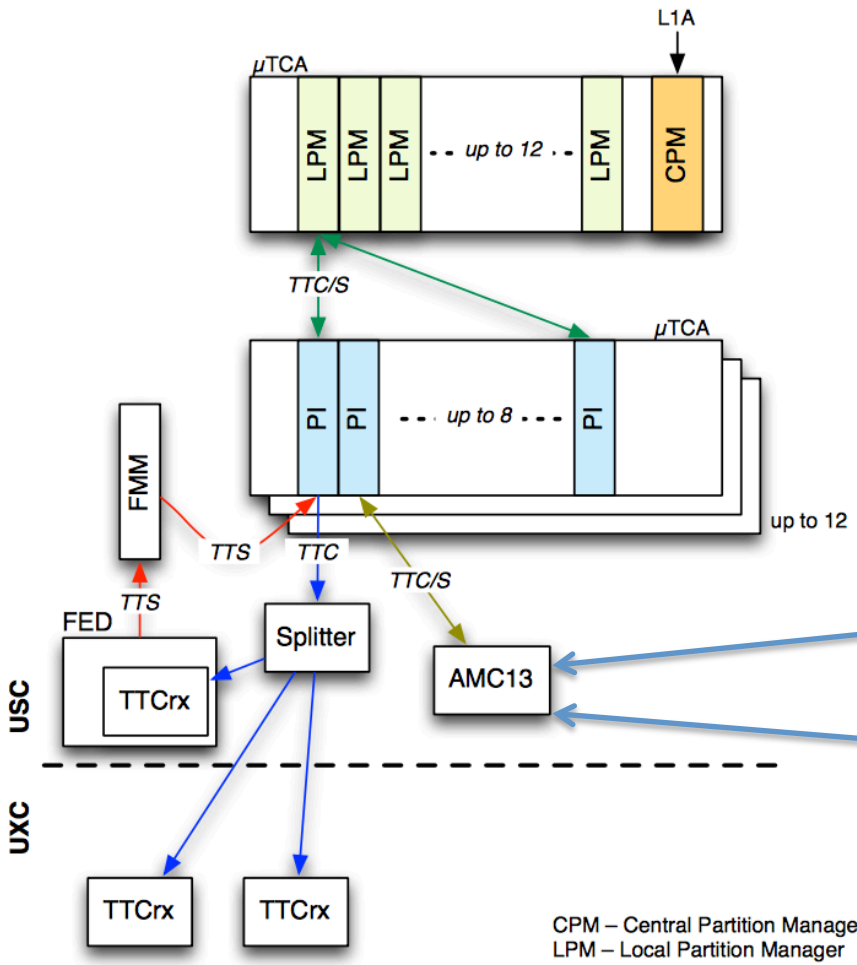
- Functionalities
  - Fast Control
    - Interfacing to CMS DTH To get TTC/TCDS(Backplane)
    - Providing TTC to FE Electronics (GBT)
  - DAQ
    - Accepting DAQ from FE Electronics (GBT)
    - Sending data to Central DAQ via CMS DTH (Panel)
  - Slow Control
    - Interfacing to Slow Control (MCH/PC)
  - Trigger Layer1 Processor for Barrel and Endcap
- ATCA compliant module

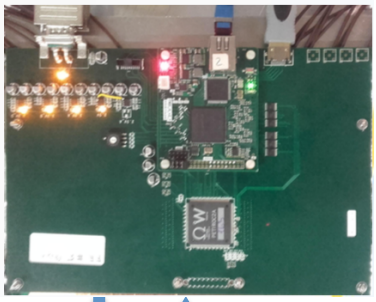


China Proposals(RPC/Muon Workshops) and Status

- RE3.1/RE4.1 Design
- Progress on RE3.1/4.1
- General Purpose Backend Module Design
- RPC Backend Solution

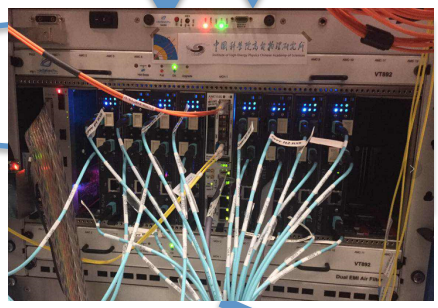
RE3.1/4.1 Backend Electronics(TDAQ+TTC/SC)

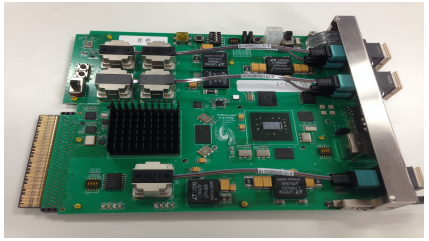




Data

GBT

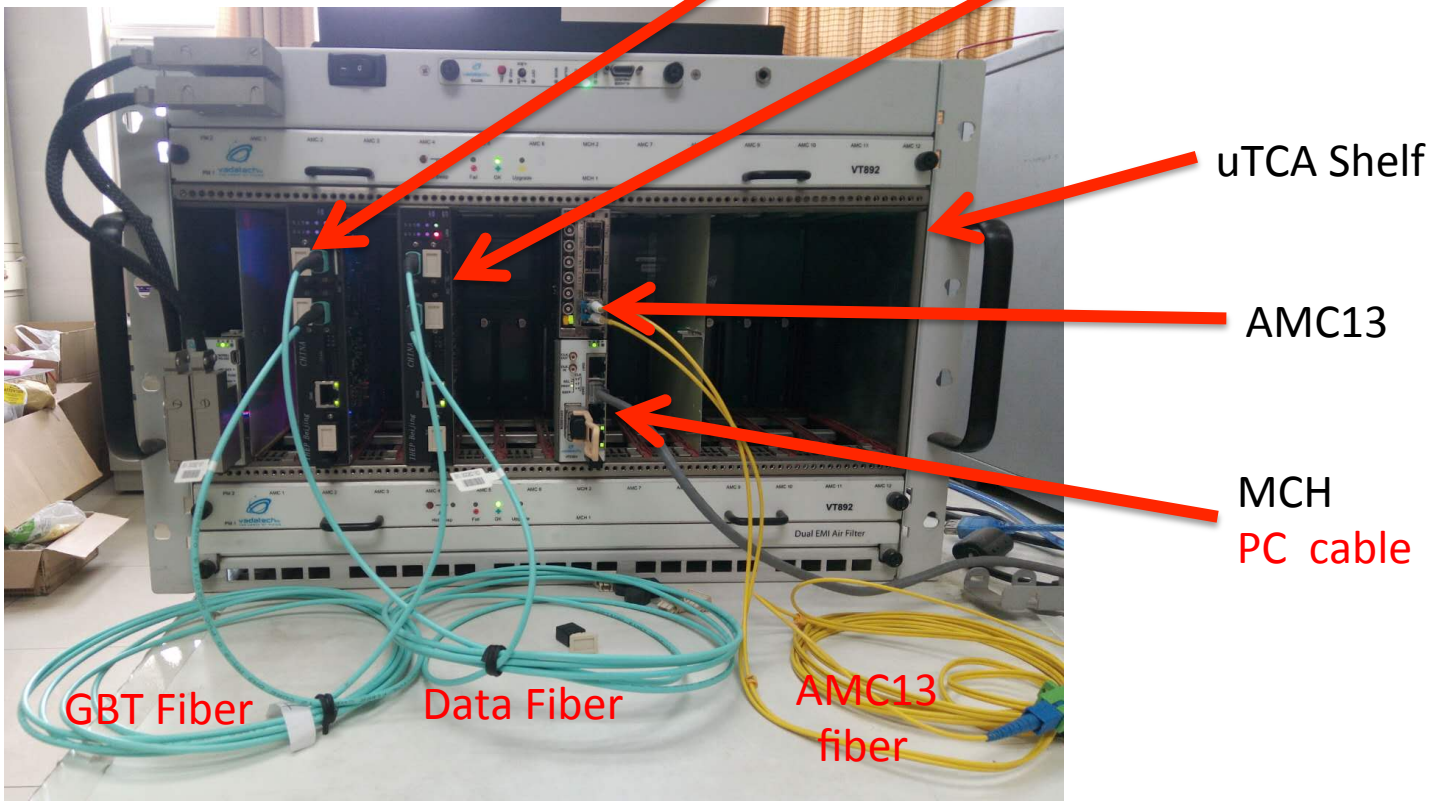




EMTF

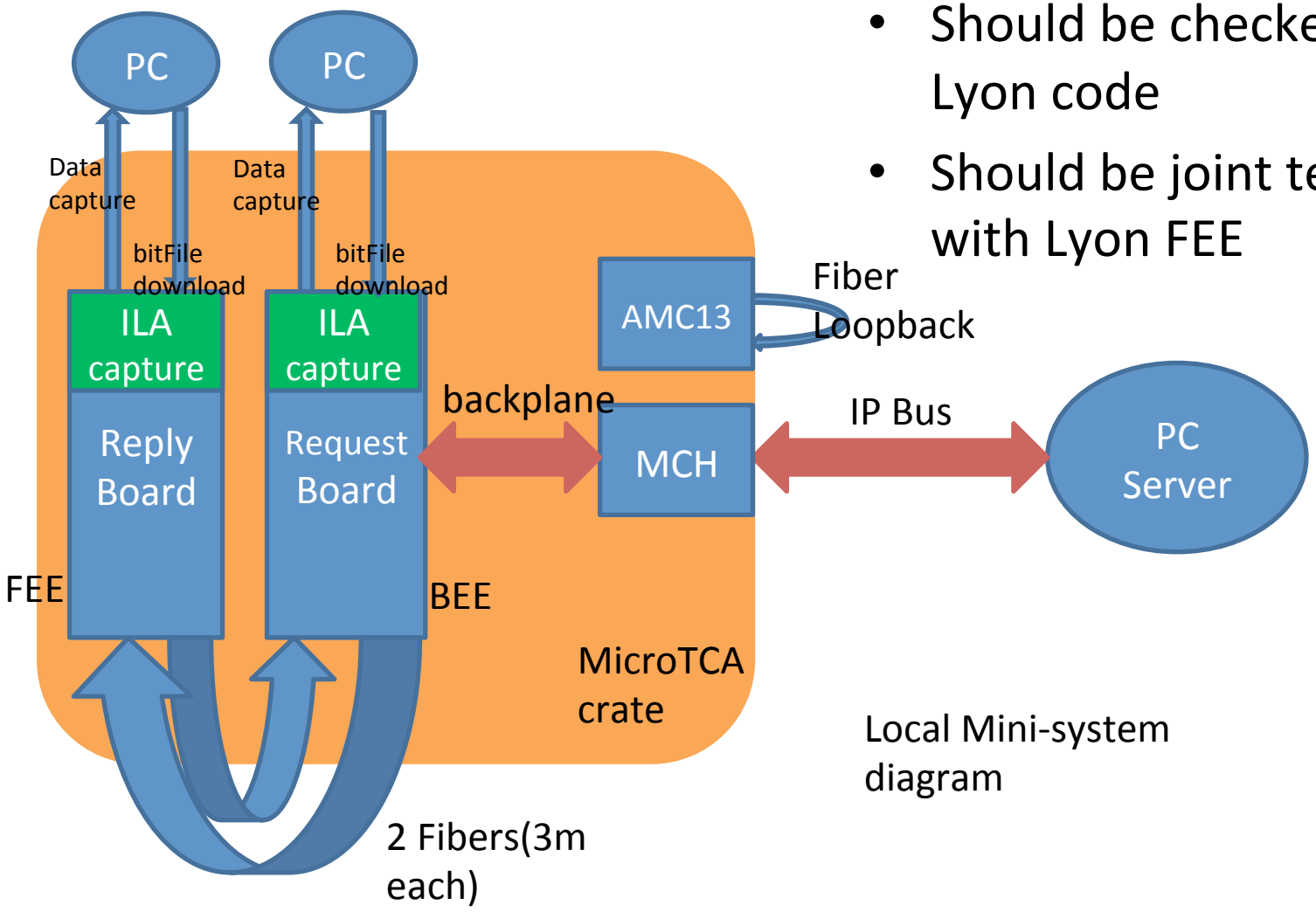
Status of Firmware Development

- Demo/test system at TriggerLab/IHEP ready
  - GBT transmission and receiving done
  - FEE Code expected from Lyon friend in November, will confirm again.



Demo system with Data flow

- The system works
- Should be checked with Lyon code
- Should be joint tested with Lyon FEE



Local Mini-system diagram

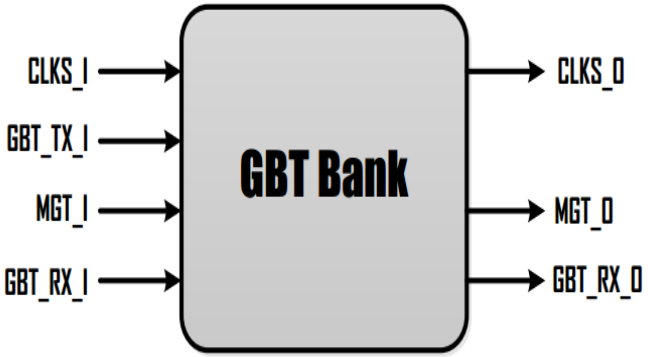
GBT BANK Implementation in test board

- GBT-FPGA is implemented in CPPF step by step, firstly is the protocol layer(also known as GBT BANK) as shown following
  - The scrambler/descrambler, RS encoder/decoder, SerDes which are the main functions in GBT-FPGA are implemented in this level
- This test is done in one CPPF board, one GTH channel at 4.8Gbps, in fiber(3m) loopback mode
- Customized 4bits(slow control)+80bits(user data)=84bits fake data to verify the functionality of the GBT BANK after migrated to CPPF
- The test results show that GBT BANK performs well in CPPF
  - Data captured in ILA shows the RX data is as the same sequence as the TX data, latency is not measured

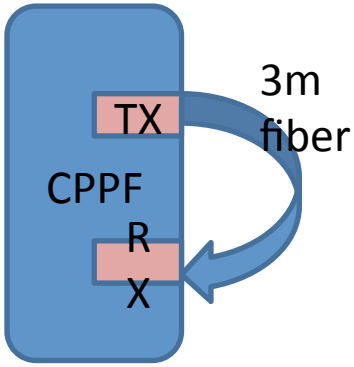
84bits TX data

84bits RX data

GBT BANK



Loopback test

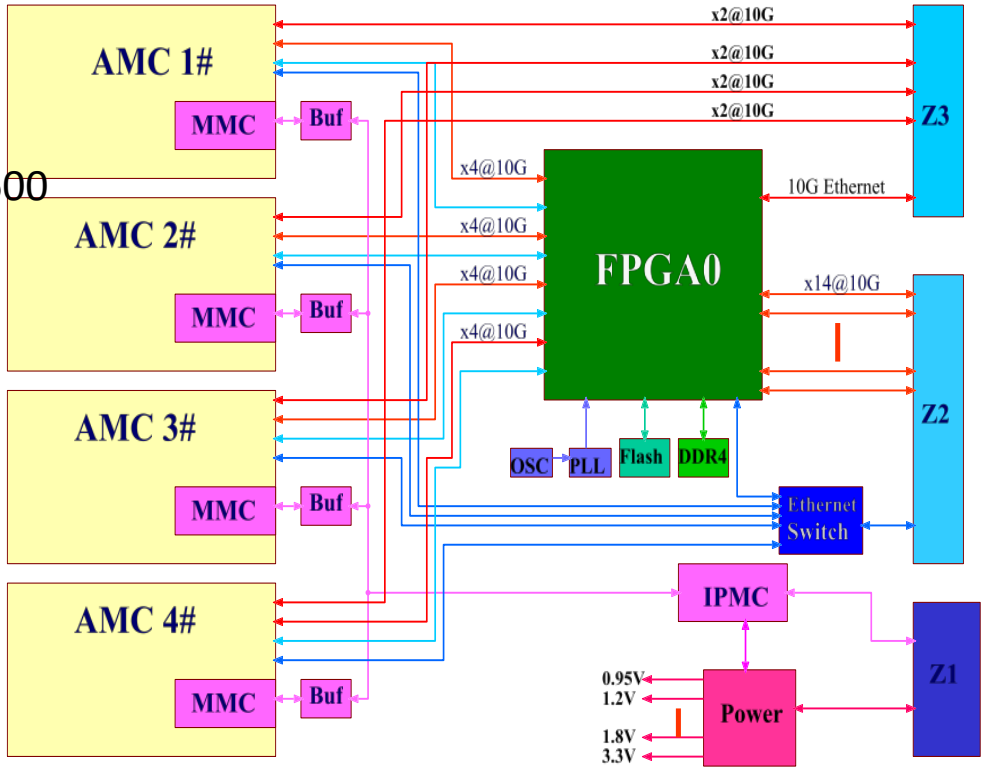


Progress on R&D-First Prototype for RPC/CMS

- Complete Module
  - Carrier Board (new design for CMS, Full ATCA size)
    - To get TTC/TCDS via Backplane from DTH (~10Gbps)
    - Distributing TTC to AMCs (max 10Gbps)
    - Providing interconnection between AMCs (DAQ) (~ 10Gbps)
    - IPMC/MMC
  - AMC for Control/DAQ (present, double AMC)
    - GBT with FEE (4.8 Gbps) for iRPC
  - AMC for CPPF
  - RTM (backups)

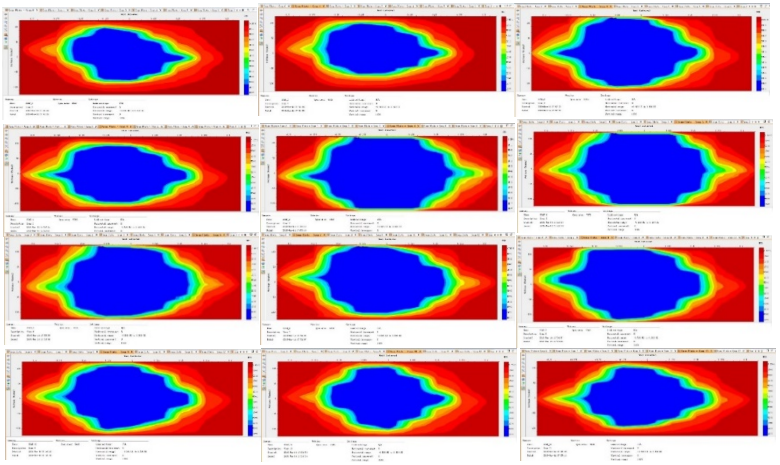
General Purpose BE /ATCA Carrier Design

- **FPGA:** Ultrascale Kintex xcku060
- **RAM:** 16 GB DDR4 (8 chips)
- **MGTs:** 16.3 Gbps
  - 4 links to each AMC card (currently: 4 x600 Mbps LVDS)
  - 12 links to ATCA backplane
  - 1 link to RTM (10G Ethernet)
- **GbE switch:**
  - 4 xFPs/2CPPFs ,
  - 1 switch FPGA,
  - 1 uplink to ATCA Base Interface
  - 1 RTM RJ45
- 10 Gigabit Ethernet to RTM(SPF+)
- **Configuration**
- **Programmable MGT clock**
- CPLD as **JTAG hub**

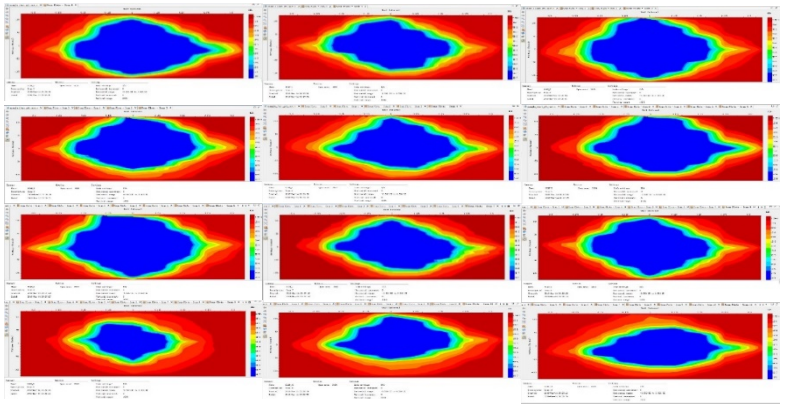


Backplane chains test 10 Gbps OK

- Backplane Communication
  - 12 Backplane channel point-to-point connection between two blade,
  - 10Gbps/ch for Backplane connector.
  - 24 hours, No error on 12.5Gbps.
- Results: 10Gbps OK

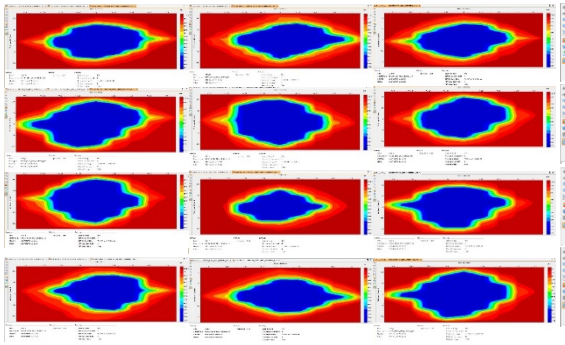


Backplane MGT 10G 12channel

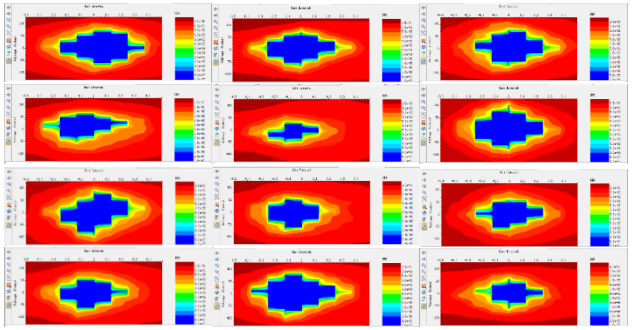


Backplane MGT 12.5G 12channel

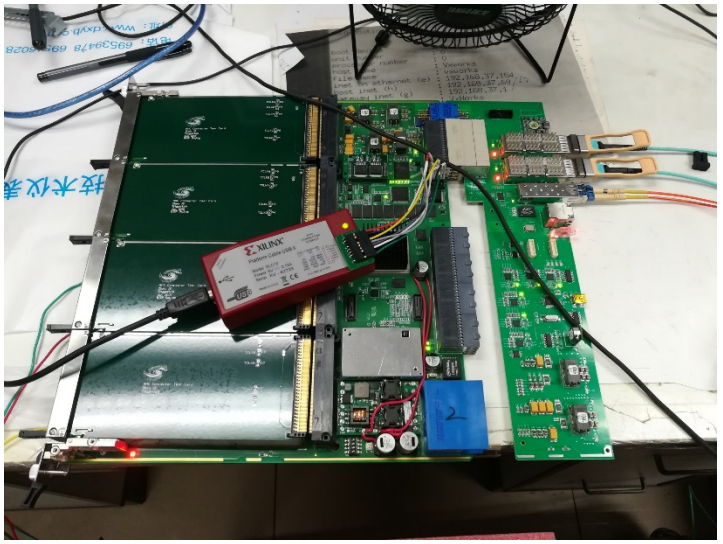
AMC and RTM links tested 10Gbps OK



AMC MGT 10G



AMC MGT Pre-Cursor 12.5G



12 hours, No error on 10Gbps and 12.5Gbps.

Serial I/O Links

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-C
Ungrouped Links (0)										
Link Group 0 (14)							Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 14	MGT_X1Y2/TX	MGT_X1Y2/RX	10.000 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 15	MGT_X1Y3/TX	MGT_X1Y3/RX	10.002 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 16	MGT_X1Y4/TX	MGT_X1Y4/RX	10.002 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 18	MGT_X1Y6/TX	MGT_X1Y6/RX	9.999 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 19	MGT_X1Y7/TX	MGT_X1Y7/RX	10.002 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 20	MGT_X1Y8/TX	MGT_X1Y8/RX	10.000 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 22	MGT_X1Y10/TX	MGT_X1Y10/RX	9.998 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 23	MGT_X1Y11/TX	MGT_X1Y11/RX	10.002 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 24	MGT_X1Y12/TX	MGT_X1Y12/RX	10.000 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 26	MGT_X1Y14/TX	MGT_X1Y14/RX	10.000 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 27	MGT_X1Y15/TX	MGT_X1Y15/RX	9.999 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 28	MGT_X1Y16/TX	MGT_X1Y16/RX	10.000 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 30	MGT_X1Y18/TX	MGT_X1Y18/RX	10.002 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB
Link 31	MGT_X1Y19/TX	MGT_X1Y19/RX	10.000 Gbps	6.54...	0	0	1.528E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB

Serial I/O Links

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor
Ungrouped Links (0)										
Link Group 0 (12)							Reset	PRBS 7-bit	PRBS 7-bit	Multiple
Link 0	MGT_X1Y4/TX	MGT_X1Y4/RX	12.49...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 10	MGT_X1Y14/TX	MGT_X1Y14/RX	12.50...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 11	MGT_X1Y15/TX	MGT_X1Y15/RX	12.50...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 12	MGT_X1Y16/TX	MGT_X1Y16/RX	12.49...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 14	MGT_X1Y18/TX	MGT_X1Y18/RX	12.50...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 15	MGT_X1Y19/TX	MGT_X1Y19/RX	12.50...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 2	MGT_X1Y6/TX	MGT_X1Y6/RX	12.50...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 3	MGT_X1Y7/TX	MGT_X1Y7/RX	12.50...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 4	MGT_X1Y8/TX	MGT_X1Y8/RX	12.49...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 6	MGT_X1Y10/TX	MGT_X1Y10/RX	12.49...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 7	MGT_X1Y11/TX	MGT_X1Y11/RX	12.50...	3.974E14	0	0	2.517E-15	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)
Link 8	MGT_X1Y12/TX	MGT_X1Y12/RX	12.49...	3.948E14	0	0	2.533E-15	Reset	PRBS 7-bit	PRBS 7-bit	2.50 dB (01010)

Characteristic of this module

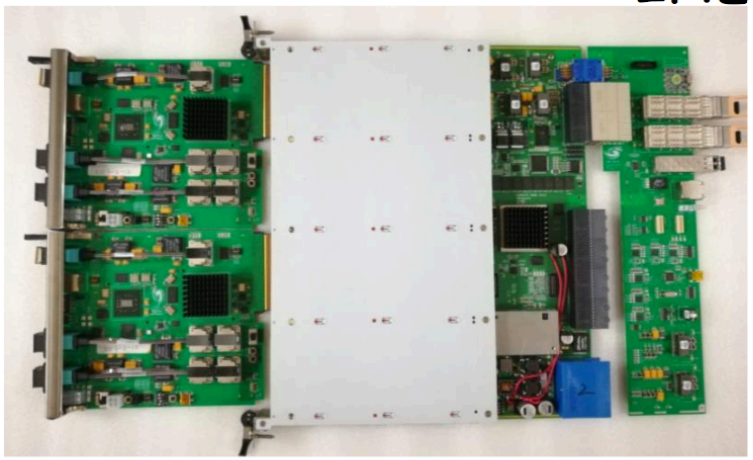
- Similar Module designed for PANDA Project
  - **DOI:** 10.1109/RTC.2010.5750331, **arXiv:1806.09128v2**
- Similar Module taking data at Belle II/PXD
  - https://indico.mitp.uni-mainz.de/event/119/session/1/contribution/58/material/slides/0.pdf
  - https://indico.desy.de/indico/event/7866/session/3/contribution/55/material/slides/0.pdf
- Modularity
  - Carrier Board will match with DTH for TTC
  - AMC board for Control/DAQ
  - AMC board for trigger Concentration/layer1 processing/Fan-out
- Inter-changeability
  - AMC board can work both as ATCA/daughter or in uTCA crate

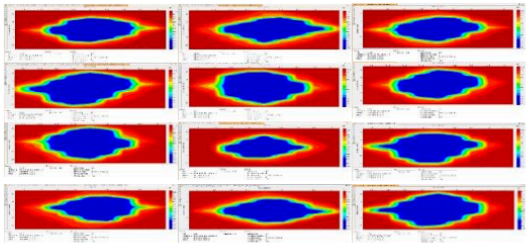
Report given in TDAQ Review by Darin

R&D Status with RPC BE/Concentration

IHEP

- ATCA: 1 Carrier + 2 AMC Processor + 1 RTM
- AMC Processor
  - Data throughput
    - 3 MiniPoD, support 360Gb/s INPUT,
    - 2 MiniPoD, support 240Gb/s OUTPUT
  - XC7VX415T-2 (Virtex-7)
    - Core FPGA for data processing,
    - 48 channel GTH Transceivers,
    - Support up to 13.1 Gbps per channel。
  - XC7K70T-2 (Kintex-7)
    - Control FPGA,
    - Configure and Control CPPF.
  - AT32UC3A1512 (Atmel)
    - MMC, Module Management Controller.
- Carrier
  - Ultrascale Kintex xcku060
  - Designed for RPC backend
  - Communication with CMS DTH
  - Link speed 12-16.3Gbps





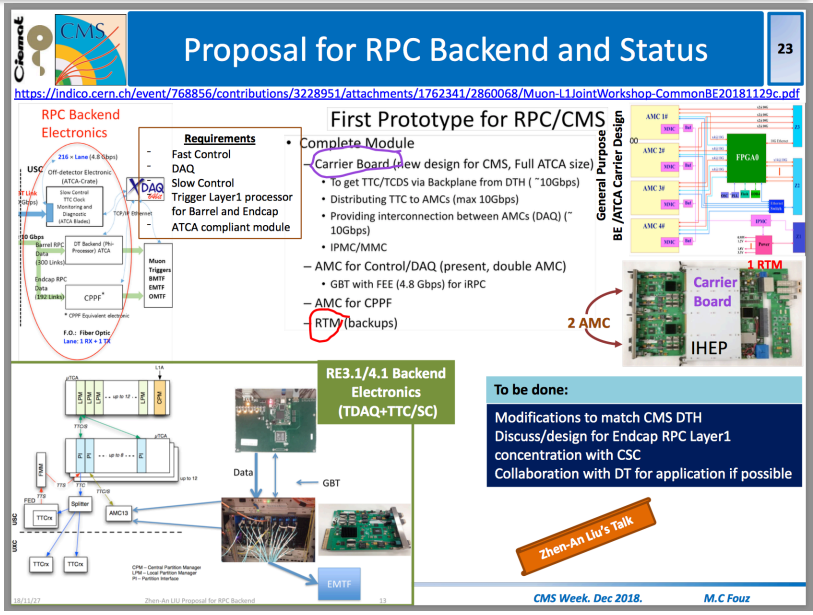
Report be given in TDAQ Review(2)

Trigger Concentration future plan IHEP

- Common ATCA board development
  - Carrier modification to match CMS DTH
    - TTC
    - Slow control
    - RPC DAQ
  - AMC processor for iRPC and RPC control
  - AMC processor for concentration of RPC/CSC at least, better also iRPC and GEM inputs before Endcap tracker finding
    - 10 Gbps inputs
    - 26 Gbps output

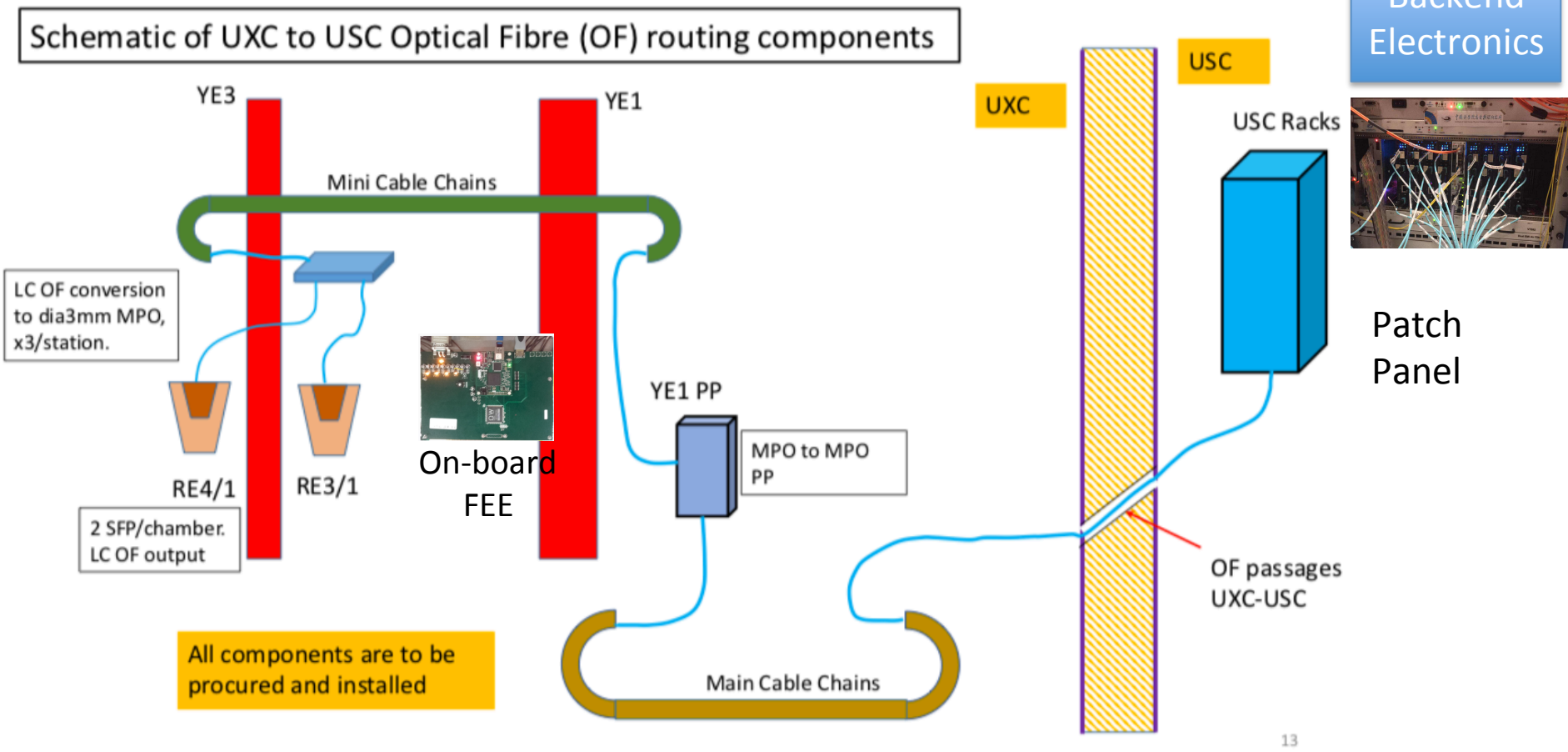
Most recent Status(December 2018)

- First ATCA Prototype in CMS reported to the collaboration(RPC,Muon review,CMS week report)
- China Proposal was summaried in CMS Week
- RPC and Muon Group had common understanding for the responsibilities
  - RE3.1/RE4.1
  - RPC Backend



Fiber Arrangement decided

- Andres, Anton, Behzad, Ian, Zhen-An
- Experience from China play an important role



Further Development

- Joint test for Implementation of iRPC control and DAQ
- Standardized Carrier for CMS DTH
- Control/DAQ card improve for DTH
- Discuss/design for Endcap RPC Layer1 concentration with CSC, and/or more if possible
- Collaboration with DT/DTH colleagues for application

Summary

- Stronger responsibility in CPPF system running
- Phase II design going well
  - An RPC Backend Electronics Solution is accepted
  - A prototype for CMS is presented with similar application in PANDA and Belle II experiments
  - Characteristic of modularity of this ATCA board make it a multi-purpose module for iRPC Control, iRPC DAQ, iRPC trigger, RPC Backend, Trigger layer1 concentration/processing
- Future plan is described