Design of the LHCb Sci-Fi tracker read-out electronics and the QA system

2018.12.19

Yuyue Gan[1], Ming Zeng[1], Guanghua Gong[1], Zhenwei Yang[1], Li Xu[1],
Yifei Jin[1], Xinchao Fang[1], Albert Comerma[2], Xiaoxue Han[2]

[1]Department of Engineering Physics, Tsinghua University
[2]Physikalisches Institut, Universität Heidelberg

Outline

- Sci-Fi Tracker readout electronics
- QA system for Frontend Boards
- QA system for packaged ASICs

Outline

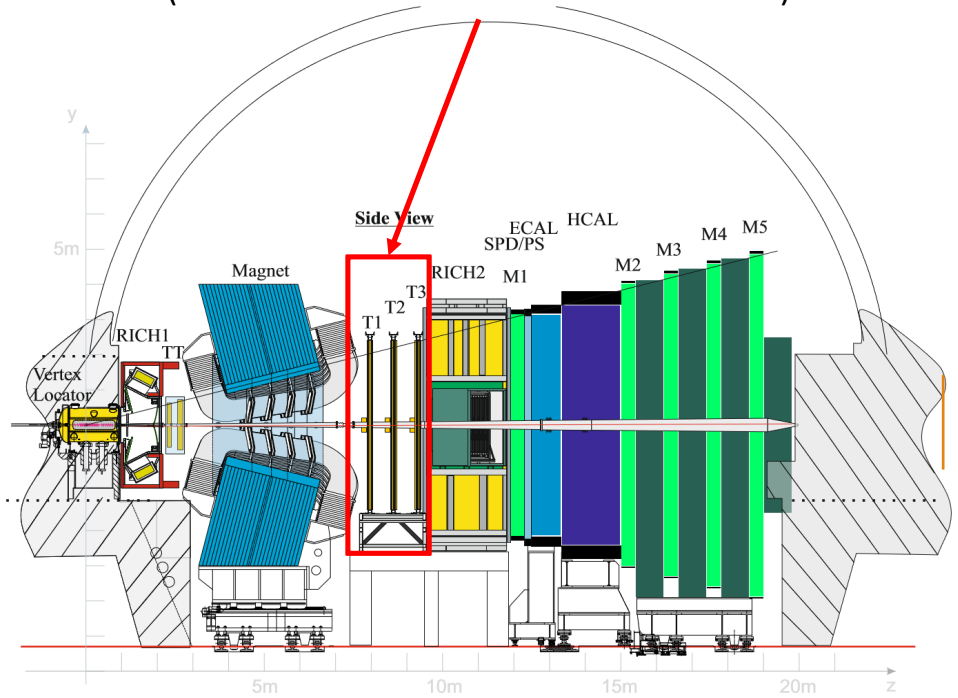
- Sci-Fi Tracker readout electronics
- QA system for Frontend Boards
- QA system for packaged ASICs

LHCb Upgrade

- Goal: increase statistics by more than ×10
  - ✓Operate at $2 \times 10^{33} cm^{-2} s^{-1} \rightarrow 50\ fb^{-1}$
  - ✓Triggerless 40MHz readout

- Scintillating Fibre (Sci-Fi) Tracker
  - ✓Fast, high efficiency (~99%)
  - ✓High granularity (250µm)
  - ✓High resolution (<100µm)
  - ✓Low mass (<1% X_0/layer)
  - ✓Radiation hardness (up to 35kGy)

The current Tracking Stations
(Gas Straw Tube Tracker + Silicon Tracker)

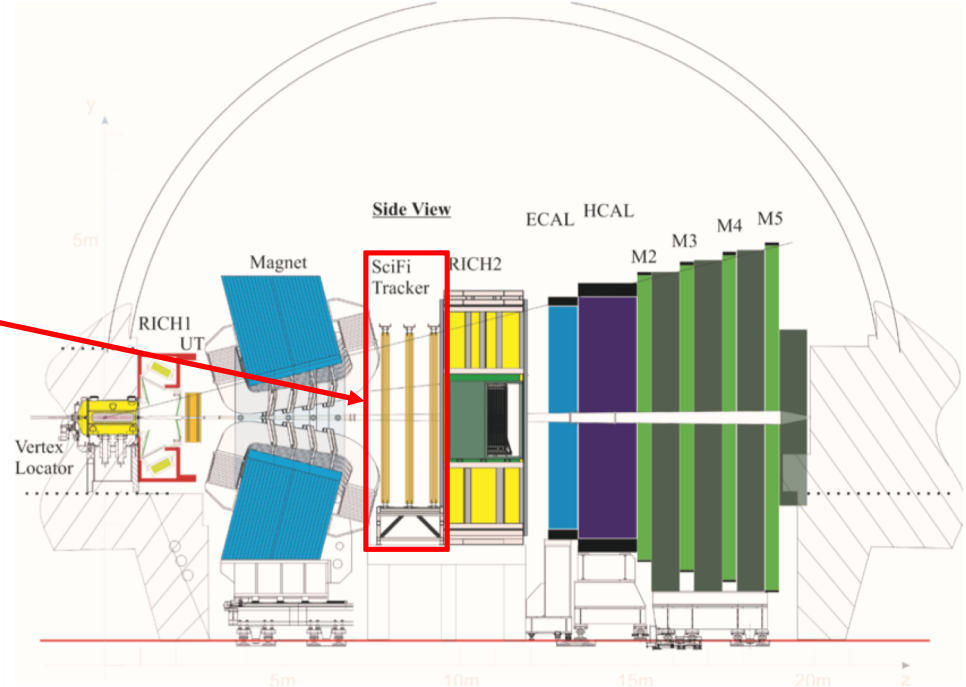


Schematic view of the current LHCb detector

LHCb Upgrade

- Goal: increase statistics by more than ×10
  - ✓Operate at $2 \times 10^{33} cm^{-2} s^{-1} \rightarrow 50\ fb^{-1}$
  - ✓Triggerless 40MHz readout

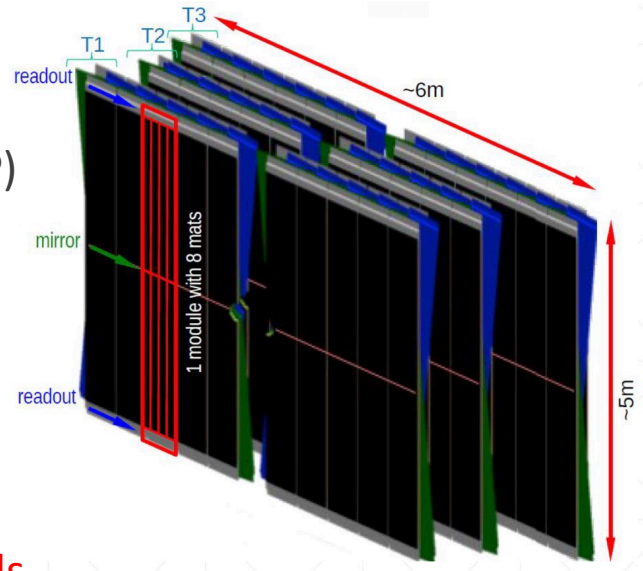
- Scintillating Fibre (Sci-Fi) Tracker
  - ✓Fast, high efficiency (~99%)
  - ✓High granularity (250µm)
  - ✓High resolution (<100µm)
  - ✓Low mass (<1% X_0/layer)
  - ✓Radiation hardness (up to 35kGy)

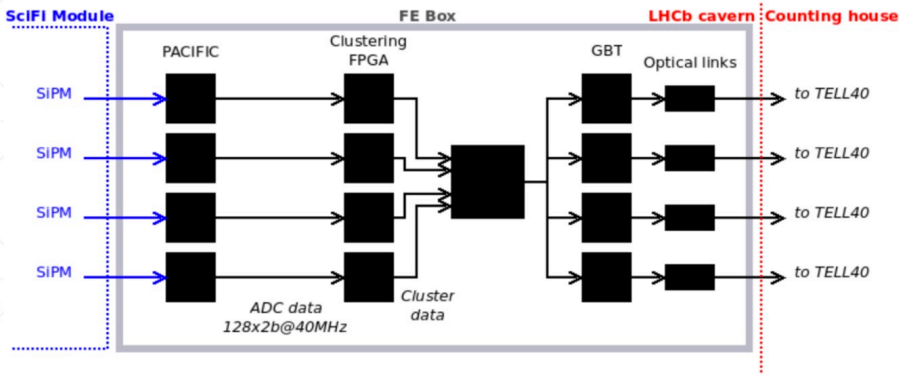


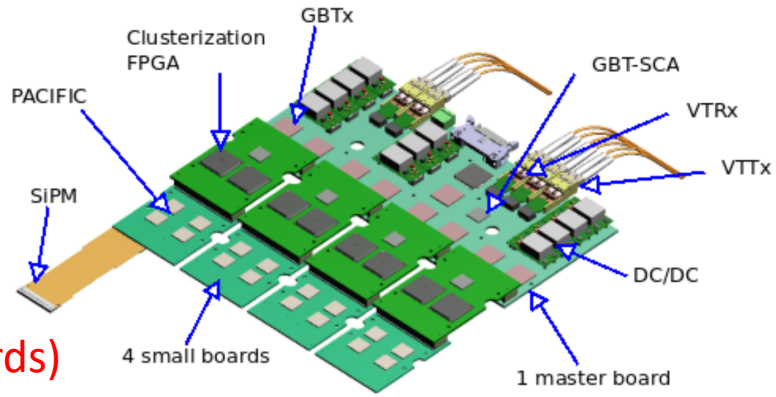
Schematic view of the current LHCb detector

Sci-Fi readout electronics (FE)

- Tracker structure:
  - ✓3 Tracking Stations
    - ✓12 detector layers (X-U-V-X, 5°)
      - ✓144 modules
- Electronics design:
  - ✓~340m² total active surface
  - ✓524,000 SiPM channels
  - ✓12,000 PACIFIC chips needed
  - ✓2,500 Frontend Electronic Boards



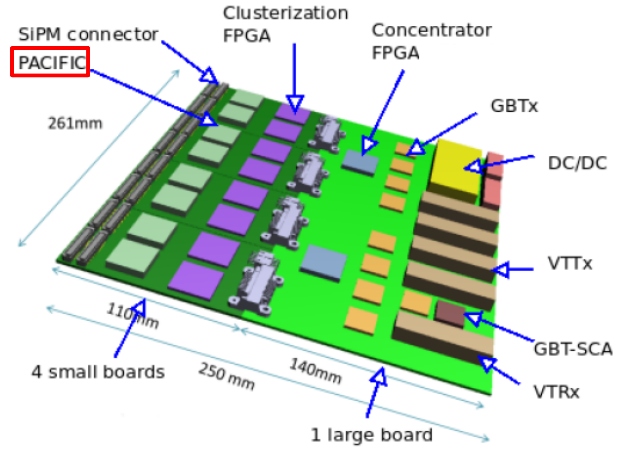


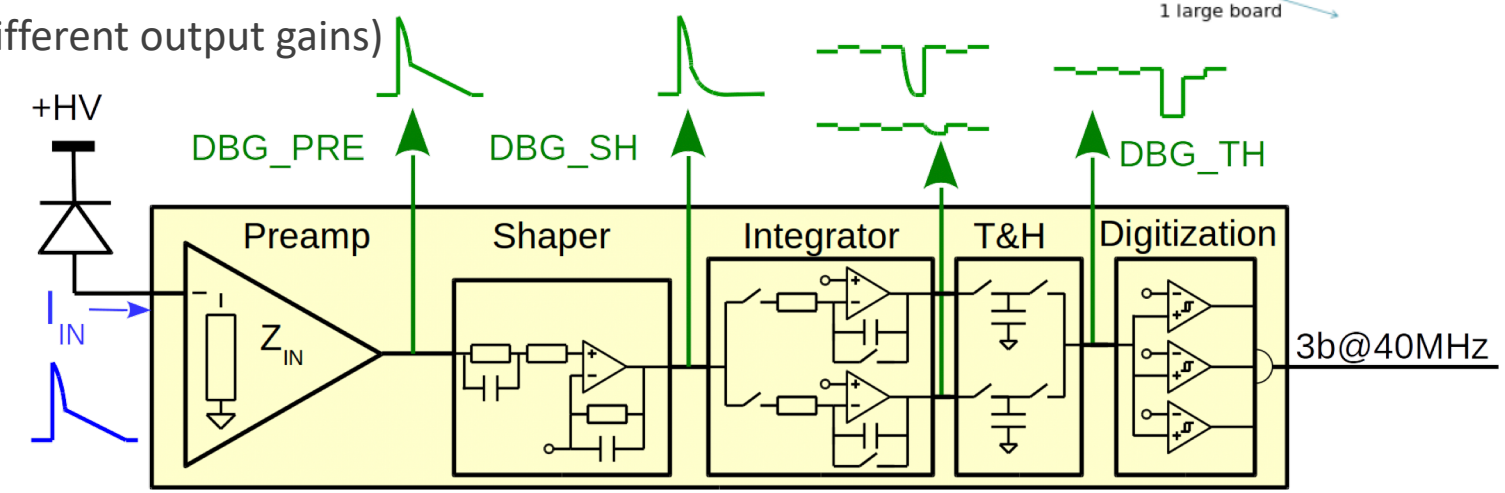


- LHCb China Group 2016~2018:
  - ✓Co-design Sci-Fi Frontend Electronic Boards
  - ✓Manufacturing all Frontend Boards in China, testing a part
  - ✓Sci-Fi Readout Electronics Quality Assurance System (For chips and boards)
  - ✓Readout Electronics for Detector Performance Evaluation (>20 setups in Sci-Fi group)

PACIFIC5

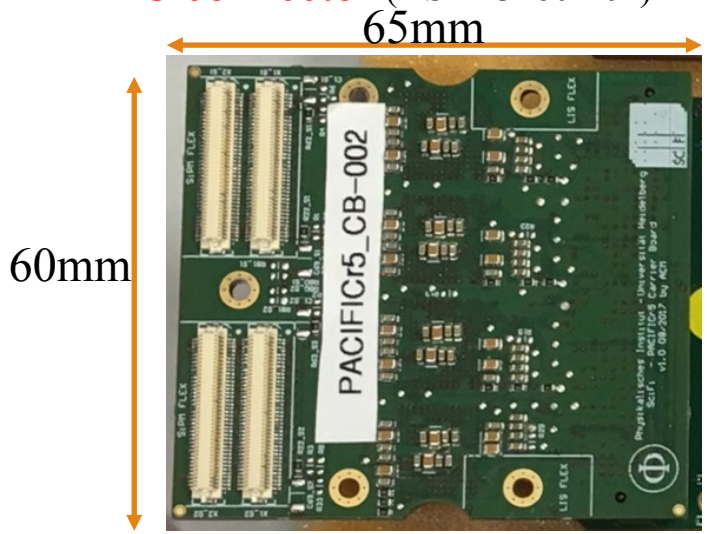
- 64-channel SiPM readout ASIC for the Sci-Fi Tracker
- Current mode input
- Low input impedance (≈50Ω)
- High Bandwidth preamplifier (≈250MHz)
- Output： 8bit×16pair@320MHz
- Main functional blocks:
  - ✓Pre-amplifier(Current->Voltage, 4 different output gains)
  - ✓Shaper
  - ✓Offset trim
  - ✓Integrators×2 (20MHz)
  - ✓Track & Hold
  - ✓Digitization (with 3 comparators)



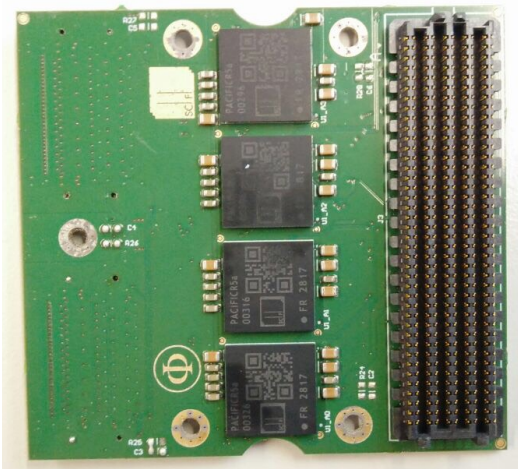


Frontend (PACIFIC Carrier) Board

- 4 × PACIFIC ASICs (196-pin BGA packaged)
- 4 × temperature measurement circuits (voltage divider circuits with NTC , 2 for SiPMs, 2 for the ASICs)
- 4 × SiPM bias voltage measurement circuits (voltage divider circuits)
- 1 × BoardID IC (DS2401 64-bit unique, factory-lasered silicon serial number, no permanent damage up to 140Gy)
  http://radwg.web.cern.ch/RadWG/Pages/showExternal.aspx?GotoUrl=https://twiki.cern.ch/twiki/bin/viewauth/Main/TulliosPreferredPartList
- 4 × SiPM flex cable connectors (Hirose DF12(3.0)-80DS-0.5V), SLVS differential outputs of 256-CH
- 1 × FMC connector (ASP-134602-01)

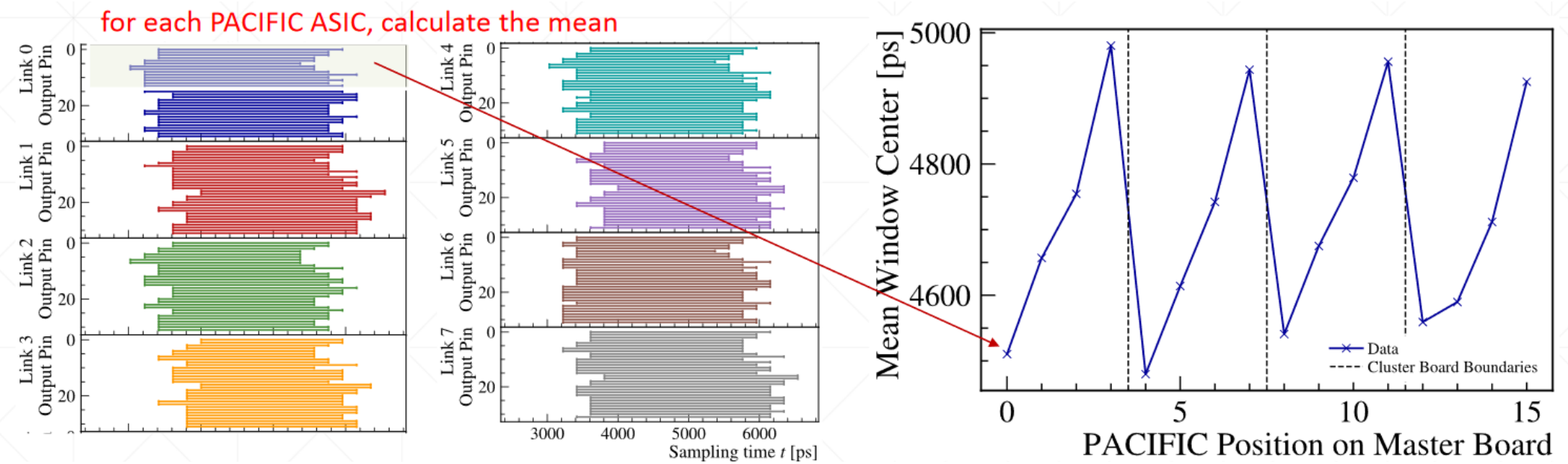


front view of the PACIFIC Carrier Board


back view of the PACIFIC Carrier Board

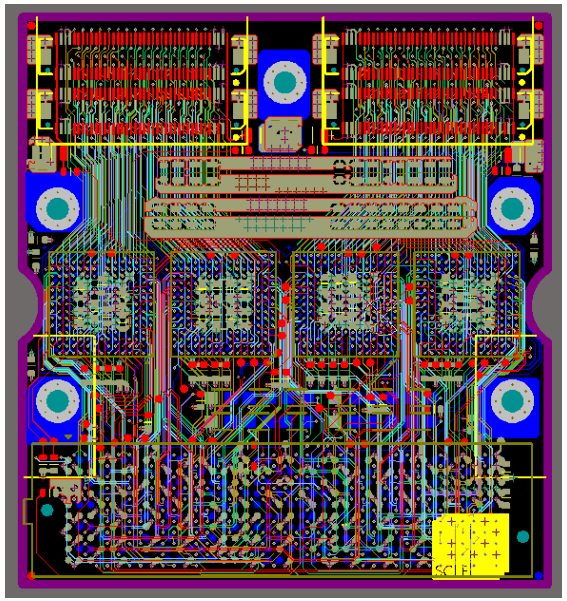
A question raised in old Carrier Boards

- Different offsets of the sampling window across all data output, reduce the sampling window **from 2.4ns to 1.4ns**, tested by Daniel Berninghoff in Heidelberg (https://indico.cern.ch/event/721309/contributions/3011775/attachments/1653078/2644967/ElectronicsStatus_0518_SciFiGM.pdf)



Redesign of PACIFIC Carrier Board

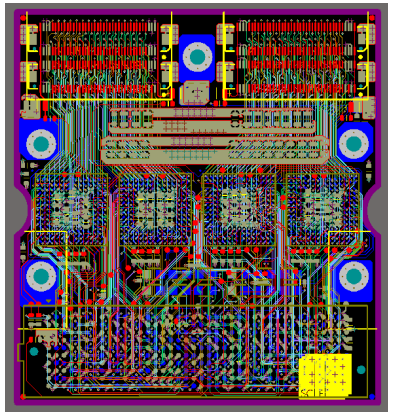
- We decided to re-optimize the routing of the PACIFIC Carrier Board
  - ✓ for a higher production yield
  - ✓ more strict routing constraints, to gain larger size of the sampling window
    - 4 pairs of PACIFIC Clock lines (CLKIN_0~3) : routing length match < 1mm
    - 4 SYNC lines (SYNC_0~3): routing length match < 1mm
    - 64 pairs of data lines (DATA_0~3_X) : routing length match <3mm.
    - well separate the analog input signals and the output data lines, the CLOCK lines
    - from 8-layers to 14-layers
    - Calculate impedance for Halogen Free (TU-862HF), and keep thickness 1.7mm

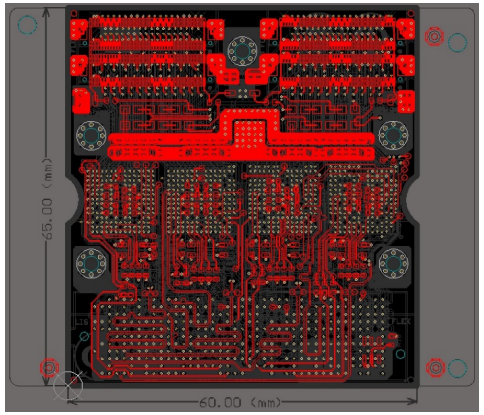


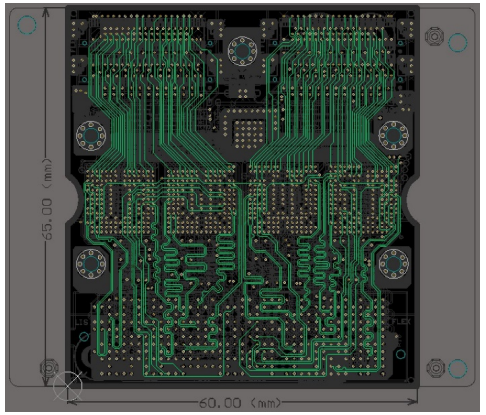
Re-optimized PACIFIC Carrier Board r4

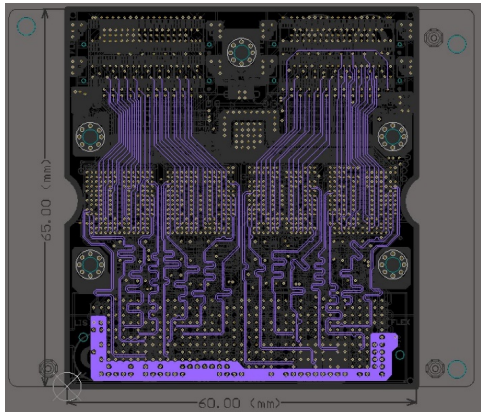
- The design has been completed.
  - ✓ For the first 250 PACIFIC Carrier Boards, we have assembled first 10 PCBs, and checked with the Sci-Fi readout electronics (MB+CB) to make sure everything works fine after this optimization.

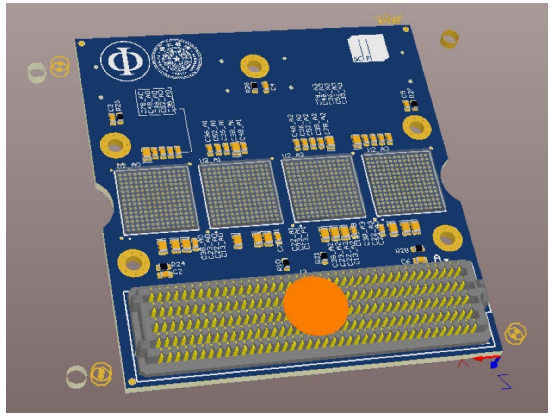
Redesign of PACIFIC Carrier Board

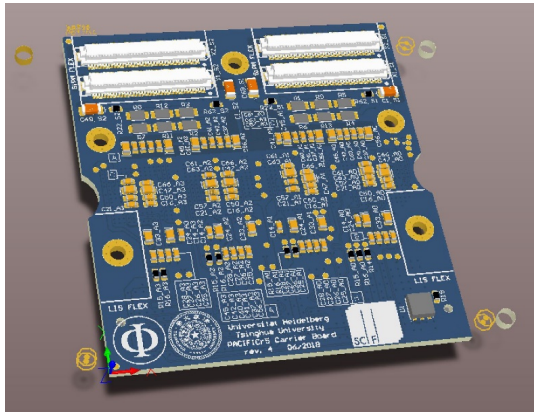








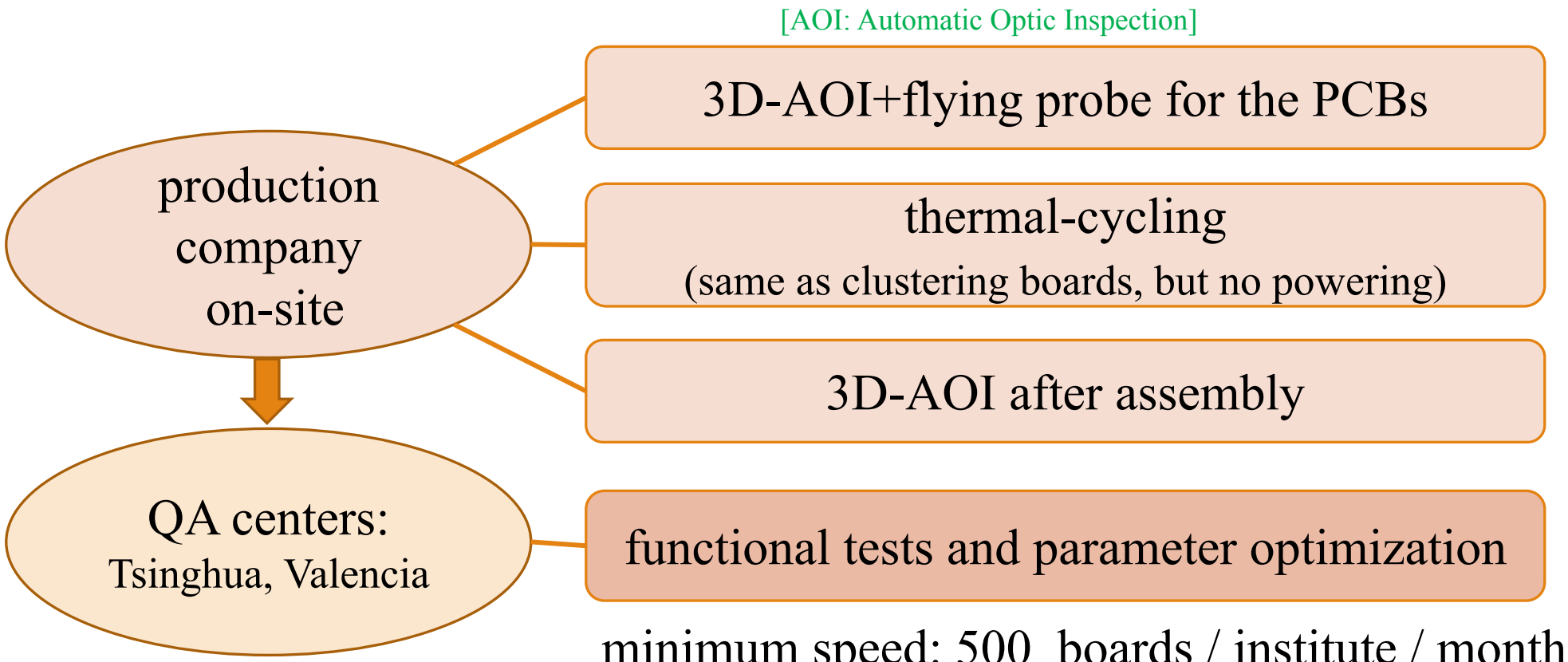




Selection of the production companies

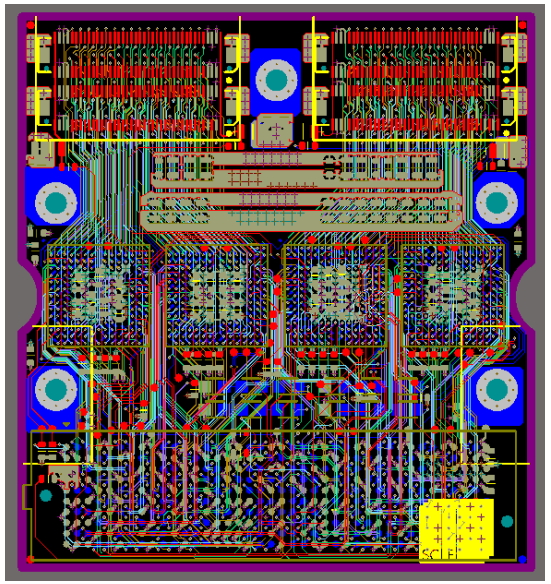
Company	ShenZhen SinoFast Electronics （PCB + Assembly）	ShenZhen Fastprint Circuit Tech （PCB + Assembly）
PCB standard	IPC 600G class 3	
assembly standard	IPC-A-610E CLASS 2	IPC-A-610E CLASS 3
delivery schedule	15 days (10 pcs ~ 2500 pcs)	20 days
On-site QA facilities	✓ AOI for each layer (PCB) ✓ flying probe test: shorts and continuity (PCB) ✓ 3D AOI (assembly) ✓ X-Ray of BGA-packaged components (assembly) ✓ values of all passive component (assembly) ✓ thermal-cycling test (assembly, Fastprint)	
PROs	✓ same manufacturer for CMS GEM frontend boards	✓ Largest and first listed company of PCB manufacturer ✓ thermal-cycling test
CONs	✓ IPC-A-610E CLASS 2 instead of CLASS 3 ✓ thermal-cycling test has to be done at Tsinghua	✓ longer delivery time

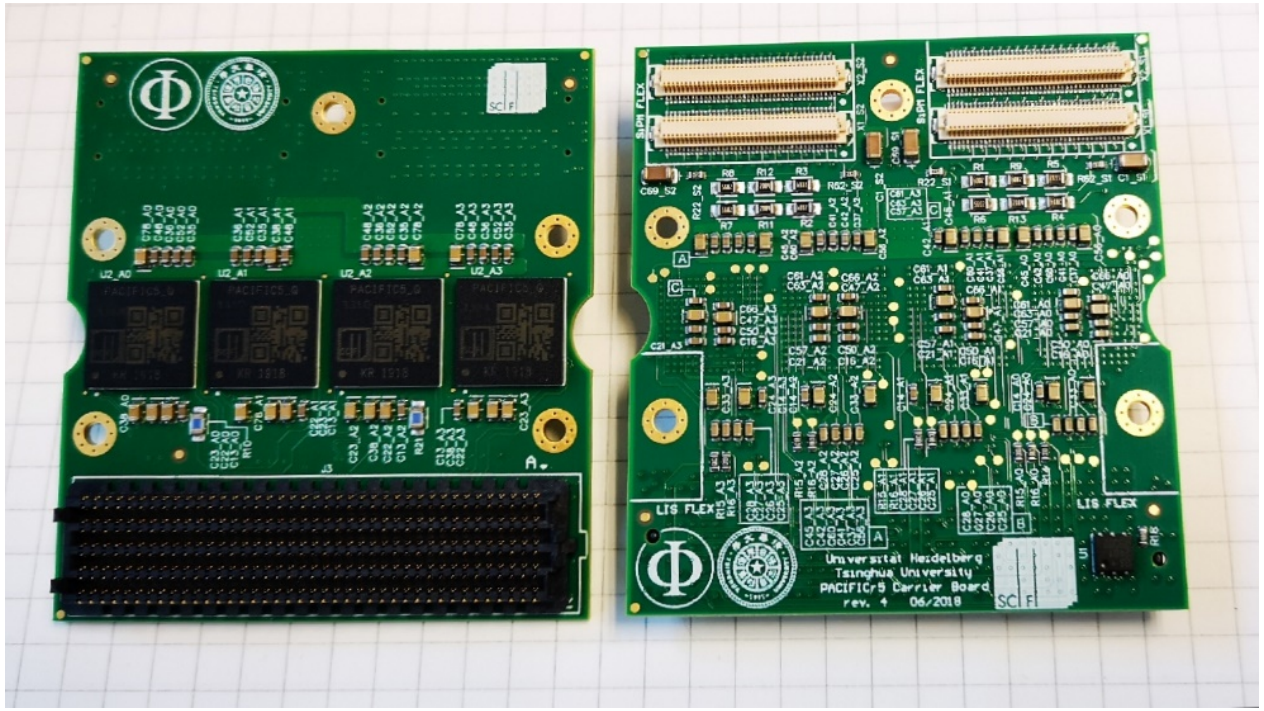
Quality Assurance (QA)



minimum speed: 500 boards / institute / month
<13mins/board

Redesign of PACIFIC Carrier Board & Mass Production





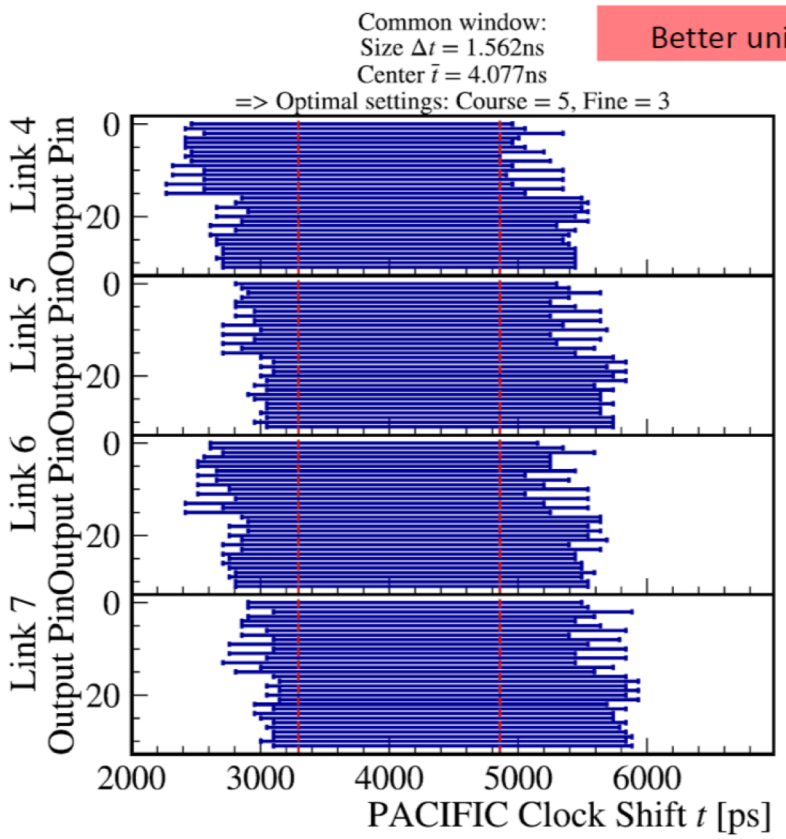
2018.09 - First 250 PACIFIC Carrier Boards finished

Check with Sci-Fi ROB cooling frame

First C-Frame of the Sci-Fi tracker
(Sci-Fi milestone of 2018)

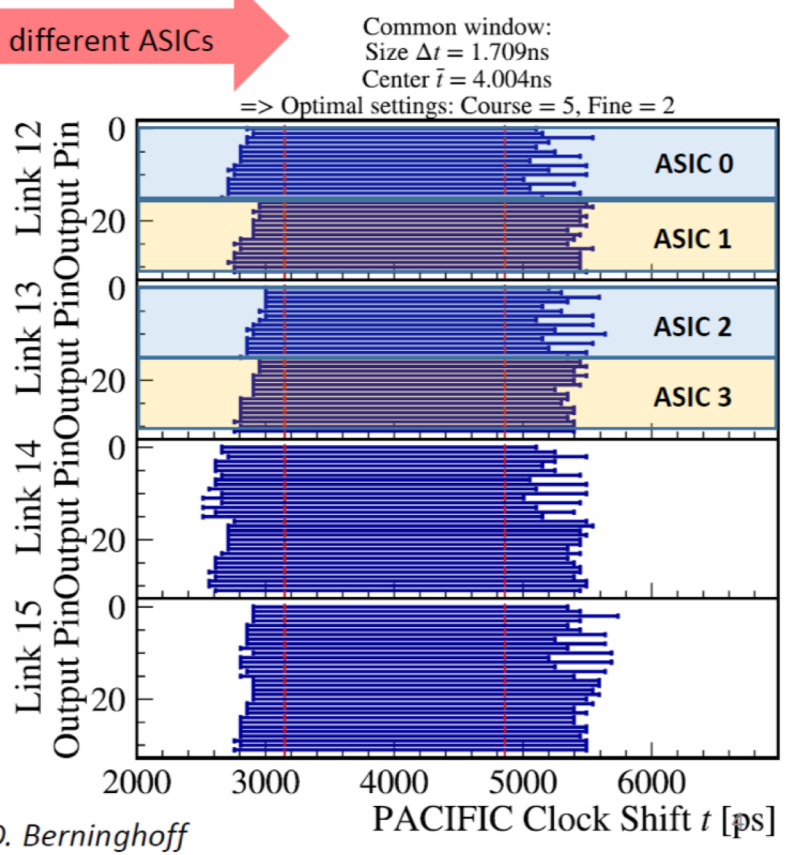
BER test with Sci-Fi FE

- Position: Master Board 0, PBs 2+3, old design



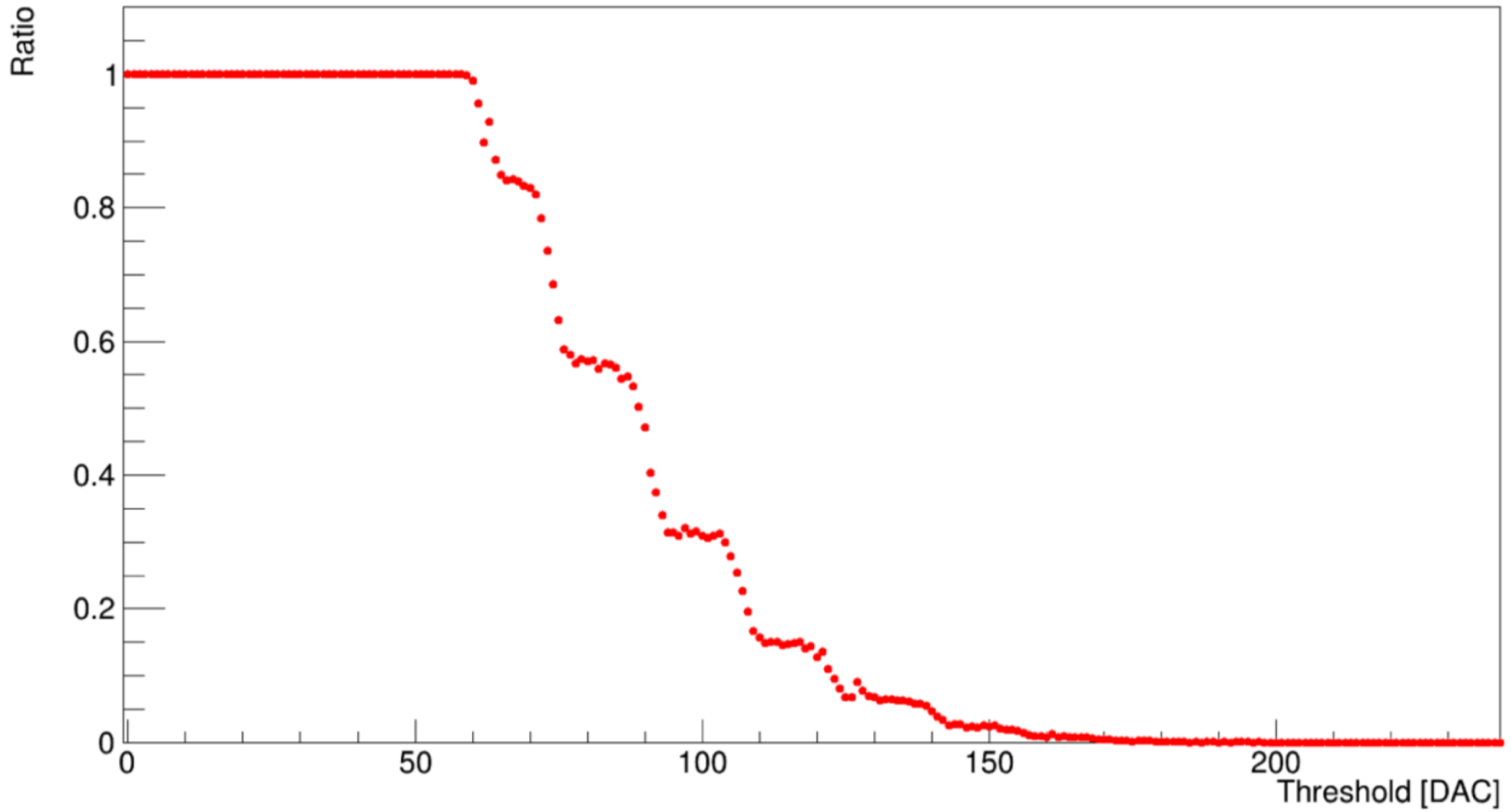
Better uniformity among different ASICs

- Position: Master Board 1, PBs 2+3, new design



Result from D. Berninghoff

Test with SiPM + Light Injection System

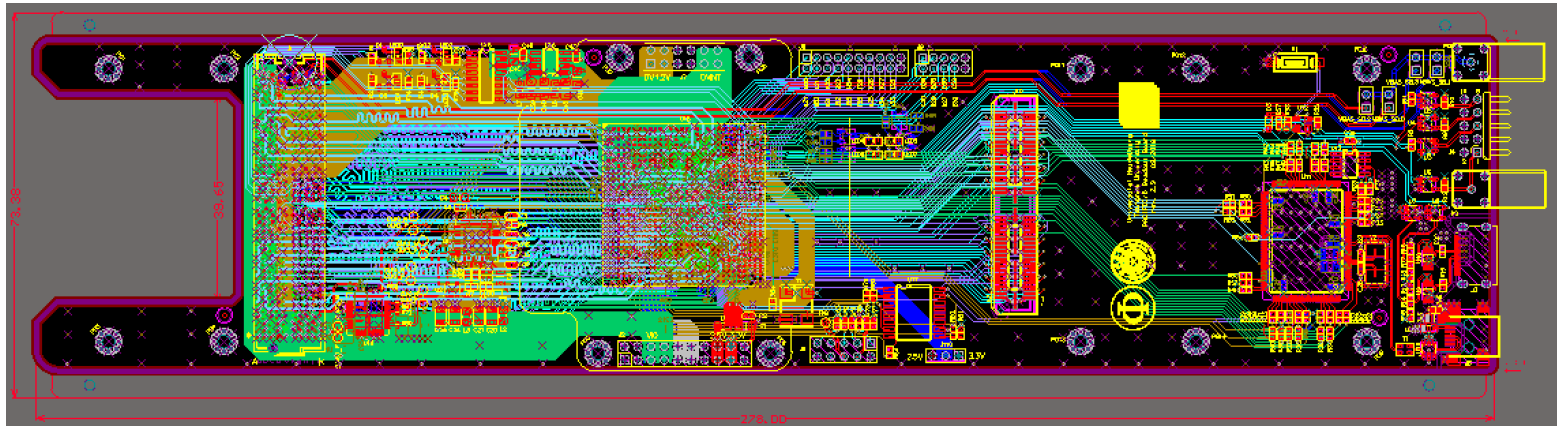


Outline

- Sci-Fi Tracker readout electronics
- QA system for Frontend Boards
- QA system for packaged ASICs

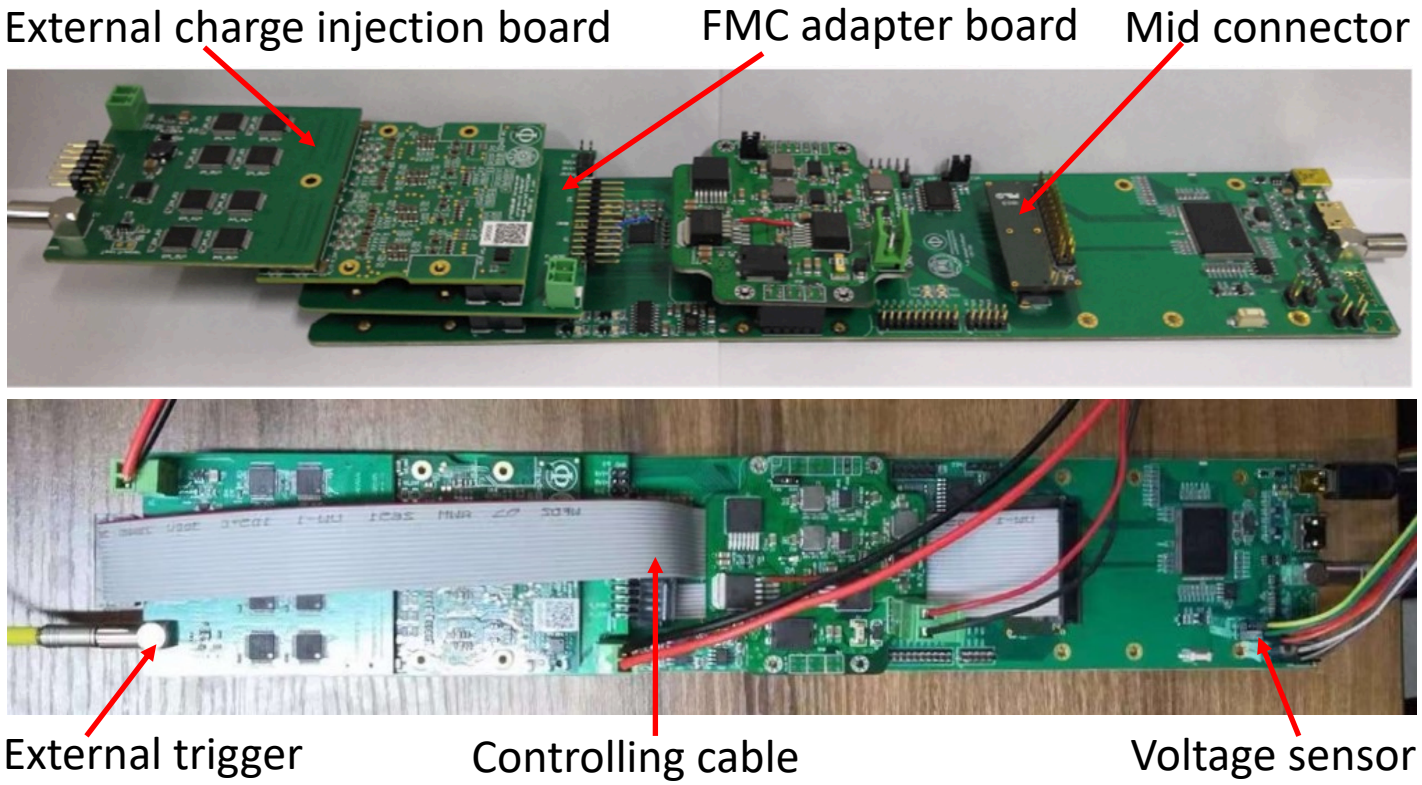
QA functional test setup for Carrier Boards

- Custom designed test DAQ (PACIFICROB): [fully tested, 3 for Heidelberg (delivered), 3 for Barcelona, 3 for Valencia]
  - ✓ Altera Cyclone FPGA (clock generation, ASIC configuration, data process, sensor readout ...)
  - ✓ precise clock conditioner to fine tune the clock for each ASIC
  - ✓ LVDS-SLVS convertor
  - ✓ 8-channel, 12-bit ADC
  - ✓ USB interface to PC
- FMC connector intermedia board:
  - ✓ Simple pin-to-pin adapter PCBs
  - ✓ To avoid broken FMC connectors
- Charge injection board
- DC power supply
  - ✓ Output 5V/3A at least
- Arbitrary waveform generator
- Linux PC

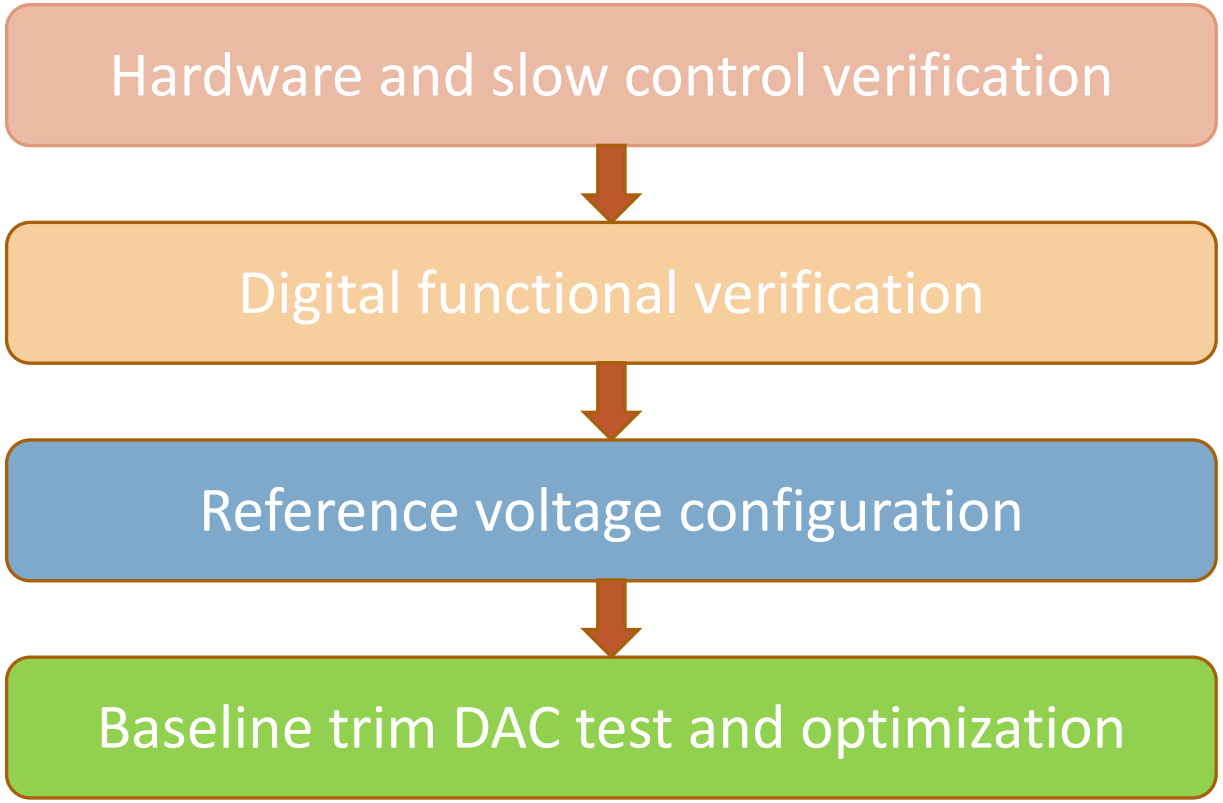


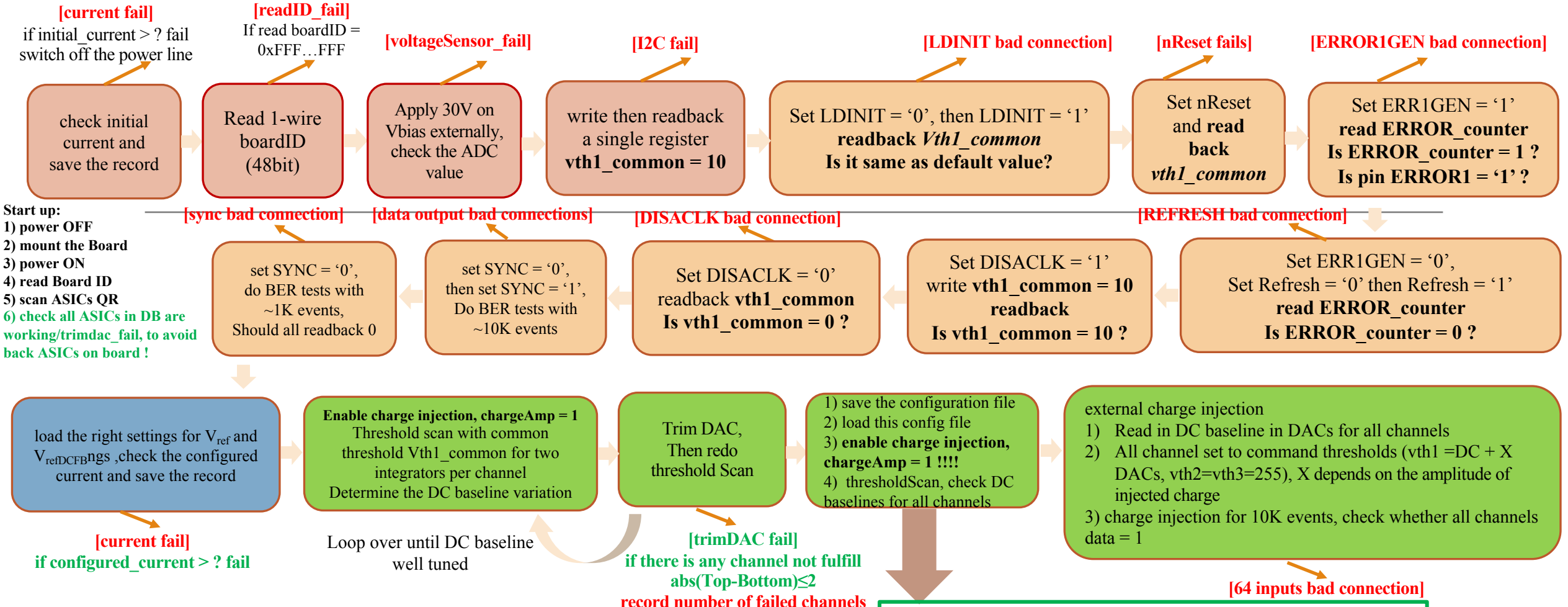
QA functional test setup for Carrier Boards

- Custom designed test DAQ (PACIFICROB): [fully tested, 3 for Heidelberg (delivered), 3 for Barcelona, 3 for Valencia]
  - ✓ Altera Cyclone FPGA (clock generation, ASIC configuration, data process, sensor readout ...)
  - ✓ precision clock conditioner to fine tune the clock for each ASIC
  - ✓ (LVDS-SLVS convertor)
  - ✓ 8-channel, 12-bit ADC
  - ✓ USB interface to PC
- FMC connector intermedia board:
  - ✓ Simple pin-to-pin adapter PCBs
  - ✓ To avoid broken FMC connectors
- Charge injection board
- DC power supply
  - ✓ Output 5V/3A at least
- Arbitrary waveform generator
- Linux PC



PACIFICr5 carrier board QA test routine



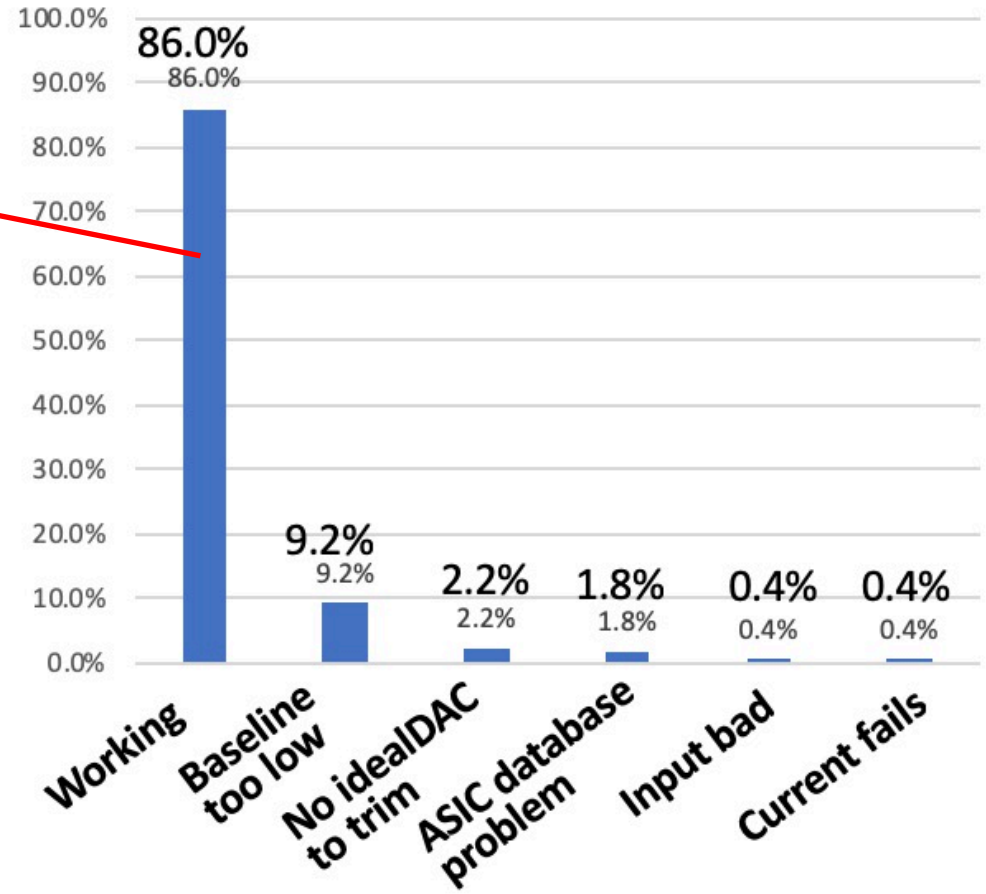


PACIFIC Carrier Board QA test routine

Save results to database:
1) test log
2) all parameters into a configuration file: PB_XX.conf, which can be read later by SciFi readout system.
3) after trimming DC-baseline distribution
- ✓ **1-D histogram of 0.5ratio-transition-DAC value for all channels (both Top and Bottom DAC) for each ASIC**
- ✓ **1-D histogram of difference of Top and bottom DAC within the same channel for each ASIC**

First 250 PACIFIC Carrier Boards Tested

- 86.0% Working
- 14.0% Failed:
  - ✓Baseline too low
  - ✓No ideal DAC to trim
  - ✓ASIC database problem
  - ✓Input bad
  - ✓Current fails

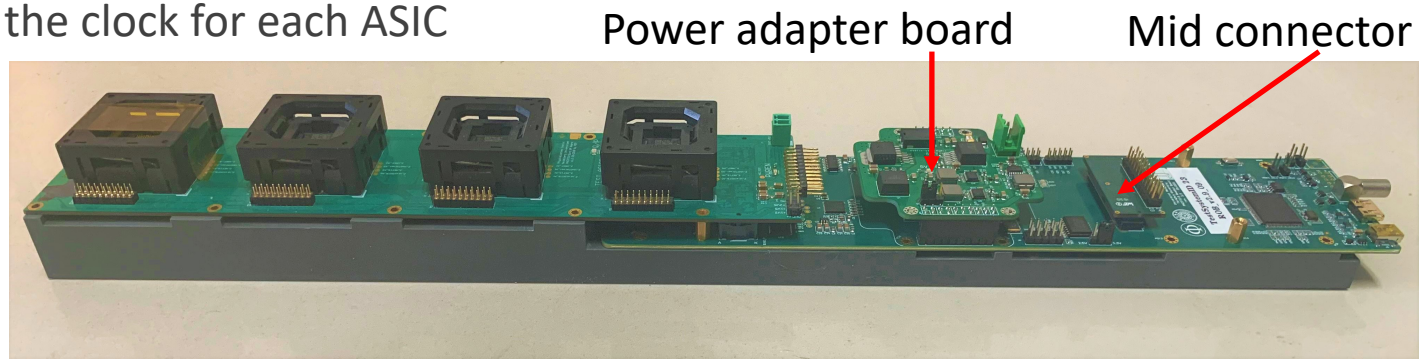


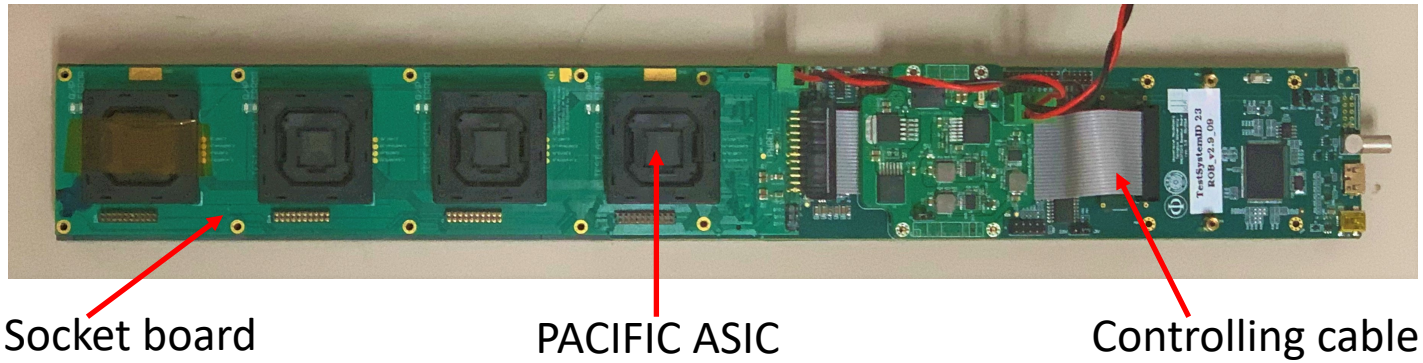
Outline

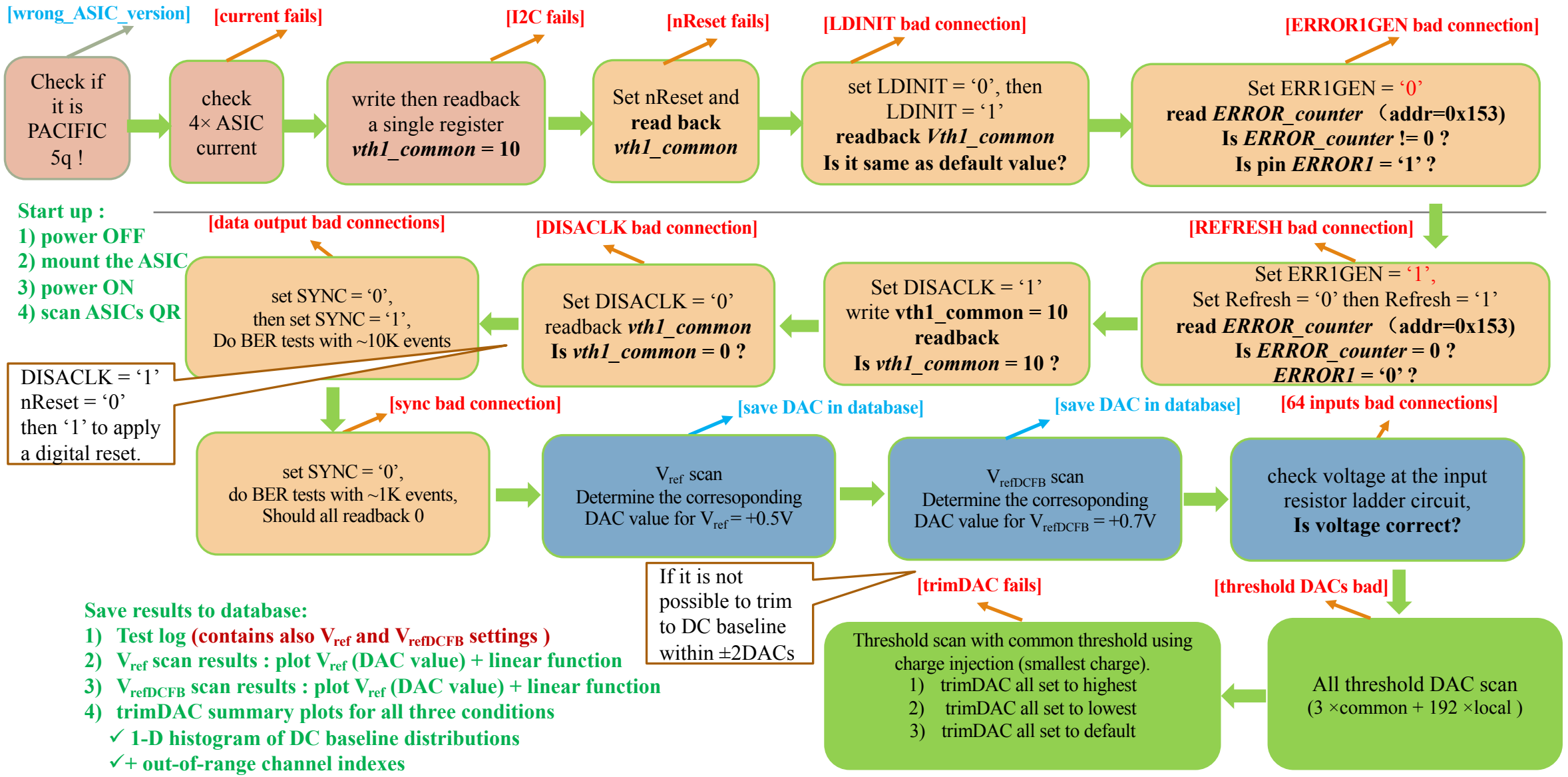
- Sci-Fi Tracker readout electronics
- QA system for Frontend Boards
- QA system for packaged ASICs

QA functional test setup for packaged chips

- Custom designed test DAQ (PACIFICROB): [fully tested, 4 for Heidelberg, 3 for Barcelona, 3 for Valencia]
  - ✓Altera Cyclone FPGA (clock generation, ASIC configuration, data process, sensor readout ...)
  - ✓precision clock conditioner to fine tune the clock for each ASIC
  - ✓(LVDS-SLVS convertor)
  - ✓8-channel, 12-bit ADC
  - ✓USB interface to PC
- Socket Board:
  - ✓4 sockets to nip chips
  - ✓Connected with FMC & controlling cable
- DC power supply
  - ✓Output 5V/3A at least
- Linux PC
- Robot arm (Barcelona)







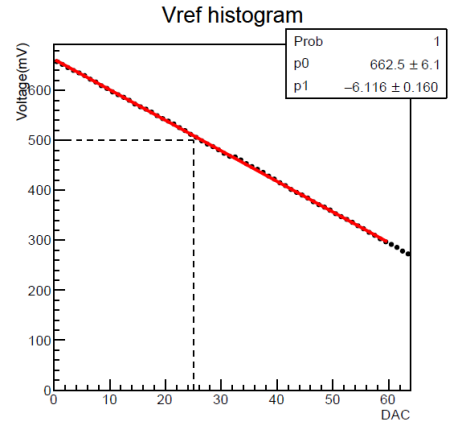
Save results to database:

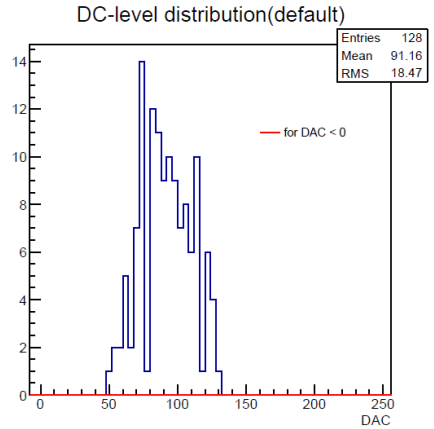
1) **Test log (contains also V_{ref} and $V_{refDCFB}$ settings)**
2) **V_{ref} scan results : plot V_{ref} (DAC value) + linear function**
3) **$V_{refDCFB}$ scan results : plot V_{ref} (DAC value) + linear function**
4) **trimDAC summary plots for all three conditions**
   - ✓ **1-D histogram of DC baseline distributions**
   - ✓**+ out-of-range channel indexes**

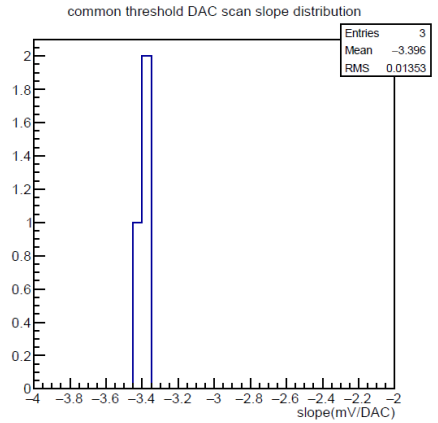
PACIFIC ASIC QA test routine

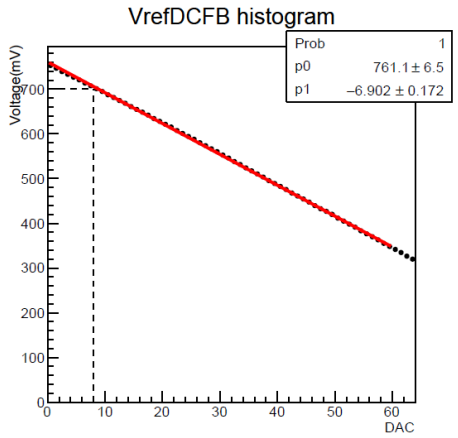
Raw data from all the scans will be save into one file to reproduce the results.

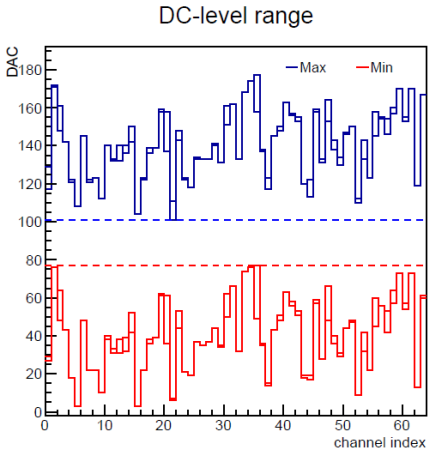
Main features of test results for one chip

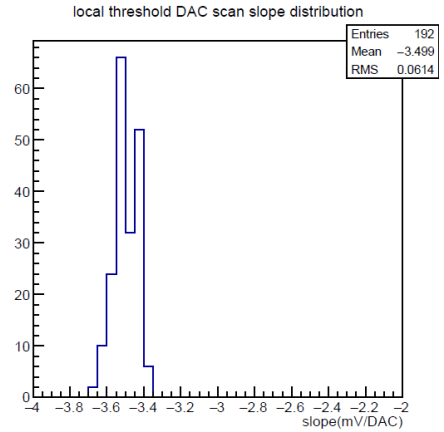






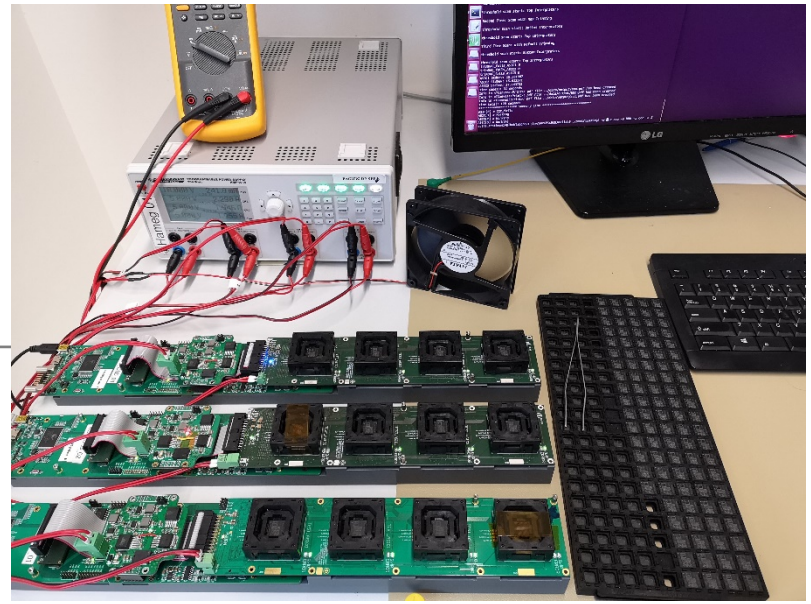






test automatically uploading results to DB

final check the QA test routine

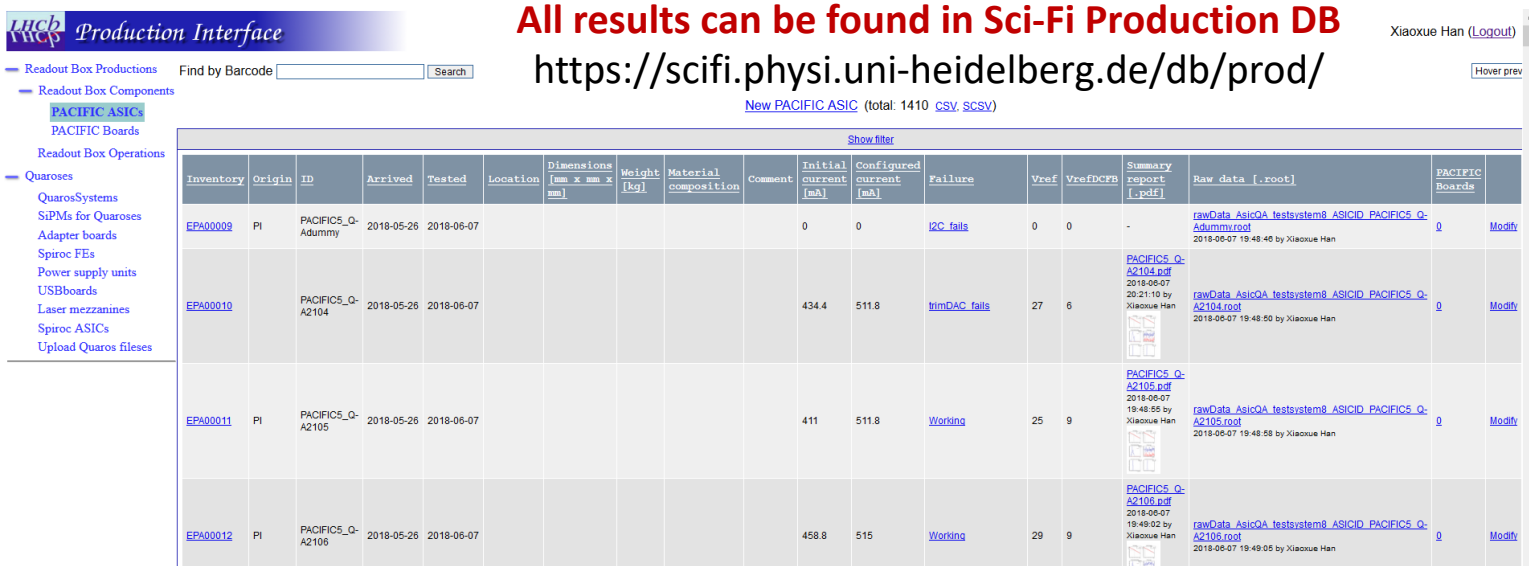


QA test running : 10 ASICs/run , ~100ASICs/hour

finish all 1st batch 1420 PACIFIC5q test

All results can be found in Sci-Fi Production DB

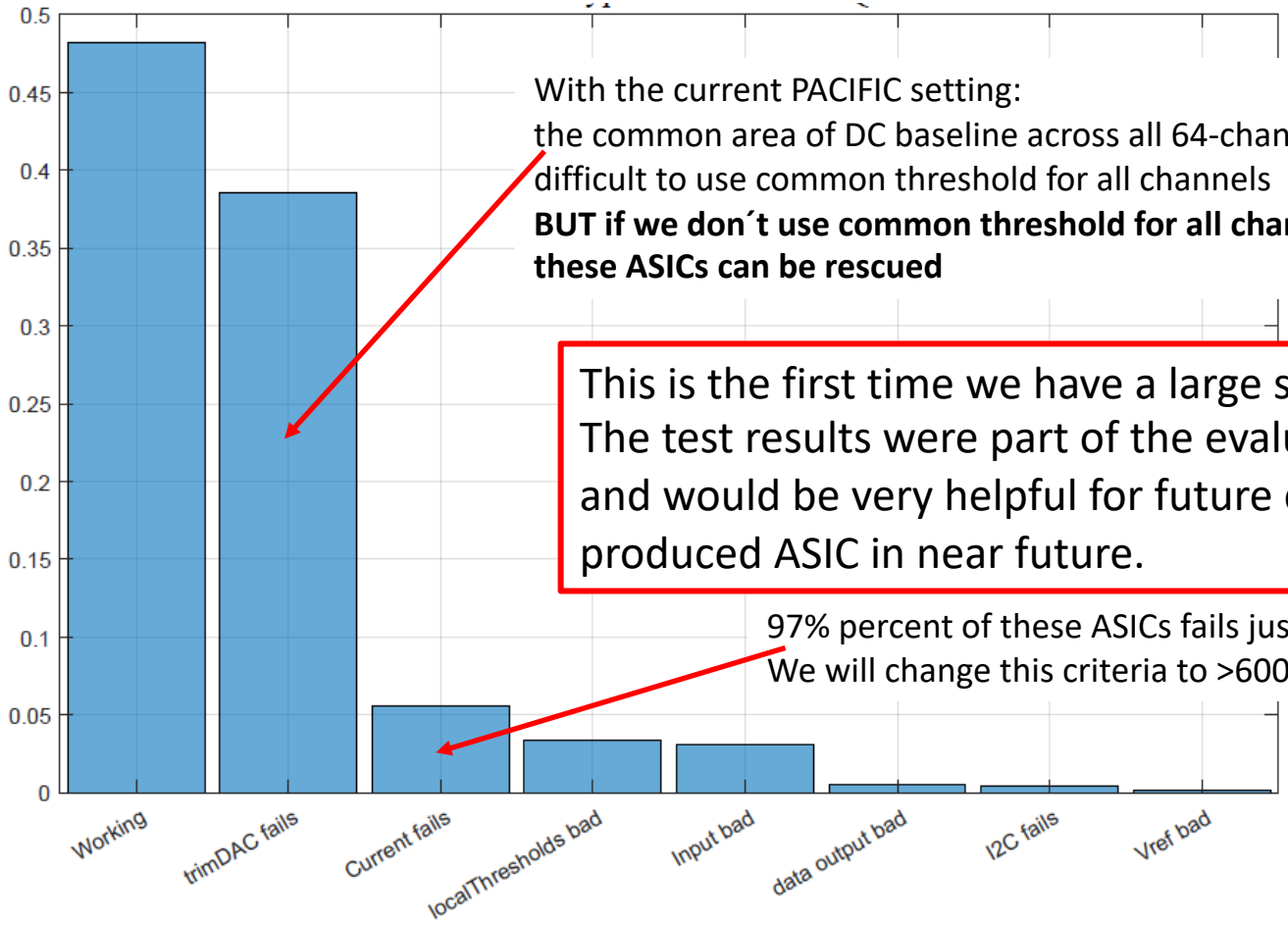
https://scifi.physi.uni-heidelberg.de/db/prod/



Inventory	Origin	ID	Arrived	Tested	Location	Dimensions [mm x mm x mm]	Weight [kg]	Material composition	Comment	Initial current [mA]	Configured current [mA]	Failure	Vref	VrefDCPB	Summary report [.pdf]	Raw data [.root]	PACIFIC Boards	
EPA00009	PI	PACIFIC5_Q-Adummy	2018-05-26	2018-06-07						0	0	I2C fails	0	0	-	rawData_AsicQA_testsystem8_ASICID_PACIFIC5_Q-Adummy.root 2018-06-07 19:48:46 by Xiaoxue Han	0	Modify
EPA00010		PACIFIC5_Q-A2104	2018-05-26	2018-06-07						434.4	511.8	trimDAC fails	27	6	PACIFIC5_Q-A2104.pdf 2018-06-07 20:21:10 by Xiaoxue Han	rawData_AsicQA_testsystem8_ASICID_PACIFIC5_Q-A2104.root 2018-06-07 19:48:50 by Xiaoxue Han	0	Modify
EPA00011	PI	PACIFIC5_Q-A2105	2018-05-26	2018-06-07						411	511.8	Working	25	9	PACIFIC5_Q-A2105.pdf 2018-06-07 19:48:55 by Xiaoxue Han	rawData_AsicQA_testsystem8_ASICID_PACIFIC5_Q-A2105.root 2018-06-07 19:48:58 by Xiaoxue Han	0	Modify
EPA00012	PI	PACIFIC5_Q-A2106	2018-05-26	2018-06-07						458.8	515	Working	29	9	PACIFIC5_Q-A2106.pdf 2018-06-07 19:49:02 by Xiaoxue Han	rawData_AsicQA_testsystem8_ASICID_PACIFIC5_Q-A2106.root 2018-06-07 19:49:05 by Xiaoxue Han	0	Modify

QA test for 1st batch of packaged PACIFIC5q

1st batch of 1420 chips

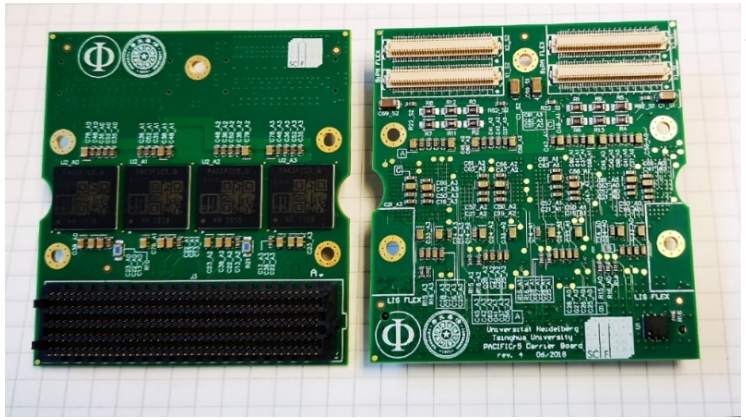


With the current PACIFIC setting:
the common area of DC baseline across all 64-channels is less than 4DACs,
difficult to use common threshold for all channels
BUT if we don´t use common threshold for all channels or tune the PACIFIC settings , these ASICs can be rescued

This is the first time we have a large statistical sample of the ASICs. The test results were part of the evaluation of the Sci-Fi electronics and would be very helpful for future classification of mass-produced ASIC in near future.

97% percent of these ASICs fails just because the initial current > 500mA
We will change this criteria to >600mA and re-measure these ASICs

Summary



- LHCb China Group (2018) finished:
  - ✓>1500 PACIFIC ASICs tested
  - ✓Frontend Boards redesigned and verified
  - ✓250 Frontend Boards manufactured and tested in China
  - ✓6 Readout Electronic Quality Assurance System set up in Heidelberg, Barcelona and Valencia

- 2019 To Do:
  - ✓ALL 12,000 PACIFIC ASICs to test (with Barcelona group)
  - ✓ALL 2,500 Frontend Boards to manufacture in China [in progress] and to test (with Valencia group)

Thanks for
Your attention!