Status of Digital Pixel

Tianya Wu

CEPC MOST2 Chips Meeting

twu@ifae.es

14-08-2018

IFAE
Institut de Física
d'Altes Energies

R

EXCELENCIA
SEVERO
OCHOA
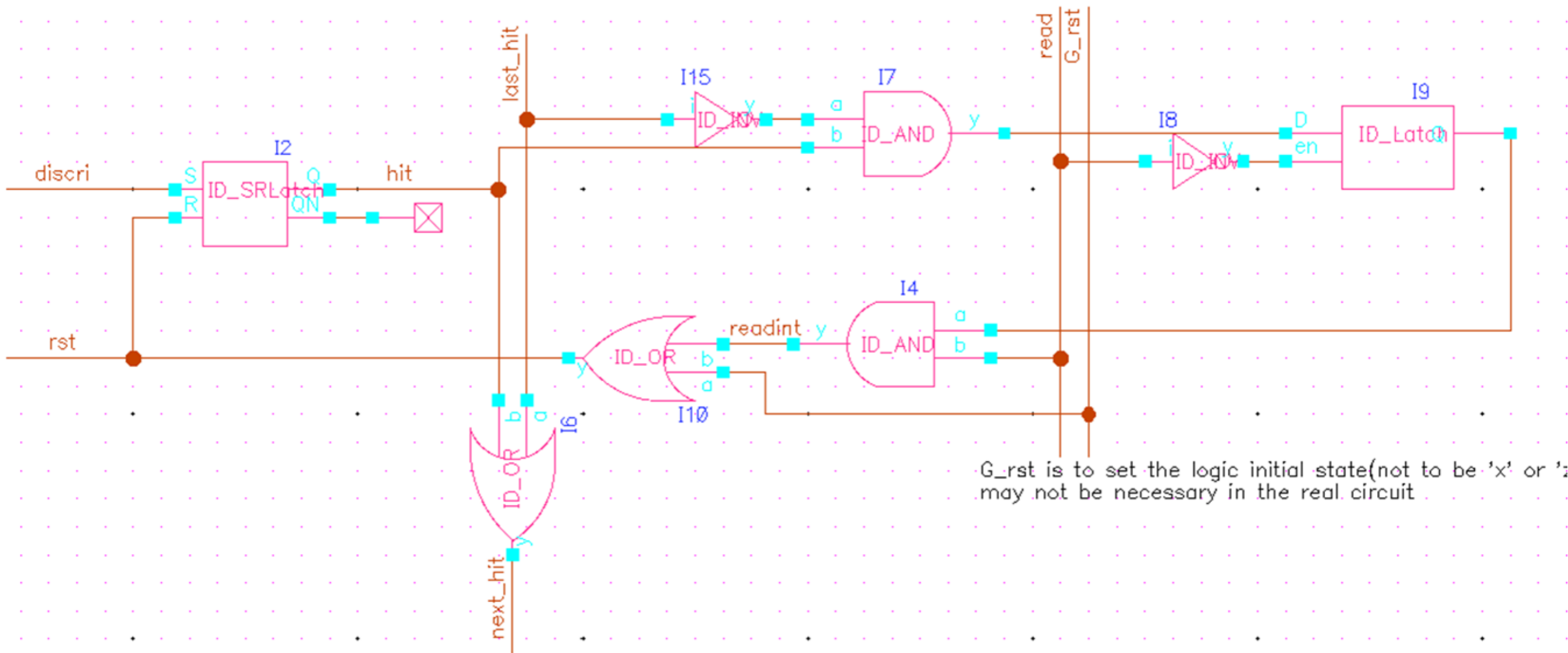
BIST Barcelona Institute of Science and Technology

CENTRAL CHINA NORMAL UNIVERSITY

G_rst is to set the logic initial state(not to be 'x' or 'z)
may not be necessary in the real circuit

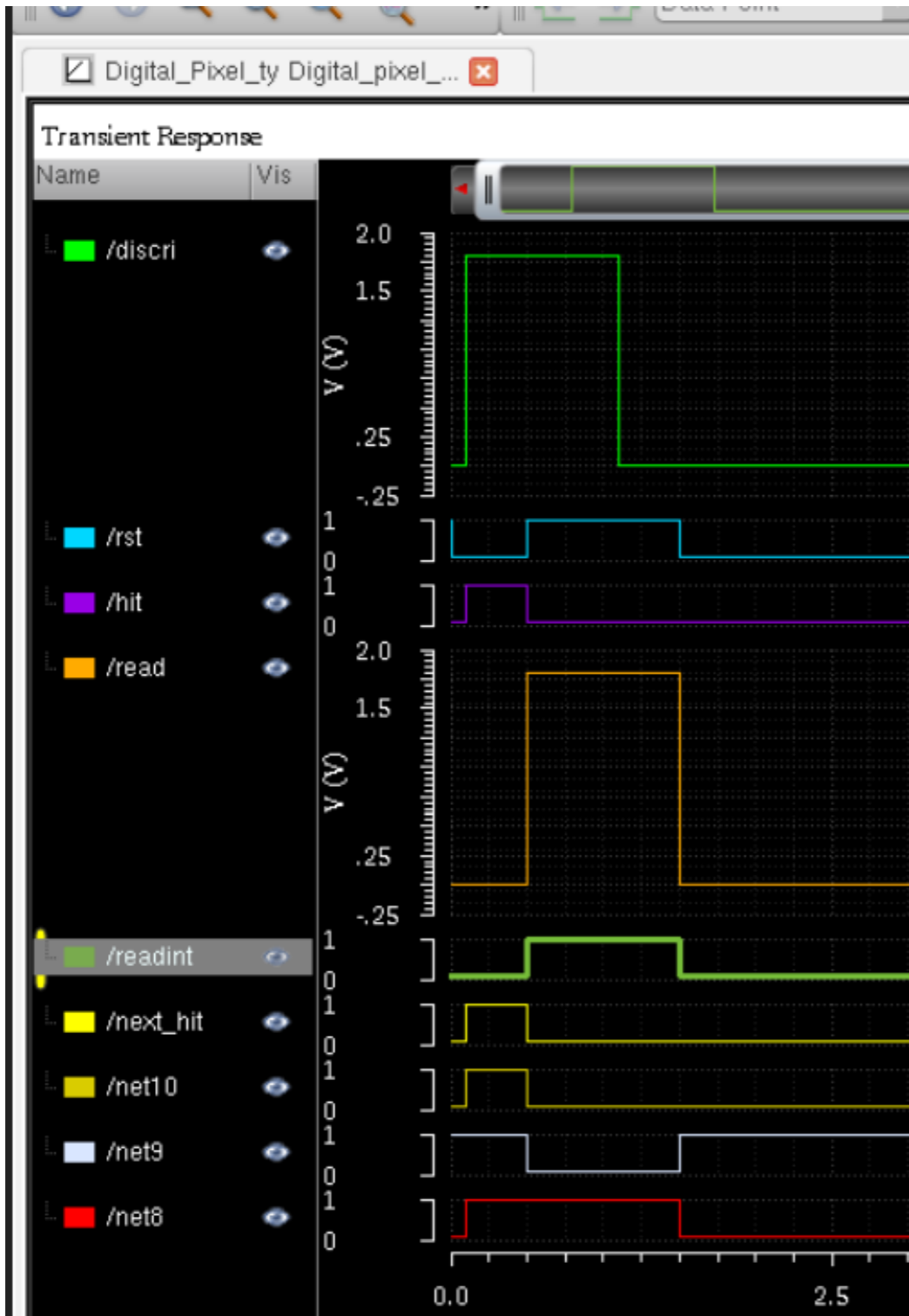● From the waveform of simulation, we can see that this logic structure works fine.

I exchanged all the logic gates from TowerJazz digital library. Everything seems fine, but I can't simulate it with pure Verilog blocks correctly.
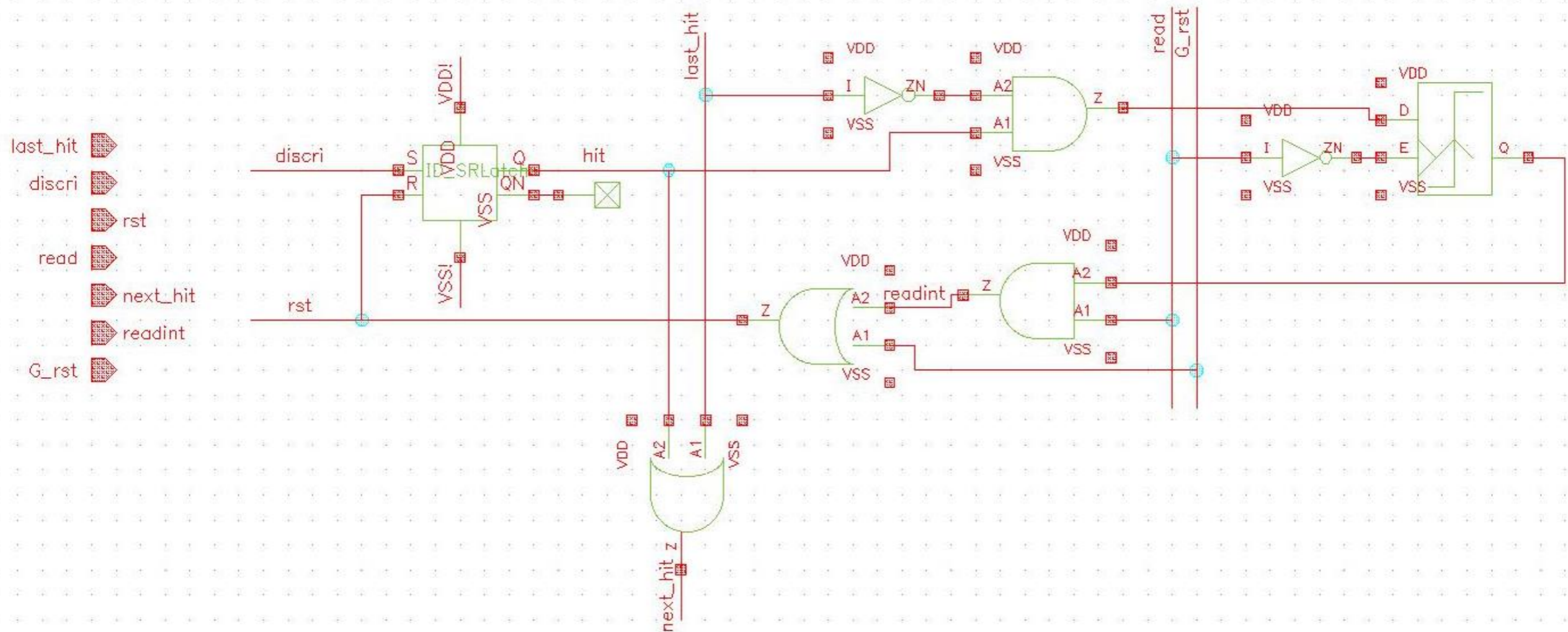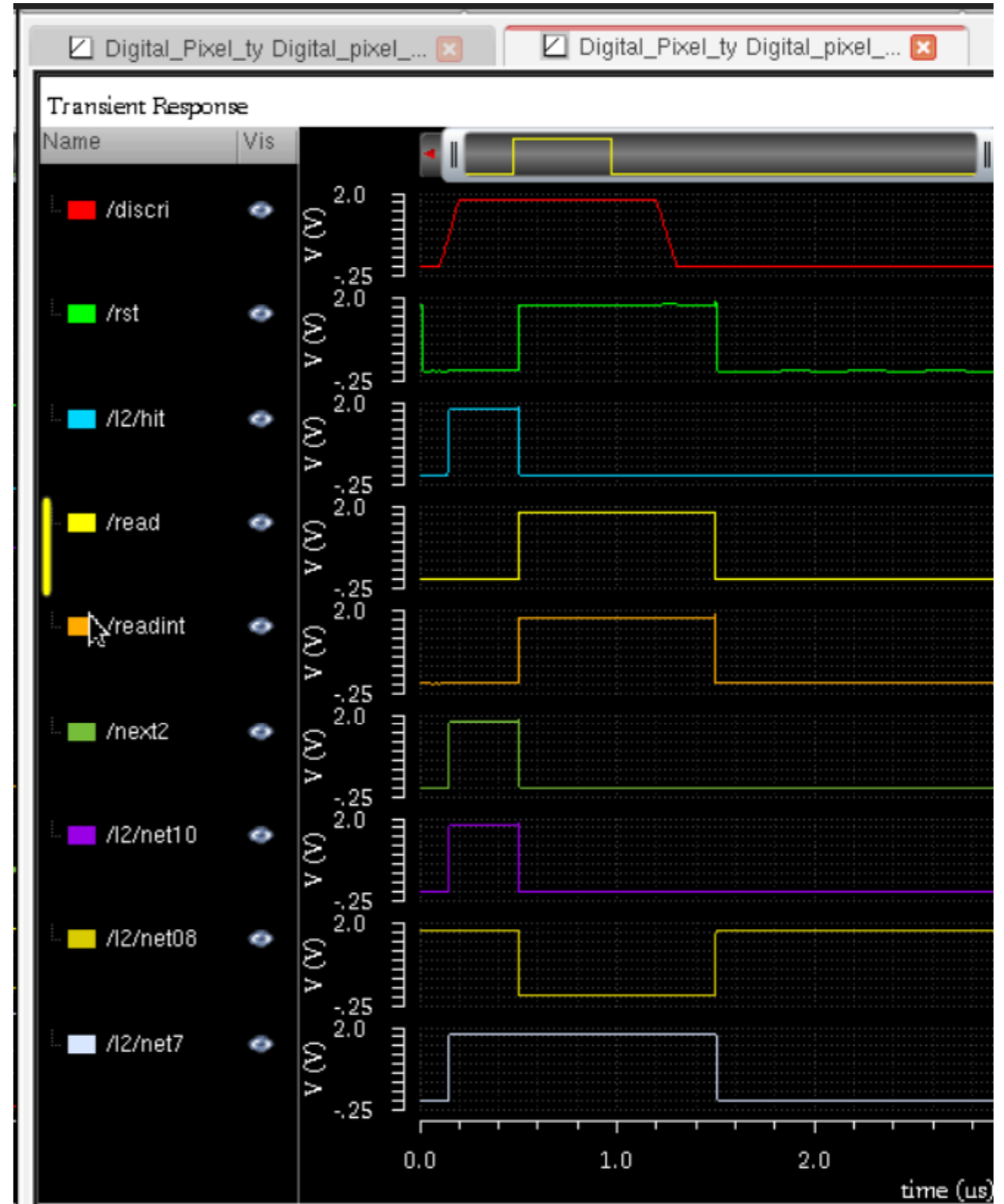
Simulation result:

the real circuit output is the same with functional one.
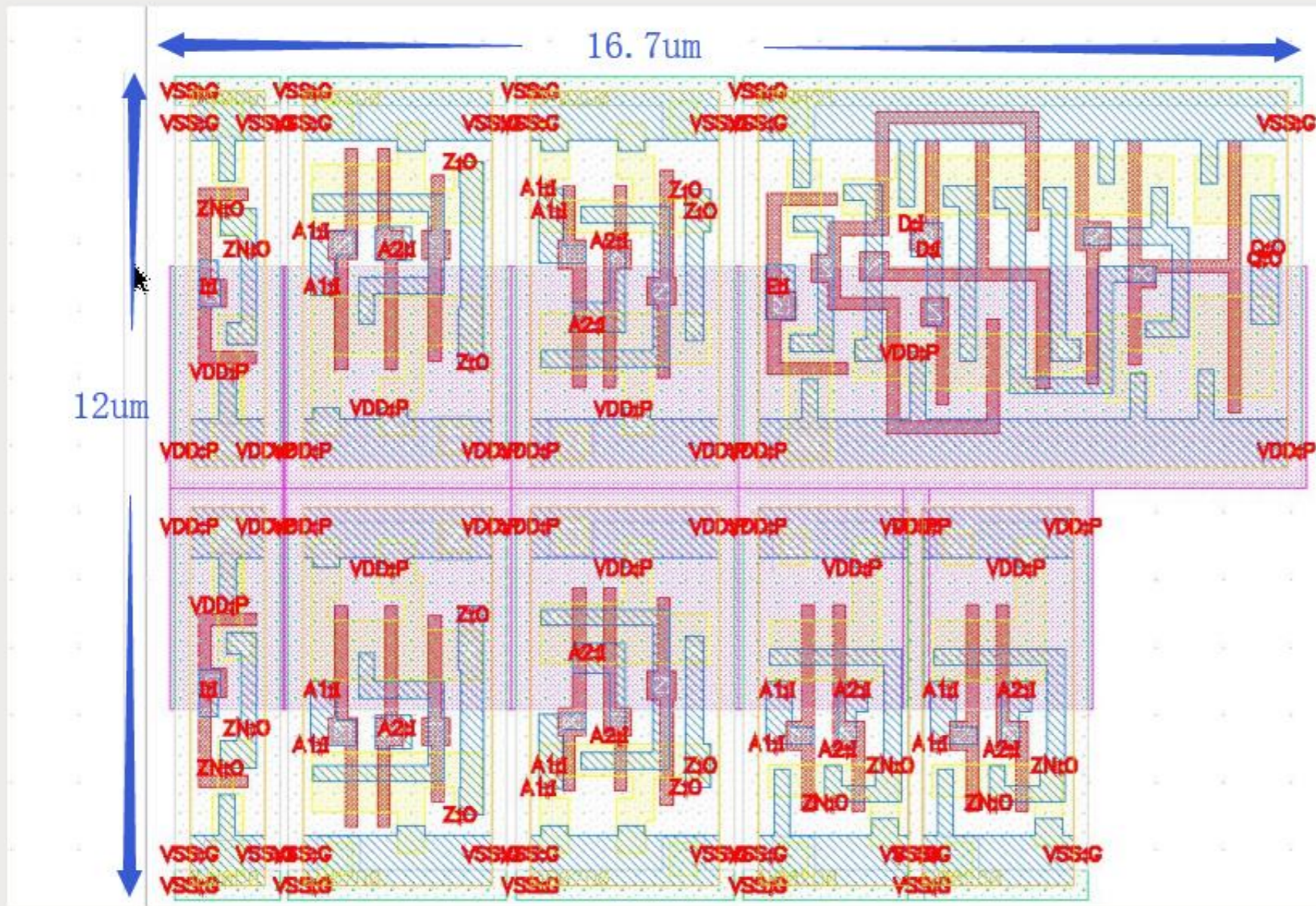

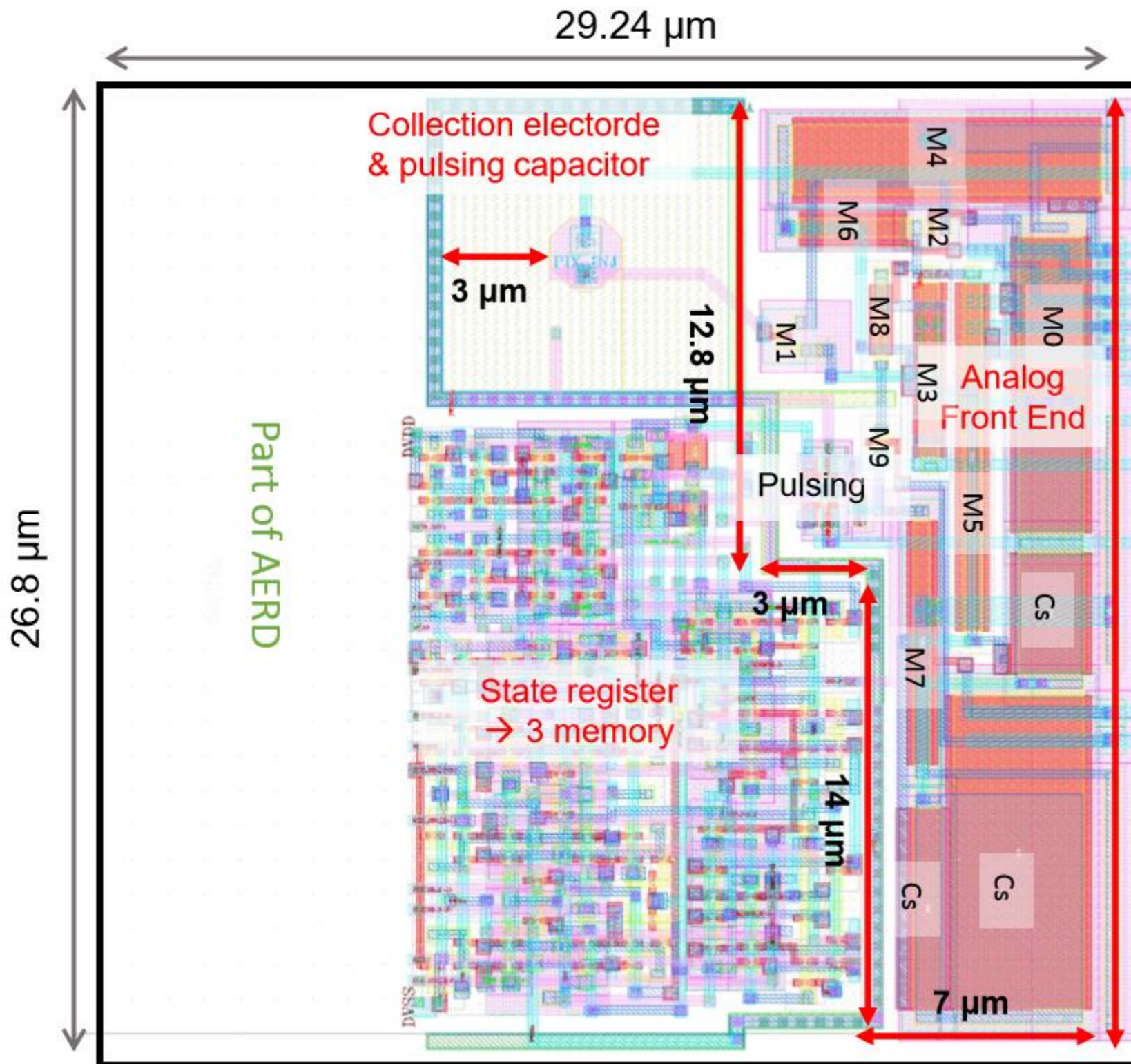
Functional
simulation output

Real circuit
simulation output

First layout of every single gate without any wires.
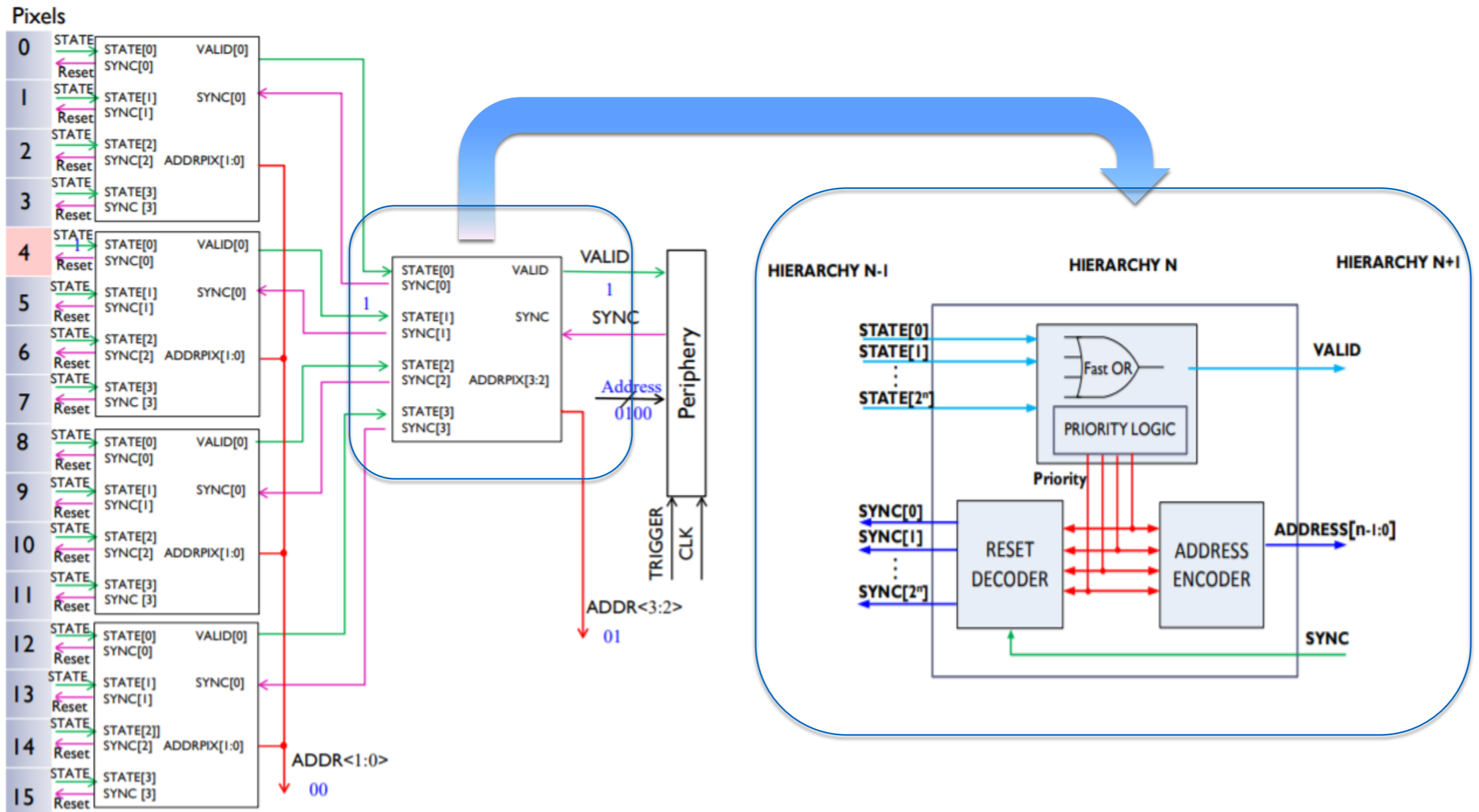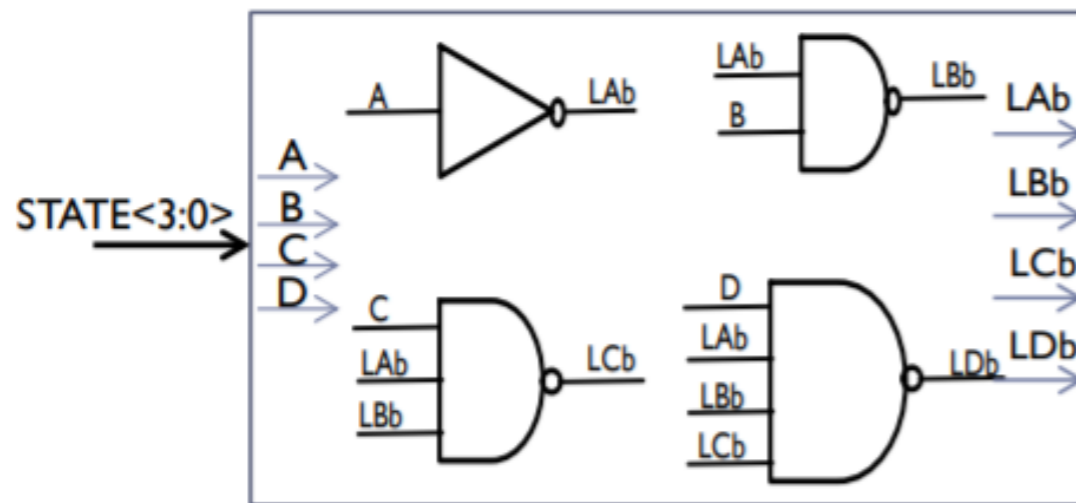I think it can be smaller but won't be too much.

Layout on ALPIDE

- If the analog front end is the same with ALPIDE, that means digital part should be within 13x19 um

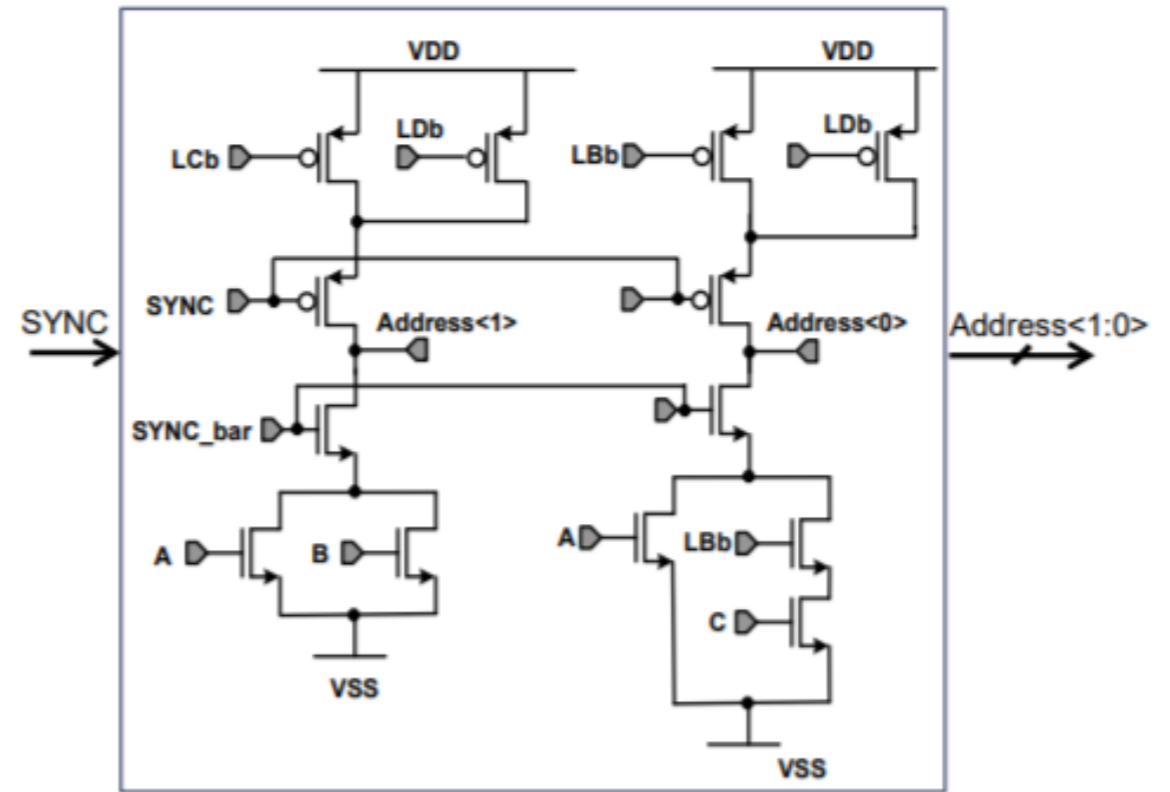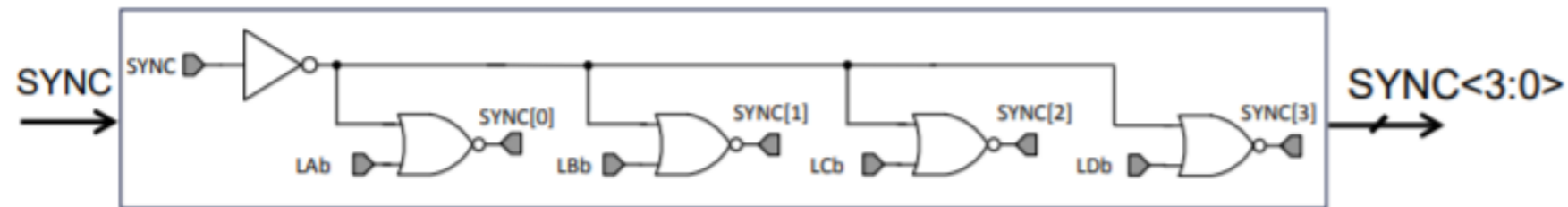# The decode scheme and basic block structure of ALPIDE

The implemented circuit of the basic block of ALPIDE

(a) priority logic of four inputs.

(b) combinatorial address encoder logic.

(c) reset decoder logic.

Thanks for your attention.